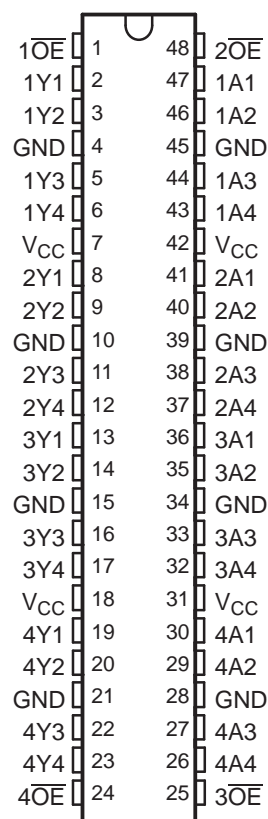


FEATURES

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54LVTH16244A . . . WD PACKAGE
SN74LVTH16244A . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The 'LVTH16244A devices are 16-bit buffers and line drivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

SN54LVTH16244A, SN74LVTH16244A

3.3-V ABT 16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

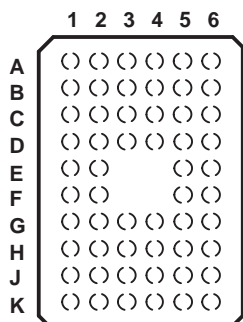
SCBS142T–MAY 1992–REVISED NOVEMBER 2006

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	FBGA – GRD	Reel of 1000	SN74LVTH16244AGRDR	LL244A
	FBGA – ZRD (Pb-free)		SN74LVTH16244AZRDR	
	SSOP – DL	Tube of 25	SN74LVTH16244ADL	LVTH16244A
			SN74LVTH16244ADLG4	
		Reel of 1000	SN74LVTH16244ADLR	
			74LVTH16244ADLRG4	
	TSSOP – DGG	Reel of 2000	SN74LVTH16244ADGGR	LVTH16244A
			74LVTH16244ADGGRE4	
			74LVTH16244ADGGRG4	
	TVSOP – DGV	Reel of 2000	SN74LVTH16244ADGVR	LL244A
			74LVTH16244ADGVRE4	
–55°C to 125°C	VFBGA – GQL	Reel of 1000	SN74LVTH16244AGQLR	LL244A
	VFBGA – ZQL (Pb-free)		SN74LVTH16244AZQLR	
	CFP – WD	Tube	SNJ54LVTH16244AWD	SNJ54LVTH16244AWD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

GQL OR ZQL PACKAGE
(TOP VIEW)

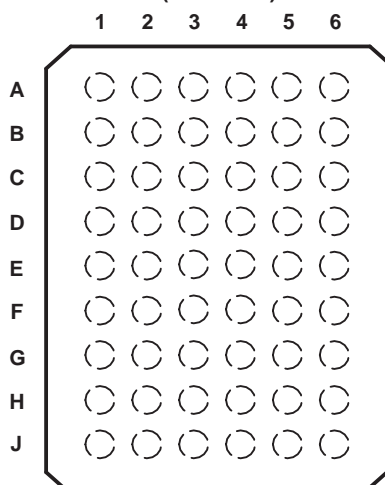


TERMINAL ASSIGNMENTS⁽¹⁾
(56-Ball GQL/ZQL Package)

	1	2	3	4	5	6
A	1 \overline{OE}	NC	NC	NC	NC	2 \overline{OE}
B	1Y2	1Y1	GND	GND	1A1	1A2
C	1Y4	1Y3	V _{CC}	V _{CC}	1A3	1A4
D	2Y2	2Y1	GND	GND	2A1	2A2
E	2Y4	2Y3			2A3	2A4
F	3Y1	3Y2			3A2	3A1
G	3Y3	3Y4	GND	GND	3A4	3A3
H	4Y1	4Y2	V _{CC}	V _{CC}	4A2	4A1
J	4Y3	4Y4	GND	GND	4A4	4A3
K	4 \overline{OE}	NC	NC	NC	NC	3 \overline{OE}

(1) NC – No internal connection

GRD OR ZRD PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS⁽¹⁾
(54-Ball GRD/ZRD Package)

	1	2	3	4	5	6
A	1Y1	NC	1 \overline{OE}	2 \overline{OE}	NC	1A1
B	1Y3	1Y2	NC	NC	1A2	1A3
C	2Y1	1Y4	V _{CC}	V _{CC}	1A4	2A1
D	2Y3	2Y2	GND	GND	2A2	2A3
E	3Y1	2Y4	GND	GND	2A4	3A1
F	3Y3	3Y2	GND	GND	3A2	3A3
G	4Y1	3Y4	V _{CC}	V _{CC}	3A4	4A1
H	4Y3	4Y2	NC	NC	4A2	4A3
J	4Y4	NC	4 \overline{OE}	3 \overline{OE}	NC	4A4

(1) NC – No internal connection

SN54LVTH16244A, SN74LVTH16244A

3.3-V ABT 16-BIT BUFFERS/DRIVERS

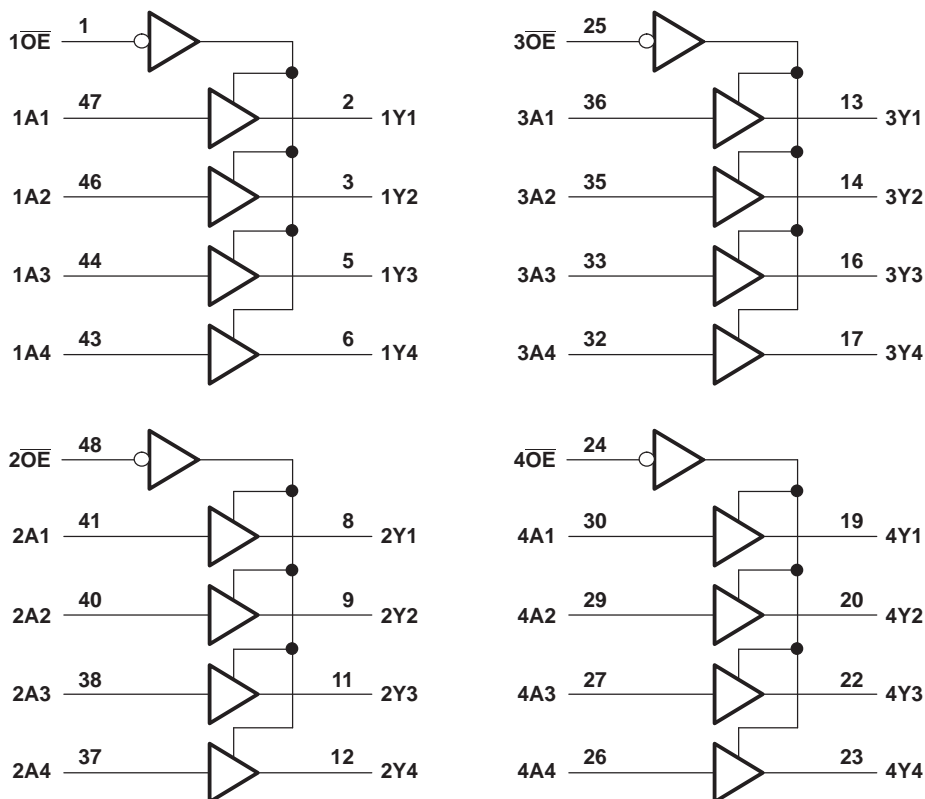
WITH 3-STATE OUTPUTS

SCBS142T—MAY 1992—REVISED NOVEMBER 2006

FUNCTION TABLE
(EACH 4-BIT BUFFER)

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DGV, DL, and WD packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		−0.5	4.6	V
V _I	Input voltage range ⁽²⁾		−0.5	7	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		−0.5	7	V
V _O	Voltage range applied to any output in the high state ⁽²⁾		−0.5	V _{CC} + 0.5	
I _O	Current into any output in the low state	SN54LVTH16244A	96		V
		SN74LVTH16244A	128		
I _O	Current into any output in the high state ⁽³⁾	SN54LVTH16244A	48		V
		SN74LVTH16244A	64		
I _{IK}	Input clamp current	V _I < 0	−50		mA
I _{OK}	Output clamp current	V _O < 0	−50		mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DGG package	70		°C/W
		DGV package	58		
		DL package	63		
		GQL/ZQL package	42		
		GRD/ZRD package	36		
T _{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) The current flows only when the output is in the high state and $V_O > V_{CC}$.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		SN54LVTH16244A		SN74LVTH16244A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–25		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LVTH16244A, SN74LVTH16244A

3.3-V ABT 16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCBS142T–MAY 1992–REVISED NOVEMBER 2006

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH16244A		SN74LVTH16244A			UNIT		
				MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾		MAX	
V _{IK}		V _{CC} = 2.7 V, I _I = −18 mA		−1.2		−1.2			V		
V _{OH}		V _{CC} = 2.7 V to 3.6 V, I _{OL} = −100 μA		V _{CC} − 0.2		V _{CC} − 0.2			V		
		V _{CC} = 2.7 V, I _{OH} = −8 mA		2.4		2.4					
		V _{CC} = 3 V		I _{OH} = −24 mA		2					
				I _{OH} = −32 mA				2			
V _{OL}		V _{CC} = 2.7 V		I _{OL} = 100 μA		0.2			V		
				I _{OL} = 24 mA		0.5					
		V _{CC} = 3 V		I _{OL} = 16 mA		0.4					
				I _{OL} = 32 mA		0.5					
				I _{OL} = 48 mA		0.55					
				I _{OL} = 64 mA		0.55					
I _I		V _{CC} = 0 or 3.6 V, V _I = 5.5 V		50		10			μA		
	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1		±1					
	Data inputs	V _{CC} = 3.6 V		V _I = V _{CC}		1					
				V _I = 0		−5					
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100			μA		
I _{I(hold)}	Data inputs	V _{CC} = 3 V		V _I = 0.8 V		75				μA	
				V _I = 2 V		−75		−75			
		V _{CC} = 3.6 V ⁽²⁾ , V _I = 0 to 3.6 V						500 − 750			
I _{OZH}		V _{CC} = 3.6 V, V _O = 3 V		5		5			μA		
I _{OZL}		V _{CC} = 3.6 V, V _O = 0.5 V		−5		−5			μA		
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care		±100 ⁽³⁾		±100			μA		
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care		±100 ⁽³⁾		±100			μA		
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		0.19		0.19		mA	
				Outputs low		5		5			
				Outputs disabled		0.19		0.19			
ΔI _{CC} ⁽⁴⁾		V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		0.2		0.2			mA		
C _i		V _I = 3 V or 0 V		4		4			pF		
C _o		V _O = 3 V or 0 V		9		9			pF		

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) On products compliant to MIL-PRF-38535, this parameter does not apply.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

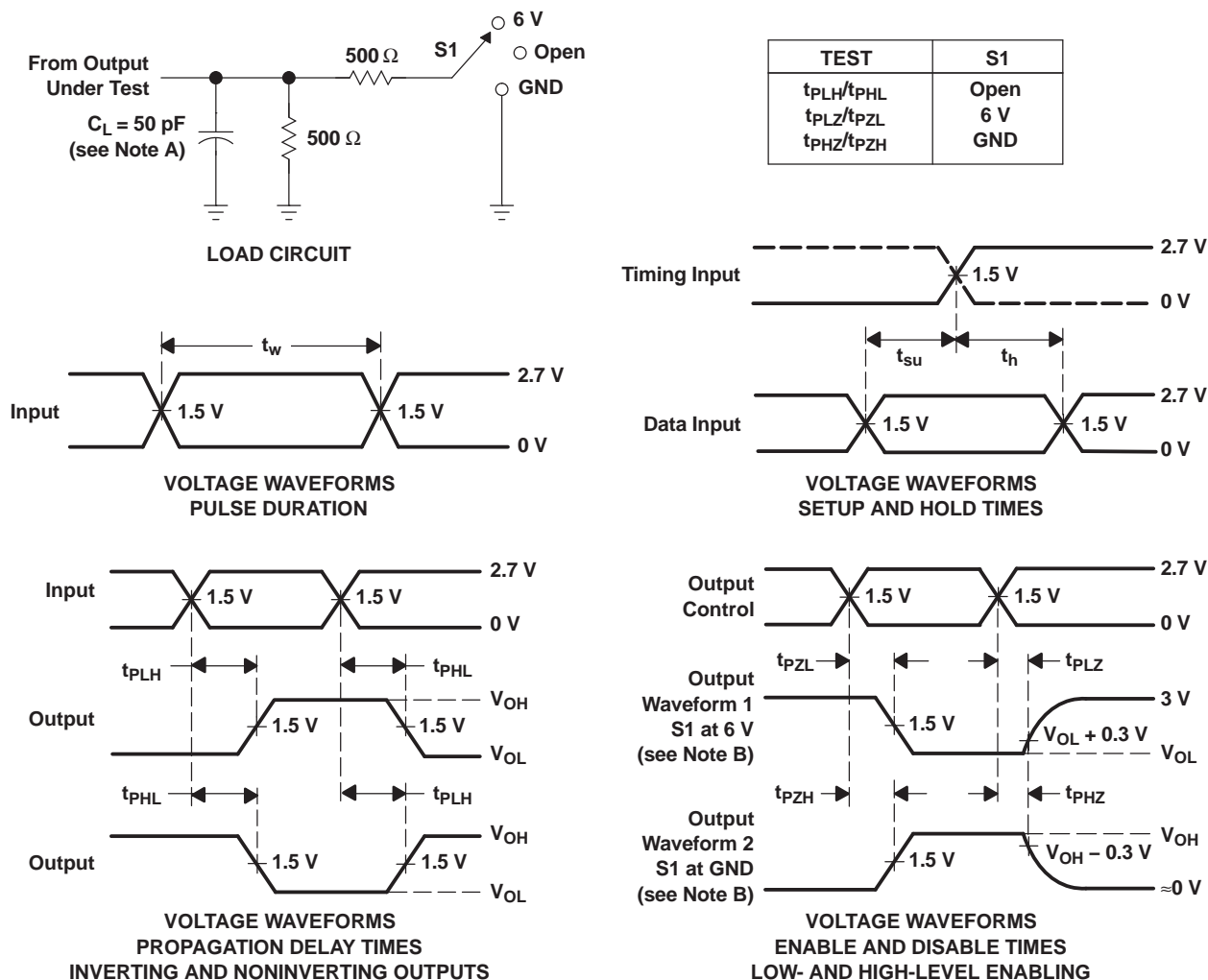
Switching Characteristics

over recommended operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16244A				SN74LVTH16244A				UNIT	
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYP ⁽¹⁾	MAX	MIN		MAX
t _{PLH}	A	Y	1.1	4.4		4.6	1.2	2.3	3.2		3.7	ns
t _{PHL}			1.1	3.6		3.9	1.2	2	3.2		3.7	
t _{PZH}	\overline{OE}	Y	1.1	4.6		5.4	1.2	2.6	4		5	ns
t _{PZL}			1.1	5.4		6.2	1.2	2.7	4		5	
t _{PHZ}	\overline{OE}	Y	1.6	5.7		6.2	2.2	3.3	4.5		5	ns
t _{PLZ}			1.2	5		4.7	2	3.1	4.2		4.4	
t _{sk(LH)}									0.5			ns
t _{sk(HL)}									0.5			

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
5962-9668501QXA	ACTIVE	CFP	WD	48	1	TBD	Call TI	Call TI	-55 to 125	5962-9668501QX A SNJ54LVTH16244 AWD	Samples
5962-9668501VXA	ACTIVE	CFP	WD	48	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9668501VX A SNV54LVTH16244 AWD	Samples
74LVTH16244ADGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16244A	Samples
74LVTH16244ADGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16244A	Samples
74LVTH16244ADGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LL244A	Samples
74LVTH16244ADGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LL244A	Samples
74LVTH16244ADLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16244A	Samples
SN74LVTH16244ADGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16244A	Samples
SN74LVTH16244ADGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LL244A	Samples
SN74LVTH16244ADL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16244A	Samples
SN74LVTH16244ADLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16244A	Samples
SN74LVTH16244ADLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16244A	Samples
SN74LVTH16244AGQLR	OBSOLETE	BGA MICROSTAR JUNIOR	GQL	56		TBD	Call TI	Call TI	-40 to 85	LL244A	
SN74LVTH16244AGRDR	OBSOLETE	BGA MICROSTAR JUNIOR	GRD	54		TBD	Call TI	Call TI	-40 to 85	LL244A	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74LVTH16244AZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LL244A	Samples
SN74LVTH16244AZRDR	ACTIVE	BGA MICROSTAR JUNIOR	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LL244A	Samples
SNJ54LVTH16244AWD	ACTIVE	CFP	WD	48	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9668501QX A SNJ54LVTH16244 AWD	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVTH16244A, SN54LVTH16244A-SP, SN74LVTH16244A :

- Catalog: [SN74LVTH16244A](#), [SN54LVTH16244A](#)
- Enhanced Product: [SN74LVTH16244A-EP](#), [SN74LVTH16244A-EP](#)
- Military: [SN54LVTH16244A](#)
- Space: [SN54LVTH16244A-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH16244ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74LVTH16244ADGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74LVTH16244ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVTH16244AZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
SN74LVTH16244AZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	330.0	16.4	5.8	8.3	1.55	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



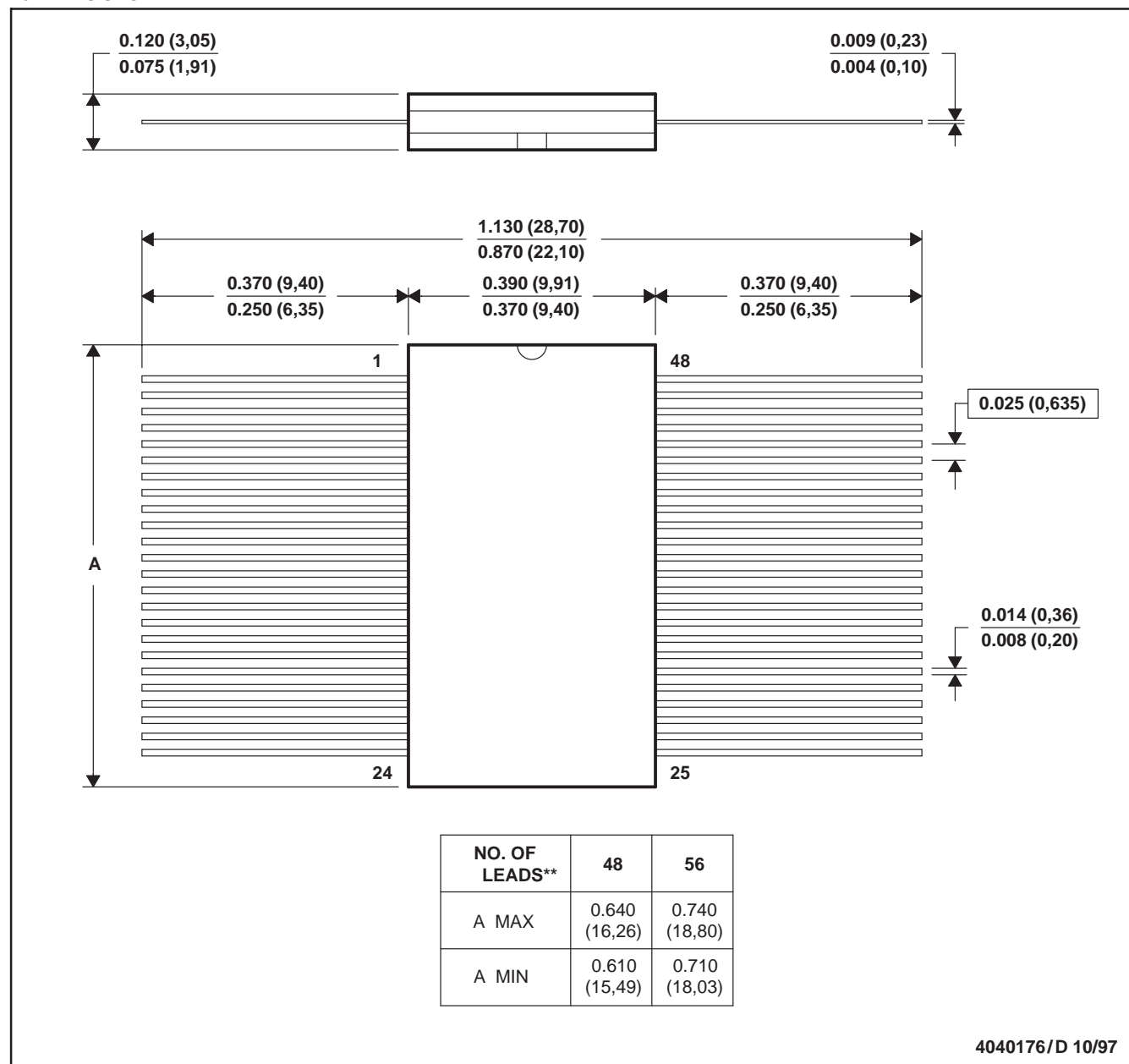
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH16244ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVTH16244ADGVR	TVSOP	DGV	48	2000	367.0	367.0	38.0
SN74LVTH16244ADLR	SSOP	DL	48	1000	367.0	367.0	55.0
SN74LVTH16244AZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	333.2	345.9	28.6
SN74LVTH16244AZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	333.2	345.9	28.6

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

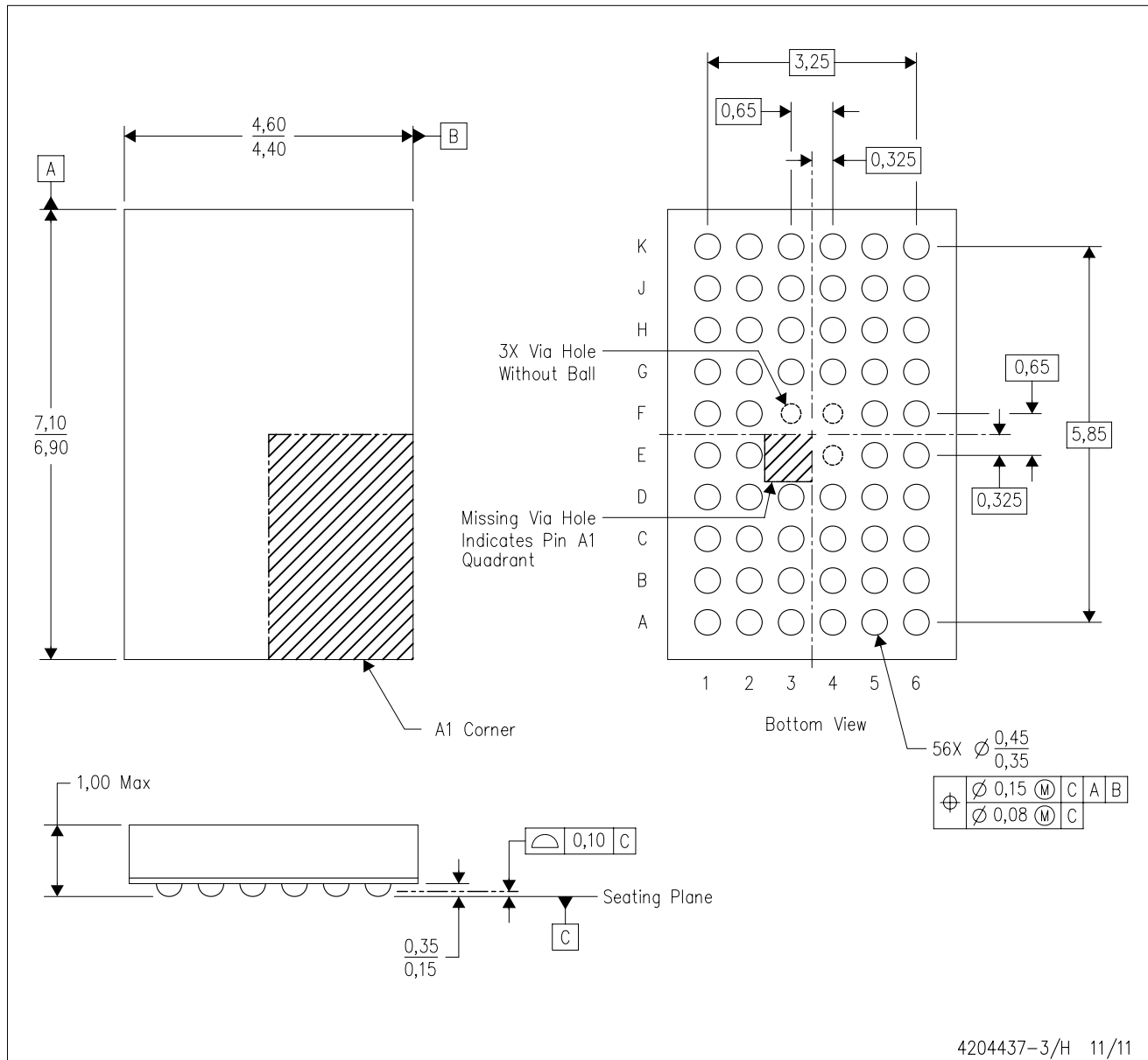
48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
 GDFP1-F56 and JEDEC MO-146AB

ZQL (R-PBGA-N56)

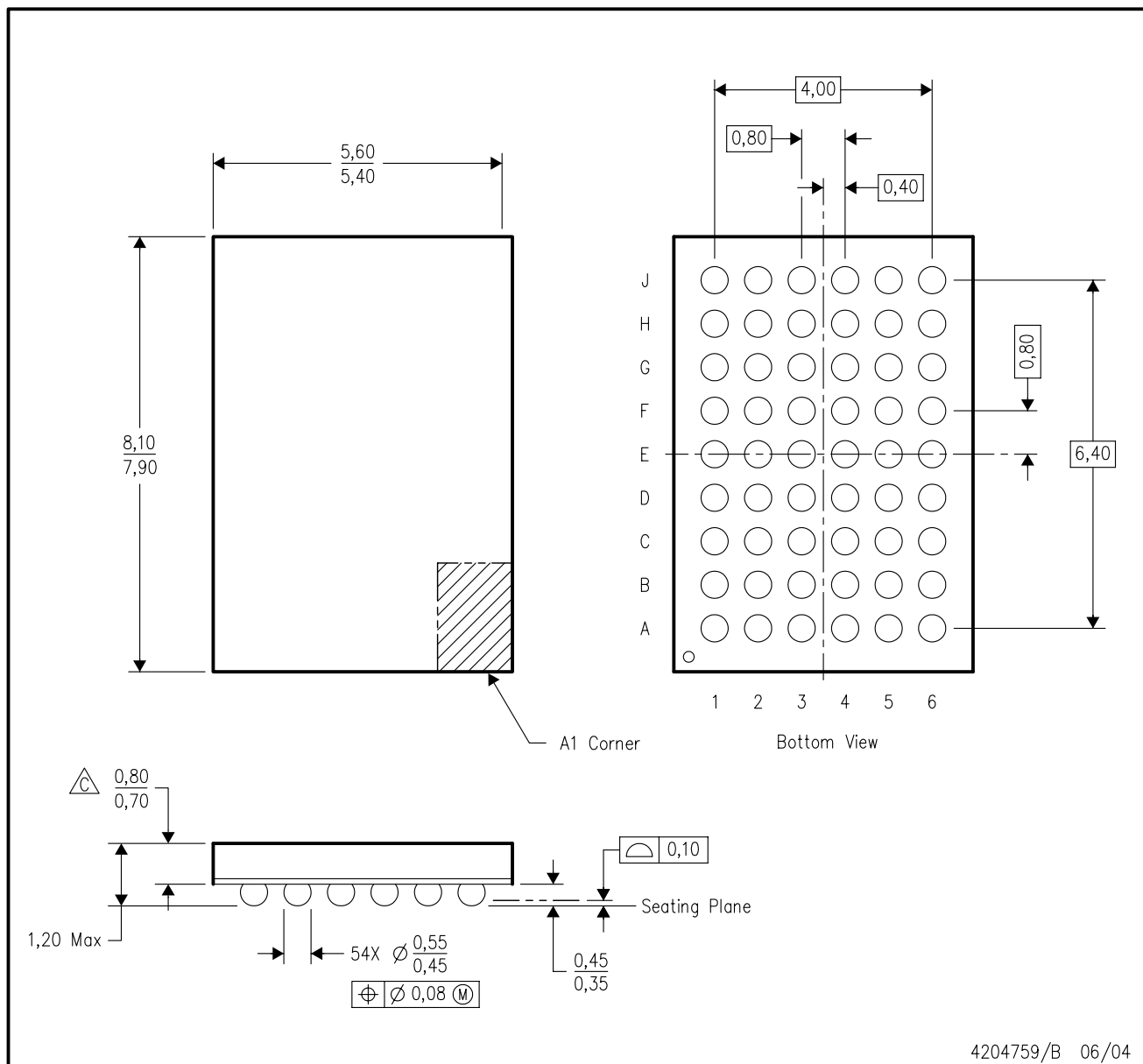
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is Pb-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

GRD (R-PBGA-N54)

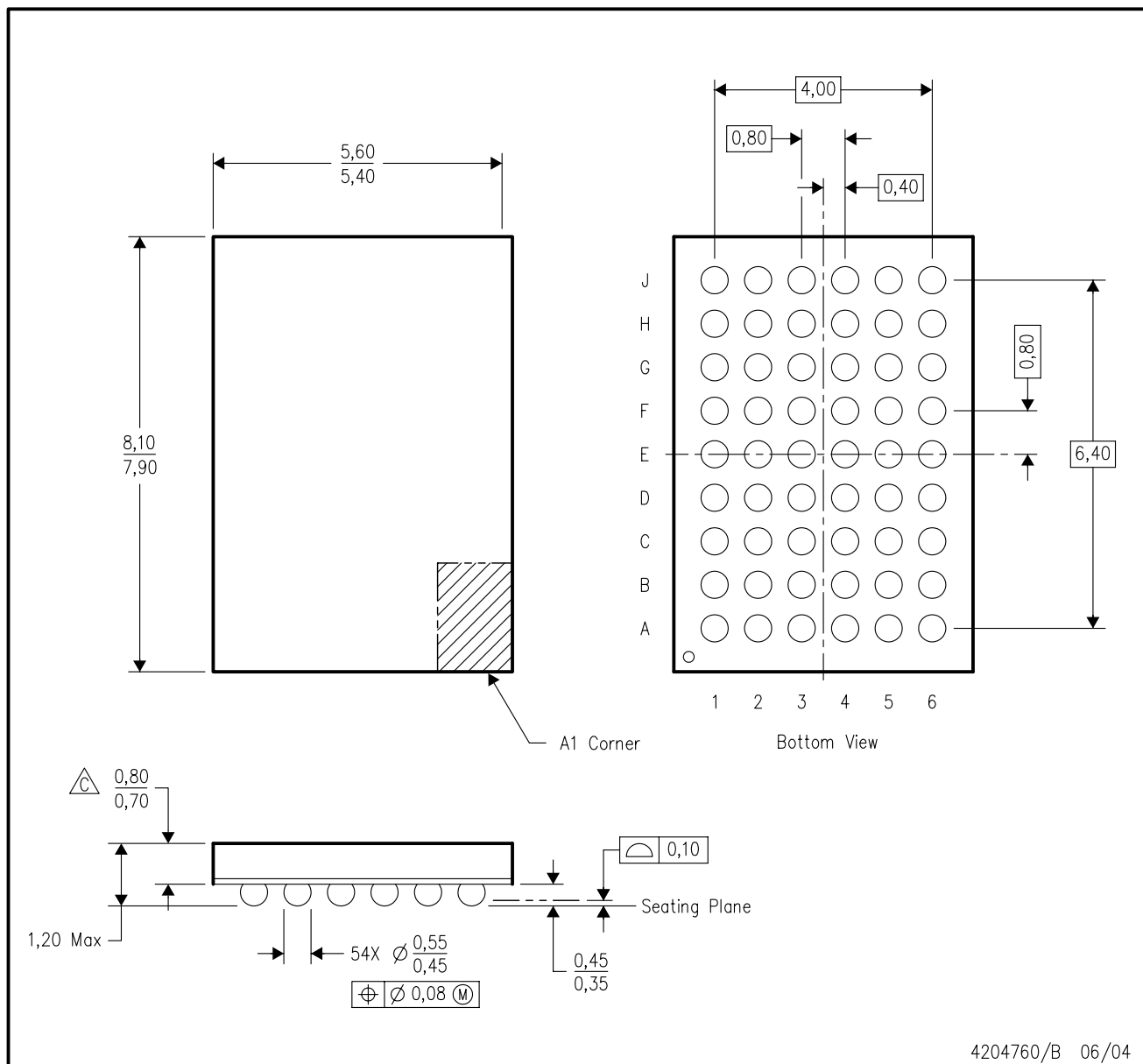
PLASTIC BALL GRID ARRAY




- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation DD.
 - D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

ZRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MO-205 variation DD.
 - D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

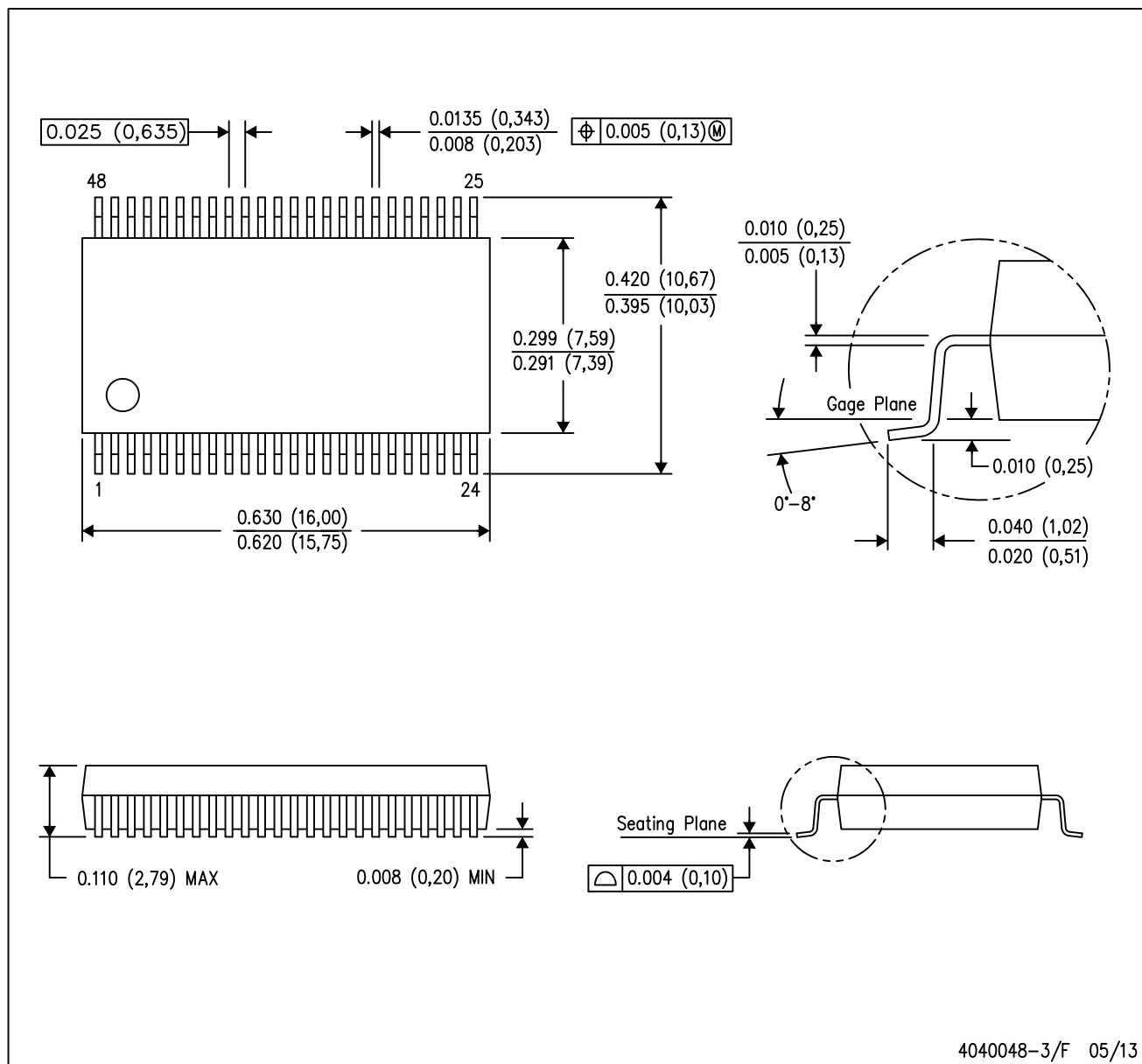
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G48)

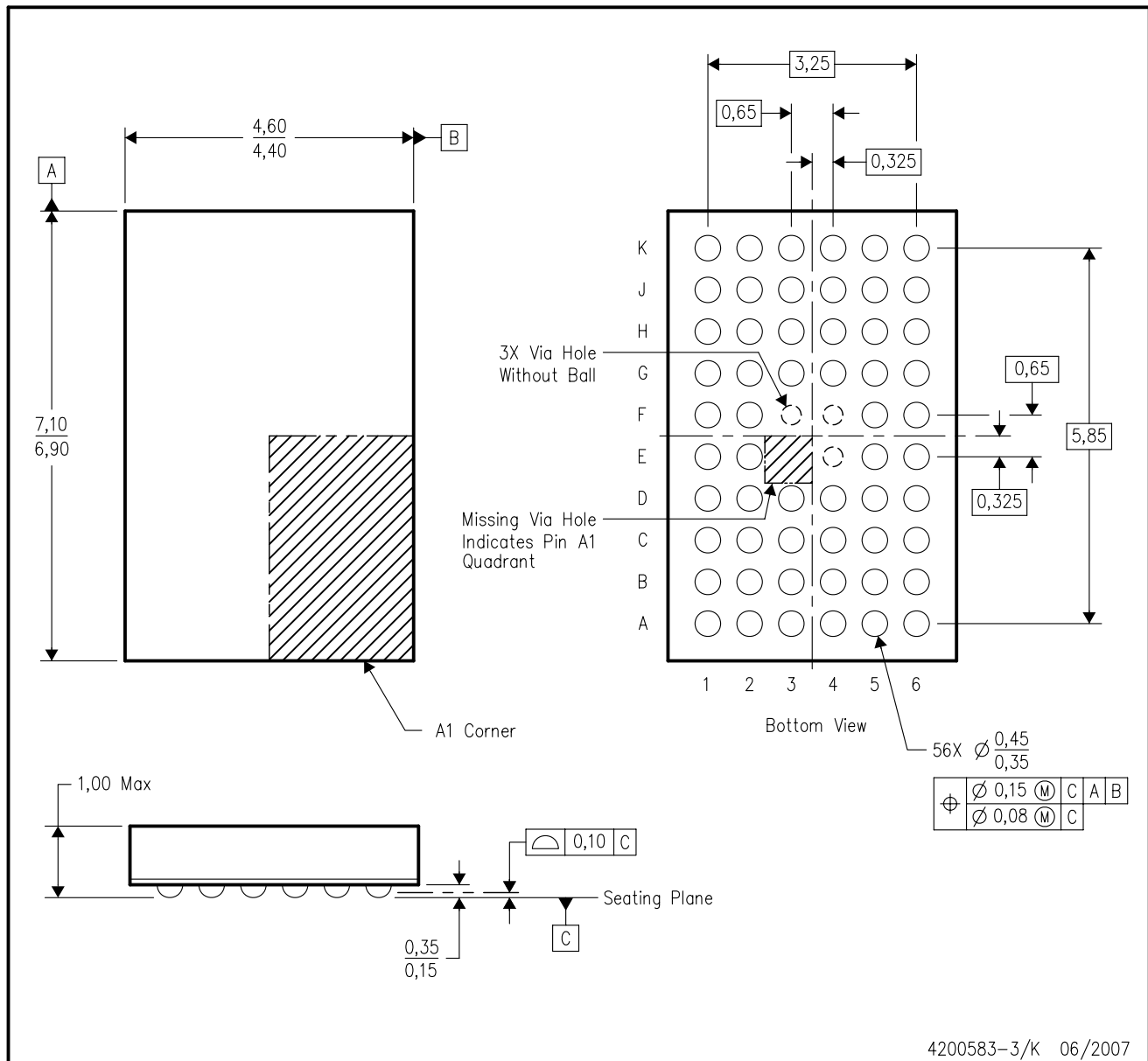
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



4200583-3/K 06/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Texas Instruments:

[SN74LVTH16244ADGVR](#) [SN74LVTH16244AGQLR](#) [SN74LVTH16244ADGGR](#) [SN74LVTH16244ADL](#)
[SN74LVTH16244ADLR](#) [74LVTH16244ADGVRE4](#) [74LVTH16244ADGGRG4](#) [74LVTH16244ADLRG4](#)
[SN74LVTH16244AZRDR](#) [SN74LVTH16244ADLG4](#) [SN74LVTH16244AZQLR](#) [74LVTH16244ADGVRG4](#)
[SN74LVTH16244AGRDR](#) [74LVTH16244ADGGRE4](#) [5962-9668501VXA](#)