



**Is Now Part of**



**ON Semiconductor®**

**To learn more about ON Semiconductor, please visit our website at**  
**[www.onsemi.com](http://www.onsemi.com)**

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (\_), the underscore (\_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (\_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at [www.onsemi.com](http://www.onsemi.com). Please email any questions regarding the system integration to [Fairchild\\_questions@onsemi.com](mailto:Fairchild_questions@onsemi.com).

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## 74LVX161284

### Low Voltage IEEE 161284 Translating Transceiver

#### General Description

The LVX161284 contains eight bidirectional data buffers and eleven control/status buffers to implement a full IEEE 1284 compliant interface. The device supports the IEEE 1284 standard and is intended to be used in an Extended Capabilities Port mode (ECP). The pinout allows for easy connection from the Peripheral (A-side) to the Host (cable side).

Outputs on the cable side can be configured to be either open drain or high drive ( $\pm 14$  mA) and are connected to a separate power supply pin ( $V_{CC}$ -cable) to allow these outputs to be driven by a higher supply voltage than the A-side. The pull-up and pull-down series termination resistance of these outputs on the cable side is optimized to drive an external cable. In addition, all inputs (except HLH) and outputs on the cable side contain internal pull-up resistors connected to the  $V_{CC}$ -cable supply to provide proper termination and pull-ups for open drain mode.

Outputs on the Peripheral side are standard low-drive CMOS outputs designed to interface with 3V logic. The DIR input controls data flow on the  $A_1$ - $A_8$ / $B_1$ - $B_8$  transceiver pins.

#### Features

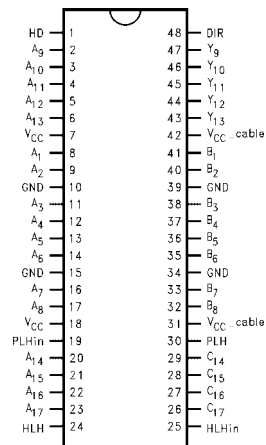
- Supports IEEE 1284 Level 1 and Level 2 signaling standards for bidirectional parallel communications between personal computers and printing peripherals
- Translation capability allows outputs on the cable side to interface with 5V signals
- All inputs have hysteresis to provide noise margin
- B and Y output resistance optimized to drive external cable
- B and Y outputs in high impedance mode during power down
- Inputs and outputs on cable side have internal pull-up resistors
- Flow-through pin configuration allows easy interface between the "Peripheral and Host"
- Replaces the function of two (2) 74ACT1284 devices

#### Ordering Code

| Order Number   | Package Number | Package Description                                                         |
|----------------|----------------|-----------------------------------------------------------------------------|
| 74LVX161284MEA | MS48A          | 48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide      |
| 74LVX161284MTD | MTD48          | 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

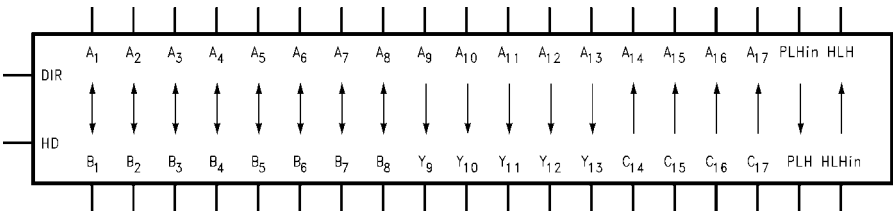
#### Connection Diagram



#### Pin Descriptions

| Pin Names           | Description                           |
|---------------------|---------------------------------------|
| HD                  | High Drive Enable Input (Active HIGH) |
| DIR                 | Direction Control Input               |
| $A_1$ - $A_8$       | Inputs or Outputs                     |
| $B_1$ - $B_8$       | Inputs or Outputs                     |
| $A_9$ - $A_{13}$    | Inputs                                |
| $Y_9$ - $Y_{13}$    | Outputs                               |
| $A_{14}$ - $A_{17}$ | Outputs                               |
| $C_{14}$ - $C_{17}$ | Inputs                                |
| PLH <sub>IN</sub>   | Peripheral Logic HIGH Input           |
| PLH                 | Peripheral Logic HIGH Output          |
| HLH <sub>IN</sub>   | Host Logic HIGH Input                 |
| HLH                 | Host Logic HIGH Output                |

Logic Symbol



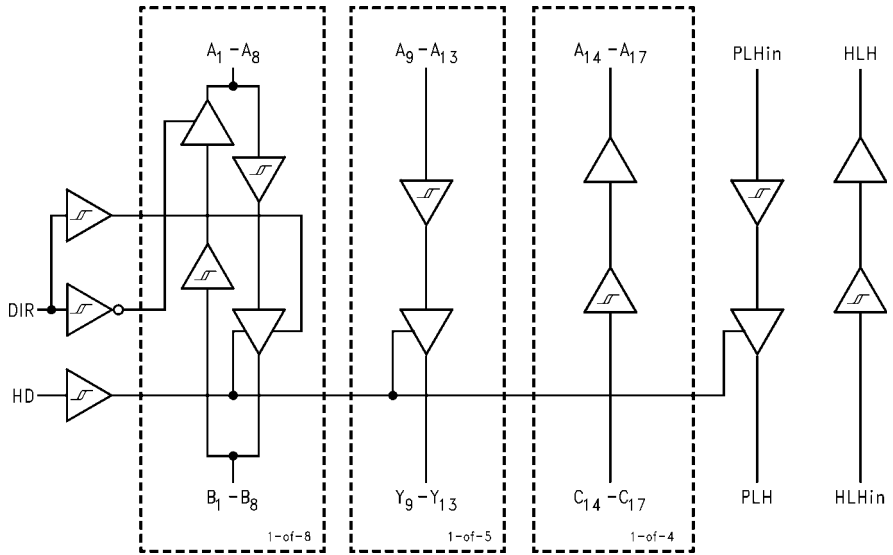
Truth Table

| Inputs |    | Outputs                                                                                                                                                                                                                                                                |
|--------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DIR    | HD |                                                                                                                                                                                                                                                                        |
| L      | L  | B <sub>1</sub> –B <sub>8</sub> Data to A <sub>1</sub> –A <sub>8</sub> , and<br>A <sub>9</sub> –A <sub>13</sub> Data to Y <sub>9</sub> –Y <sub>13</sub> (Note 1)<br>C <sub>14</sub> –C <sub>17</sub> Data to A <sub>14</sub> –A <sub>17</sub><br>PLH Open Drain Mode    |
| L      | H  | B <sub>1</sub> –B <sub>8</sub> Data to A <sub>1</sub> –A <sub>8</sub> , and<br>A <sub>9</sub> –A <sub>13</sub> Data to Y <sub>9</sub> –Y <sub>13</sub><br>C <sub>14</sub> –C <sub>17</sub> Data to A <sub>14</sub> –A <sub>17</sub>                                    |
| H      | L  | A <sub>1</sub> –A <sub>8</sub> Data to B <sub>1</sub> –B <sub>8</sub> (Note 2)<br>A <sub>9</sub> –A <sub>13</sub> Data to Y <sub>9</sub> –Y <sub>13</sub> (Note 1)<br>C <sub>14</sub> –C <sub>17</sub> Data to A <sub>14</sub> –A <sub>17</sub><br>PLH Open Drain Mode |
| H      | H  | A <sub>1</sub> –A <sub>8</sub> Data to B <sub>1</sub> –B <sub>8</sub><br>A <sub>9</sub> –A <sub>13</sub> Data to Y <sub>9</sub> –Y <sub>13</sub><br>C <sub>14</sub> –C <sub>17</sub> Data to A <sub>14</sub> –A <sub>17</sub>                                          |

Note 1: Y<sub>9</sub>–Y<sub>13</sub> Open Drain Outputs

Note 2: B<sub>1</sub>–B<sub>8</sub> Open Drain Outputs

Logic Diagram



**Absolute Maximum Ratings**(Note 3)

## Supply Voltage

|                                             |                |
|---------------------------------------------|----------------|
| $V_{CC}$                                    | -0.5V to +4.6V |
| $V_{CC}-\text{Cable}$                       | -0.5V to +7.0V |
| $V_{CC}-\text{Cable}$ Must Be $\geq V_{CC}$ |                |

Input Voltage ( $V_i$ )—(Note 4)

|                                                 |                          |
|-------------------------------------------------|--------------------------|
| $A_1-A_{13}$ , PLH <sub>IN</sub> , DIR, HD      | -0.5V to $V_{CC} + 0.5V$ |
| $B_1-B_8$ , $C_{14}-C_{17}$ , HLH <sub>IN</sub> | -0.5V to +5.5V (DC)      |
| $B_1-B_8$ , $C_{14}-C_{17}$ , HLH <sub>IN</sub> | -2.0V to +7.0V*          |
|                                                 | *40 ns Transient         |

Output Voltage ( $V_O$ )

|                                   |                          |
|-----------------------------------|--------------------------|
| $A_1-A_8$ , $A_{14}-A_{17}$ , HLH | -0.5V to $V_{CC} + 0.5V$ |
| $B_1-B_8$ , $Y_9-Y_{13}$ , PLH    | -0.5V to +5.5V (DC)      |
| $B_1-B_8$ , $Y_9-Y_{13}$ , PLH    | -2.0V to +7.0V*          |
|                                   | *40 ns Transient         |

DC Output Current ( $I_O$ )

|                          |             |
|--------------------------|-------------|
| $A_1-A_8$ , HLH          | $\pm 25$ mA |
| $B_1-B_8$ , $Y_9-Y_{13}$ | $\pm 50$ mA |
| PLH (Output LOW)         | 84 mA       |
| PLH (Output HIGH)        | -50 mA      |

Input Diode Current ( $I_{IK}$ )—(Note 4)

|                                                   |        |
|---------------------------------------------------|--------|
| DIR, HD, $A_9-A_{13}$ , PLH, HLH, $C_{14}-C_{17}$ | -20 mA |
|---------------------------------------------------|--------|

Output Diode Current ( $I_{OK}$ )

|                                   |             |
|-----------------------------------|-------------|
| $A_1-A_8$ , $A_{14}-A_{17}$ , HLH | $\pm 50$ mA |
| $B_1-B_8$ , $Y_9-Y_{13}$ , PLH    | -50 mA      |

DC Continuous  $V_{CC}$  or Ground Current $\pm 200$  mA

## Storage Temperature

-65°C to +150°C

## ESD (HBM) Last Passing Voltage

2000V

**Recommended Operating Conditions**

## Supply Voltage

|                       |              |
|-----------------------|--------------|
| $V_{CC}$              | 3.0V to 3.6V |
| $V_{CC}-\text{Cable}$ | 3.0V to 5.5V |

DC Input Voltage ( $V_i$ )

|                              |                |
|------------------------------|----------------|
| Open Drain Voltage ( $V_O$ ) | 0V to $V_{CC}$ |
|------------------------------|----------------|

Operating Temperature ( $T_A$ )

-40°C to +85°C

**Note 3:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Fairchild does not recommend operation outside the databook specifications.

**Note 4:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

| Symbol          | Parameter                               |                                                                | V <sub>CC</sub><br>(V) | V <sub>CC</sub> —Cable<br>(V) | T <sub>A</sub> = 0°C<br>to +70°C | T <sub>A</sub> = -40°C<br>to +85°C | Units | Conditions                                               |
|-----------------|-----------------------------------------|----------------------------------------------------------------|------------------------|-------------------------------|----------------------------------|------------------------------------|-------|----------------------------------------------------------|
|                 |                                         |                                                                |                        |                               | Guaranteed Limits                |                                    |       |                                                          |
| V <sub>IK</sub> | Input Clamp<br>Diode Voltage            |                                                                | 3.0                    | 3.0                           | -1.2                             | -1.2                               | V     | I <sub>I</sub> = -18 mA                                  |
| V <sub>IH</sub> | Minimum                                 | A <sub>n</sub> , B <sub>n</sub> , PLH <sub>IIN</sub> , DIR, HD | 3.0-3.6                | 3.0-5.5                       | 2.0                              | 2.0                                | V     |                                                          |
|                 | HIGH Level                              | C <sub>n</sub>                                                 | 3.0-3.6                | 3.0-5.5                       | 2.3                              | 2.3                                |       |                                                          |
|                 | Input Voltage                           | HLH <sub>IIN</sub>                                             | 3.0-3.6                | 3.0-5.5                       | 2.6                              | 2.6                                |       |                                                          |
| V <sub>IL</sub> | Maximum                                 | A <sub>n</sub> , B <sub>n</sub> , PLH <sub>IIN</sub> , DIR, HD | 3.0-3.6                | 3.0-5.5                       | 0.8                              | 0.8                                | V     |                                                          |
|                 | LOW Level                               | C <sub>n</sub>                                                 | 3.0-3.6                | 3.0-5.5                       | 0.8                              | 0.8                                |       |                                                          |
|                 | Input Voltage                           | HLH <sub>IIN</sub>                                             | 3.0-3.6                | 3.0-5.5                       | 1.6                              | 1.6                                |       |                                                          |
| ΔV <sub>T</sub> | Minimum Input<br>Hysteresis             | A <sub>n</sub> , B <sub>n</sub> , PLH <sub>IIN</sub> , DIR, HD | 3.3                    | 5.0                           | 0.4                              | 0.4                                | V     | V <sub>T</sub> <sup>+</sup> -V <sub>T</sub> <sup>-</sup> |
|                 |                                         | C <sub>n</sub>                                                 | 3.3                    | 5.0                           | 0.8                              | 0.8                                |       | V <sub>T</sub> <sup>+</sup> -V <sub>T</sub> <sup>-</sup> |
|                 |                                         | HLH <sub>IIN</sub>                                             | 3.3                    | 5.0                           | 0.2                              | 0.2                                |       | V <sub>T</sub> <sup>+</sup> -V <sub>T</sub> <sup>-</sup> |
| V <sub>OH</sub> | Minimum HIGH<br>Level Output<br>Voltage | A <sub>n</sub> , HLH                                           | 3.0                    | 3.0                           | 2.8                              | 2.8                                | V     | I <sub>OH</sub> = -50 μA                                 |
|                 |                                         |                                                                | 3.0                    | 3.0                           | 2.4                              | 2.4                                |       | I <sub>OH</sub> = -4 mA                                  |
|                 |                                         | B <sub>n</sub> , Y <sub>n</sub>                                | 3.0                    | 3.0                           | 2.0                              | 2.0                                |       | I <sub>OH</sub> = -14 mA                                 |
|                 |                                         | B <sub>n</sub> , Y <sub>n</sub>                                | 3.0                    | 4.5                           | 2.23                             | 2.23                               |       | I <sub>OH</sub> = -14 mA                                 |
|                 |                                         | PLH                                                            | 3.15                   | 3.15                          | 3.1                              | 3.1                                |       | I <sub>OH</sub> = -500 μA                                |

## DC Electrical Characteristics (Continued)

| Symbol                | Parameter                                   |                                                                                                        | V <sub>CC</sub><br>(V) | V <sub>CC—Cable</sub><br>(V) | T <sub>A</sub> = 0°C<br>to +70°C | T <sub>A</sub> = -40°C<br>to +85°C | Units | Conditions                              |
|-----------------------|---------------------------------------------|--------------------------------------------------------------------------------------------------------|------------------------|------------------------------|----------------------------------|------------------------------------|-------|-----------------------------------------|
|                       |                                             |                                                                                                        |                        |                              | Guaranteed Limits                |                                    |       |                                         |
| V <sub>OL</sub>       | Maximum LOW Level Output Voltage            | A <sub>n</sub> , HLH                                                                                   | 3.0                    | 3.0                          | 0.2                              | 0.2                                | V     | I <sub>OL</sub> = 50 μA                 |
|                       |                                             |                                                                                                        | 3.0                    | 3.0                          | 0.4                              | 0.4                                |       | I <sub>OL</sub> = 4 mA                  |
|                       |                                             | B <sub>n</sub> , Y <sub>n</sub>                                                                        | 3.0                    | 3.0                          | 0.8                              | 0.8                                |       | I <sub>OL</sub> = 14 mA                 |
|                       |                                             | B <sub>n</sub> , Y <sub>n</sub>                                                                        | 3.0                    | 4.5                          | 0.77                             | 0.77                               |       | I <sub>OL</sub> = 14 mA                 |
|                       |                                             | PLH                                                                                                    | 3.0                    | 3.0                          | 0.85                             | 0.95                               |       | I <sub>OL</sub> = 84 mA                 |
|                       |                                             | PLH                                                                                                    | 3.0                    | 4.5                          | 0.8                              | 0.9                                |       | I <sub>OL</sub> = 84 mA                 |
| R <sub>D</sub>        | Maximum Output Impedance                    | B <sub>1</sub> –B <sub>8</sub> , Y <sub>9</sub> –Y <sub>13</sub>                                       | 3.3                    | 3.3                          | 60                               | 60                                 | Ω     | (Note 5)(Note 7)                        |
|                       |                                             |                                                                                                        | 3.3                    | 5.0                          | 55                               | 55                                 |       |                                         |
|                       | Minimum Output Impedance                    | B <sub>1</sub> –B <sub>8</sub> , Y <sub>9</sub> –Y <sub>13</sub>                                       | 3.3                    | 3.3                          | 30                               | 30                                 |       | (Note 5)(Note 7)                        |
|                       |                                             |                                                                                                        | 3.3                    | 5.0                          | 35                               | 35                                 |       |                                         |
| R <sub>P</sub>        | Maximum Pull-Up Resistance                  | B <sub>1</sub> –B <sub>8</sub> , Y <sub>9</sub> –Y <sub>13</sub> ,<br>C <sub>14</sub> –C <sub>17</sub> | 3.3                    | 3.3                          | 1650                             | 1650                               | Ω     |                                         |
|                       |                                             |                                                                                                        | 3.3                    | 5.0                          | 1650                             | 1650                               |       |                                         |
|                       | Minimum Pull-Up Resistance                  | B <sub>1</sub> –B <sub>8</sub> , Y <sub>9</sub> –Y <sub>13</sub><br>C <sub>14</sub> –C <sub>17</sub>   | 3.3                    | 3.3                          | 1150                             | 1150                               | Ω     |                                         |
|                       |                                             |                                                                                                        | 3.3                    | 5.0                          | 1150                             | 1150                               |       |                                         |
| I <sub>IH</sub>       | Maximum Input Current in HIGH State         | A <sub>9</sub> –A <sub>13</sub> , PLH <sub>IN</sub> ,<br>HD, DIR, HLH <sub>IN</sub>                    | 3.6                    | 3.6                          | 1.0                              | 1.0                                | μA    | V <sub>I</sub> = 3.6V                   |
|                       |                                             |                                                                                                        | 3.6                    | 3.6                          | 50.0                             | 50.0                               |       | V <sub>I</sub> = 3.6V                   |
|                       |                                             | C <sub>14</sub> –C <sub>17</sub>                                                                       | 3.6                    | 5.5                          | 100                              | 100                                |       | V <sub>I</sub> = 5.5V                   |
| I <sub>IL</sub>       | Maximum Input Current in LOW State          | A <sub>9</sub> –A <sub>13</sub> , PLH <sub>IN</sub> ,<br>HD, DIR, HLH <sub>IN</sub>                    | 3.6                    | 3.6                          | –1.0                             | –1.0                               | μA    | V <sub>I</sub> = 0.0V                   |
|                       |                                             |                                                                                                        | 3.6                    | 3.6                          | –3.5                             | –3.5                               | mA    | V <sub>I</sub> = 0.0V                   |
|                       |                                             | C <sub>14</sub> –C <sub>17</sub>                                                                       | 3.6                    | 5.5                          | –5.0                             | –5.0                               | mA    | V <sub>I</sub> = 0.0V                   |
| I <sub>OZH</sub>      | Maximum Output Disable Current (HIGH)       | A <sub>1</sub> –A <sub>8</sub>                                                                         | 3.6                    | 3.6                          | 20                               | 20                                 | μA    | V <sub>O</sub> = 3.6V                   |
|                       |                                             | B <sub>1</sub> –B <sub>8</sub>                                                                         | 3.6                    | 3.6                          | 50                               | 50                                 | μA    | V <sub>O</sub> = 3.6V                   |
|                       |                                             | B <sub>1</sub> –B <sub>8</sub>                                                                         | 3.6                    | 5.5                          | 100                              | 100                                | μA    | V <sub>O</sub> = 5.5V                   |
| I <sub>OZL</sub>      | Maximum Output Disable Current (LOW)        | A <sub>1</sub> –A <sub>8</sub>                                                                         | 3.6                    | 3.6                          | –20                              | –20                                | μA    | V <sub>O</sub> = 0.0V                   |
|                       |                                             | B <sub>1</sub> –B <sub>8</sub>                                                                         | 3.6                    | 3.6                          | –3.5                             | –3.5                               | mA    |                                         |
|                       |                                             | B <sub>1</sub> –B <sub>8</sub>                                                                         | 3.6                    | 5.5                          | –5.0                             | –5.0                               | mA    |                                         |
| I <sub>OFF</sub>      | Power Down Output Leakage                   | B <sub>1</sub> –B <sub>8</sub> , Y <sub>9</sub> –Y <sub>13</sub> ,<br>PLH                              | 0.0                    | 0.0                          | 100                              | 100                                | μA    | V <sub>O</sub> = 5.5V                   |
| I <sub>OFF</sub>      | Power Down Input Leakage                    | C <sub>14</sub> –C <sub>17</sub> , HLH <sub>IN</sub>                                                   | 0.0                    | 0.0                          | 100                              | 100                                | μA    | V <sub>I</sub> = 5.5V                   |
| I <sub>OFF—ICC</sub>  | Power Down Leakage to V <sub>CC</sub>       |                                                                                                        | 0.0                    | 0.0                          | 250                              | 250                                | μA    | (Note 6)                                |
| I <sub>OFF—ICC2</sub> | Power Down Leakage to V <sub>CC—Cable</sub> |                                                                                                        | 0.0                    | 0.0                          | 250                              | 250                                | μA    | (Note 6)                                |
| I <sub>CC</sub>       | Maximum Supply Current                      |                                                                                                        | 3.6                    | 3.6                          | 45                               | 45                                 | mA    | V <sub>I</sub> = V <sub>CC</sub> or GND |
|                       |                                             |                                                                                                        | 3.6                    | 5.5                          | 70                               | 70                                 | mA    | V <sub>I</sub> = V <sub>CC</sub> or GND |

**Note 5:** Output impedance is measured with the output active LOW and active HIGH (HD = HIGH).

**Note 6:** Power-down leakage to V<sub>CC</sub> or V<sub>CC—Cable</sub> is tested by simultaneously forcing all pins on the cable-side (B<sub>1</sub>–B<sub>8</sub>, Y<sub>9</sub>–Y<sub>13</sub>, PLH, C<sub>14</sub>–C<sub>17</sub> and HLH<sub>IN</sub>) to 5.5V and measuring the resulting I<sub>CC</sub> or I<sub>CC—Cable</sub>.

**Note 7:** This parameter is guaranteed but not tested, characterized only.

## AC Electrical Characteristics

| Symbol                              | Parameter                                                                                                                       | T <sub>A</sub> = 0°C to +70°C     |            | T <sub>A</sub> = -40°C to +85°C   |            | Units | Figure Number         |
|-------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|------------|-----------------------------------|------------|-------|-----------------------|
|                                     |                                                                                                                                 | V <sub>CC</sub> = 3.0V–3.6V       |            | V <sub>CC</sub> = 3.0V–3.6V       |            |       |                       |
|                                     |                                                                                                                                 | V <sub>CC—Cable</sub> = 3.0V–5.5V |            | V <sub>CC—Cable</sub> = 3.0V–5.5V |            |       |                       |
|                                     |                                                                                                                                 | Min                               | Max        | Min                               | Max        |       |                       |
| t <sub>PHL</sub>                    | A <sub>1</sub> –A <sub>8</sub> to B <sub>1</sub> –B <sub>8</sub>                                                                | 2.0                               | 40.0       | 2.0                               | 44.0       | ns    | Figure 1              |
| t <sub>PLH</sub>                    | A <sub>1</sub> –A <sub>8</sub> to B <sub>1</sub> –B <sub>8</sub>                                                                | 2.0                               | 40.0       | 2.0                               | 44.0       | ns    | Figure 2              |
| t <sub>PHL</sub>                    | B <sub>1</sub> –B <sub>8</sub> to A <sub>1</sub> –A <sub>8</sub>                                                                | 2.0                               | 40.0       | 2.0                               | 44.0       | ns    | Figure 3              |
| t <sub>PLH</sub>                    | B <sub>1</sub> –B <sub>8</sub> to A <sub>1</sub> –A <sub>8</sub>                                                                | 2.0                               | 40.0       | 2.0                               | 44.0       | ns    | Figure 3              |
| t <sub>PHL</sub>                    | A <sub>9</sub> –A <sub>13</sub> to Y <sub>9</sub> –Y <sub>13</sub>                                                              | 2.0                               | 40.0       | 2.0                               | 44.0       | ns    | Figure 1              |
| t <sub>PLH</sub>                    | A <sub>9</sub> –A <sub>13</sub> to Y <sub>9</sub> –Y <sub>13</sub>                                                              | 2.0                               | 40.0       | 2.0                               | 44.0       | ns    | Figure 2              |
| t <sub>PHL</sub>                    | C <sub>14</sub> –C <sub>17</sub> to A <sub>14</sub> –A <sub>17</sub>                                                            | 2.0                               | 40.0       | 2.0                               | 44.0       | ns    | Figure 3              |
| t <sub>PLH</sub>                    | C <sub>14</sub> –C <sub>17</sub> to A <sub>14</sub> –A <sub>17</sub>                                                            | 2.0                               | 40.0       | 2.0                               | 44.0       | ns    | Figure 3              |
| t <sub>SKEW</sub>                   | LH–LH or HL–HL                                                                                                                  |                                   | 10.0       |                                   | 12.0       | ns    | (Note 9)              |
| t <sub>PHL</sub>                    | PLH <sub>IN</sub> to PLH                                                                                                        | 2.0                               | 40.0       | 2.0                               | 44.0       | ns    | Figure 1              |
| t <sub>PLH</sub>                    | PLH <sub>IN</sub> to PLH                                                                                                        | 2.0                               | 40.0       | 2.0                               | 44.0       | ns    | Figure 2              |
| t <sub>PHL</sub>                    | HLH <sub>IN</sub> to HLH                                                                                                        | 2.0                               | 40.0       | 2.0                               | 44.0       | ns    | Figure 3              |
| t <sub>PLH</sub>                    | HLH <sub>IN</sub> to HLH                                                                                                        | 2.0                               | 40.0       | 2.0                               | 44.0       | ns    | Figure 3              |
| t <sub>PHZ</sub>                    | Output Disable Time                                                                                                             | 2.0                               | 15.0       | 2.0                               | 18.0       | ns    | Figure 7              |
| t <sub>PLZ</sub>                    | DIR to A <sub>1</sub> –A <sub>8</sub>                                                                                           | 2.0                               | 15.0       | 2.0                               | 18.0       |       |                       |
| t <sub>PZH</sub>                    | Output Enable Time                                                                                                              | 2.0                               | 50.0       | 2.0                               | 50.0       | ns    | Figure 8              |
| t <sub>PZL</sub>                    | DIR to A <sub>1</sub> –A <sub>8</sub>                                                                                           | 2.0                               | 50.0       | 2.0                               | 50.0       |       |                       |
| t <sub>PHZ</sub>                    | Output Disable Time                                                                                                             | 2.0                               | 50.0       | 2.0                               | 50.0       | ns    | Figure 9              |
| t <sub>PLZ</sub>                    | DIR to B <sub>1</sub> –B <sub>8</sub>                                                                                           | 2.0                               | 50.0       | 2.0                               | 50.0       |       |                       |
| t <sub>PEN</sub>                    | Output Enable Time                                                                                                              | 2.0                               | 25.0       | 2.0                               | 28.0       | ns    | Figure 2              |
|                                     | HD to B <sub>1</sub> –B <sub>8</sub> , Y <sub>9</sub> –Y <sub>13</sub>                                                          | 2.0                               | 25.0       | 2.0                               | 28.0       |       |                       |
| t <sub>PDIS</sub>                   | Output Disable Time                                                                                                             | 2.0                               | 25.0       | 2.0                               | 28.0       | ns    | Figure 2              |
|                                     | HD to B <sub>1</sub> –B <sub>8</sub> , Y <sub>9</sub> –Y <sub>13</sub>                                                          | 2.0                               | 25.0       | 2.0                               | 28.0       |       |                       |
| t <sub>PEN</sub> –t <sub>PDIS</sub> | Output Enable–<br>Output Disable                                                                                                |                                   | 10.0       |                                   | 12.0       | ns    |                       |
| t <sub>SLEW</sub>                   | Output Slew Rate                                                                                                                |                                   |            |                                   |            |       |                       |
| t <sub>PLH</sub>                    | B <sub>1</sub> –B <sub>8</sub> , Y <sub>9</sub> –Y <sub>13</sub>                                                                | 0.05                              | 0.40       | 0.05                              | 0.40       | V/ns  | Figure 5              |
| t <sub>PHL</sub>                    |                                                                                                                                 | 0.05                              | 0.40       | 0.05                              | 0.40       |       | Figure 4              |
| t <sub>r</sub> , t <sub>f</sub>     | t <sub>RISE</sub> and t <sub>FALL</sub><br>B <sub>1</sub> –B <sub>8</sub> (Note 8),<br>Y <sub>9</sub> –Y <sub>13</sub> (Note 8) |                                   | 120<br>120 |                                   | 120<br>120 | ns    | Figure 6<br>(Note 10) |

**Note 8:** Open Drain

**Note 9:** t<sub>SKEW</sub> is measured for common edge output transitions and compares the measured propagation delay for a given path type:

- (i) A<sub>1</sub>–A<sub>8</sub> to B<sub>1</sub>–B<sub>8</sub>, A<sub>9</sub>–A<sub>13</sub> to Y<sub>9</sub>–Y<sub>13</sub>
- (ii) B<sub>1</sub>–B<sub>8</sub> to A<sub>1</sub>–A<sub>8</sub>
- (iii) C<sub>14</sub>–C<sub>17</sub> to A<sub>14</sub>–A<sub>17</sub>

**Note 10:** This parameter is guaranteed but not tested, characterized only.

## Capacitance

| Symbol                     | Parameter           | Typ | Units | Conditions                                                                                                                                      |
|----------------------------|---------------------|-----|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| C <sub>IN</sub>            | Input Capacitance   | 3   | pF    | V <sub>CC</sub> = 0.0V (HD, DIR, A <sub>9</sub> –A <sub>13</sub> , C <sub>14</sub> –C <sub>17</sub> , PLH <sub>IN</sub> and HLH <sub>IN</sub> ) |
| C <sub>I/O</sub> (Note 11) | I/O Pin Capacitance | 5   | pF    | V <sub>CC</sub> = 3.3V                                                                                                                          |

**Note 11:** C<sub>I/O</sub> is measured at frequency = 1 MHz, per MIL-STD-883B, Method 3012

## AC Loading and Waveforms

Pulse Generator for all pulses: Rate  $\leq 1.0$  MHz;  $Z_O \leq 50\Omega$ ;  $t_f \leq 2.5$  ns,  $t_r \leq 2.5$  ns.

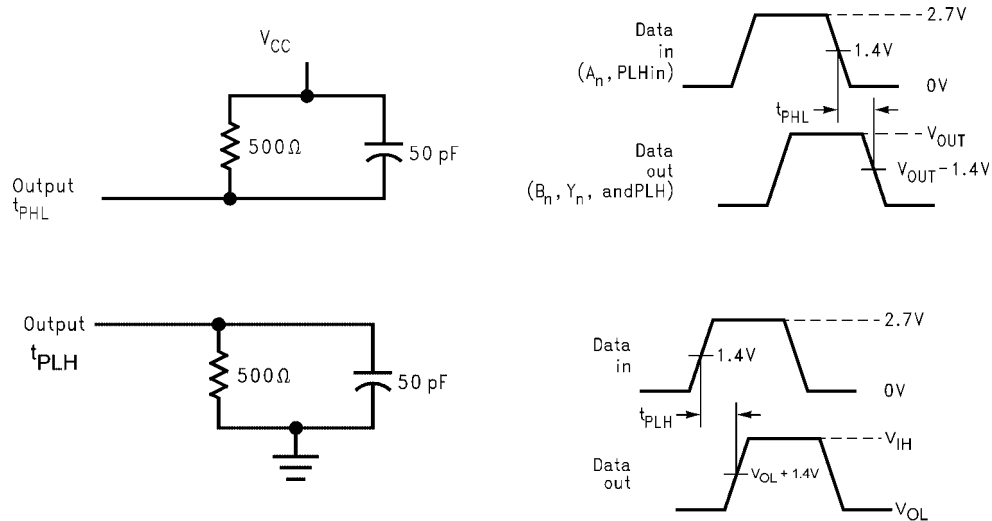


FIGURE 1. Port A to B and A to Y Propagation Delay Waveforms

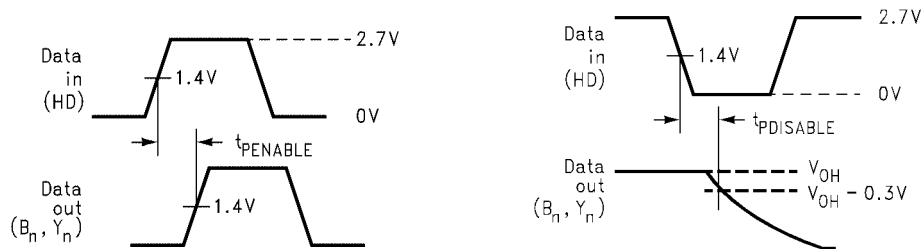


FIGURE 2. Port A to B and A to Y Output Waveforms

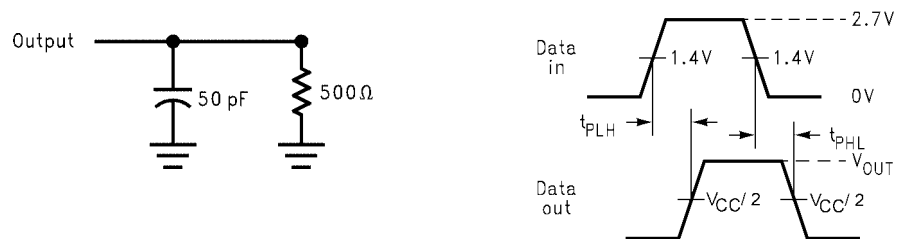


FIGURE 3. Port B to A, C to A and HLH in to HLH Propagation Delay Waveforms

## AC Loading and Waveforms (Continued)

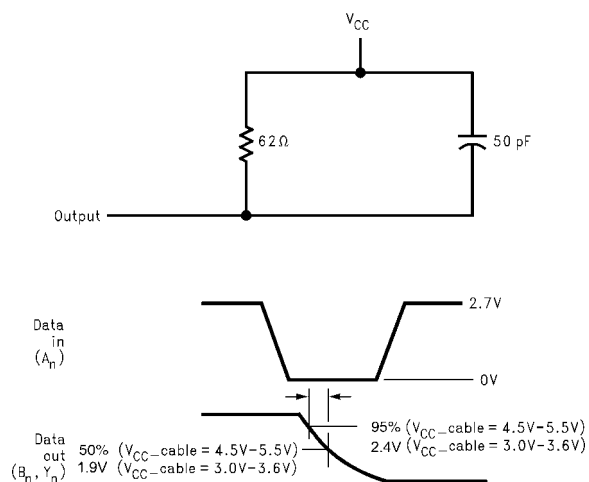


FIGURE 4. Port A to B and A to Y HL Slew Test Load and Waveforms

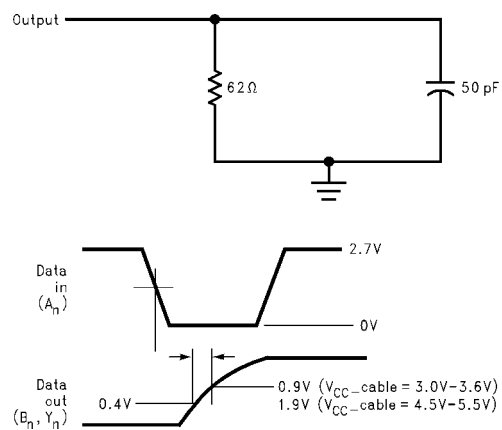


FIGURE 5. Port A to B and A to Y LH Slew Test Load and Waveforms



## AC Loading and Waveforms (Continued)

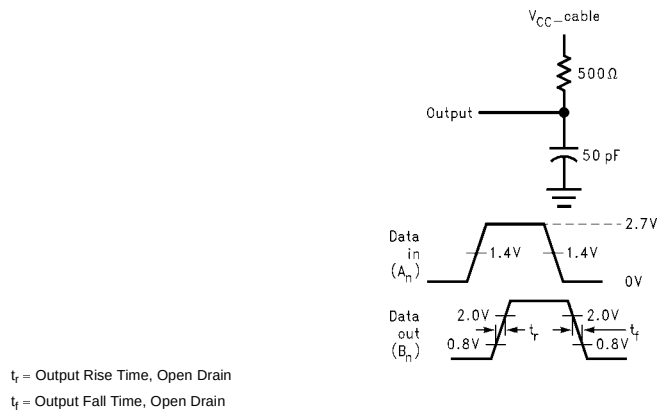
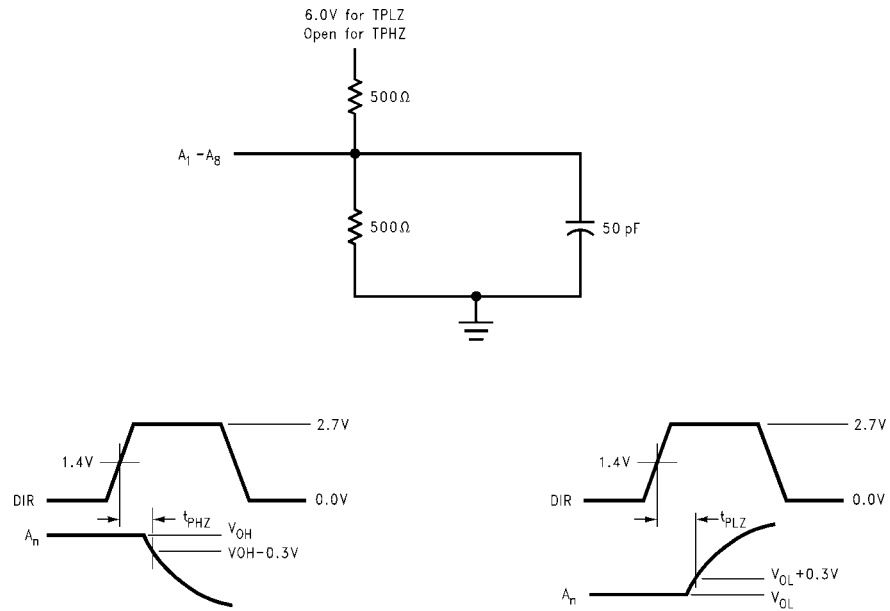
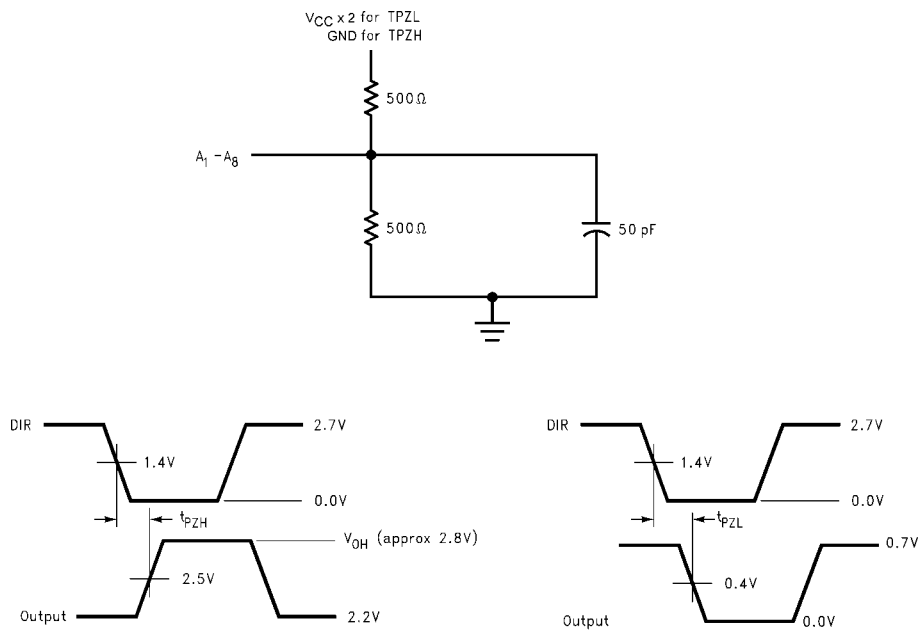
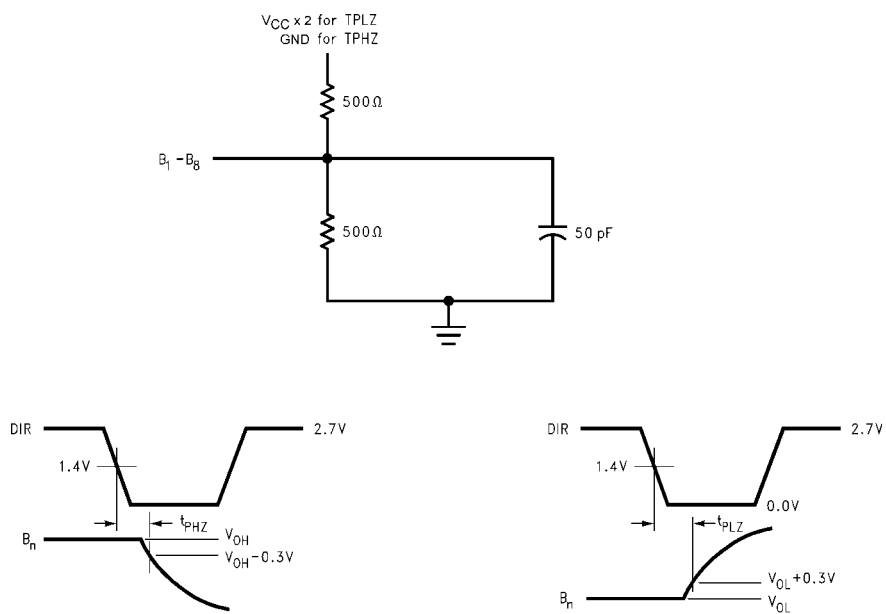


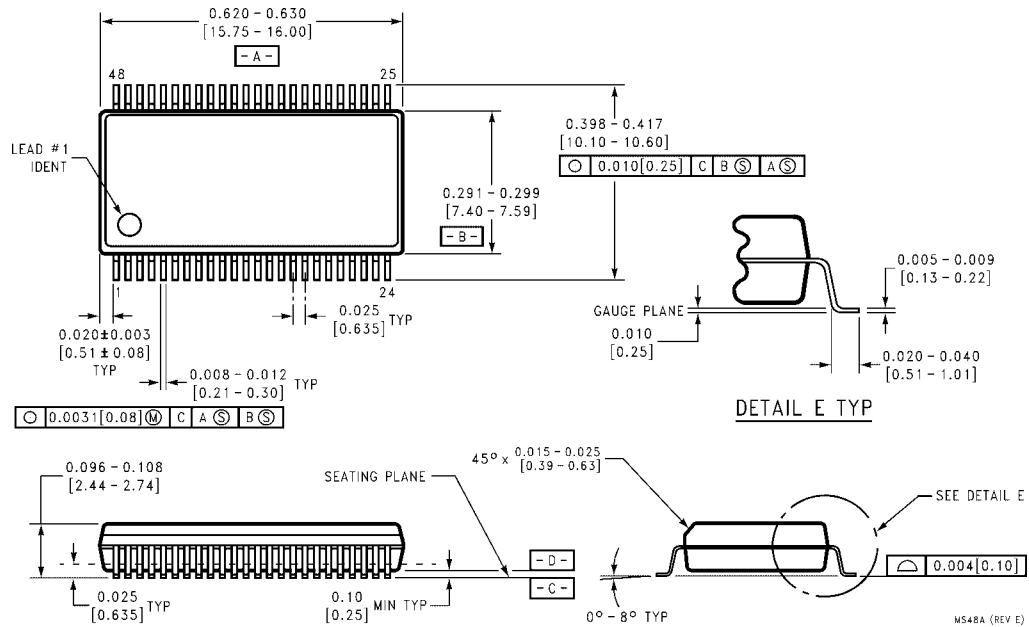
FIGURE 6. Ports A to B and A to Y Rise and Fall Test Load and Waveforms for Open Drain Outputs

FIGURE 7.  $t_{PHZ}$  and  $t_{PLZ}$  Test Load and Waveforms, DIR to  $A_1$ - $A_8$

## AC Loading and Waveforms (Continued)

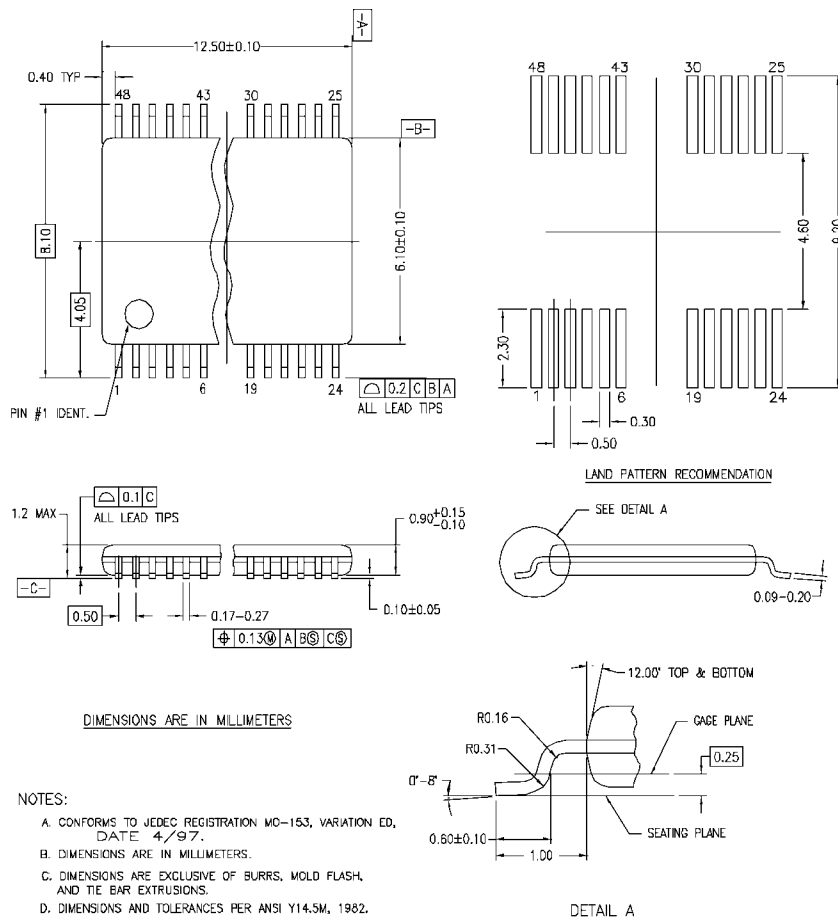
FIGURE 8.  $t_{PZH}$  and  $t_{PZL}$  Test Load and Waveforms, DIR to A<sub>1</sub>-A<sub>8</sub>FIGURE 9.  $t_{PHZ}$  and  $t_{PLZ}$  Test Load and Waveforms  
DIR to B<sub>1</sub>-B<sub>8</sub>

# Physical Dimensions inches (millimeters) unless otherwise noted



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS48A**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



MTD48REV C

## 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910

**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local  
Sales Representative

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor:](#)

[74LVX161284MTDX](#) [74LVX161284MEA](#) [74LVX161284MTD](#) [74LVX161284MEAX](#)