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74LVX573

Low Voltage Octal Latch with 3-STATE Outputs

General Description

The LVX573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (\overline{OE}) inputs. The LVX573 is functionally identical to the LVX373 but with inputs and outputs on opposite sides of the package. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

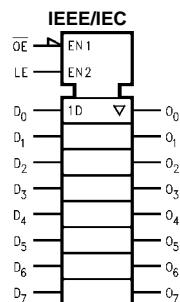
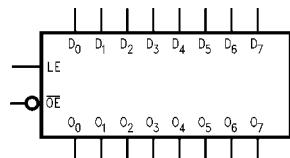
- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code:

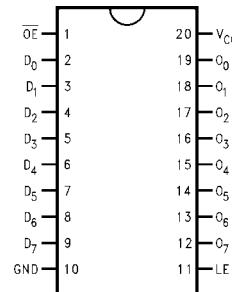
Order Number	Package Number	Package Description
74LVX573M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVX573SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX573MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Logic Symbols



Connection Diagram



Pin Descriptions

Pin Names	Description
D ₀ -D ₇	Data Inputs
LE	Latch Enable Input
\overline{OE}	3-STATE Output Enable Input
O ₀ -O ₇	3-STATE Latch Outputs

Functional Description

The LVX573 contains eight D-type latches. When the enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When OE is LOW, the buffers are enabled. When OE is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
\overline{OE}	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage

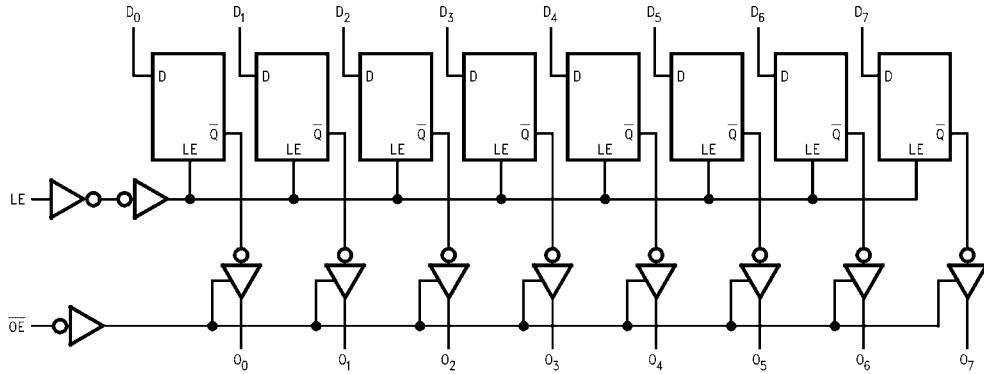
L = LOW Voltage

Z = High Impedance

X = Immaterial

O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)			Recommended Operating Conditions (Note 2)				
Supply Voltage (V_{CC})	-0.5V to +7.0V		Supply Voltage (V_{CC})	2.0V to 3.6V			
DC Input Diode Current (I_{IK})			Input Voltage (V_I)	0V to 5.5V			
$V_I = -0.5V$	-20 mA		Output Voltage (V_O)	0V to V_{CC}			
DC Input Voltage (V_I)	-0.5V to 7V		Operating Temperature (T_A)	-40°C to +85°C			
DC Output Diode Current (I_{OK})			Input Rise and Fall Time ($\Delta t/\Delta V$)	0 ns/V to 100 ns/V			
$V_O = -0.5V$	-20 mA						
$V_O = V_{CC} + 0.5V$	+20 mA						
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$						
DC Output Source or Sink Current (I_O)		±25 mA					
DC V_{CC} or Ground Current (I_{CC} or I_{GND})		±75 mA					
Storage Temperature (T_{STG})	-65°C to +150°C						
Power Dissipation	180 mW						
DC Electrical Characteristics							
Symbol	Parameter	V_{CC}	$T_A = +25^\circ C$		$T_A = -40^\circ C$ to $+85^\circ C$	Units	Conditions
			Min	Typ	Max		
V_{IH}	HIGH Level Input Voltage	2.0	1.5		1.5	V	
		3.0	2.0		2.0		
V_{IL}	LOW Level Input Voltage	2.0		0.5	0.5	V	
		3.0		0.8	0.8		
V_{OH}	HIGH Level Output Voltage	2.0	1.9	2.0	1.9	V	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 mA$
		3.0	2.9	3.0	2.9		
V_{OL}	LOW Level Output Voltage	2.0	0.0	0.1	0.1	V	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 mA$
		3.0	0.0	0.1	0.44		
I_{OZ}	3-STATE Output Off-State Current	3.6		±0.25	±2.5	μA	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND
I_{IN}	Input Leakage Current	3.6		±0.1	±1.0	μA	$V_{IN} = 5.5V$ or GND
I_{CC}	Quiescent Supply Current	3.6		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
Noise Characteristics (Note 3)							
Symbol	Parameter		V_{CC} (V)	$T_A = 25^\circ C$		Units	C_L (pF)
				Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		3.3	0.5	0.8	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}		3.3	-0.5	-0.8	V	50
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage		3.3		2.0	V	50
V_{ILD}	Maximum LOW Level Dynamic Input Voltage		3.3		0.8	V	50

Note 3: (Input $t_r = t_f = 3ns$)

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
t _{PLH} t _{PHL} D _n to O _n	Propagation Delay Time	2.7		7.6	14.5	1.0	17.5	ns	C _L = 15 pF	
				10.1	18.0	1.0	21.0		C _L = 50 pF	
	3.3 ± 0.3			5.9	9.3	1.0	11.0		C _L = 15 pF	
				8.4	12.8	1.0	14.5		C _L = 50 pF	
t _{PLH} t _{PHL} LE to O _n	Propagation Delay Time	2.7		8.2	15.6	1.0	18.5	ns	C _L = 15 pF	
				10.7	19.1	1.0	22.0		C _L = 50 pF	
	3.3 ± 0.3			6.4	10.1	1.0	12.0		C _L = 15 pF	
				8.9	13.6	1.0	15.5		C _L = 50 pF	
t _{PZL} t _{PZH}	3-STATE Output Enable Time	2.7		7.8	15.0	1.0	18.5	ns	C _L = 15 pF, R _L = 1 kΩ	
				10.3	18.5	1.0	22.0		C _L = 50 pF, R _L = 1 kΩ	
	3.3 ± 0.3			6.1	9.7	1.0	12.0		C _L = 15 pF, R _L = 1 kΩ	
				8.6	13.2	1.0	15.5		C _L = 50 pF, R _L = 1 kΩ	
t _{PLZ} t _{PHZ}	3-STATE Output Disable Time	2.7		12.1	19.1	1.0	22.0	ns	C _L = 50 pF, R _L = 1 kΩ	
			3.3 ± 0.3	10.1	13.6	1.0	15.5		C _L = 50 pF, R _L = 1 kΩ	
t _W	LE Pulse Width	2.7	6.5			7.5		ns		
		3.3 ± 0.3	5.0			5.0				
t _S	Setup Time D _n to LE	2.7	5.0			5.0		ns		
		3.3 ± 0.3	3.5			3.5				
t _H	Hold Time D _n to LE	2.7	1.5			1.5		ns		
		3.3 ± 0.3	1.5			1.5				
t _{OSHL} t _{OSLH}	Output to Output Skew (Note 4)	2.7			1.5		1.5	ns	C _L = 50 pF	
		2.3			1.5		1.5			

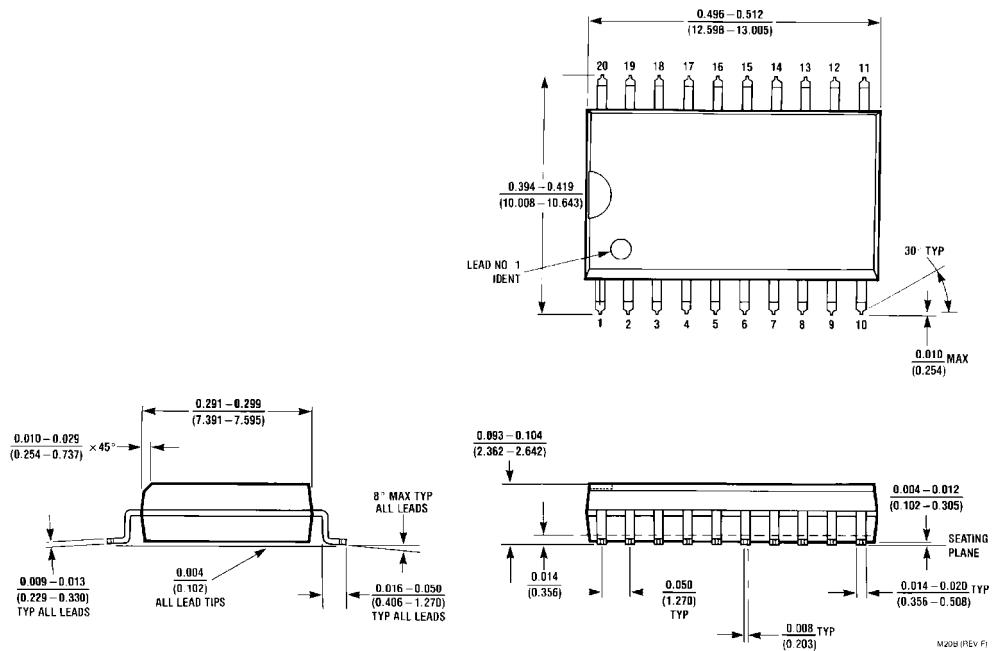
Note 4: Parameter guaranteed by design. t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|.

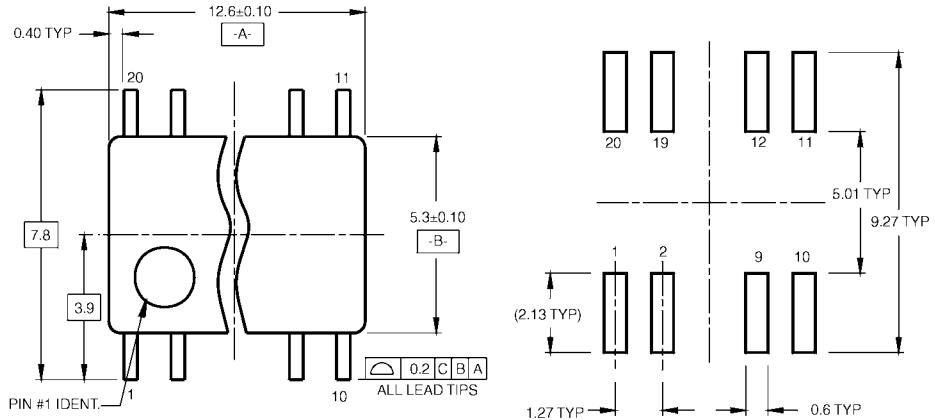
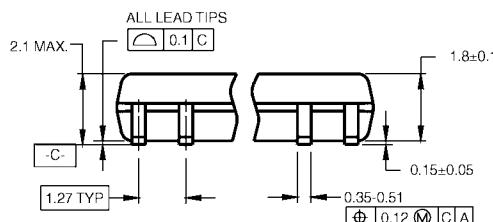
Capacitance

Symbol	Parameter	T _A = +25°C			T _A = -40°C to +85°C		Units	
		Min	Typ	Max	Min	Max		
C _{IN}	Input Capacitance				4	10		pF
C _{OUT}	Output Capacitance				6			pF
C _{PD}	Power Dissipation Capacitance (Note 5)				27			pF

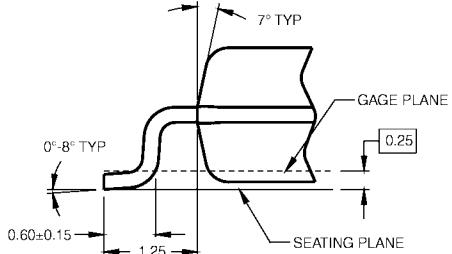
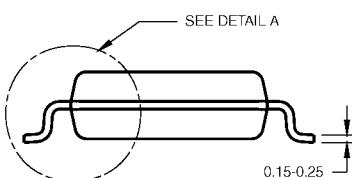
Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

$$\text{Average operating current can be obtained by the equation: } I_{CC(\text{opr.})} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per latch)}}$$

Physical Dimensions inches (millimeters) unless otherwise noted

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS



NOTES:

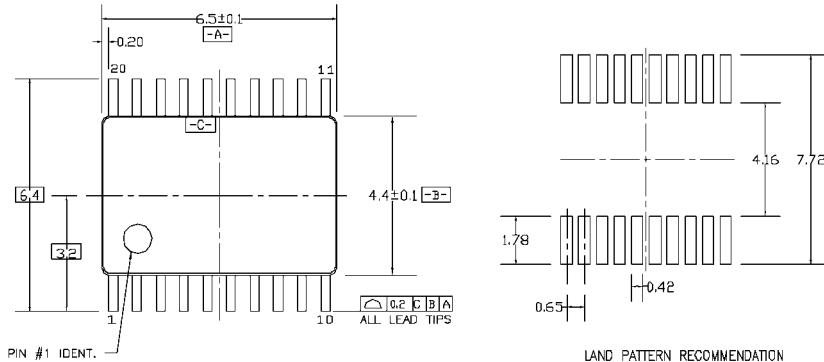
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M20DRevB1

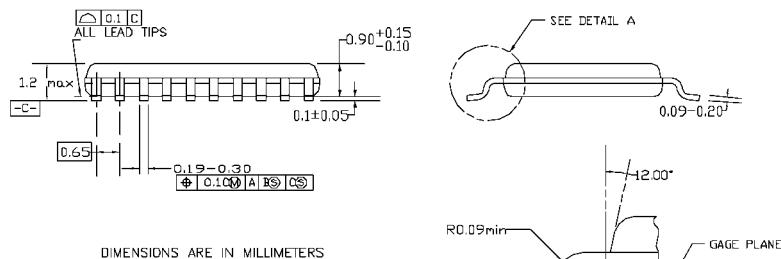
DETAIL A

Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

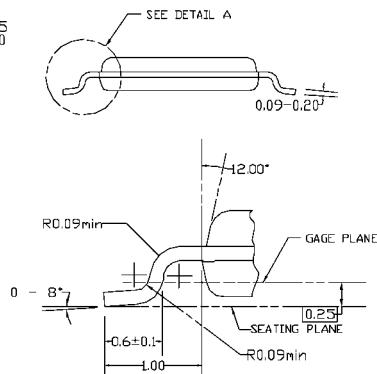
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DETAIL A

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MTC20REV01

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

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