

## 74VHC00 Quad 2-Input NAND Gate

### Features

- High Speed:  $t_{PD} = 3.7\text{ns}$  (typ.) at  $T_A = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min.)
- Power down protection is provided on all inputs
- Low noise:  $V_{OLP} = 0.8\text{V}$  (max)
- Low power dissipation:  $I_{CC} = 2\mu\text{A}$  (max.) at  $T_A = 25^\circ\text{C}$
- Pin and function compatible with 74HC00


### General Description

The VHC00 is an advanced high-speed CMOS 2-Input NAND Gate fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The internal circuit is composed of 3 stages, including buffer output, which provide high noise immunity and stable output. An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

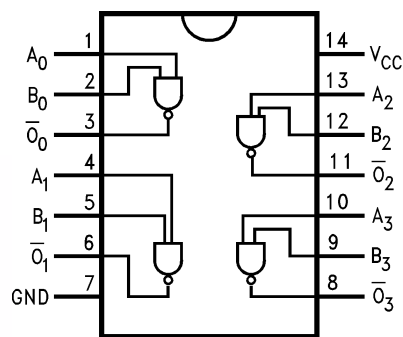
### Ordering Information

Order Number	Package Number	Package Description
74VHC00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC00MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC00N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

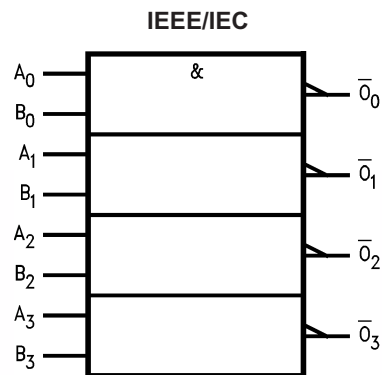
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol



Pin Description

Pin Names	Description
$A_n, B_n$	Inputs
$\overline{O}_n$	Outputs

Truth Table

A	B	$\overline{O}$
L	L	H
L	H	H
H	L	H
H	H	L

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	−0.5V to +7.0V
$V_{IN}$	DC Input Voltage	−0.5V to +7.0V
$V_{OUT}$	DC Output Voltage	−0.5V to $V_{CC} + 0.5V$
$I_{IK}$	Input Diode Current	−20mA
$I_{OK}$	Output Diode Current	±20mA
$I_{OUT}$	DC Output Current	±25mA
$I_{CC}$	DC $V_{CC}$ /GND Current	±50mA
$T_{STG}$	Storage Temperature	−65°C to +150°C
$T_L$	Lead Temperature (Soldering, 10 seconds)	260°C

## Recommended Operating Conditions<sup>(1)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	2.0V to +5.5V
$V_{IN}$	Input Voltage	0V to +5.5V
$V_{OUT}$	Output Voltage	0V to $V_{CC}$
$T_{OPR}$	Operating Temperature	−40°C to +85°C
$t_r, t_f$	Input Rise and Fall Time, $V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$	0ns/V ~ 100ns/V 0ns/V ~ 20ns/V

### Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units
				Min.	Typ.	Max.	Min.	Max.	
$V_{IH}$	HIGH Level Input Voltage	2.0		1.50			1.50		V
		3.0–5.5		$0.7 \times V_{CC}$			$0.7 \times V_{CC}$		
$V_{IL}$	LOW Level Input Voltage	2.0				0.50		0.50	V
		3.0–5.5				$0.3 \times V_{CC}$		$0.3 \times V_{CC}$	
$V_{OH}$	HIGH Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\mu\text{A}$	1.9	2.0		1.9	V
		3.0			2.9	3.0		2.9	
		4.5			4.4	4.5		4.4	
		3.0		$I_{OH} = -4\text{mA}$	2.58			2.48	
		4.5		$I_{OH} = -8\text{mA}$	3.94			3.80	
$V_{OL}$	LOW Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\mu\text{A}$		0.0	0.1	0.1	V
		3.0				0.0	0.1	0.1	
		4.5				0.0	0.1	0.1	
		3.0		$I_{OL} = 4\text{mA}$			0.36	0.44	
		4.5		$I_{OL} = 8\text{mA}$			0.36	0.44	
$I_{IN}$	Input Leakage Current	0–5.5	$V_{IN} = 5.5\text{V or GND}$			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND			2.0		20.0	$\mu\text{A}$

## Noise Characteristics

Symbol	Parameter	$V_{CC}$ (V)	Conditions	$T_A = 25^\circ\text{C}$		Units
				Typ.	Limits	
$V_{OLP}^{(2)}$	Quiet Output Maximum Dynamic $V_{OL}$	5.0	$C_L = 50\text{pF}$	0.3	0.8	V
$V_{OLV}^{(2)}$	Quiet Output Minimum Dynamic $V_{OL}$	5.0	$C_L = 50\text{pF}$	–0.3	–0.8	V
$V_{IHD}^{(2)}$	Minimum HIGH Level Dynamic Input Voltage	5.0	$C_L = 50\text{pF}$		3.5	V
$V_{ILD}^{(2)}$	Maximum LOW Level Dynamic Input Voltage	5.0	$C_L = 50\text{pF}$		1.5	V

## Note:

2. Parameter guaranteed by design.

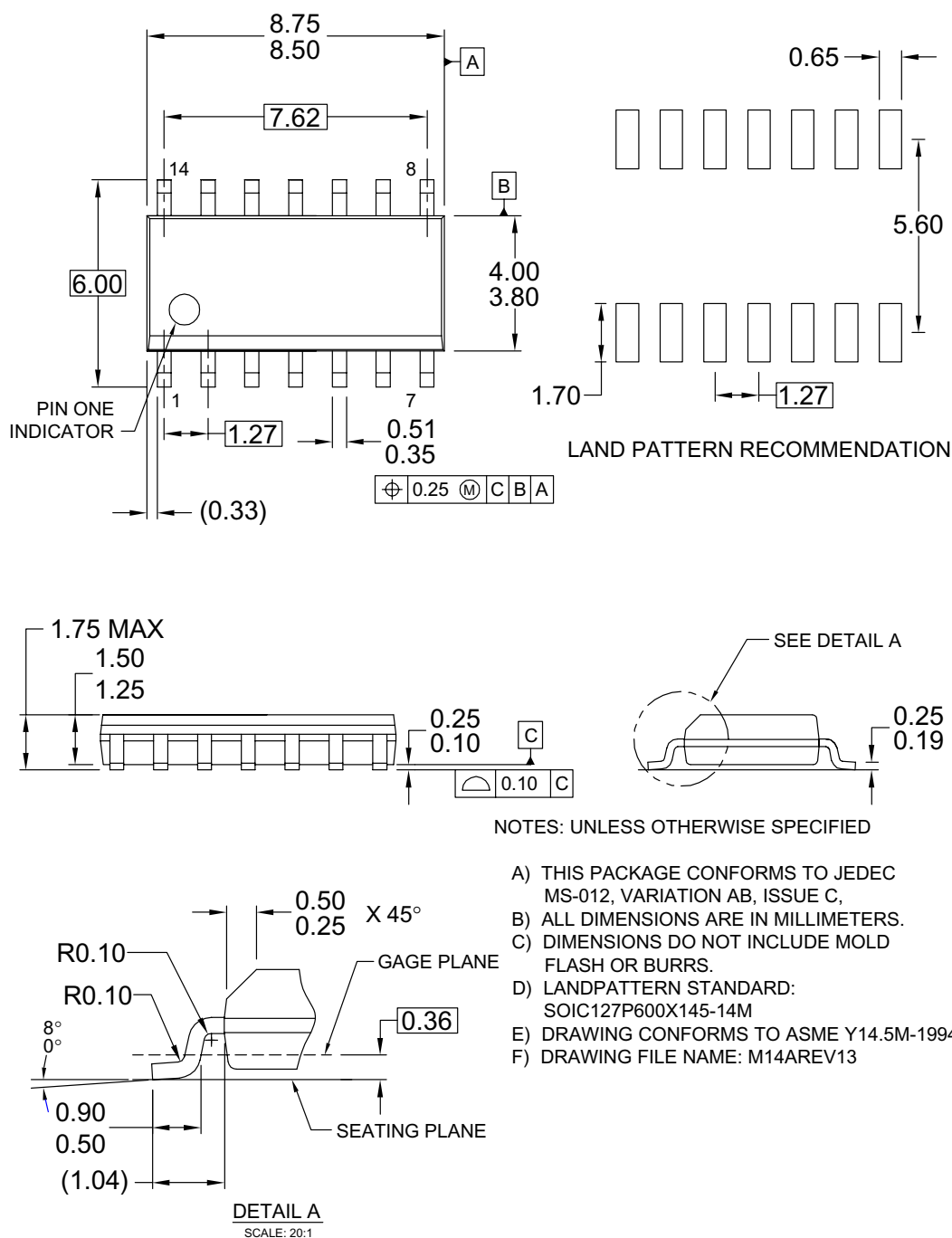
## AC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		Units
				Min.	Typ.	Max.	Min.	Max.	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay	$3.3 \pm 0.3$	$C_L = 15\text{pF}$		5.5	7.9	1.0	9.5	ns
			$C_L = 50\text{pF}$		8.0	11.4	1.0	13.0	
		$5.0 \pm 0.5$	$C_L = 15\text{pF}$		3.7	5.5	1.0	6.5	ns
			$C_L = 50\text{pF}$		5.2	7.5	1.0	8.5	
$C_{IN}$	Input Capacitance		$V_{CC} = \text{Open}$		4	10		10	pF
$C_{PD}$	Power Dissipation Capacitance		<sup>(3)</sup>		19				pF

**Note:**

3.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  
 $I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4$  (per gate).

## Physical Dimensions



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## Physical Dimensions (Continued)



## NOTES:

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- DIMENSIONS ARE IN MILLIMETERS
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- LANDPATTERN STANDARD: SOP65P640X110-14M
- DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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**Physical Dimensions** (Continued)**NOTES: UNLESS OTHERWISE SPECIFIED**

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A) JEDEC MS-001 VARIATION BA

B) ALL DIMENSIONS ARE IN MILLIMETERS.

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MOLD FLASH, AND TIE BAR EXTRUSIONS.D) DIMENSIONS AND TOLERANCES PER  
ASME Y14.5-1994

E) DRAWING FILE NAME: MKT-N14AREV7

**Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**

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