

74VHC9595FT

1. Functional Description

- 8-Bit Shift Register/Latch

2. General

The 74VHC9595FT is an advanced high speed 8-BIT SHIFT REGISTER/LATCH fabricated with silicon gate C²MOS technology.

74VHC9595FT combines low power consumption of CMOS with Schottky TTL speeds.

Shift operation is accomplished on the positive going transition of the SCK input. The output register is loaded with the contents of the shift register on the positive going transition of the RCK input. Since RCK and SCK signal are independent, parallel outputs can be held stable during the shift operation.

This register can be used in serial-to-parallel conversion, data receivers, etc.

All the inputs have hysteresis between the positive-going and negative-going thresholds. Thus the 74VHC9595FT is capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity. Additionally, all the inputs have a newly developed protection circuit without a diode returned to V_{CC}. This enables the inputs to be tolerant of up to 5.5 volts even when power supply is down.

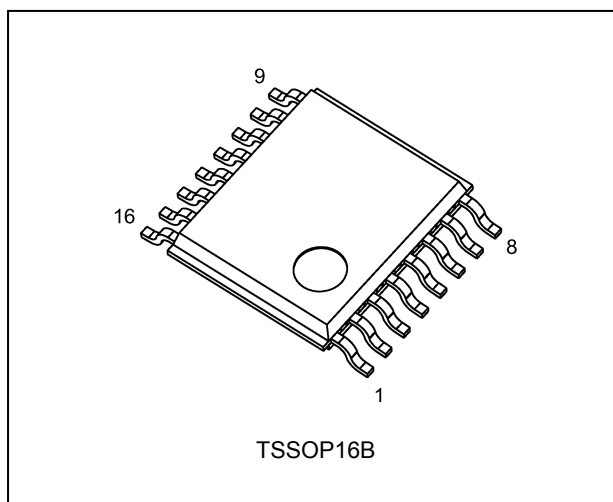
The input power-down protection capability makes the 74VHC9595FT ideal for a wide range of applications, such as interfacing between different voltages, voltage translation from 5 V to 3 V and battery back-up circuits.

A variant of the TC 74HC/VHC/AHC/LV595, the 74VHC9595FT contains negative-edge-triggered flip-flops to improve timing margins that are affected by long wires or slowly changing clocks when multiple parts are cascaded together.

3. Features

- (1) High speed: $f_{\text{MAX}} = 224 \text{ MHz (typ.)}$ at $V_{\text{CC}} = 5 \text{ V}$
- (2) Low power dissipation: $I_{\text{CC}} = 4 \mu\text{A (max)}$ at $T_a = 25^\circ\text{C}$
- (3) Power-down protection is provided on all inputs.
- (4) Balanced propagation delays: $t_{\text{PLH}} \approx t_{\text{PHL}}$
- (5) Wide operating voltage range: $V_{\text{CC(opr)}} = 2 \text{ V to } 5.5 \text{ V}$

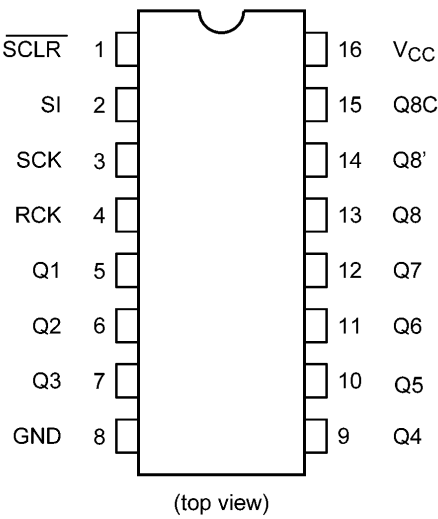
4. Packaging



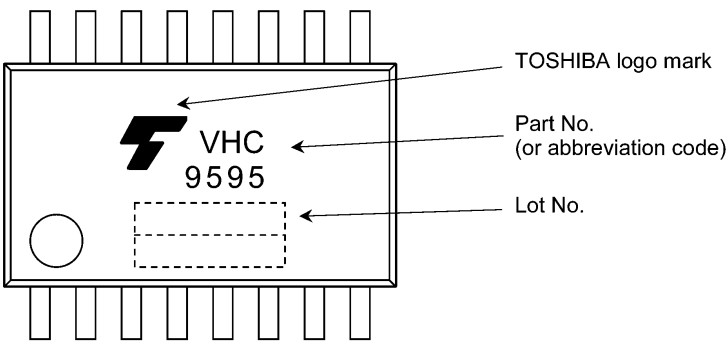
Start of commercial production

2014-12

5. Pin Assignment



6. Marking

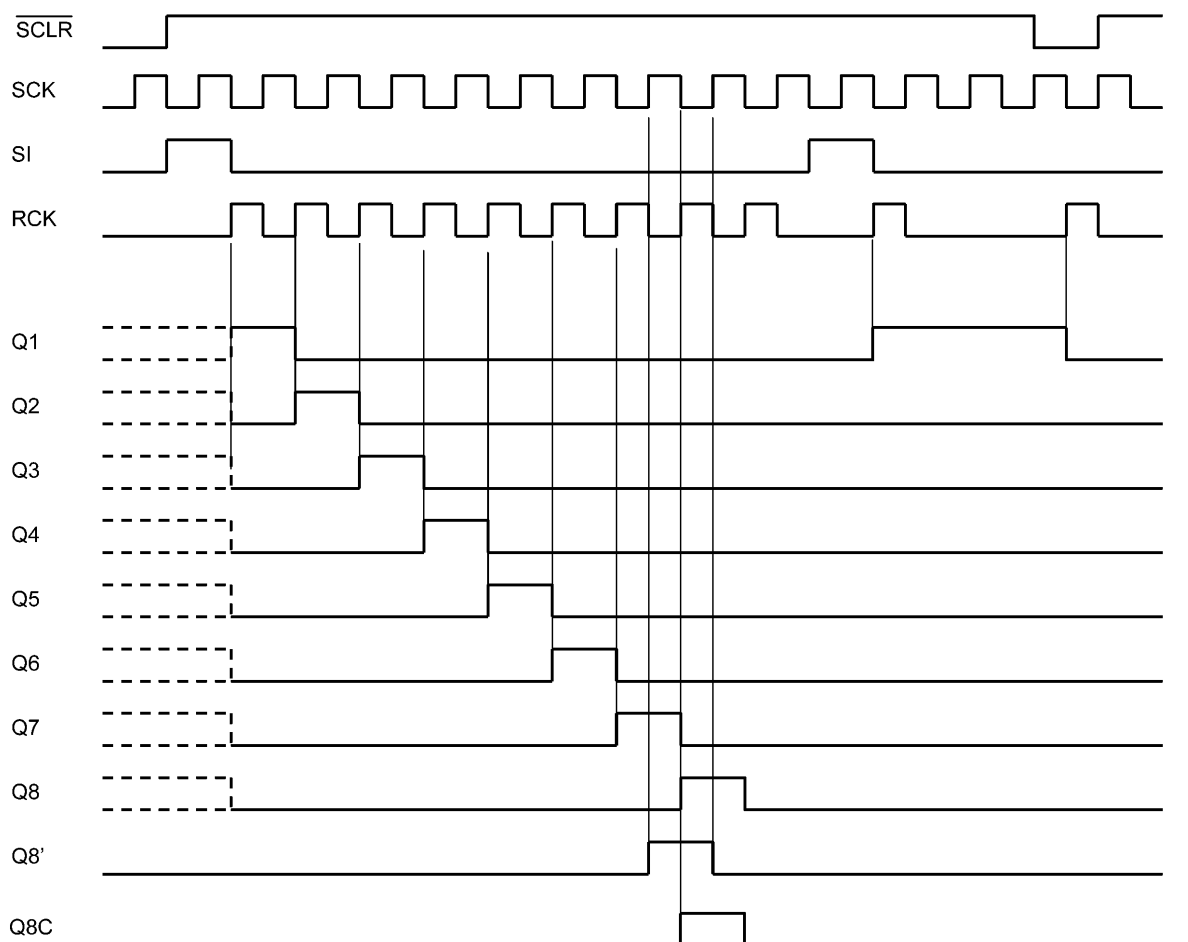


7. Truth Table

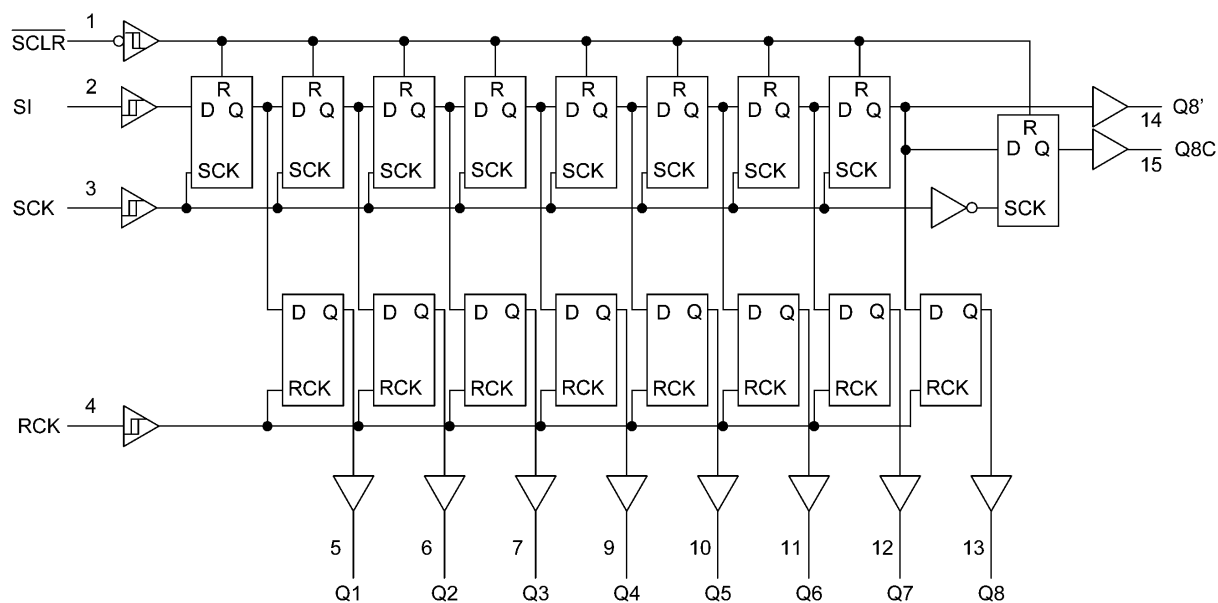
Inputs				Function
$\overline{\text{SCLR}}$	SI	SCK	RCK	
L	X	X	X	Shift register is cleared.
H	L		X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H	H		X	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
H	X		X	Shift register is not changed. Q8C outputs store the data of previous stage, respectively.
H	X	X		S.R. data is stored into storage register.
X	X	X		Storage register stage is not changed.

X: Don't care

8. Timing Chart



9. System Diagram



10. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	-0.5 to 7.0	V
Input voltage	V_{IN}	-0.5 to 7.0	V
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20	mA
Output current	I_{OUT}	± 25	mA
V_{CC} /ground current	I_{CC}	± 75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

11. Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either V_{CC} or GND.

12. Electrical Characteristics

12.1. DC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^{\circ}\text{C}$)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
Positive threshold voltage	V_P	—		3.0	—	—	2.20	V
				4.5	—	—	3.15	
				5.5	—	—	3.85	
Negative threshold voltage	V_N	—		3.0	0.90	—	—	V
				4.5	1.35	—	—	
				5.5	1.65	—	—	
Hysteresis voltage	V_H	—		3.0	0.30	—	1.20	V
				4.5	0.40	—	1.40	
				5.5	0.50	—	1.60	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.58	—	—	
			$I_{OH} = -8\text{ mA}$	4.5	3.94	—	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	—	0.36	
			$I_{OL} = 8\text{ mA}$	4.5	—	—	0.36	
Input leakage current	I_{IN}	$V_{IN} = 5.5\text{ V}$ or GND		0 to 5.5	—	—	± 0.1	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	—	4.0	μA

12.2. DC Characteristics (Unless otherwise specified, $T_a = -40\text{ to }85\text{ }^{\circ}\text{C}$)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Positive threshold voltage	V_P	—		3.0	—	2.20	V
				4.5	—	3.15	
				5.5	—	3.85	
Negative threshold voltage	V_N	—		3.0	0.90	—	V
				4.5	1.35	—	
				5.5	1.65	—	
Hysteresis voltage	V_H	—		3.0	0.30	1.20	V
				4.5	0.40	1.40	
				5.5	0.50	1.60	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.48	—	
			$I_{OH} = -8\text{ mA}$	4.5	3.80	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	0.44	
			$I_{OL} = 8\text{ mA}$	4.5	—	0.44	
Input leakage current	I_{IN}	$V_{IN} = 5.5\text{ V}$ or GND		0 to 5.5	—	± 1.0	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	40.0	μA

12.3. Timing Requirements (Unless otherwise specified, $T_a = 25^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (SCK, RCK)	$t_{w(L)}, t_{w(H)}$	—	3.3 ± 0.3	5.0	ns
			5.0 ± 0.5	5.0	
Minimum pulse width ($\overline{\text{SCLR}}$)	$t_{w(L)}$	—	3.3 ± 0.3	5.0	ns
			5.0 ± 0.5	5.0	
Minimum setup time (SI-SCK)	t_s	—	3.3 ± 0.3	5.0	ns
			5.0 ± 0.5	3.5	
Minimum setup time (SCK-RCK)	t_s	—	3.3 ± 0.3	8.0	ns
			5.0 ± 0.5	5.0	
Minimum setup time ($\overline{\text{SCLR}}$ -RCK)	t_s	—	3.3 ± 0.3	8.0	ns
			5.0 ± 0.5	5.5	
Minimum hold time (SI-SCK)	t_h	—	3.3 ± 0.3	0	ns
			5.0 ± 0.5	0	
Minimum hold time (SCK-RCK, $\overline{\text{SCLR}}$ -RCK)	t_h	—	3.3 ± 0.3	0	ns
			5.0 ± 0.5	0	
Minimum removal time ($\overline{\text{SCLR}}$)	t_{rem}	—	3.3 ± 0.3	5.0	ns
			5.0 ± 0.5	3.0	

12.4. Timing Requirements (Unless otherwise specified, $T_a = -40$ to 85°C , Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (SCK, RCK)	$t_{w(L)}, t_{w(H)}$	—	3.3 ± 0.3	5.0	ns
			5.0 ± 0.5	5.0	
Minimum pulse width ($\overline{\text{SCLR}}$)	$t_{w(L)}$	—	3.3 ± 0.3	5.0	ns
			5.0 ± 0.5	5.0	
Minimum setup time (SI-SCK)	t_s	—	3.3 ± 0.3	5.5	ns
			5.0 ± 0.5	3.5	
Minimum setup time (SCK-RCK)	t_s	—	3.3 ± 0.3	8.5	ns
			5.0 ± 0.5	5.0	
Minimum setup time ($\overline{\text{SCLR}}$ -RCK)	t_s	—	3.3 ± 0.3	9.0	ns
			5.0 ± 0.5	6.5	
Minimum hold time (SI-SCK)	t_h	—	3.3 ± 0.3	0	ns
			5.0 ± 0.5	0	
Minimum hold time (SCK-RCK, $\overline{\text{SCLR}}$ -RCK)	t_h	—	3.3 ± 0.3	0	ns
			5.0 ± 0.5	0	
Minimum removal time ($\overline{\text{SCLR}}$)	t_{rem}	—	3.3 ± 0.3	6.0	ns
			5.0 ± 0.5	3.5	

12.5. AC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^{\circ}\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Unit
Propagation delay time (SCK-Q8', Q8C)	t_{PLH}, t_{PHL}		—	3.3 ± 0.3	15	—	6.3	10.1	ns
					50	—	8.5	13.7	
				5.0 ± 0.5	15	—	4.5	6.8	
					50	—	6.3	9.3	
Propagation delay time (SCLR-Q8', Q8C)	t_{PHL}		—	3.3 ± 0.3	15	—	10.6	16.2	ns
					50	—	12.9	19.6	
				5.0 ± 0.5	15	—	8.1	11.5	
					50	—	10.2	14.5	
Propagation delay time (RCK-Q _n)	t_{PLH}, t_{PHL}		—	3.3 ± 0.3	15	—	7.0	11.2	ns
					50	—	9.8	15.1	
				5.0 ± 0.5	15	—	5.3	8.3	
					50	—	7.7	10.9	
Maximum clock frequency	f_{MAX}		—	3.3 ± 0.3	15	99	160	—	MHz
					50	73	118	—	
				5.0 ± 0.5	15	148	224	—	
					50	108	160	—	
Input capacitance	C_{IN}		—			—	4	10	pF
Power dissipation capacitance	C_{PD}	(Note 1)	—			—	67	—	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$$

12.6. AC Characteristics (Unless otherwise specified, $T_a = -40\text{ to }85\text{ }^{\circ}\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time (SCK-Q8', Q8C)	t_{PLH}, t_{PHL}	—	3.3 ± 0.3	15	1.0	11.5	ns
				50	1.0	15.7	
			5.0 ± 0.5	15	1.0	7.8	
				50	1.0	10.6	
Propagation delay time (SCLR-Q8', Q8C)	t_{PHL}	—	3.3 ± 0.3	15	1.0	18.5	ns
				50	1.0	22.4	
			5.0 ± 0.5	15	1.0	13.1	
				50	1.0	16.6	
Propagation delay time (RCK-Q _n)	t_{PLH}, t_{PHL}	—	3.3 ± 0.3	15	1.0	12.8	ns
				50	1.0	17.2	
			5.0 ± 0.5	15	1.0	9.5	
				50	1.0	12.4	
Maximum clock frequency	f_{MAX}	—	3.3 ± 0.3	15	87	—	MHz
				50	64	—	
			5.0 ± 0.5	15	129	—	
				50	94	—	
Input capacitance	C_{IN}	—			—	10	pF

12.7. Noise Characteristics (Unless otherwise specified, $T_a = 25^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Limit	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	$C_L = 50\text{ pF}$	5.0	0.6	1.0	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	$C_L = 50\text{ pF}$	5.0	-0.6	-1.0	V
Minimum high-level dynamic input voltage	V_{IHD}	$C_L = 50\text{ pF}$	5.0	—	3.5	V
Maximum low-level dynamic input voltage	V_{ILD}	$C_L = 50\text{ pF}$	5.0	—	1.5	V

Unit: mm

Weight: 0.055 g (typ.)

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