

## General Description

The ICS849N2505I is a clock synthesizer designed for wireless infrastructure applications.

The device generates a selectable 25MHz, 50MHz, 125MHz or 156.25MHz clock signal from a 10MHz input with excellent phase jitter performance.

The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance, combined with a low power consumption and high power supply noise rejection.

The device supports a 3.3V voltage supply and is packaged in a small, lead-free (RoHS 6) 32-lead VFQFN package.

The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements. The device is a member of the high-performance clock family from IDT.

## Features

- Fourth generation FemtoClock® Next Generation (NG) technology
- Selectable 25MHz, 50MHz, 125MHz or 156.25MHz output clock synthesized from a 10MHz fundamental mode crystal or 10MHz differential input
- Four selectable differential LVPECL or LVDS outputs
- Crystal interface designed for 10MHz, 12pF parallel resonant crystal
- RMS phase jitter (12kHz - 20MHz): 0.336ps (typical), LVPECL outputs
- Period jitter: 2.7ps (maximum), LVPECL outputs
- Full 3.3V supply voltage
- Available in Lead-free (RoHS 6) packageing
- -40°C to 85°C ambient operating temperature

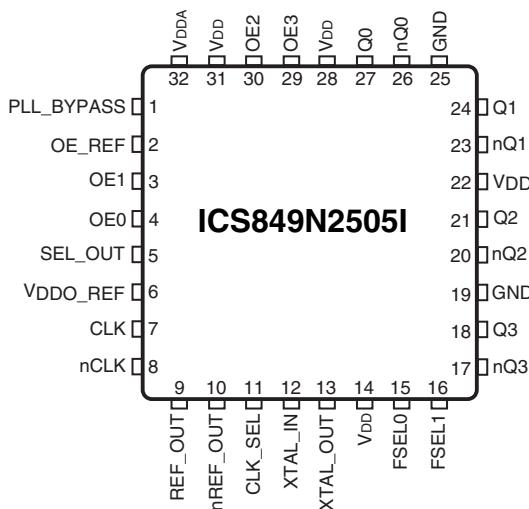
## Frequency Select Function Table

| FSEL1, FSEL0 | Input Frequency (MHz) | Output Frequency (MHz) |
|--------------|-----------------------|------------------------|
| 00 (default) | 10                    | 25                     |
| 01           | 10                    | 50                     |
| 10           | 10                    | 125                    |
| 11           | 10                    | 156.25                 |

## SEL\_OUT Function Table

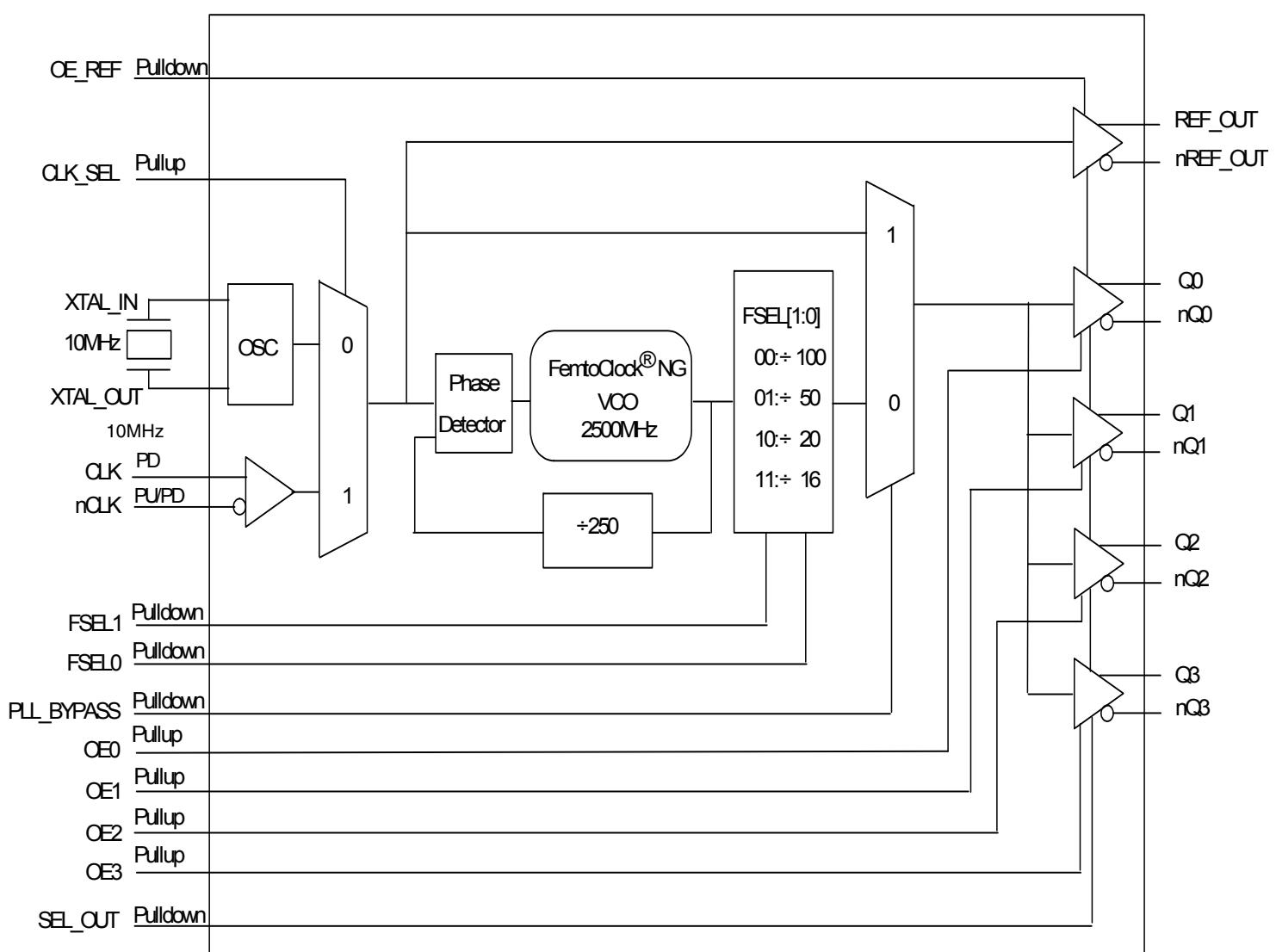
| SEL_OUT     | Q[0:3], nQ[0:3], REF_OUT/nREF_OUT |
|-------------|-----------------------------------|
| 0 (default) | LVPECL                            |
| 1           | LVDS                              |

## Pin Assignment



**32-Lead VFQFN**  
**5mm x 5mm x 0.925mm package body**  
**K Package**  
**Top View**

## Block Diagram



**Table 1. Pin Descriptions**

| Number            | Name                 | Type   |                     | Description  |
|-------------------|----------------------|--------|---------------------|--|
| 1                 | PLL_BYPASS           | Input  | Pulldown            | PLL mode select. When LOW, selects PLL operation. When HIGH, selects PLL bypass. LVCMOS/LVTTL interface levels.  |
| 2                 | OE_REF               | Input  | Pulldown            | Controls enabling and disabling of REF_OUT, nREF_OUT outputs. When logic HIGH, the outputs are enabled and active. When logic LOW, the outputs are disabled and forced to High-Impedance. LVCMOS/LVTTL interface levels. |
| 3                 | OE1                  | Input  | Pullup              | Controls enabling and disabling of Q1, nQ1 outputs. When logic HIGH, the outputs are enabled and active. When logic LOW, the outputs are disabled and forced to High-Impedance. LVCMOS/LVTTL interface levels.           |
| 4                 | OE0                  | Input  | Pullup              | Controls enabling and disabling of Q0, nQ0 outputs. When logic HIGH, the outputs are enabled and active. When logic LOW, the outputs are disabled and forced to High-Impedance. LVCMOS/LVTTL interface levels.           |
| 5                 | SEL_OUT              | Input  | Pulldown            | Output select pin. When LOW, outputs are LVPECL levels. When HIGH, outputs are LVDS levels. LVCMOS/LVTTL interface levels.   |
| 6                 | V <sub>DDO_REF</sub> | Power  |                     | Output supply pin for differential REF_OUT.  |
| 7                 | CLK                  | Input  | Pulldown            | Non-inverting differential clock input.  |
| 8                 | nCLK                 | Input  | Pullup/<br>Pulldown | Inverting differential clock input. V <sub>DD</sub> /2 default when left floating.   |
| 9,<br>10          | REF_OUT,<br>nREF_OUT | Output |                     | Reference clock output pair. LVPECL or LVDS interface levels.  |
| 11                | CLK_SEL              | Input  | Pullup              | Clock select input. When LOW selects XTAL inputs. When HIGH selects CLK/nCLK inputs. LVCMOS /LVTTL interface levels.   |
| 12,<br>13         | XTAL_IN,<br>XTAL_OUT | Input  |                     | Crystal oscillator interface. The XTAL_IN is the input. XTAL_OUT is the output.  |
| 14, 22,<br>28, 31 | V <sub>DD</sub>      | Power  |                     | Core supply pins.  |
| 15, 16            | FSEL0, FSEL1         | Input  | Pulldown            | Frequency select pins. LVCMOS/LVTTL interface levels.  |
| 17, 18            | nQ3, Q3              | Output |                     | Differential output pair. LVPECL or LVDS interface levels.   |
| 19, 25            | GND                  | Power  |                     | Power supply ground.   |
| 20, 21            | nQ2, Q2              | Output |                     | Differential output pair. LVPECL or LVDS interface levels.   |
| 23, 24            | nQ1, Q1              | Output |                     | Differential output pair. LVPECL or LVDS interface levels.   |
| 26, 27            | nQ0, Q0              | Output |                     | Differential output pair. LVPECL or LVDS interface levels.   |
| 29                | OE3                  | Input  | Pullup              | Controls enabling and disabling of Q3, nQ3 outputs. When logic HIGH, the outputs are enabled and active. When logic LOW, the outputs are disabled and forced to High-Impedance. LVCMOS/LVTTL interface levels.           |
| 30                | OE2                  | Input  | Pullup              | Controls enabling and disabling of Q2, nQ2 outputs. When logic HIGH, the outputs are enabled and active. When logic LOW, the outputs are disabled and forced to High-Impedance. LVCMOS/LVTTL interface levels.           |
| 32                | V <sub>DDA</sub>     | Power  |                     | Analog supply pin.   |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

| Symbol                | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |         | 4       |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                 |         | 51      |         | kΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |         | 51      |         | kΩ    |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item   | Rating                               |
|--|--------------------------------------|
| Supply Voltage, $V_{DD}$                     | 3.63V                                |
| Inputs, $V_I$<br>XTAL_IN<br>Other Inputs     | 0V to 2V<br>-0.5V to $V_{DD} + 0.5V$ |
| Outputs, $I_O$                               |                                      |
| LVPECL<br>Continuos Current<br>Surge Current | 50mA<br>100mA                        |
| LVDS<br>Continuos Current<br>Surge Current   | 10mA<br>15mA                         |
| Package Thermal Impedance, $\theta_{JA}$     | 33.1°C/W (0 mps)                     |
| Storage Temperature, $T_{STG}$               | -65°C to 150°C                       |

## DC Electrical Characteristics

**Table 4A. LVPECL Power Supply DC Characteristics,  $V_{DD} = V_{DDO\_REF} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol         | Parameter             | Test Conditions | Minimum         | Typical | Maximum  | Units |
|----------------|-----------------------|-----------------|-----------------|---------|----------|-------|
| $V_{DD}$       | Core Supply Voltage   |                 | 3.135           | 3.3     | 3.465    | V     |
| $V_{DDA}$      | Analog Supply Voltage |                 | $V_{DD} - 0.35$ | 3.3     | $V_{DD}$ | V     |
| $V_{DDO\_REF}$ | Output Supply Voltage |                 | 3.135           | 3.3     | 3.465    | V     |
| $I_{EE}$       | Power Supply Current  | $SEL\_OUT = 0$  |                 |         | 200      | mA    |
| $I_{DDA}$      | Analog Supply Current |                 |                 |         | 35       | mA    |

**Table 4B. LVDS Power Supply DC Characteristics,  $V_{DD} = V_{DDO\_REF} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol         | Parameter             | Test Conditions | Minimum         | Typical | Maximum  | Units |
|----------------|-----------------------|-----------------|-----------------|---------|----------|-------|
| $V_{DD}$       | Core Supply Voltage   |                 | 3.135           | 3.3     | 3.465    | V     |
| $V_{DDA}$      | Analog Supply Voltage |                 | $V_{DD} - 0.35$ | 3.3     | $V_{DD}$ | V     |
| $V_{DDO\_REF}$ | Output Supply Voltage |                 | 3.135           | 3.3     | 3.465    | V     |
| $I_{DD}$       | Power Supply Current  | $SEL\_OUT = 1$  |                 |         | 223      | mA    |
| $I_{DDA}$      | Analog Supply Current |                 |                 |         | 35       | mA    |
| $I_{DDO}$      | Output Supply Current | $SEL\_OUT = 1$  |                 |         | 53       | mA    |

**Table 4C. LVCMS/LVTTL DC Characteristics,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol   | Parameter          | Test Conditions             |  | Minimum | Typical | Maximum        | Units         |
|----------|--------------------|-----------------------------|--|---------|---------|----------------|---------------|
| $V_{IH}$ | Input High Voltage |                             |  | 2.2     |         | $V_{DD} + 0.3$ | V             |
| $V_{IL}$ | Input Low Voltage  |                             |  | -0.3    |         | 0.8            | V             |
| $I_{IH}$ | Input High Current | CLK_SEL, OEx                | $V_{DD} = V_{IN} = 3.465\text{V}$            |         |         | 10             | $\mu\text{A}$ |
|          |                    | PLL_BYPASS, SEL_OUT, OE_REF | $V_{DD} = V_{IN} = 3.465\text{V}$            |         |         | 150            | $\mu\text{A}$ |
| $I_{IL}$ | Input Low Current  | CLK_SEL, OEx                | $V_{DD} = 3.465\text{V}, V_{IN} = 0\text{V}$ | -150    |         |                | $\mu\text{A}$ |
|          |                    | PLL_BYPASS, SEL_OUT, OE_REF | $V_{DD} = V_{IN} = 3.465\text{V}$            | -10     |         |                | $\mu\text{A}$ |

**Table 4D. Differential Input DC Characteristics,  $V_{DD} = V_{DDO\_REF} = 3.3\text{V} \pm 5\%$ ,  $V_{EE} = 0\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol    | Parameter                         | Test Conditions |           | Minimum  | Typical | Maximum         | Units         |
|-----------|-----------------------------------|-----------------|-----------|----------|---------|-----------------|---------------|
| $I_{IH}$  | Input High Current                |                 | CLK, nCLK |          |         | 150             | $\mu\text{A}$ |
| $I_{IL}$  | Input Low Current                 | CLK             |           | -10      |         |                 | $\mu\text{A}$ |
|           |                                   | nCLK            |           | -150     |         |                 | $\mu\text{A}$ |
| $V_{PP}$  | Peak-to-Peak Input Voltage        |                 |           | 0.15     |         | 1.3             | V             |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1 |                 |           | $V_{EE}$ |         | $V_{DD} - 0.85$ | V             |

NOTE 1: Common mode input voltage is defined as the crossing point.

**Table 4E. LVPECL DC Characteristics,  $V_{DD} = V_{DDO\_REF} = 3.3\text{V} \pm 5\%$ ,  $V_{EE} = 0\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol      | Parameter                                 | Test Conditions |  | Minimum         | Typical | Maximum          | Units |
|-------------|---|-----------------|--|-----------------|---------|------------------|-------|
| $V_{OH}$    | Output High Voltage                       |                 |  | $V_{DDO} - 1.1$ |         | $V_{DDO} - 0.75$ | V     |
| $V_{OL}$    | Output Low Voltage                        |                 |  | $V_{DDO} - 2.0$ |         | $V_{DDO} - 1.6$  | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing; NOTE 1 |                 |  | 0.6             |         | 1.0              | V     |

NOTE 1: Outputs termination with  $50\Omega$  to  $V_{DDO\_REF} - 2\text{V}$ .

**Table 4F. LVDS DC Characteristics,  $V_{DD} = V_{DDO\_REF} = 3.3\text{V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol          | Parameter                   | Test Conditions |  | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|--|---------|---------|---------|-------|
| $V_{OD}$        | Differential Output Voltage |                 |  | 247     |         | 454     | mV    |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change   |                 |  |         |         | 60      | mV    |
| $V_{os}$        | Offset Voltage              |                 |  | 1.125   |         | 1.375   | V     |
| $\Delta V_{os}$ | $V_{os}$ Magnitude Change   |                 |  |         |         | 50      | mV    |

**Table 5. Crystal Characteristics**

| Parameter                          | Test Conditions | Minimum | Typical     | Maximum | Units |
|------------------------------------|-----------------|---------|-------------|---------|-------|
| Mode of Oscillation                |                 |         | Fundamental |         |       |
| Frequency                          |                 |         | 10          |         | MHz   |
| Equivalent Series Resistance (ESR) |                 |         |             | 50      | Ω     |
| Shunt Capacitance                  |                 |         |             | 7       | pF    |

**AC Electrical Characteristics****Table 6A. LVPECL AC Characteristics,  $V_{DD} = V_{DDO\_REF} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

| Symbol            | Parameter                     | Test Conditions                                 | Minimum | Typical | Maximum | Units |
|-------------------|-------------------------------|---|---------|---------|---------|-------|
| $f_{OUT}$         | Output Frequency              |   | 25      |         | 156.25  | MHz   |
| $\tau_{jit(cc)}$  | Cycle-to-Cycle Jitter; NOTE 1 |   |         |         | 8       | ps    |
| $\tau_{jit(per)}$ | Period jitter, RMS; NOTE 2    |   |         | 1.95    | 2.7     | ps    |
| $\tau_{jit}$      | RMS Phase Jitter; NOTE 3      | 156.25MHz,<br>Integration Range: 12kHz to 20MHz |         | 0.336   |         | ps    |
| $t_R / t_F$       | Output Rise/Fall Time         | 20% to 80%                                      | 125     |         | 450     | ps    |
| odc               | Output Duty Cycle             |   | 48      |         | 52      | %     |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 2: If using the RMS Period Jitter to calculate peak-to-peak jitter, then use the typical RMS Period Jitter specification x the RMS multiplier. For example, for a bit error rate of 10E-12, the peak-to-peak jitter would be  $1.95 \times 14 = 27.3$ ps.

NOTE 3: See Phase Noise Plot.

**Table 6B. LVDS AC Characteristics,  $V_{DD} = V_{DDO\_REF} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

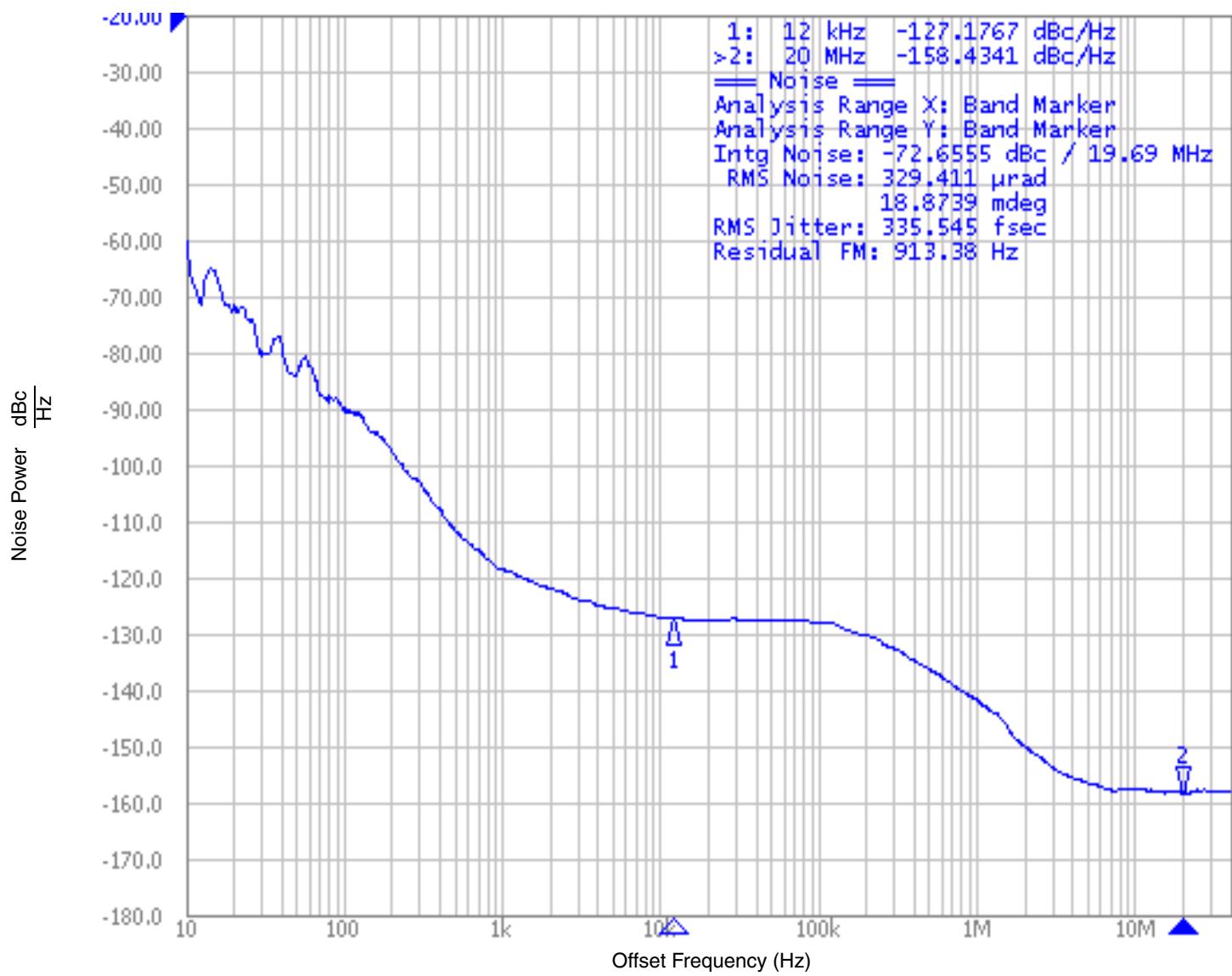
| Symbol            | Parameter                     | Test Conditions                                 | Minimum | Typical | Maximum | Units |
|-------------------|-------------------------------|---|---------|---------|---------|-------|
| $f_{OUT}$         | Output Frequency              |   | 25      |         | 156.25  | MHz   |
| $\tau_{jit(cc)}$  | Cycle-to-Cycle Jitter; NOTE 1 |   |         |         | 8       | ps    |
| $\tau_{jit(per)}$ | Period jitter, RMS; NOTE 2    |   |         | 3.35    | 4.75    | ps    |
| $\tau_{jit}$      | RMS Phase Jitter; NOTE 3      | 156.25MHz,<br>Integration Range: 12kHz to 20MHz |         | 0.351   |         | ps    |
| $t_R / t_F$       | Output Rise/Fall Time         | 20% to 80%                                      | 120     |         | 450     | ps    |
| odc               | Output Duty Cycle             |   | 48      |         | 52      | %     |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

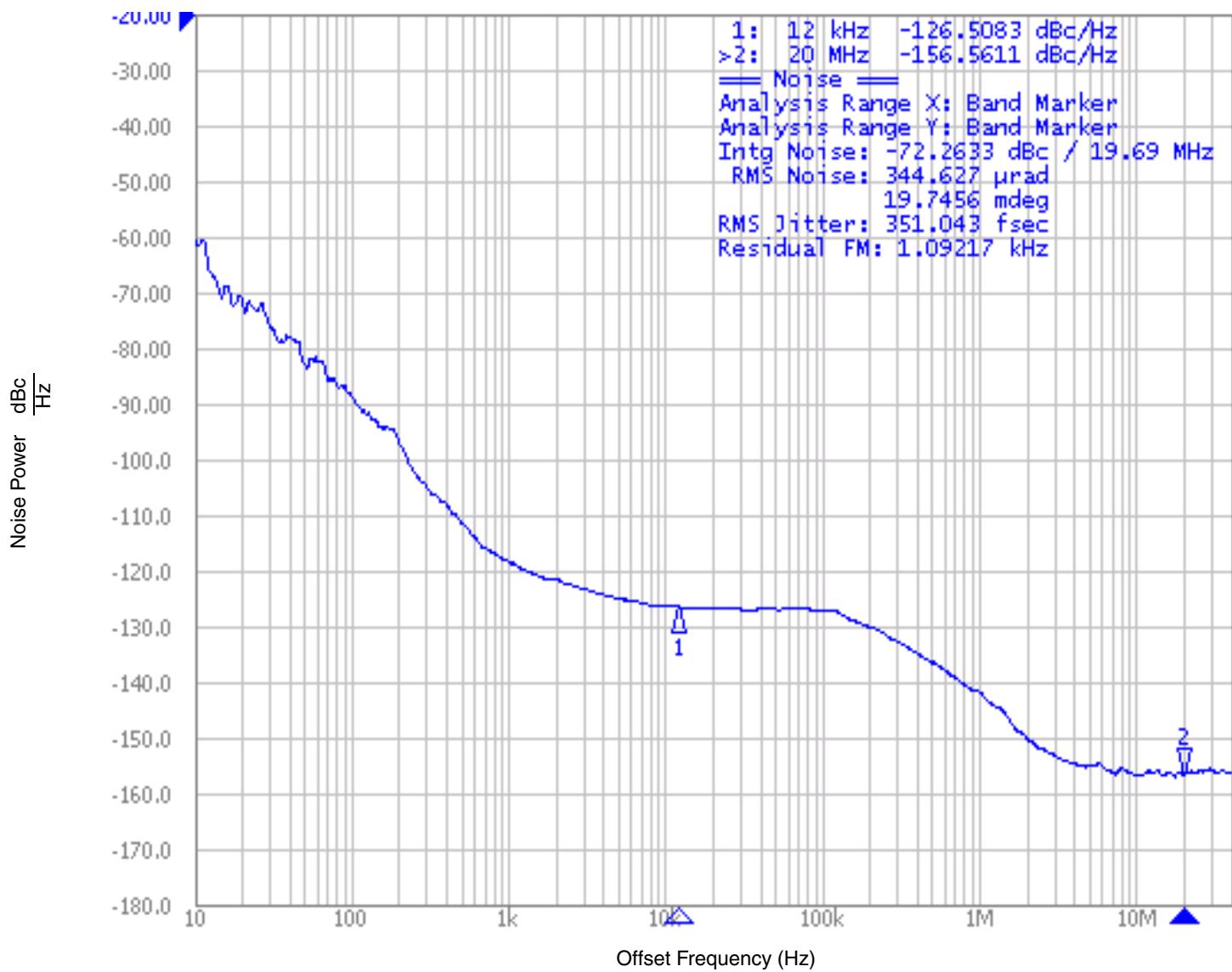
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 2: If using the RMS Period Jitter to calculate peak-to-peak jitter, then use the typical RMS Period Jitter specification x the RMS multiplier. For example, for a bit error rate of 10E-12, the peak-to-peak jitter would be  $3.35 \times 14 = 46.9$ ps.

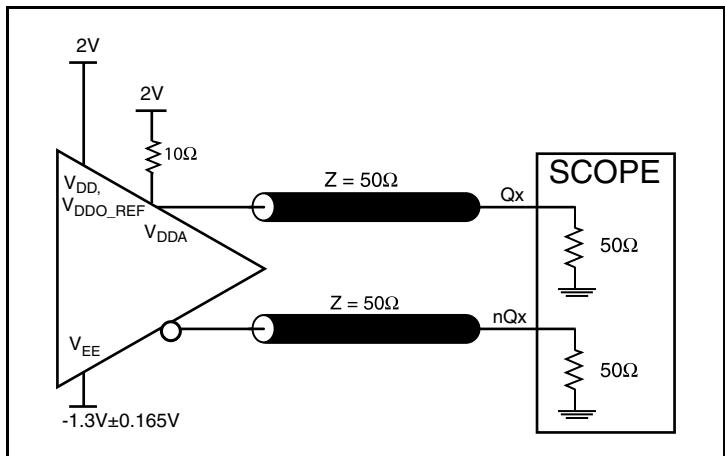
NOTE 3: See Phase Noise Plot.

**Typical Phase Noise at 156.25MHz (LVPECL output)**

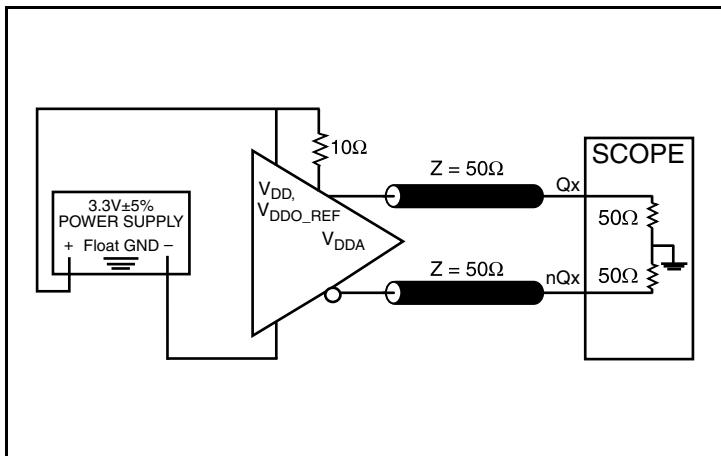
## Typical Phase Noise at 156.25MHz (LVDS output)



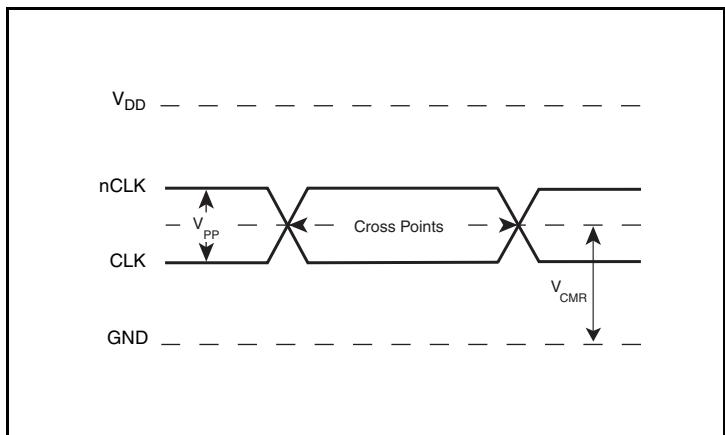
## Parameter Measurement Information



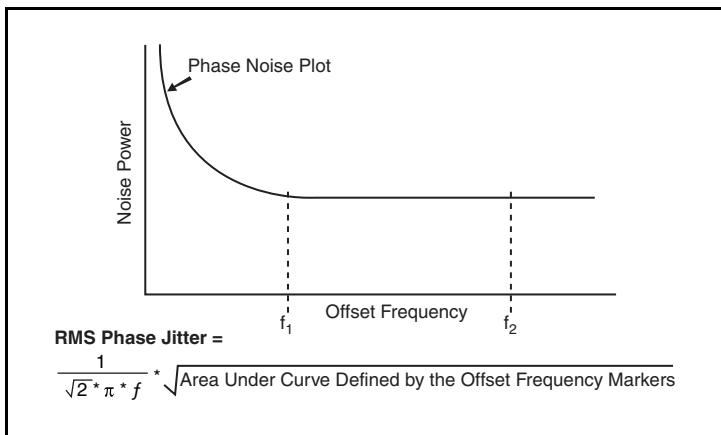
3.3V LVPECL Output Load AC Test Circuit



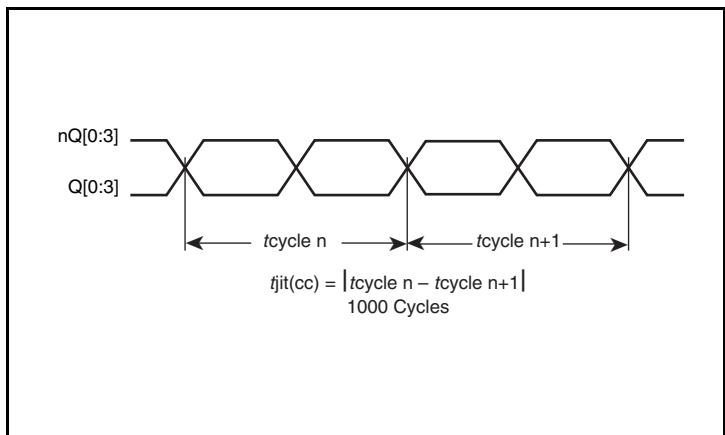
3.3V LVDS Output Load AC Test Circuit



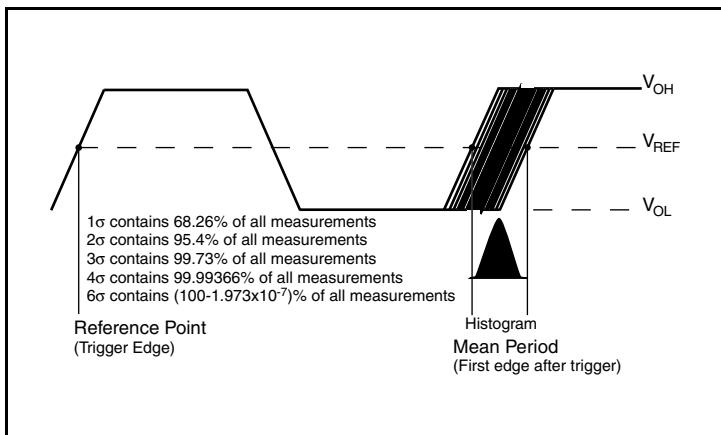
Differential Input Level



RMS Phase Jitter

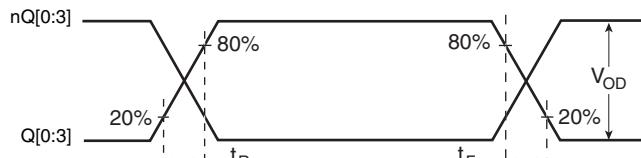


Cycle-to-Cycle Jitter

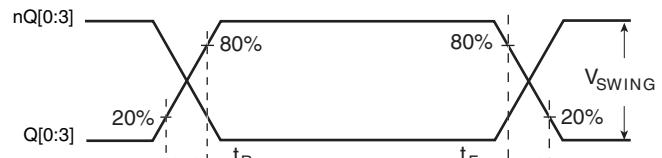


RMS Period Jitter

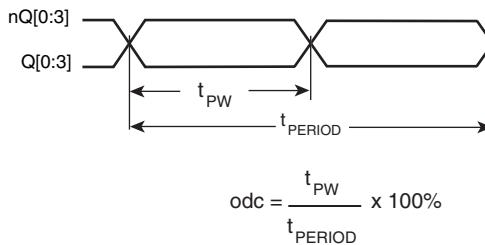
## Parameter Measurement Information, continued



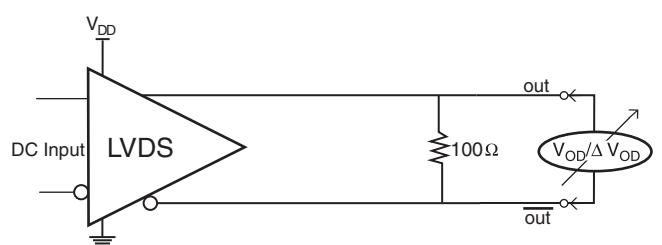
LVDS Output Rise/Fall Time



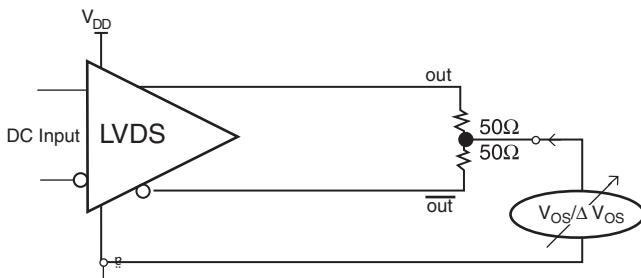
LVPECL Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Differential Output Voltage Setup



Offset Voltage Setup

## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### LVC MOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

##### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from XTAL\_IN to ground.

##### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from CLK to ground.

#### Outputs:

##### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

##### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with  $100\Omega$  across. If they are left floating, there should be no trace attached.

### Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the Vref in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{DD} = 3.3\text{V}$ , R1 and R2 value should be adjusted to set Vref at 1.25V. The values below are for when both the single ended swing and  $V_{DD}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First,  $R_3$  and  $R_4$  in parallel should equal the transmission

line impedance. For most  $50\Omega$  applications,  $R_3$  and  $R_4$  can be  $100\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVC MOS driver. When using single ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVC MOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than  $-0.3\text{V}$  and  $V_{IH}$  cannot be more than  $V_{DD} + 0.3\text{V}$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

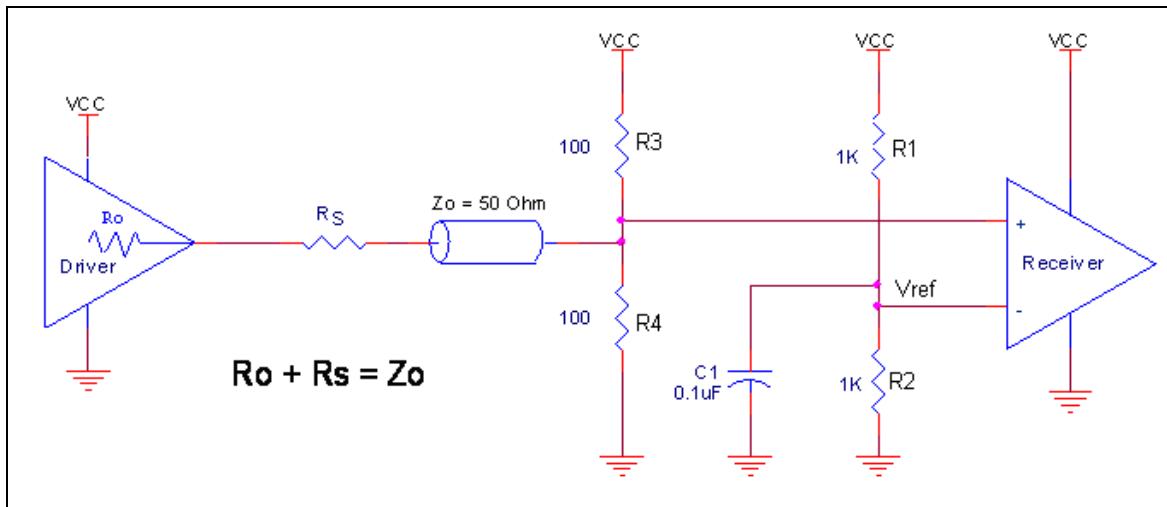
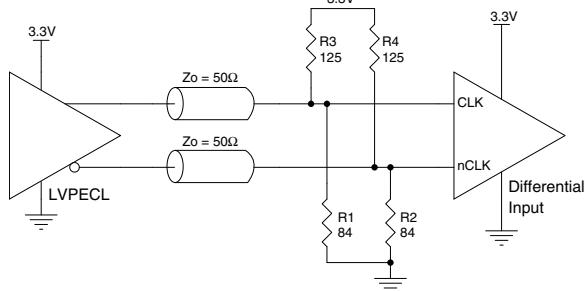


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

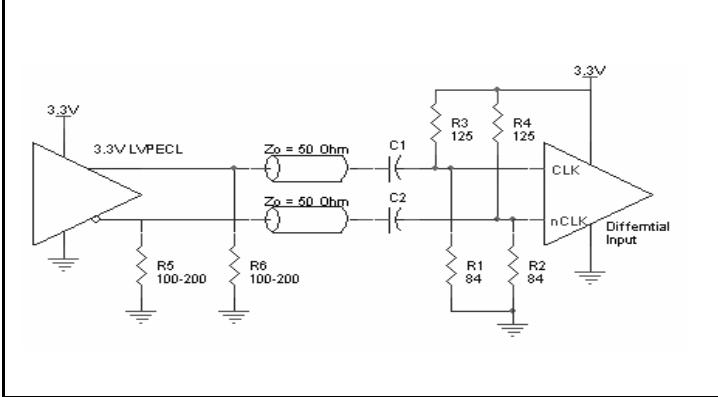
## Differential Clock Input Interface

The CLK/nCLK accepts LVPECL, LVDS and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 2A to 2C* show interface examples for the CLK/nCLK input driven by the most common driver types. The input

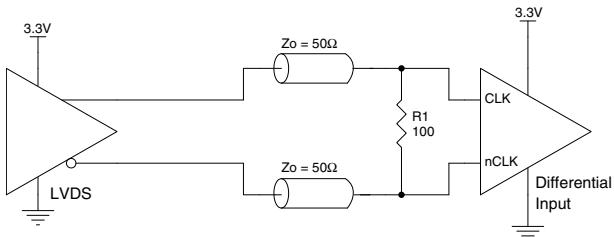
interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



**Figure 2A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver with AC Couple**

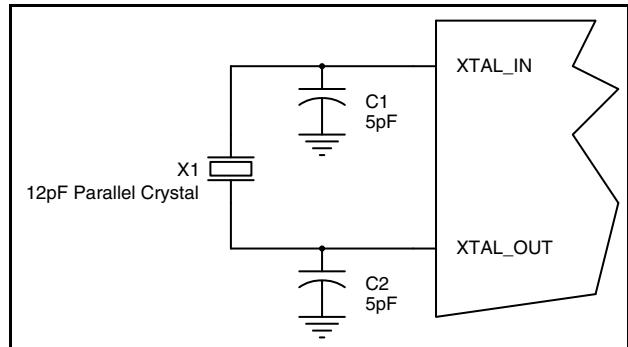


**Figure 2C. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

## Crystal Input Interface

The ICS849N2505I has been characterized with 12pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 3* below were determined using a 10MHz, 12pF parallel resonant

crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

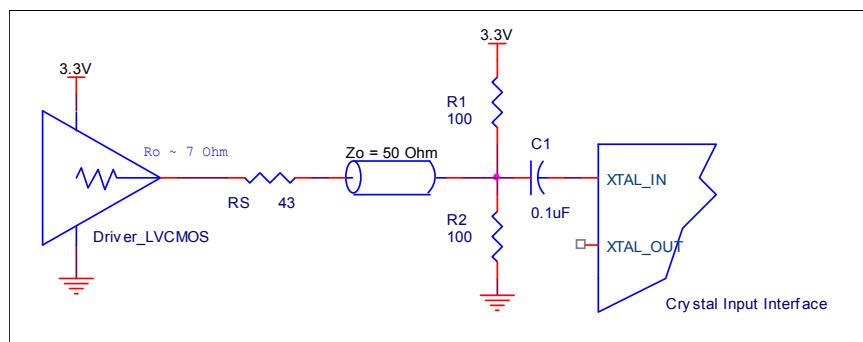


**Figure 3. Crystal Input Interface**

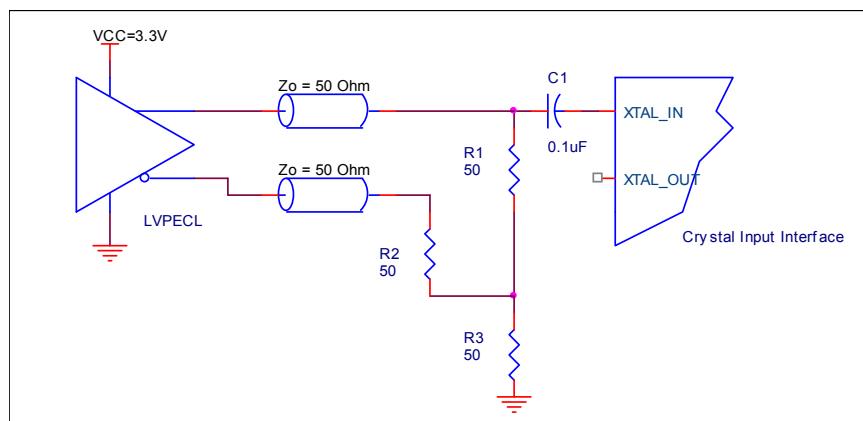
## Overdriving the XTAL Interface

The XTAL\_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4A*. The XTAL\_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition,

matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most  $50\Omega$  applications,  $R_1$  and  $R_2$  can be  $100\Omega$ . This can also be accomplished by removing  $R_1$  and making  $R_2 50\Omega$ . By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.



**Figure 4A. General Diagram for LVCMOS Driver to XTAL Input Interface**

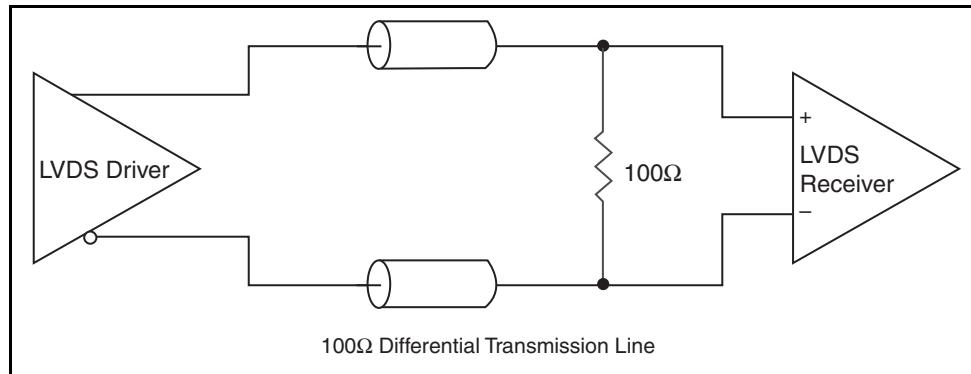


**Figure 4B. General Diagram for LVPECL Driver to XTAL Input Interface**

## LVDS Driver Termination

A general LVDS interface is shown in *Figure 5*. Standard termination for LVDS type output structure requires both a  $100\Omega$  parallel resistor at the receiver and a  $100\Omega$  differential transmission line environment. In order to avoid any transmission line reflection issues, the  $100\Omega$  resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard

termination schematic as shown in Figure 5 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.



**Figure 5. Typical LVDS Driver Termination**

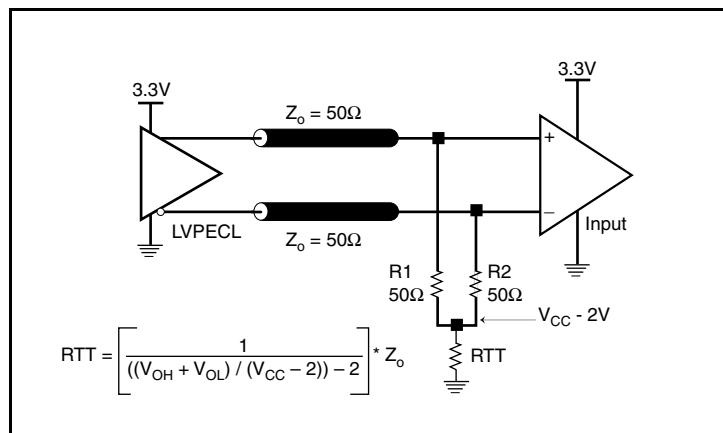
## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

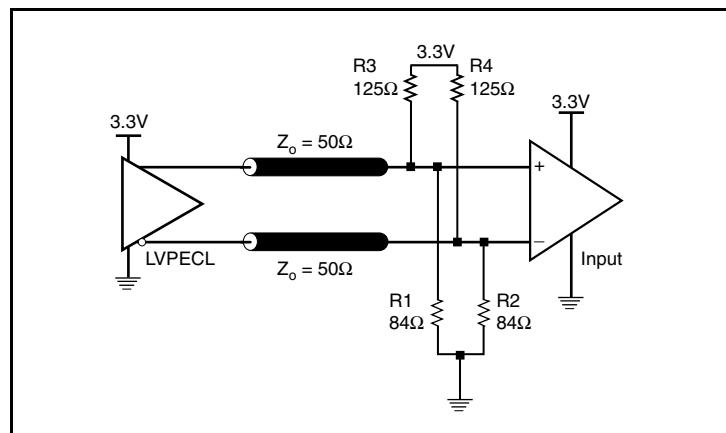
The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive  $50\Omega$

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

*Figures 6A and 6B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



**Figure 6A. 3.3V LVPECL Output Termination**



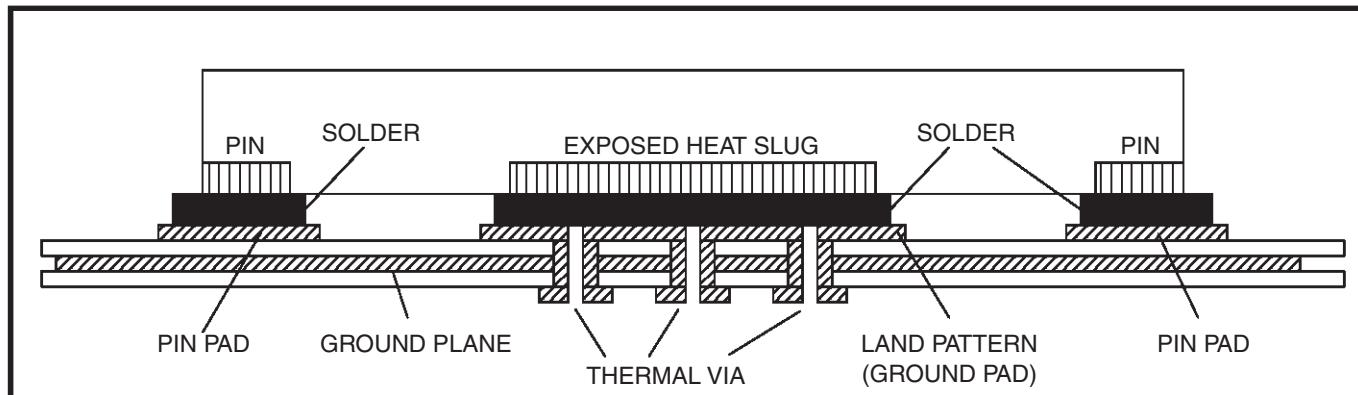
**Figure 6B. 3.3V LVPECL Output Termination**

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 7*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 7. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## Power Considerations (LVPECL)

This section provides information on power dissipation and junction temperature for the ICS849N2505I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS849N2505I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{EE\_MAX} = 3.465V * 200mA = 693\text{mW}$
- Power (outputs)<sub>MAX</sub> = **31.55mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $5 * 31.55\text{mW} = 157.75\text{mW}$

**Total Power<sub>MAX</sub>** (3.465V, with all outputs switching) =  $693\text{mW} + 157.75\text{mW} = 850.75\text{mW}$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and it directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * P_{d\_total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$P_{d\_total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$85^\circ\text{C} + 0.851\text{W} * 33.1^\circ\text{C/W} = 113.2^\circ\text{C}$ . This is below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

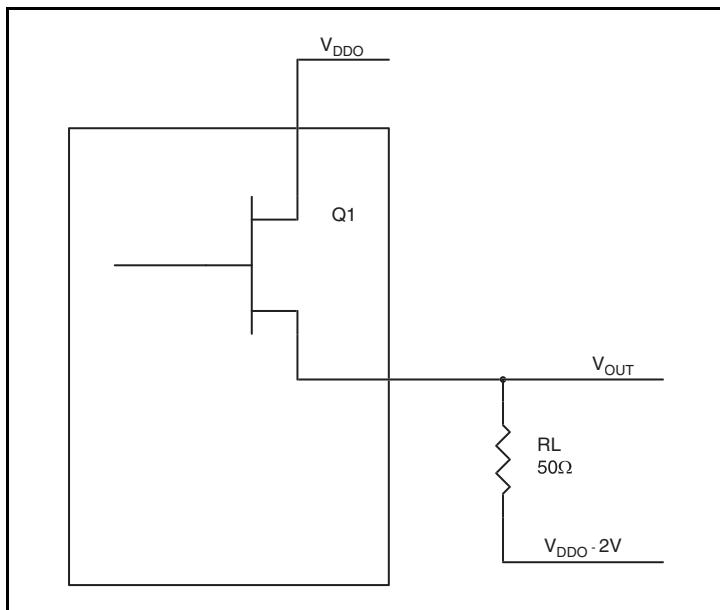
**Table 7. Thermal Resistance  $\theta_{JA}$  for 32 Lead VFQFN, Forced Convection**

| $\theta_{JA}$ by Velocity                   |          |          |          |
|---|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 3        |
| Multi-Layer PCB, JEDEC Standard Test Boards | 33.1°C/W | 28.1°C/W | 25.4°C/W |

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 8*.



**Figure 8. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a  $50\Omega$  load, and a termination voltage of  $V_{DD} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{DD\_MAX} - 0.75V$   
 $(V_{DD\_MAX} - V_{OH\_MAX}) = 0.75V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{DD\_MAX} - 1.6V$   
 $(V_{DD\_MAX} - V_{OL\_MAX}) = 1.6V$

$P_{d\_H}$  is power dissipation when the output drives high.

$P_{d\_L}$  is the power dissipation when the output drives low.

$$P_{d\_H} = [(V_{OH\_MAX} - (V_{DD\_MAX} - 2V))/R_L] * (V_{DD\_MAX} - V_{OH\_MAX}) = [(2V - (V_{DD\_MAX} - V_{OH\_MAX}))/R_L] * (V_{DD\_MAX} - V_{OH\_MAX}) = [(2V - 0.75V)/50\Omega] * 0.75V = 18.75mW$$

$$P_{d\_L} = [(V_{OL\_MAX} - (V_{DD\_MAX} - 2V))/R_L] * (V_{DD\_MAX} - V_{OL\_MAX}) = [(2V - (V_{DD\_MAX} - V_{OL\_MAX}))/R_L] * (V_{DD\_MAX} - V_{OL\_MAX}) = [(2V - 1.6V)/50\Omega] * 1.6V = 12.80mW$$

Total Power Dissipation per output pair =  $P_{d\_H} + P_{d\_L} = 31.55mW$

## Power Considerations (LVDS Outputs)

This section provides information on power dissipation and junction temperature for the ICS849N2505I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS849N2505I is the sum of the core power plus the analog power plus the power dissipation in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V * (223mA + 35mA) = 893.97mW$
- Power (outputs)<sub>MAX</sub> =  $V_{DDO\_MAX} * I_{DDO\_REF\_MAX} = 3.465V * 53mA = 183.645mW$

**Total Power<sub>MAX</sub>** = 893.97mW + 183.645mW = **1077.615mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * P_{d\_total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$P_{d\_total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 8 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 1.078W * 33.1^\circ C/W = 120.7^\circ C$ . This is below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 8. Thermal Resistance  $\theta_{JA}$  for 32 Lead VFQFN, Forced Convection**

| $\theta_{JA}$ by Velocity                   |          |          |          |
|---|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 3        |
| Multi-Layer PCB, JEDEC Standard Test Boards | 33.1°C/W | 28.1°C/W | 25.4°C/W |

## Reliability Information

**Table 9.  $\theta_{JA}$  vs. Air Flow Table for a 32 Lead VFQFN**

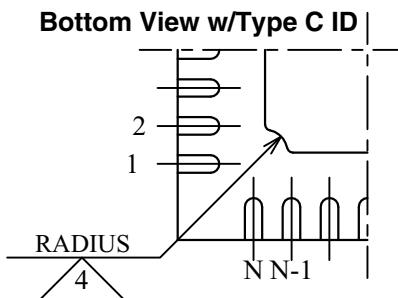
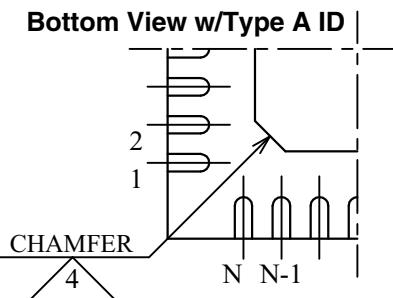
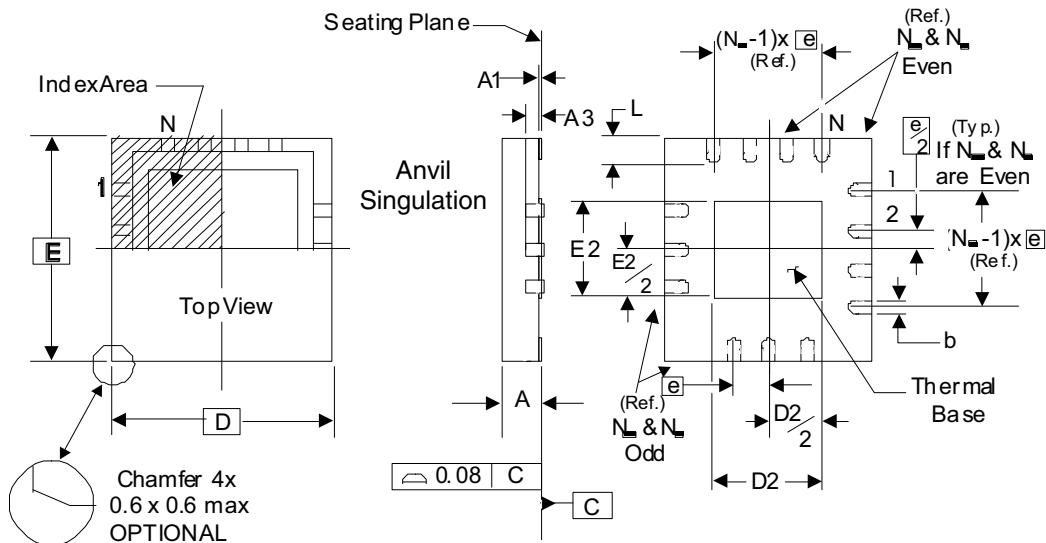
| $\theta_{JA}$ vs. Air Flow                  |          |          |          |
|---|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 3        |
| Multi-Layer PCB, JEDEC Standard Test Boards | 33.1°C/W | 28.1°C/W | 25.4°C/W |

## Transistor Count

The transistor count for ICS849N2505I is: 23,974

## Package Outline and Package Dimensions

### Package Outline - K Suffix for 32 Lead VFQFN



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

**Table 10. Package Dimensions**

| JEDEC Variation: VHHD-2/4       |         |            |         |
|---------------------------------|---------|------------|---------|
| All Dimensions in Millimeters   |         |            |         |
| Symbol                          | Minimum | Nominal    | Maximum |
| N                               |         | 32         |         |
| A                               | 0.80    |            | 1.00    |
| A1                              | 0       |            | 0.05    |
| A3                              |         | 0.25 Ref.  |         |
| b                               | 0.18    | 0.25       | 0.30    |
| N <sub>D</sub> & N <sub>E</sub> |         |            | 8       |
| D & E                           |         | 5.00 Basic |         |
| D2 & E2                         | 3.0     |            | 3.3     |
| e                               |         | 0.50 Basic |         |
| L                               | 0.30    | 0.40       | 0.50    |

The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 10.

Reference Document: JEDEC Publication 95, MO-220

## Ordering Information

**Table 11. Ordering Information**

| Part/Order Number | Marking     | Package                   | Shipping Packaging | Temperature    |
|-------------------|-------------|---------------------------|--------------------|----------------|
| 849N2505AKILF     | ICSN2505AIL | "Lead-Free" 32 Lead VFQFN | Tray               | -40°C to +85°C |
| 849N2505AKILFT    | ICSN2505AIL | "Lead-Free" 32 Lead VFQFN | 2500 Tape & Reel   | -40°C to +85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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## Revision History Sheet

| Rev | Table    | Page    | Description of Change  | Date     |
|-----|----------|---------|--|----------|
| B   | T6A -T6B | 6<br>20 | AC Characterisitcs Tables - updated Period Jitter specs.<br>Updated Package Outline. | 11/9/10  |
| B   | AMR      | 4       | Per Errata NEN-11-03; changed AMR from 4.6V to 3.63V                                 | 10/11/12 |

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