40MX and 42MX FPGA Families

Features

High Capacity

- Single-Chip ASIC Alternative
- 3,000 to 54,000 System Gates
- Up to 2.5 kbits Configurable Dual-Port SRAM
- Fast Wide-Decode Circuitry
- Up to 202 User-Programmable I/O Pins

High Performance

- 5.6 ns Clock-to-Out
- 250 MHz Performance
- 5 ns Dual-Port SRAM Access
- 100 MHz FIFOs
- 7.5 ns 35-Bit Address Decode

HiRel Features

- Commercial, Industrial, Automotive, and Military Temperature Plastic Packages
- Commercial, Military Temperature, and MIL-STD-883 Ceramic Packages
- QML Certification
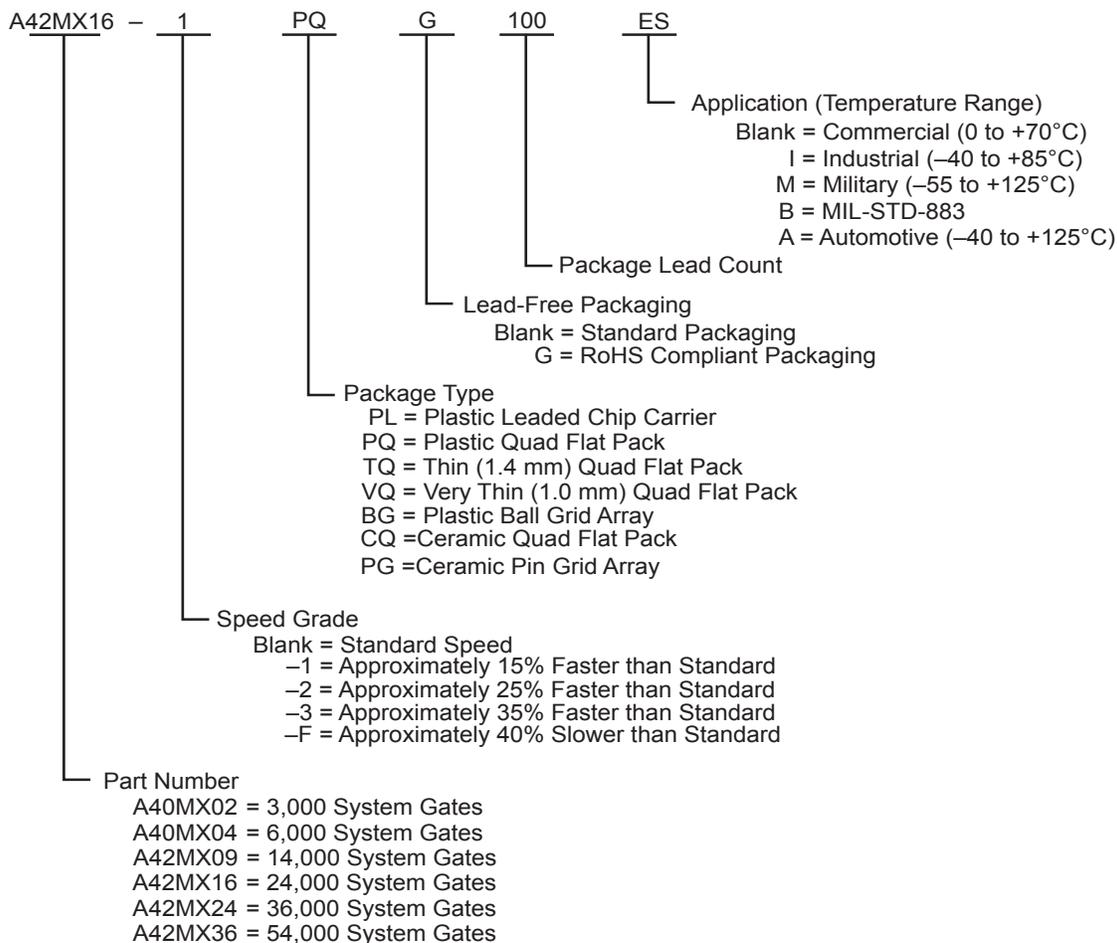- Ceramic Devices Available to DSCC SMD

Ease of Integration

- Mixed-Voltage Operation (5.0 V or 3.3 V for core and I/Os), with PCI-Compliant I/Os
- Up to 100% Resource Utilization and 100% Pin Locking
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Low Power Consumption
- IEEE Standard 1149.1 (JTAG) Boundary Scan Testing

Product Profile

Device	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
Capacity						
System Gates	3,000	6,000	14,000	24,000	36,000	54,000
SRAM Bits	–	–	–	–	–	2,560
Logic Modules						
Sequential	–	–	348	624	954	1,230
Combinatorial	295	547	336	608	912	1,184
Decode	–	–	–	–	24	24
Clock-to-Out	9.5 ns	9.5 ns	5.6 ns	6.1 ns	6.1 ns	6.3 ns
SRAM Modules (64x4 or 32x8)	–	–	–	–	–	10
Dedicated Flip-Flops	–	–	348	624	954	1,230
Maximum Flip-Flops	147	273	516	928	1,410	1,822
Clocks	1	1	2	2	2	6
User I/O (maximum)	57	69	104	140	176	202
PCI	–	–	–	–	Yes	Yes
Boundary Scan Test (BST)	–	–	–	–	Yes	Yes
Packages (by pin count)						
PLCC	44, 68	44, 68, 84	84	84	84	–
PQFP	100	100	100, 144, 160	100, 160, 208	160, 208	208, 240
VQFP	80	80	100	100	–	–
TQFP	–	–	176	176	176	–
CQFP	–	–	–	172	–	208, 256
PBGA	–	–	–	–	–	272
CPGA	–	–	132	–	–	–

Ordering Information

```
A42MX16  –  1     PQ     G    100     ES
```

Application (Temperature Range)
Blank = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)
M = Military (–55 to +125°C)
B = MIL-STD-883
A = Automotive (–40 to +125°C)

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS Compliant Packaging

Package Type
PL = Plastic Leaded Chip Carrier
PQ = Plastic Quad Flat Pack
TQ = Thin (1.4 mm) Quad Flat Pack
VQ = Very Thin (1.0 mm) Quad Flat Pack
BG = Plastic Ball Grid Array
CQ =Ceramic Quad Flat Pack
PG =Ceramic Pin Grid Array

Speed Grade
Blank = Standard Speed
–1 = Approximately 15% Faster than Standard
–2 = Approximately 25% Faster than Standard
–3 = Approximately 35% Faster than Standard
–F = Approximately 40% Slower than Standard

Part Number
A40MX02 = 3,000 System Gates
A40MX04 = 6,000 System Gates
A42MX09 = 14,000 System Gates
A42MX16 = 24,000 System Gates
A42MX24 = 36,000 System Gates
A42MX36 = 54,000 System Gates

Plastic Device Resources

Device	User I/Os											
	PLCC 44-Pin	PLCC 68-Pin	PLCC 84-Pin	PQFP 100-Pin	PQFP 144-Pin	PQFP 160-Pin	PQFP 208-Pin	PQFP 240-Pin	VQFP 80-Pin	VQFP 100-Pin	TQFP 176-Pin	PBGA 272-Pin
A40MX02	34	57	–	57	–	–	–	–	57	–	–	–
A40MX04	34	57	69	69	–	–	–	–	69	–	–	–
A42MX09	–	–	72	83	95	101	–	–	–	83	104	–
A42MX16	–	–	72	83	–	125	140	–	–	83	140	–
A42MX24	–	–	72	–	–	125	176	–	–	–	150	–
A42MX36	–	–	–	–	–	–	176	202	–	–	–	202

Note: **Package Definitions**
PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array

Ceramic Device Resources

Device	User I/Os			
	CPGA 132-Pin	CQFP 172-Pin	CQFP 208-Pin	CQFP 256-Pin
A42MX09	95			
A42MX16		131		
A42MX36			176	202

Note: **Package Definitions**   *CQFP = Ceramic Quad Flat Pack*

Temperature Grade Offerings

Package	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
PLCC 44	C, I, M	C, I, M				
PLCC 68	C, I, A, M	C, I, M				
PLCC 84		C, I, A, M	C, I, A, M	C, I, M	C, I, M	
PQFP 100	C, I, A, M	C, I, A, M	C, I, A, M	C, I, M		
PQFP 144			C			
PQFP 160			C, I, A, M	C, I, M	C, I, A, M	
PQFP 208				C, I, A, M	C, I, A, M	C, I, A, M
PQFP 240						C, I, A, M
VQFP 80	C, I, A, M	C, I, A, M				
VQFP 100			C, I, A, M	C, I, A, M		
TQFP 176			C, I, A, M	C, I, A, M	C, I, A, M	
PBGA 272						C, I, M
CQFP 172				C, M, B		
CQFP 208						C, M, B
CQFP 256						C, M, B
CPGA 132			C, M, B			

Note:

    C = Commercial

    I = Industrial

    A = Automotive

    M = Military

    B = MIL-STD-883 Class B

Speed Grade Offerings

	− F	Std	−1	−2	−3
C	✓	✓	✓	✓	✓
I		✓	✓	✓	✓
A		✓			
M		✓	✓		
B		✓	✓		

Note: *Refer to the* 40MX and 42MX Automotive Family FPGAs *datasheet for details on automotive-grade MX offerings.*

Contact your local Microsemi SoC Products Group representative for device availability.

Table of Contents

1 – 40MX and 42MX FPGA Families

General Description

Microsemi's 40MX and 42MX families offer a cost-effective design solution at 5V. The MX devices are single-chip solutions and provide high performance while shortening the system design and development cycle. MX devices can integrate and consolidate logic implemented in multiple PALs, CPLDs, and FPGAs. Example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and co-processor functions.

The MX device architecture is based on Microsemi's patented antifuse technology implemented in a 0.45µm triple-metal CMOS process. With capacities ranging from 3,000 to 54,000 system gates, the MX devices provide performance up to 250 MHz, are live on power-up and have one-fifth the standby power consumption of comparable FPGAs. MX FPGAs provide up to 202 user I/Os and are available in a wide variety of packages and speed grades.

A42MX24 and A42MX36 devices also feature MultiPlex I/Os, which support mixed-voltage systems, enable programmable PCI, deliver high-performance operation at both 5.0V and 3.3V, and provide a low-power mode. The devices are fully compliant with the PCI Local Bus Specification (version 2.1). They deliver 200 MHz on-chip operation and 6.1 ns clock-to-output performance.

The 42MX24 and 42MX36 devices include system-level features such as IEEE Standard 1149.1 (JTAG) Boundary Scan Testing and fast wide-decode modules. In addition, the A42MX36 device offers dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage. The storage elements can efficiently address applications requiring wide datapath manipulation and can perform transformation functions such as those required for telecommunications, networking, and DSP.

All MX devices are fully tested over automotive and military temperature ranges. In addition, the largest member of the family, the A42MX36, is available in both CQ208 and CQ256 ceramic packages screened to MIL-STD-883 levels. For easy prototyping and conversion from plastic to ceramic, the CQ208 and PQ208 devices are pin-compatible.

MX Architectural Overview

The MX devices are composed of fine-grained building blocks that enable fast, efficient logic designs. All devices within these families are composed of logic modules, I/O modules, routing resources and clock networks, which are the building blocks for fast logic designs. In addition, the A42MX36 device contains embedded dual-port SRAM modules, which are optimized for high-speed datapath functions such as FIFOs, LIFOs and scratchpad memory. A42MX24 and A42MX36 also contain wide-decode modules.

Logic Modules

The 40MX logic module is an eight-input, one-output logic circuit designed to implement a wide range of logic functions with efficient use of interconnect routing resources (Figure 1-1 on page 1-2).

The logic module can implement the four basic logic functions (NAND, AND, OR and NOR) in gates of two, three, or four inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs and OR-ANDs. No dedicated hard-wired latches or flip-flops are required in the array; latches and flip-flops can be constructed from logic modules whenever required in the application.
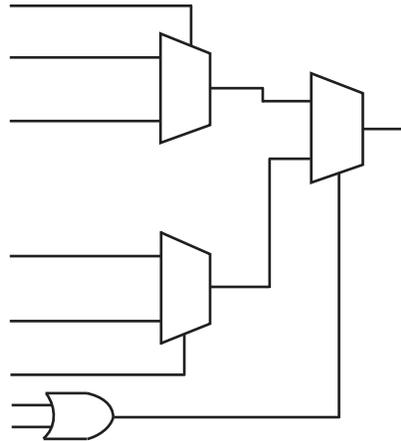
Figure 1-1 • **42MX C-Module Implementation**

The 42MX devices contain three types of logic modules: combinatorial (C-modules), sequential (S-modules) and decode (D-modules). Figure 1-2 illustrates the combinatorial logic module. The S-module, shown in Figure 1-3, implements the same combinatorial logic function as the C-module while adding a sequential element. The sequential element can be configured as either a D-flip-flop or a transparent latch. The S-module register can be bypassed so that it implements purely combinatorial logic.
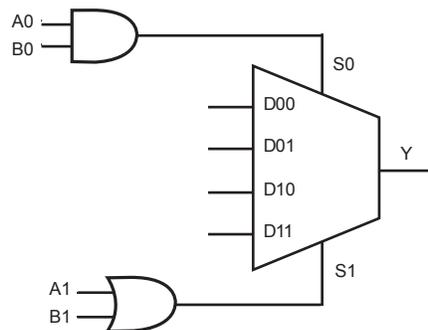

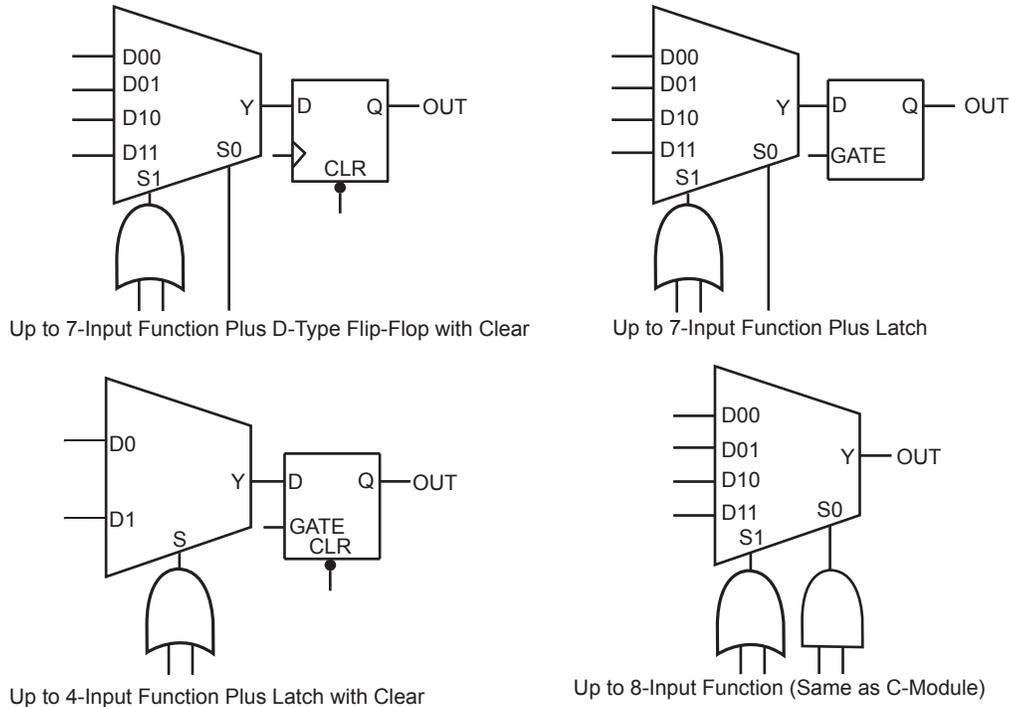*Figure 1-2 •* **42MX C-Module Implementation**

Up to 7-Input Function Plus D-Type Flip-Flop with Clear

Up to 7-Input Function Plus Latch

Up to 4-Input Function Plus Latch with Clear

Up to 8-Input Function (Same as C-Module)

Figure 1-3 • **42MX S-Module Implementation**

A42MX24 and A42MX36 devices contain D-modules, which are arranged around the periphery of the device. D-modules contain wide-decode circuitry, providing a fast, wide-input AND function similar to that found in CPLD architectures (Figure 1-4 on page 1-4). The D-module allows A42MX24 and A42MX36 devices to perform wide-decode functions at speeds comparable to CPLDs and PALs. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hardwired to an output pin, and can also be fed back into the array to be incorporated into other logic.

Dual-Port SRAM Modules

The A42MX36 device contains dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32x8 or 64x4. SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the A42MX36 dual-port SRAM block is shown in Figure 1-5 on page 1-4.

The A42MX36 SRAM modules are true dual-port structures containing independent read and write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4-bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]), which are connected to segmented vertical routing tracks.

The A42MX36 dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring FIFO and LIFO queues. The ACTgen Macro Builder within Microsemi's Designer software provides capability to quickly design memory functions with the SRAM blocks. Unused SRAM blocks can be used to implement registers for other user logic within the design.
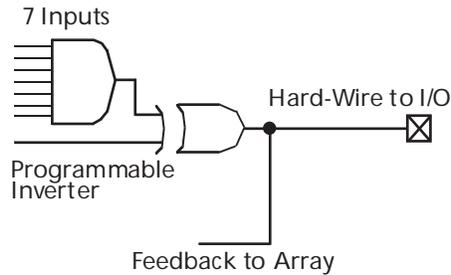
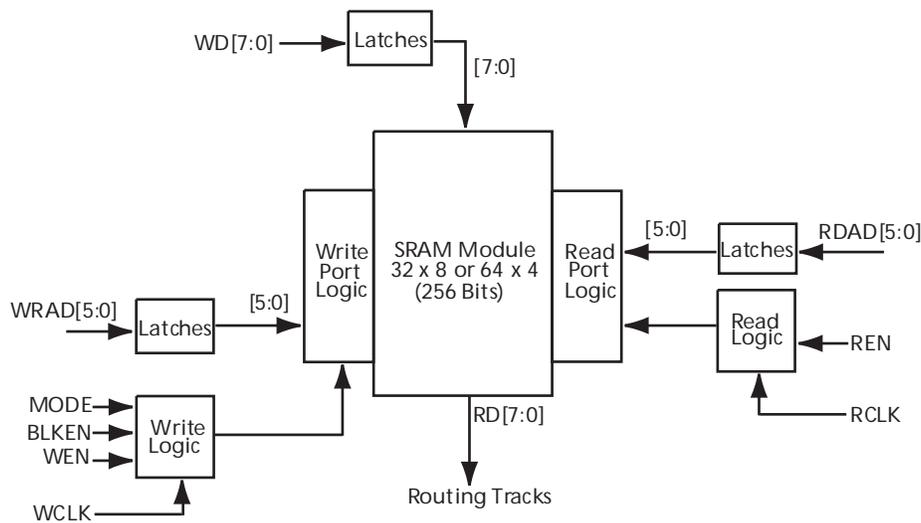*Figure 1-4 •*   **A42MX24 and A42MX36 D-Module Implementation**

Figure 1-5 •   **A42MX36 Dual-Port SRAM Block**

Routing Structure

The MX architecture uses vertical and horizontal routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may be continuous or split into segments. Varying segment lengths allow the interconnect of over 90% of design tracks to occur with only two antifuse connections. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track. All interconnects can be accomplished with a maximum of four antifuses.

Horizontal Routing

Horizontal routing tracks span the whole row length or are divided into multiple segments and are located in between the rows of modules. Any segment that spans more than one-third of the row length is considered a long horizontal segment. A typical channel is shown in Figure 1-6. Within horizontal routing, dedicated routing tracks are used for global clock networks and for power and ground tie-off tracks. Non-dedicated tracks are used for signal nets.

Vertical Routing

Another set of routing tracks run vertically through the module. There are three types of vertical tracks: input, output, and long. Long tracks span the column length of the module, and can be divided into multiple segments. Each segment in an input track is dedicated to the input of a particular module; each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing.

Each output segment spans four channels (two above and two below), except near the top and bottom of the array, where edge effects occur. Long vertical tracks contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 1-6.

Antifuse Structures

An antifuse is a "normally open" structure. The use of antifuses to implement a programmable logic device results in highly testable structures as well as efficient programming algorithms. There are no pre-existing connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed and individual circuit structures to be tested, which can be done before and after programming. For instance, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.
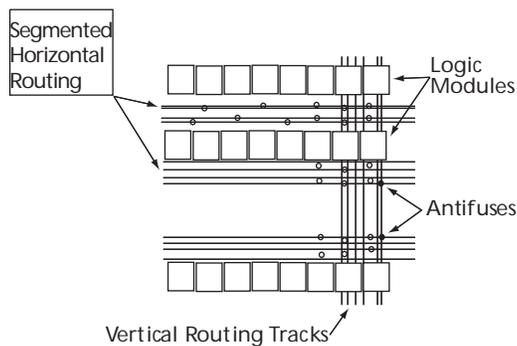
Figure 1-6 • **MX Routing Structure**

Clock Networks

The 40MX devices have one global clock distribution network (CLK). A signal can be put on the CLK network by being routed through the CLKBUF buffer.

In 42MX devices, there are two low-skew, high-fanout clock distribution networks, referred to as CLKA and CLKB. Each network has a clock module (CLKMOD) that can select the source of the clock signal from any of the following (Figure 1-7 on page 1-6):

- Externally from the CLKA pad, using CLKBUF buffer
- Externally from the CLKB pad, using CLKBUF buffer
- Internally from the CLKINTA input, using CLKINT buffer
- Internally from the CLKINTB input, using CLKINT buffer

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

Clock input pads in both 40MX and 42MX devices can also be used as normal I/Os, bypassing the clock networks.

The A42MX36 device has four additional register control resources, called quadrant clock networks (Figure 1-8 on page 1-6). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.
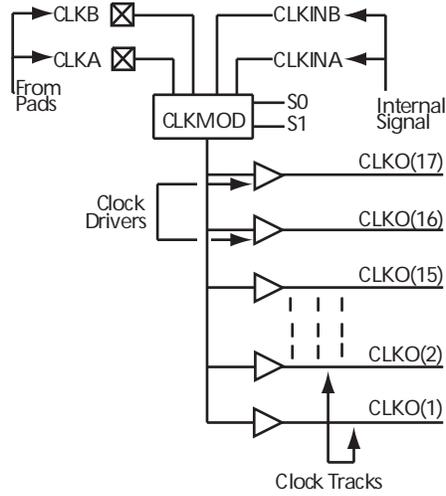
Figure 1-7 • **Clock Networks of 42MX Devices**
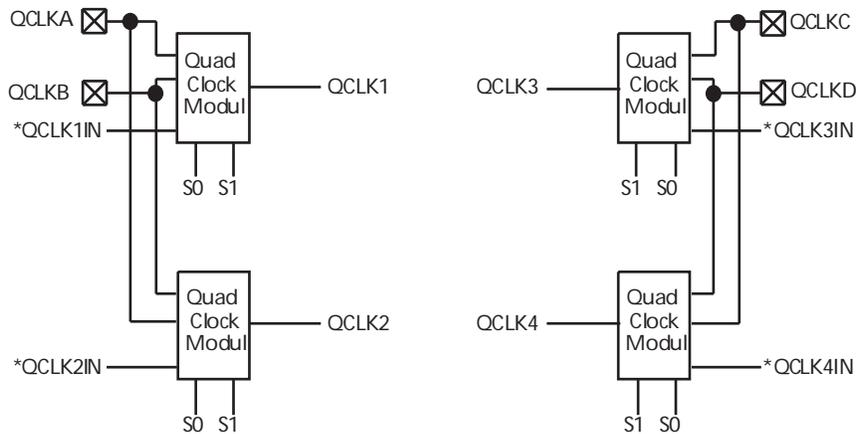
*Note: *QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.*

Figure 1-8 • **Quadrant Clock Network of A42MX36 Devices**

MultiPlex I/O Modules

42MX devices feature Multiplex I/Os and support 5.0 V, 3.3 V, and mixed 3.3 V/5.0 V operations.

The MultiPlex I/O modules provide the interface between the device pins and the logic array. Figure 1-9 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (Refer to the *Antifuse Macro Library Guide* for more information.) All 42MX I/O modules contain tristate buffers, with input and output latches that can be configured for input, output, or bidirectional operation.

All 42MX devices contain flexible I/O structures, where each output pin has a dedicated output-enable control (Figure 1-9). The I/O module can be used to latch input or output data, or both, providing fast set-up time. In addition, the Designer software tools can build a D-type flip-flop using a C-module combined with an I/O module to register input and output signals. Refer to the *Antifuse Macro Library Guide* for more details.

A42MX24 and A42MX36 devices also offer selectable PCI output drives, enabling 100% compliance with version 2.1 of the PCI specification. For low-power systems, all inputs and outputs are turned off to reduce current consumption to below 500 μA.

To achieve 5.0 V or 3.3 V PCI-compliant output drives on A42MX24 and A42MX36 devices, a chip-wide PCI fuse is programmed via the Device Selection Wizard in the Designer software (Figure 1-10). When the PCI fuse is not programmed, the output drive is standard.

Designer software development tools provide a design library of I/O macro functions that can implement all I/O configurations supported by the MX FPGAs.
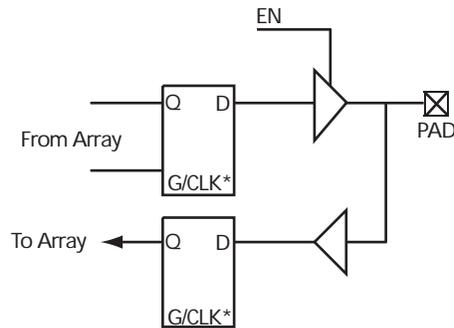
*Note: *Can be configured as a Latch or D Flip-Flop (Using C-Module)*
Figure 1-9 •   42MX I/O Module
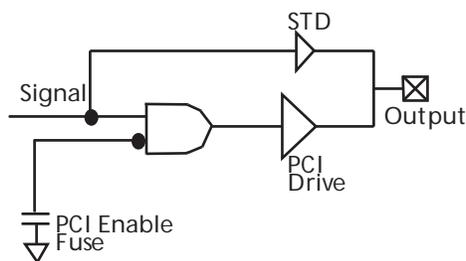
Figure 1-10 •   PCI Output Structure of A42MX24 and A42MX36 Devices

Other Architectural Features

Performance

MX devices can operate with internal clock frequencies of 250 MHz, enabling fast execution of complex logic functions. MX devices are live on power-up and do not require auxiliary configuration devices and thus are an optimal platform to integrate the functionality contained in multiple programmable logic devices. In addition, designs that previously would have required a gate array to meet performance can be integrated into an MX device with improvements in cost and time-to-market. Using timing-driven place-and-route (TDPR) tools, designers can achieve highly deterministic device performance.

User Security

Microsemi FuseLock provides robust security against design theft. Special security fuses are hidden in the fabric of the device and protect against unauthorized users attempting to access the programming and/or probe interfaces. It is virtually impossible to identify or bypass these fuses without damaging the device, making Microsemi antifuse FPGAs protected with the highest level of security available from both invasive and noninvasive attacks.

Special security fuses in 40MX devices include the Probe Fuse and Program Fuse. The former disables the probing circuitry while the latter prohibits further programming of all fuses, including the Probe Fuse. In 42MX devices, there is the Security Fuse which, when programmed, both disables the probing circuitry and prohibits further programming of the device.

Programming

Device programming is supported through the Silicon Sculptor series of programmers. Silicon Sculptor is a compact, robust, single-site and multi-site device programmer for the PC. With standalone software, Silicon Sculptor is designed to allow concurrent programming of multiple units from the same PC.

Silicon Sculptor programs devices independently to achieve the fastest programming times possible. After being programmed, each fuse is verified to insure that it has been programmed correctly. Furthermore, at the end of programming, there are integrity tests that are run to ensure no extra fuses have been programmed. Not only does it test fuses (both programmed and non-programmed), Silicon Sculptor also allows self-test to verify its own hardware extensively.

The procedure for programming an MX device using Silicon Sculptor is as follows:

1. Load the *.AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via In-House Programming from the factory.

For more details on programming MX devices, please refer to the *AC225: Programming Antifuse Devices* application note and the *Silicon Sculptor 3 Programmers User Guide*.

Power Supply

MX devices are designed to operate in both 5.0V and 3.3V environments. In particular, 42MX devices can operate in mixed 5.0 V/3.3 V systems. Table 1-1 describes the voltage support of MX devices.

Table 1-1 • **Voltage Support of MX Devices**

Device	VCC	VCCA	VCCI	Maximum Input Tolerance	Nominal Output Voltage
40MX	5.0 V	–	–	5.5 V	5.0 V
	3.3 V	–	–	3.6 V	3.3 V
42MX	–	5.0 V	5.0 V	5.5 V	5.0 V
	–	3.3 V	3.3 V	3.6 V	3.3 V
	–	5.0 V	3.3 V	5.5 V	3.3 V

For A42MX24 and A42MX36 devices the VCCA supply has to be monotonic during power up in order for the POR to issue reset to the JTAG state machine correctly. For more information, refer to *AC291: 42MX Family Devices Power-Up Behavior*.

Power-Up/Down in Mixed-Voltage Mode

When powering up 42MX in mixed voltage mode (VCCA = 5.0 V and VCCI = 3.3 V), VCCA must be greater than or equal to VCCI throughout the power-up sequence. If VCCI exceeds VCCA during power-up, one of two things will happen:

- The input protection diode on the I/Os will be forward biased
- The I/Os will be at logical High

In either case, ICC rises to high levels.

For power-down, any sequence with VCCA and VCCI can be implemented.

Transient Current

Due to the simultaneous random logic switching activity during power-up, a transient current may appear on the core supply (VCC). Customers must use a regulator for the VCC supply that can source a minimum of 100 mA for transient current during power-up. Failure to provide enough power can prevent the system from powering up properly and result in functional failure. However, there are no reliability concerns, since transient current is distributed across the die instead of confined to a localized spot.

Since the transient current is not due to I/O switching, its value and duration are independent of the VCCI.

Low Power Mode

42MX devices have been designed with a Low Power Mode. This feature, activated with setting the special LP pin to HIGH for a period longer than 800 ns, is particularly useful for battery-operated systems where battery life is a primary concern. In this mode, the core of the device is turned off and the device consumes minimal power with low standby current. In addition, all input buffers are turned off, and all outputs and bidirectional buffers are tristated. Since the core of the device is turned off, the states of the registers are lost. The device must be re-initialized when exiting Low Power Mode. I/Os can be driven during LP mode, and clock pins should be driven HIGH or LOW and should not float to avoid drawing current. To exit LP mode, the LP pin must be pulled LOW for over 200 µs to allow for charge pumps to power up, and device initialization will begin.

Power Dissipation

The general power consumption of MX devices is made up of static and dynamic power and can be expressed with the following equation.

General Power Equation

P = [ICCstandby + ICCactive] * VCCI + IOL* VOL* N + IOH * (VCCI – VOH) * M

where:

ICCstandby is the current flowing when no inputs or outputs are changing.

ICCactive is the current flowing due to CMOS switching.

IOL, IOH are TTL sink/source currents.

VOL, VOH are TTL level output voltages.

N equals the number of outputs driving TTL loads to VOL.

M equals the number of outputs driving TTL loads to VOH.

Accurate values for N and M are difficult to determine because they depend on the family type, on design details, and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

The static power due to standby current is typically a small component of the overall power consumption. Standby power is calculated for commercial, worst-case conditions. The static power dissipation by TTL loads depends on the number of outputs driving, and on the DC load current. For instance, a 32-bit bus sinking 4mA at 0.33V will generate 42mW with all outputs driving LOW, and 140mW with all outputs driving HIGH. The actual dissipation will average somewhere in between, as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the dynamic power dissipation. Dynamic power consumption is frequency-dependent and is a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitances due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

The power dissipated by a CMOS circuit can be expressed by the equation:

Power (µW) = C_{EQ} * VCCA2 * F(1)

where:

C_{EQ} = Equivalent capacitance expressed in picofarads (pF)

VCCA = Power supply in volts (V)

F = Switching frequency in megahertz (MHz)

Equivalent Capacitance

Equivalent capacitance is calculated by measuring ICCactive at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

C_{EQ} Values for Microsemi MX FPGAs

Modules (C_{EQM})3.5

Input Buffers (C_{EQI})6.9

Output Buffers (C_{EQO})18.2

Routed Array Clock Buffer Loads (C_{EQCR})1.4

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. The equation below shows a piece-wise linear summation over all components.

$$\text{Power} = VCCA^2 * [(m \times C_{EQM} * f_m)_{Modules} +$$
$$(n * C_{EQI} * f_n)_{Inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} +$$
$$0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} +$$
$$0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} \quad (2)$$

where:

m	=	Number of logic modules switching at frequency f_m
n	=	Number of input buffers switching at frequency f_n
p	=	Number of output buffers switching at frequency f_p
q_1	=	Number of clock loads on the first routed array clock
q_2	=	Number of clock loads on the second routed array clock
r_1	=	Fixed capacitance due to first routed array clock
r_2	=	Fixed capacitance due to second routed array clock
C_{EQM}	=	Equivalent capacitance of logic modules in pF
C_{EQI}	=	Equivalent capacitance of input buffers in pF
C_{EQO}	=	Equivalent capacitance of output buffers in pF
C_{EQCR}	=	Equivalent capacitance of routed array clock in pF
C_L	=	Output load capacitance in pF
f_m	=	Average logic module switching rate in MHz
f_n	=	Average input buffer switching rate in MHz
f_p	=	Average output buffer switching rate in MHz
f_{q1}	=	Average first routed array clock rate in MHz
f_{q2}	=	Average second routed array clock rate in MHz

Fixed Capacitance Values for MX FPGAs (pF)

Device Type	r1 routed_Clk1	r2 routed_Clk2
A40MX02	41.4	N/A
A40MX04	68.6	N/A
A42MX09	118	118
A42MX16	165	165
A42MX24	185	185
A42MX36	220	220

Test Circuitry and Silicon Explorer II Probe

MX devices contain probing circuitry that provides built-in access to every node in a design, via the use of Silicon Explorer II. Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer software, allow users to examine any of the internal nets of the device while it is operating in a prototyping or a production system. The user can probe into an MX device without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle and providing a true representation of the device under actual functional situations.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

Silicon Explorer II is used to control the MODE, DCLK, SDI and SDO pins in MX devices to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the MODE pin is held HIGH.

Figure 1-11 illustrates the interconnection between Silicon Explorer II and 40MX devices, while Figure 1-12 on page 1-12 illustrates the interconnection between Silicon Explorer II and 42MX devices

To allow for probing capabilities, the security fuses must not be programmed. (Refer to "User Security" section on page 1-8 for the security fuses of 40MX and 42MX devices). Table 1-2 on page 1-13 summarizes the possible device configurations for probing.

PRA and PRB pins are dual-purpose pins. When the "Reserve Probe Pin" is checked in the Designer software, PRA and PRB pins are reserved as dedicated outputs for probing. If PRA and PRB pins are required as user I/Os to achieve successful layout and "Reserve Probe Pin" is checked, the layout tool will override the option and place user I/Os on PRA and PRB pins.
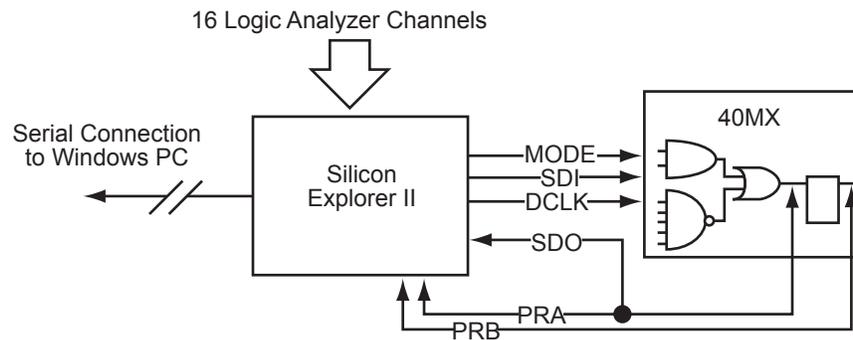
Figure 1-11 • **Silicon Explorer II Setup with 40MX**
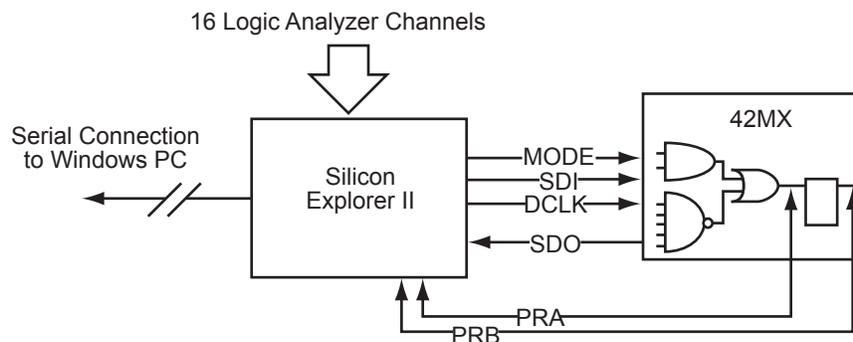
Figure 1-12 • **Silicon Explorer II Setup with 42MX**

Table 1-2 • **Device Configuration Options for Probe Capability**

Security Fuse(s) Programmed	Mode	PRA, PRB[1]	SDI, SDO, DCLK[1]
No	LOW	User I/Os[2]	User I/Os[2]
No	HIGH	Probe Circuit Outputs	Probe Circuit Inputs
Yes	–	Probe Circuit Secured	Probe Circuit Secured

Notes:

1. *Avoid using SDI, SDO, DCLK, PRA and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
2. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. See the "Pin Descriptions" section on page 1-83 for information on unused I/O pins.*

Design Consideration

It is recommended to use a series 70Ω termination resistor on every probe connector (SDI, SDO, MODE, DCLK, PRA and PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

IEEE Standard 1149.1 Boundary Scan Test (BST) Circuitry

42MX24 and 42MX36 devices are compatible with IEEE Standard 1149.1 (informally known as Joint Testing Action Group Standard or JTAG), which defines a set of hardware architecture and mechanisms for cost-effective board-level testing. The basic MX boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers and instruction register (Figure 1-13 on page 1-14). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and some optional instructions. Table 1-3 on page 1-14 describes the ports that control JTAG testing, while Table 1-4 on page 1-14 describes the test instructions supported by these MX devices.

Each test section is accessed through the TAP, which has four associated pins: TCK (test clock input), TDI and TDO (test data input and output), and TMS (test mode selector).

The TAP controller is a four-bit state machine. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles.

42MX24 and 42MX36 devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (lowest significant byte (LSB), ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

Each I/O cell has three boundary-scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin. The serial pins are used to serially connect all the boundary-scan register cells in a device into a boundary-scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic tile and the input, output and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.
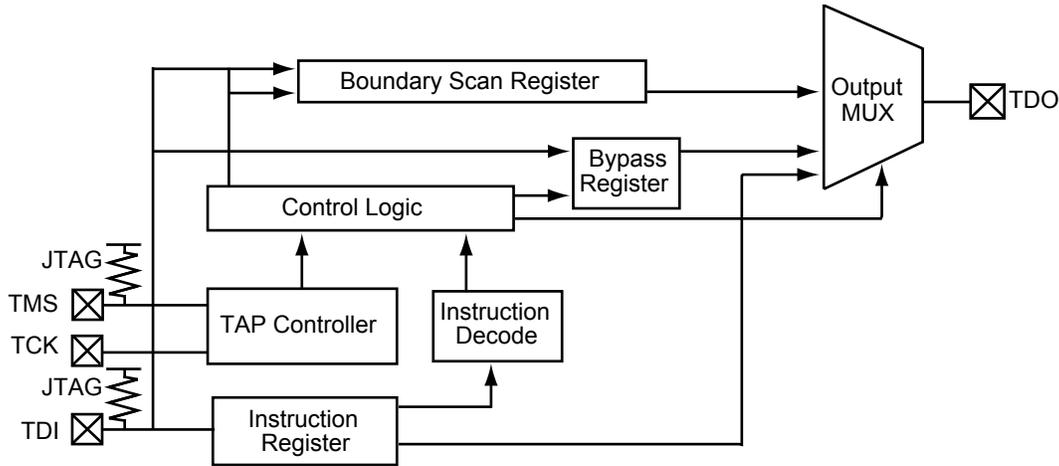
Figure 1-13 • **42MX IEEE 1149.1 Boundary Scan Circuitry**

Table 1-3 • **Test Access Port Descriptions**

Port	Description
TMS (Test Mode Select)	Serial input for the test logic control bits. Data is captured on the rising edge of the test logic clock (TCK).
TCK (Test Clock Input)	Dedicated test logic clock used serially to shift test instruction, test data, and control inputs on the rising edge of the clock, and serially to shift the output data on the falling edge of the clock. The maximum clock frequency for TCK is 20 MHz.
TDI (Test Data Input)	Serial input for instruction and test data. Data is captured on the rising edge of the test logic clock.
TDO (Test Data Output)	Serial output for test instruction and data from the test logic. TDO is set to an Inactive Drive state (high impedance) when data scanning is not in progress.

Table 1-4 • **Supported BST Public Instructions**

Instruction	IR Code (IR2.IR0)	Instruction Type	Description
EXTEST	000	Mandatory	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
SAMPLE/PRELOAD	001	Mandatory	Allows a snapshot of the signals at the device pins to be captured and examined during operation
HIGH Z	101	Optional	Tristates all I/Os to allow external signals to drive pins. Please refer to the IEEE Standard 1149.1 specification.
CLAMP	110	Optional	Allows state of signals driven from component pins to be determined from the Boundary-Scan Register. Please refer to the IEEE Standard 1149.1 specification for details.
BYPASS	111	Mandatory	Enables the bypass register between the TDI and TDO pins. The test data passes through the selected device to adjacent devices in the test chain.

JTAG Mode Activation

The JTAG test logic circuit is activated in the Designer software by selecting **Tools > Device Selection**. This brings up the Device Selection dialog box as shown in Figure 1-14. The JTAG test logic circuit can be enabled by clicking the "Reserve JTAG Pins" check box. Table 1-5 explains the pins' behavior in either mode.

Figure 1-14 • **Device Selection Wizard**

Table 1-5 • **Boundary Scan Pin Configuration and Functionality**

Reserve JTAG	Checked	Unchecked
TCK	BST input; must be terminated to logical HIGH or LOW to avoid floating	User I/O
TDI, TMS	BST input; may float or be tied to HIGH	User I/O
TDO	BST output; may float or be connected to TDI of another device	User I/O

TRST Pin and TAP Controller Reset

An active reset (TRST) pin is not supported; however, MX devices contain power-on circuitry that resets the boundary scan circuitry upon power-up. Also, the TMS pin is equipped with an internal pull-up resistor. This allows the TAP controller to remain in or return to the Test-Logic-Reset state when there is no input or when a logical 1 is on the TMS pin. To reset the controller, TMS must be HIGH for at least five TCK cycles.

Boundary Scan Description Language (BSDL) File

Conforming to the IEEE Standard 1149.1 requires that the operation of the various JTAG components be documented. The BSDL file provides the standard format to describe the JTAG components that can be used by automatic test equipment software. The file includes the instructions that are supported, instruction bit pattern, and the boundary-scan chain order. For an in-depth discussion on BSDL files, please refer to the *BSDL Files Format Description* application note.

BSDL files are grouped into two categories - generic and device-specific. The generic files assign all user I/Os as inouts. Device-specific files assign user I/Os as inputs, outputs or inouts.

Generic files for MX devices are available on the Microsemi SoC Product Group's website:

http://www.microsemi.com/soc/techdocs/models/bsdl.html.

Development Tool Support

The MX family of FPGAs is fully supported by Libero® Integrated Design Environment (IDE). Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes SynplifyPro from Synopsys, ModelSim® HDL Simulator from Mentor Graphics,® and Viewdraw.

Libero IDE includes place-and-route and provides a comprehensive suite of backend support tools for FPGA development, including timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor.

Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Microsemi's integrated verification and logic analysis tool. Another tool included in the Libero software is the SmartGen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Microsemi's Libero software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synopsys, and Cadence Design Systems.

Refer to the Libero IDE web content at www.microsemi.com/soc/products/software/libero/default.aspx for further information on licensing and current operating system support.

Related Documents

Application Notes

AC278: BSDL Files Format Description

AC225: Programming Antifuse Devices

AC168: Implementation of Security in Microsemi Antifuse FPGAs

User Guides and Manuals

Antifuse Macro Library Guide

Silicon Sculptor Programmers User Guide

Miscellaneous

Libero IDE Flow Diagram

5.0 V Operating Conditions

Table 1-6 • **Absolute Maximum Ratings for 40MX Devices***

Symbol	Parameter	Limits	Units
VCC	DC Supply Voltage	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCC+0.5	V
VO	Output Voltage	–0.5 to VCC+0.5	V
t_{STG}	Storage Temperature	–65 to +150	°C

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Table 1-7 • **Absolute Maximum Ratings for 42MX Devices***

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	–0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCCI+0.5	V
VO	Output Voltage	–0.5 to VCCI+0.5	V
t_{STG}	Storage Temperature	–65 to +150	°C

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Table 1-8 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCC (40MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCA (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V

Note: ** Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.*

5 V TTL Electrical Specifications

Table 1-9 •   5V TTL Electrical Specifications

Symbol	Parameter	Commercial		Commercial -F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH[1]	IOH = –10 mA	2.4		2.4						V
	IOH = –4 mA					3.7		3.7		V
VOL[1]	IOL = 10 mA		0.5		0.5					V
	IOL = 6 mA						0.4		0.4	V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH (40MX)		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIH (42MX)		2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	V
IIL	VIN = 0.5 V		–10		–10		–10		–10	µA
IIH	VIN = 2.7 V		–10		–10		–10		–10	µA
Input Transition Time, T_R and T_F			500		500		500		500	ns
C_{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC[2]	A40MX02, A40MX04		3		25		10		25	mA
	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		20		25		25		25	mA
Low power mode Standby Current	42MX devices only		0.5		ICC – 5.0		ICC – 5.0		ICC – 5.0	mA
IIO, I/O source sink current	Can be derived from the *IBIS model* (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

Notes:

1. *Only one output tested at a time. VCC/VCCI = min.*
2. *All outputs unloaded. All inputs = VCC/VCCI or GND.*

3.3 V Operating Conditions

Table 1-10 • **Absolute Maximum Ratings for 40MX Devices***

Symbol	Parameter	Limits	Units
VCC	DC Supply Voltage	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCC + 0.5	V
VO	Output Voltage	–0.5 to VCC + 0.5	V
t$_{STG}$	Storage Temperature	–65 to + 150	°C

Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Table 1-11 • **Absolute Maximum Ratings for 42MX Devices***

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	–0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCCI+0.5	V
VO	Output Voltage	–0.5 to VCCI+0.5	V
t$_{STG}$	Storage Temperature	–65 to +150	°C

Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Table 1-12 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCC (40MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCA (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCI (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.*

3.3 V LVTTL Electrical Specifications

Table 1-13 • **3.3V LVTTL Electrical Specifications**

Symbol	Parameter	Commercial		Commercial -F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH[1]	IOH = –4 mA	2.15		2.15		2.4		2.4		V
VOL[1]	IOL = 6 mA		0.4		0.4		0.48		0.48	V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH (40MX)		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIH (42MX)		2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	V
IIL			–10		–10		–10		–10	μA
IIH			–10		–10		–10		–10	μA
Input Transition Time, T_R and T_F			500		500		500		500	ns
C_{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC[2]	A40MX02, A40MX04		3		25		10		25	mA
	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		15		25		25		25	mA
Low-Power Mode Standby Current	42MX devices only		0.5		ICC - 5.0		ICC - 5.0		ICC - 5.0	mA
IIO, I/O source sink current	Can be derived from the *IBIS model* (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

Notes:

1. *Only one output tested at a time. VCC/VCCI = min.*
2. *All outputs unloaded. All inputs = VCC/VCCI or GND.*

Mixed 5.0 V / 3.3 V Operating Conditions (for 42MX Devices Only)

Table 1-14 • **Absolute Maximum Ratings***

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	–0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCCA +0.5	V
VO	Output Voltage	–0.5 to VCCI + 0.5	V
t_{STG}	Storage Temperature	–65 to +150	°C

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Table 1-15 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCCA	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI	3.14 to 3.47	3.0 to 3.6	3.0 to 3.6	V

Note: **Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.*

Mixed 5.0V/3.3V Electrical Specifications

Table 1-16 • **Mixed 5.0V/3.3V Electrical Specifications**

Symbol	Parameter	Commercial Min.	Commercial Max.	Commercial –F Min.	Commercial –F Max.	Industrial Min.	Industrial Max.	Military Min.	Military Max.	Units
VOH[1]	IOH = –10 mA	2.4		2.4						V
	IOH = –4 mA					2.4		2.4		V
VOL[1]	IOL = 10 mA		0.5		0.5					V
	IOL = 6 mA						0.4		0.4	V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH		2.0	VCCA + 0.3	2.0	VCCA + 0.3	2.0	VCCA + 0.3	2.0	VCCA + 0.3	V
IL	VIN = 0.5 V		–10		–10		–10		–10	µA
IH	VIN = 2.7 V		–10		–10		–10		–10	µA
Input Transition Time, T_R and T_F			500		500		500		500	ns
C_{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC[2]	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		20		25		25		25	mA
Low Power Mode Standby Current			0.5		ICC – 5.0		ICC – 5.0		ICC – 5.0	mA
IIO I/O source sink current	Can be derived from the *IBIS model* (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

Notes:

1. *Only one output tested at a time. VCCI = min.*
2. *All outputs unloaded. All inputs = VCCI or GND.*

Output Drive Characteristics for 5.0 V PCI Signaling

MX PCI device I/O drivers were designed specifically for high-performance PCI systems. Figure 1-15 on page 1-25 shows the typical output drive characteristics of the MX devices. MX output drivers are compliant with the PCI Local Bus Specification.

Table 1-17 • **DC Specification (5.0 V PCI Signaling)[1]**

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
VCCI	Supply Voltage for I/Os		4.75	5.25	4.75	5.25[2]	V
VIH	Input High Voltage		2.0	VCC + 0.5	2.0	VCCI + 0.3	V
VIL	Input Low Voltage		–0.5	0.8	–0.3	0.8	V
IIH	Input High Leakage Current	VIN = 2.7 V		70	—	10	µA
IIL	Input Low Leakage Current	VIN=0.5 V		–70	—	–10	µA
VOH	Output High Voltage	IOUT = –2 mA IOUT = –6 mA	2.4		3.84		V
VOL	Output Low Voltage	IOUT = 3 mA, 6 mA		0.55	—	0.33	V
C_{IN}	Input Pin Capacitance			10	—	10	pF
C_{CLK}	CLK Pin Capacitance		5	12	—	10	pF
L_{PIN}	Pin Inductance			20	—	< 8 nH[3]	nH

Notes:

1. *PCI Local Bus Specification, Version 2.1, Section 4.2.1.1.*
2. *Maximum rating for VCCI –0.5 V to 7.0 V.*
3. *Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.*

Table 1-18 • **AC Specifications (5.0V PCI Signaling)[*]**

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
ICL	Low Clamp Current	–5 < VIN ≤ –1	–25 + (VIN +1) /0.015		–60	–10	mA
Slew (r)	Output Rise Slew Rate	0.4 V to 2.4 V load	1	5	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	2.4 V to 0.4 V load	1	5	2.8	4.3	V/ns

Note: **PCI Local Bus Specification, Version 2.1, Section 4.2.1.2.*

Output Drive Characteristics for 3.3 V PCI Signaling

Table 1-19 • **DC Specification (3.3 V PCI Signaling)[1]**

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
VCCI	Supply Voltage for I/Os		3.0	3.6	3.0	3.6	V
VIH	Input High Voltage		0.5	VCC + 0.5	0.5	VCCI + 0.3	V
VIL	Input Low Voltage		–0.5	0.8	–0.3	0.8	V
IIH	Input High Leakage Current	VIN = 2.7 V		70		10	µA
IIL	Input Leakage Current			–70		–10	µA
VOH	Output High Voltage	IOUT = –2 mA	0.9		3.3		V
VOL	Output Low Voltage	IOUT = 3 mA, 6 mA		0.1		0.1 VCCI	V
C_{IN}	Input Pin Capacitance			10		10	pF
C_{CLK}	CLK Pin Capacitance		5	12		10	pF
L_{PIN}	Pin Inductance			20		< 8 nH[3]	nH

Notes:

1. *PCI Local Bus Specification, Version 2.1, Section 4.2.2.1.*
2. *Maximum rating for VCCI –0.5 V to 7.0V.*
3. *Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.*

Table 1-20 • **AC Specifications for (3.3 V PCI Signaling)[*]**

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
ICL	Low Clamp Current	–5 < VIN ≤ –1	–25 + (VIN +1) /0.015		–60	–10	mA
Slew (r)	Output Rise Slew Rate	0.2 V to 0.6 V load	1	4	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	0.6 V to 0.2 V load	1	4	2.8	4.0	V/ns

Note: **PCI Local Bus Specification, Version 2.1, Section 4.2.2.2.*
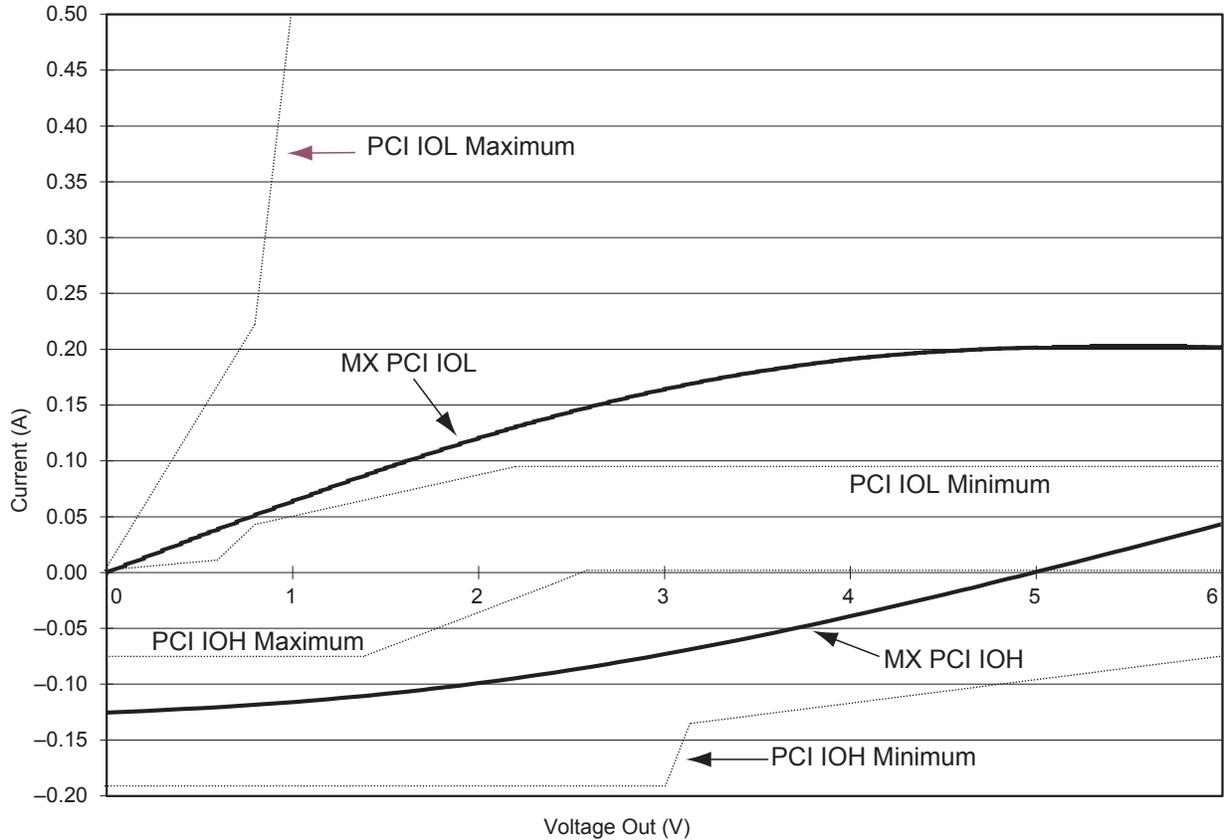
Figure 1-15 • **Typical Output Drive Characteristics (Based Upon Measured Data)**

Junction Temperature (T$_J$)

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. EQ , shown below, can be used to calculate junction temperature.

Junction Temperature = $\Delta T + T_a$ (1)

EQ 1

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$\Delta T = \theta_{ja} * P$ (2)

P = Power

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in Table 1-21 on page 1-26.

Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc}, and the junction-to-ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

The maximum junction temperature is 150°C.

Maximum power dissipation for commercial- and industrial-grade devices is a function of θ_{ja}.

A sample calculation of the absolute maximum power dissipation allowed for a TQ176 package at commercial temperature and still air is given in EQ 2.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{150°C - 70°C}{28°C/W} = 2.86 \text{ W}$$

EQ 2

The maximum power dissipation for military-grade devices is a function of θ_{jc}. A sample calculation of the absolute maximum power dissipation allowed for CQFP 208-pin package at military temperature and still air is given in EQ 3.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{jc}(\text{°C/W})} = \frac{150°C - 125°C}{6.3°C/W} = 3.97 \text{ W}$$

EQ 3

Table 1-21 • **Package Thermal Characteristics**

Plastic Packages	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	1.0 m/s 200 ft/min.	2.5 m/s 500 ft/min.	
Plastic Quad Flat Pack	100	12.0	27.8	23.4	21.2	°C/W
Plastic Quad Flat Pack	144	10.0	26.2	22.8	21.1	°C/W
Plastic Quad Flat Pack	160	10.0	26.2	22.8	21.1	°C/W
Plastic Quad Flat Pack	208	8.0	26.1	22.5	20.8	°C/W
Plastic Quad Flat Pack	240	8.5	25.6	22.3	20.8	°C/W
Plastic Leaded Chip Carrier	44	16.0	20.0	24.5	22.0	°C/W
Plastic Leaded Chip Carrier	68	13.0	25.0	21.0	19.4	°C/W
Plastic Leaded Chip Carrier	84	12.0	22.5	18.9	17.6	°C/W
Thin Plastic Quad Flat Pack	176	11.0	24.7	19.9	18.0	°C/W
Very Thin Plastic Quad Flat Pack	80	12.0	38.2	31.9	29.4	°C/W
Very Thin Plastic Quad Flat Pack	100	10.0	35.3	29.4	27.1	°C/W
Plastic Ball Grid Array	272	3.0	18.3	14.9	13.9	°C/W
Ceramic Packages						
Ceramic Pin Grid Array	132	4.8	25.0	20.6	18.7	°C/W
Ceramic Quad Flat Pack	208	2.0	22.0	19.8	18.0	°C/W
Ceramic Quad Flat Pack	256	2.0	20.0	16.5	15.0	°C/W

Timing Models
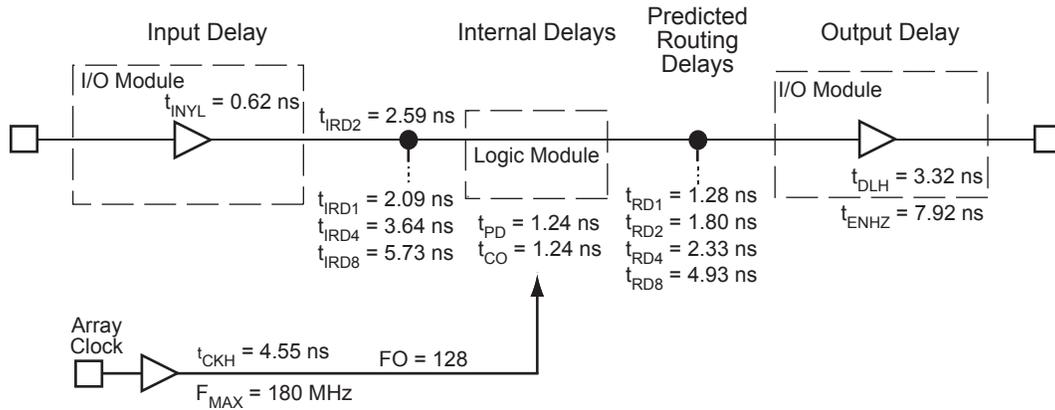
Note: Values are shown for 40MX –3 speed devices at 5.0 V worst-case commercial conditions.

Figure 1-16 • 40MX Timing Model
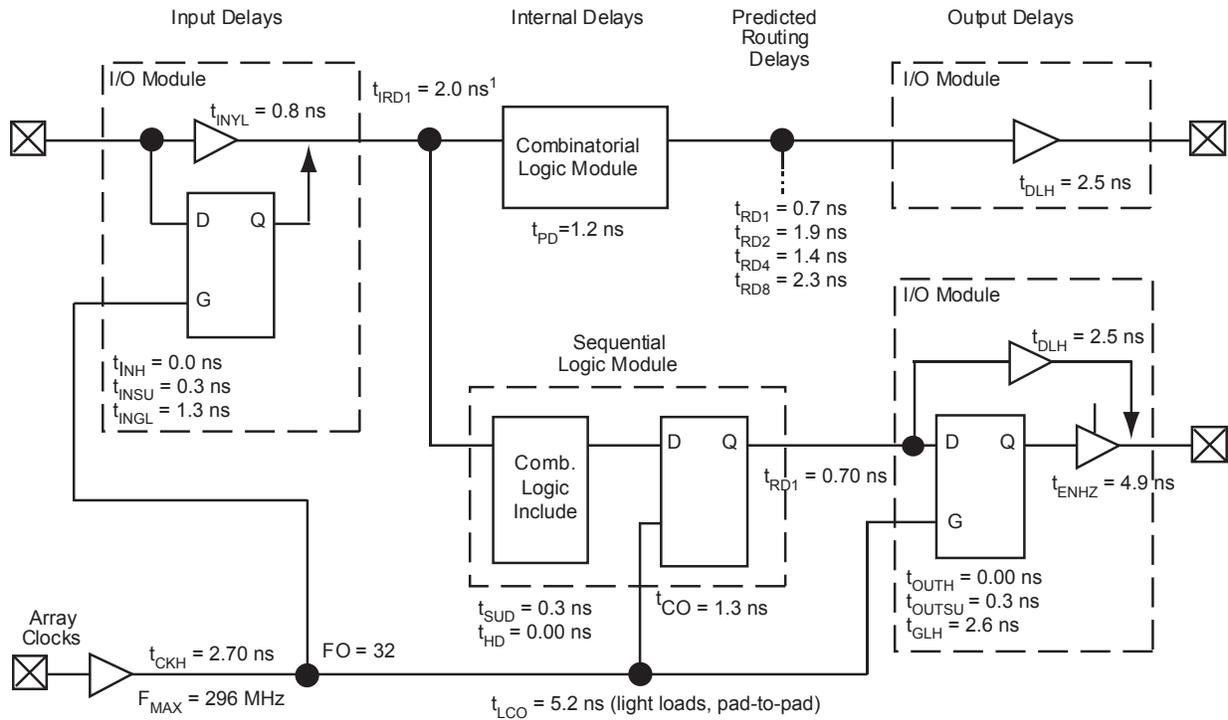
Notes:

1. Input module predicted routing delay
2. Values are shown for A42MX09 –3 at 5.0 V worst-case commercial conditions.

Figure 1-17 • 42MX Timing Model
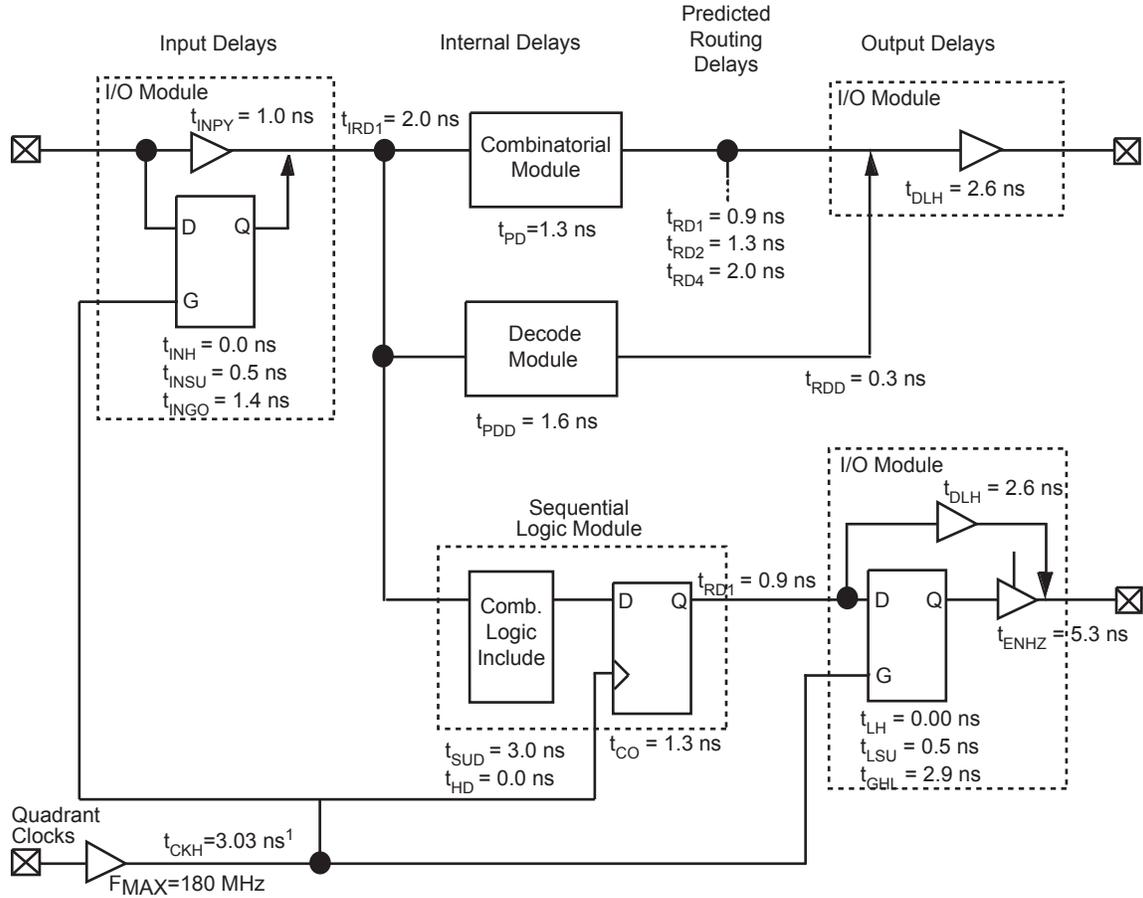
Notes:

1. *Load-dependent*
2. *Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions.*

Figure 1-18 • 42MX Timing Model (Logic Functions Using Quadrant Clocks)
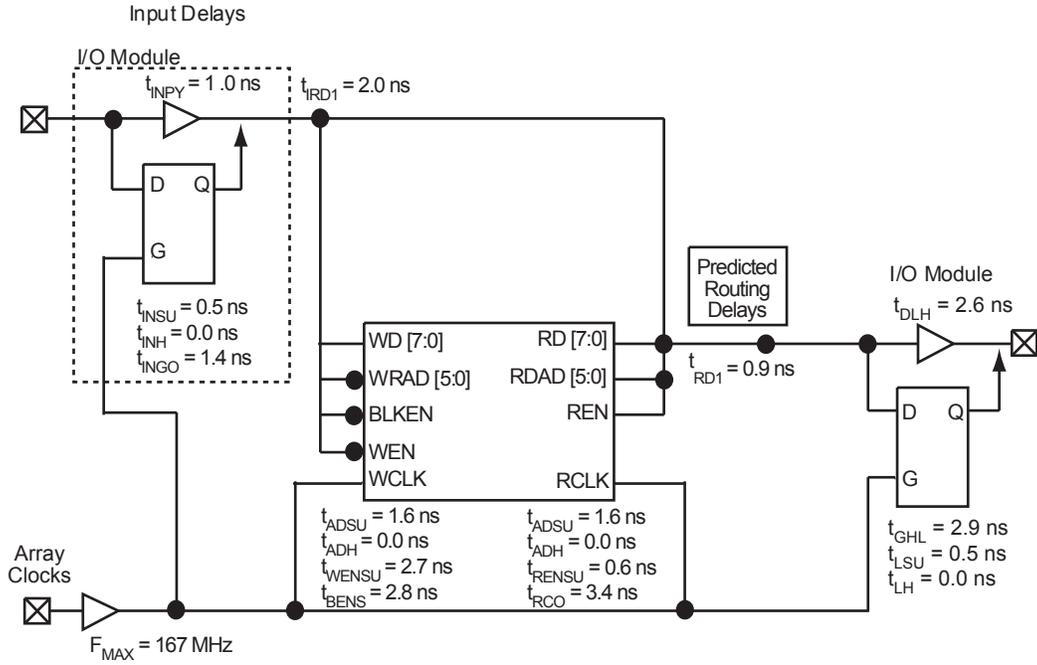
Input Delays

Note: Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions.

***Figure 1-19 •* 42MX Timing Model (SRAM Functions)**

Parameter Measurement
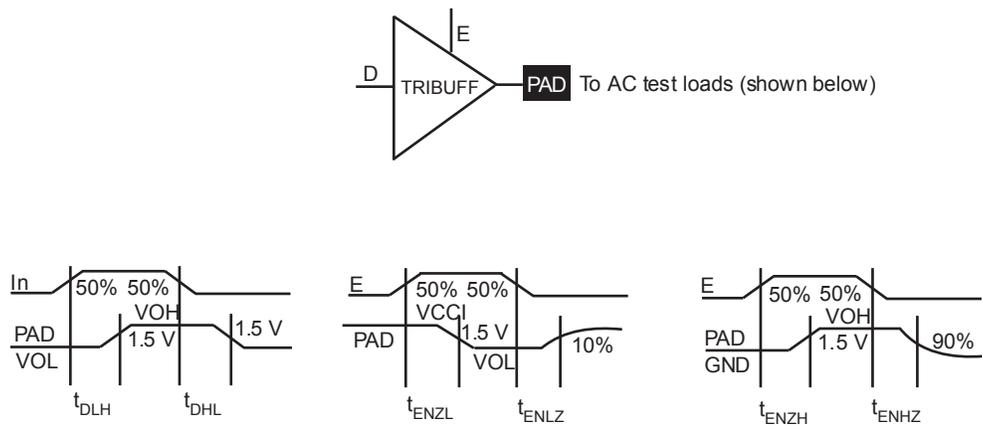
Figure 1-20 • **Output Buffer Delays**
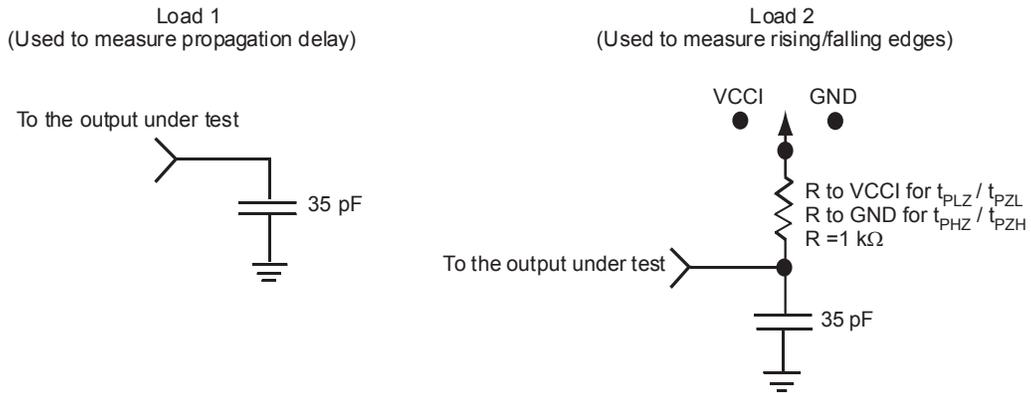
Figure 1-21 • **AC Test Loads**
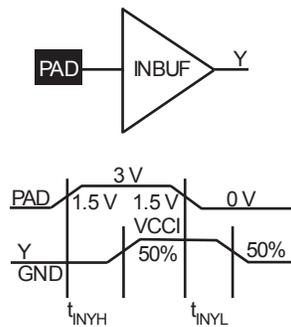
Figure 1-22 • **Input Buffer Delays**
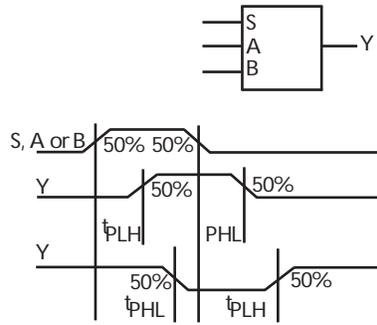
Figure 1-23 • **Module Delays**

Sequential Module Timing Characteristics

(Positive Edge-Triggered)
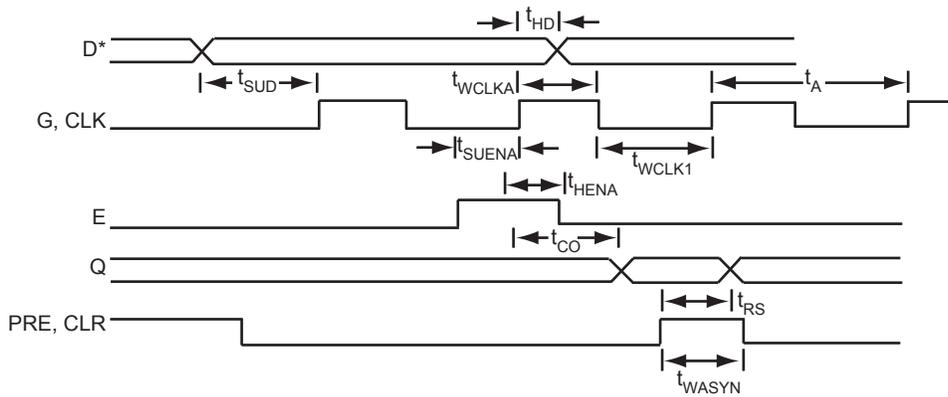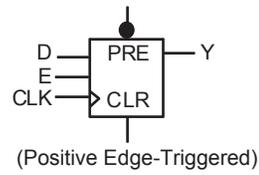
Note: *D represents all data functions involving A, B, and S for multiplexed flip-flops.*

Figure 1-24 • **Flip-Flops and Latches**

Sequential Timing Characteristics
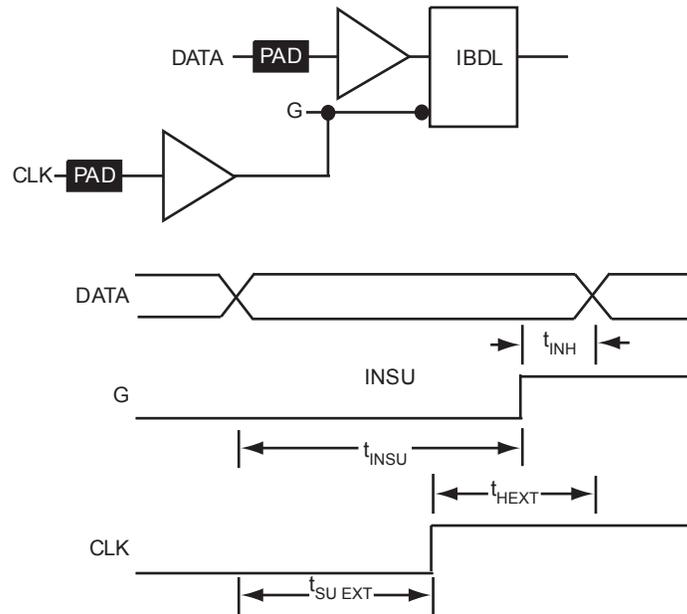
Figure 1-25 • **Input Buffer Latches**
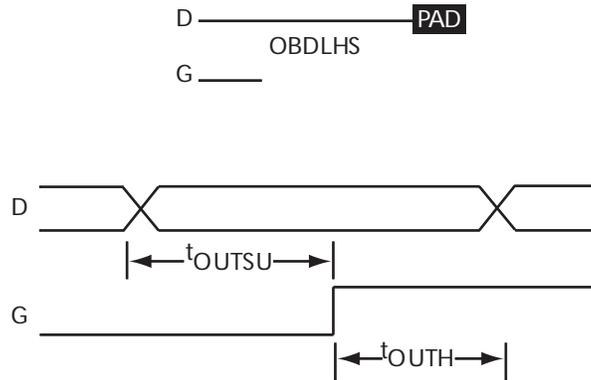
Figure 1-26 • **Output Buffer Latches**

Decode Module Timing
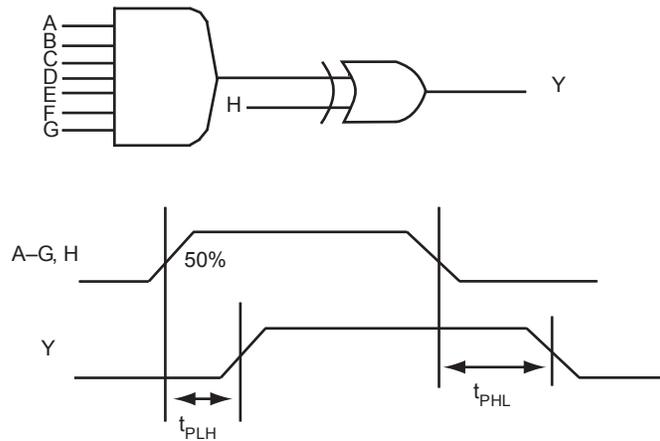
Figure 1-27 • **Decode Module Timing**

SRAM Timing Characteristics
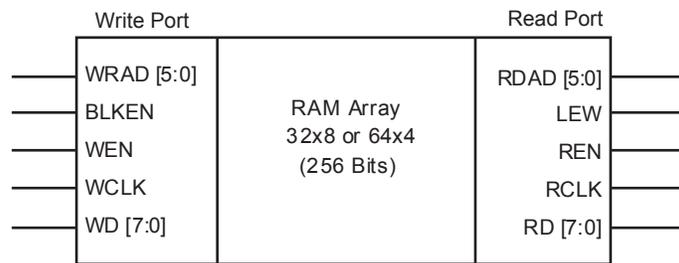
Figure 1-28 • **SRAM Timing Characteristics**

Dual-Port SRAM Timing Waveforms
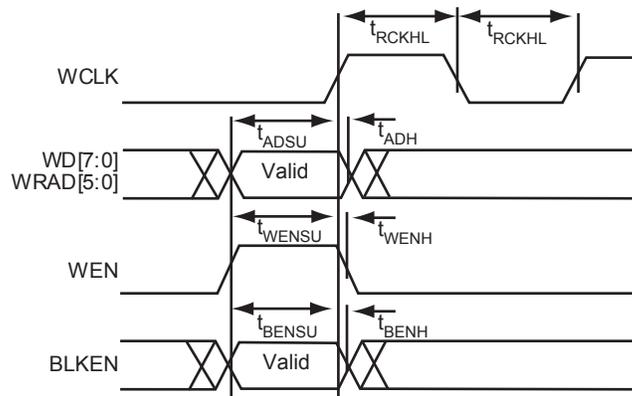
Note: Identical timing for falling edge clock.

Figure 1-29 • **42MX SRAM Write Operation**
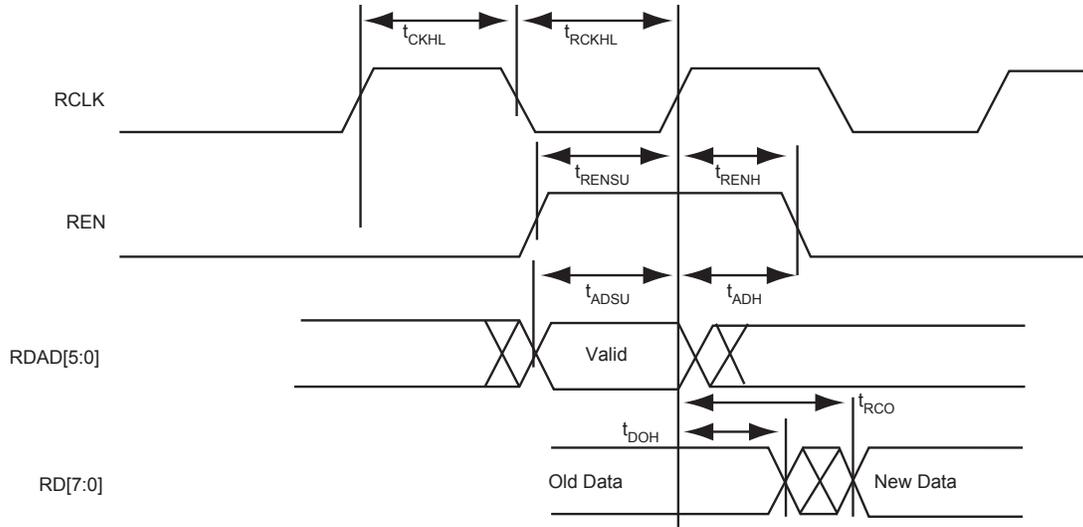
Note: Identical timing for falling edge clock.

*Figure 1-30 • **42MX SRAM Synchronous Read Operation***
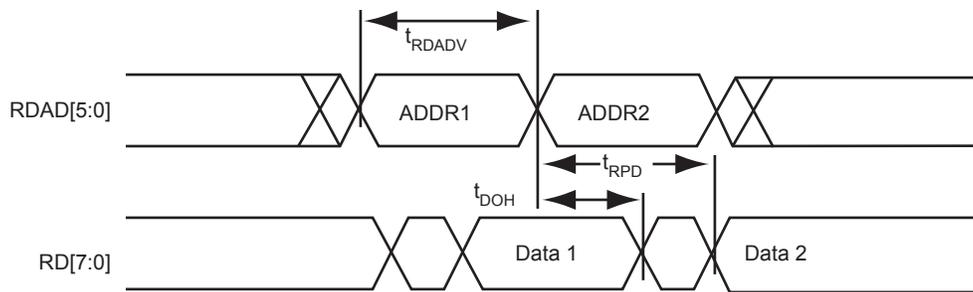
*Figure 1-31 • **42MX SRAM Asynchronous Read Operation—Type 1 (Read Address Controlled)***
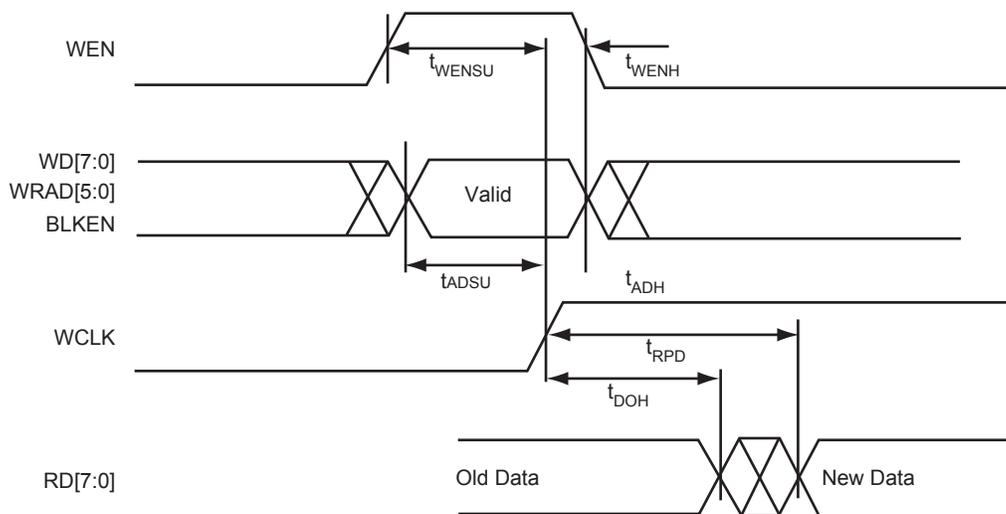
*Figure 1-32 • **42MX SRAM Asynchronous Read Operation—Type 2 (Write Address Controlled)***

Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The MX FPGAs deliver a tight fanout delay distribution, which is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Microsemi's patented antifuse offers a very low resistive/capacitive interconnect. The antifuses, fabricated in 0.45 μm lithography, offer nominal levels of 100 Ω resistance and 7.0 fF capacitance per antifuse.

MX fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90 percent of interconnects using only two antifuses.

Timing Characteristics

Device timing characteristics fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all MX devices. Internal routing delays are device-dependent; actual delays are not determined until after place-and-route of the user's design is complete. Delay values may then be determined by using the Designer software utility or by performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment in Microsemi's Designer software prior to placement and routing. Up to 6% of the nets in a design may be designated as critical.

Long Tracks

Some nets in the design use long tracks, which are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections, which increase capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks add approximately a 3 ns to a 6 ns delay, which is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section, shown in Table 1-28 on page 1-40.

Timing Derating

MX devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature and worst-case processing.

Temperature and Voltage Derating Factors

Table 1-22 • **42MX Temperature and Voltage Derating Factors**
(Normalized to T$_J$ = 25°C, VCCA = 5.0 V)

42MX Voltage	Temperature						
	−55°C	−40°C	0°C	25°C	70°C	85°C	125°C
4.50	0.93	0.95	1.05	1.09	1.25	1.29	1.41
4.75	0.88	0.90	1.00	1.03	1.18	1.22	1.34
5.00	0.85	0.87	0.96	1.00	1.15	1.18	1.29
5.25	0.84	0.86	0.95	0.97	1.12	1.14	1.28
5.50	0.83	0.85	0.94	0.96	1.10	1.13	1.26
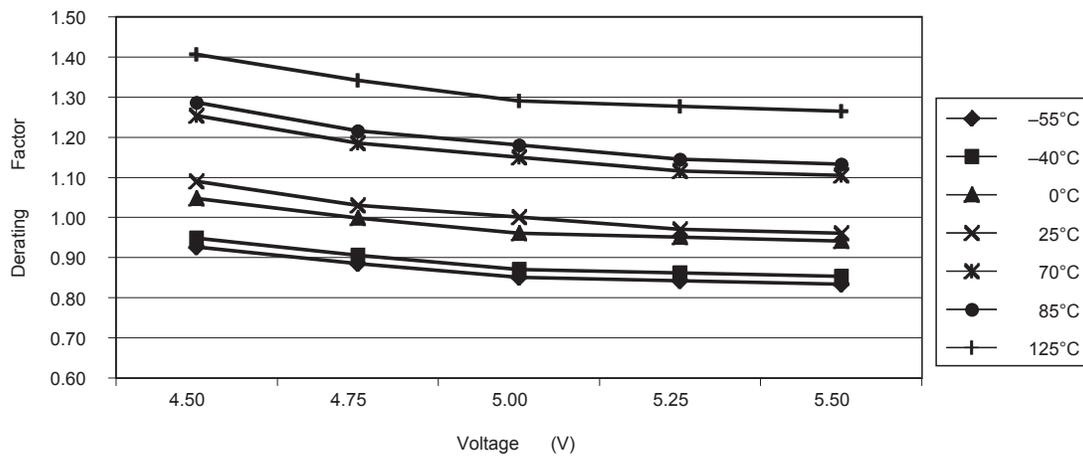
Note: This derating factor applies to all routing and propagation delays.

Figure 1-33 • **42MX Junction Temperature and Voltage Derating Curves**
(Normalized to T$_J$ = 25°C, VCCA = 5.0 V)

Table 1-23 • **40MX Temperature and Voltage Derating Factors**
(Normalized to T$_J$ = 25°C, VCC = 5.0 V)

40MX Voltage	Temperature						
	−55°C	−40°C	0°C	25°C	70°C	85°C	125°C
4.50	0.89	0.93	1.02	1.09	1.25	1.31	1.45
4.75	0.84	0.88	0.97	1.03	1.18	1.24	1.37
5.00	0.82	0.85	0.94	1.00	1.15	1.20	1.33
5.25	0.80	0.82	0.91	0.97	1.12	1.16	1.29
5.50	0.79	0.82	0.90	0.96	1.10	1.15	1.28
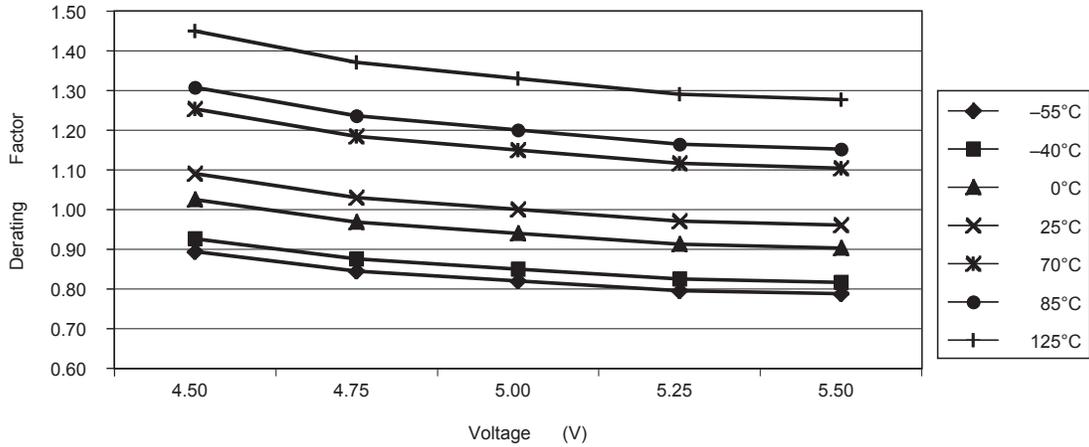
Note: This derating factor applies to all routing and propagation delays

Figure 1-34 • **40MX Junction Temperature and Voltage Derating Curves**
(Normalized to T$_J$ = 25°C, VCC = 5.0 V)

Table 1-24 • **42MX Temperature and Voltage Derating Factors**
(Normalized to T$_J$ = 25°C, VCCA = 3.3 V)

42MX Voltage	Temperature						
	−55°C	**−40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
3.00	0.97	1.00	1.10	1.15	1.32	1.36	1.45
3.30	0.84	0.87	0.96	1.00	1.15	1.18	1.26
3.60	0.81	0.84	0.92	0.96	1.10	1.13	1.21
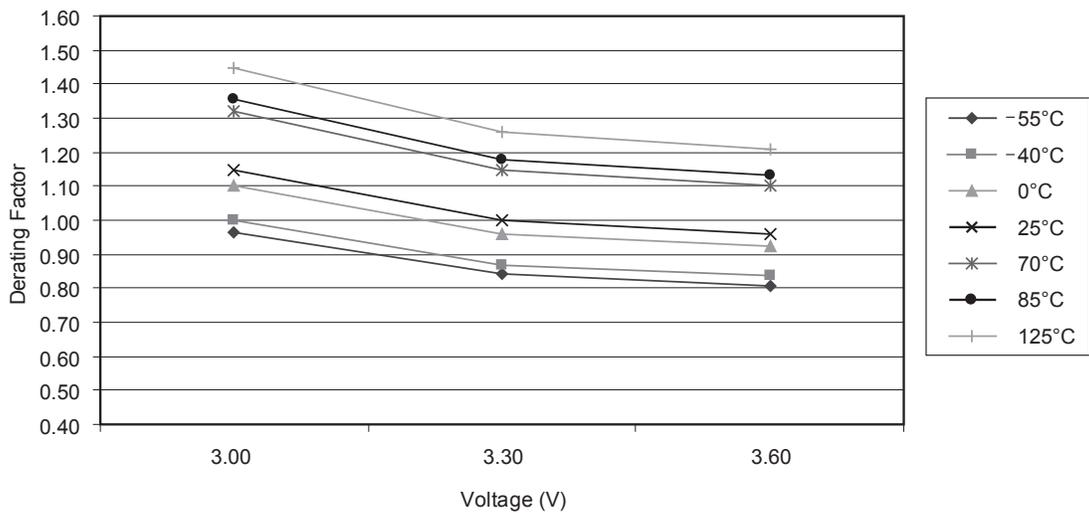
Note: This derating factor applies to all routing and propagation delays.

Figure 1-35 • **42MX Junction Temperature and Voltage Derating Curves**
(Normalized to T$_J$ = 25°C, VCCA = 3.3 V)

Table 1-25 • **40MX Temperature and Voltage Derating Factors**
(Normalized to T$_J$ = 25°C, VCC = 3.3 V)

40MX Voltage	Temperature						
	−55°C	**−40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
3.00	1.08	1.12	1.21	1.26	1.50	1.64	2.00
3.30	0.86	0.89	0.96	1.00	1.19	1.30	1.59
3.60	0.83	0.85	0.92	0.96	1.14	1.25	1.53
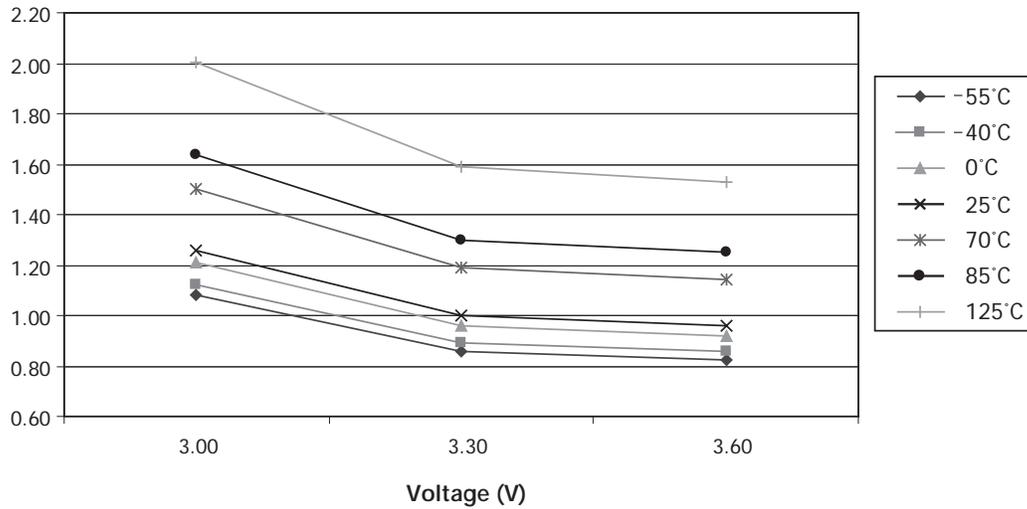
Note: *This derating factor applies to all routing and propagation delays.*

Figure 1-36 • **40MX Junction Temperature and Voltage Derating Curves**
(Normalized to T$_J$ = 25°C, VCC = 3.3 V)

PCI System Timing Specification

Table 1-26 and Table 1-27 list the critical PCI timing parameters and the corresponding timing parameters for the MX PCI-compliant devices.

PCI Models

Microsemi provides synthesizable VHDL and Verilog-HDL models for a PCI Target interface, a PCI Target and Target+DMA Master interface. Contact your Microsemi sales representative for more details.

Table 1-26 • **Clock Specification for 33 MHz PCI**

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	CLK Cycle Time	30	–	4.0	–	4.0	–	ns
t_{HIGH}	CLK High Time	11	–	1.9	–	1.9	–	ns
t_{LOW}	CLK Low Time	11	–	1.9	–	1.9	–	ns

Table 1-27 • **Timing Parameters for 33 MHz PCI**

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{VAL}	CLK to Signal Valid—Bused Signals	2	11	2.0	9.0	2.0	9.0	ns
$t_{VAL(PTP)}$	CLK to Signal Valid—Point-to-Point	2 [2]	12	2.0	9.0	2.0	9.0	ns
t_{ON}	Float to Active	2	–	2.0	4.0	2.0	4.0	ns
t_{OFF}	Active to Float	–	28	–	8.3[1]	–	8.3[1]	ns
t_{SU}	Input Set-Up Time to CLK—Bused Signals	7	–	1.5	–	1.5	–	ns
$t_{SU(PTP)}$	Input Set-Up Time to CLK—Point-to-Point	10, 12[2]	–	1.5	–	1.5	–	ns
t_H	Input Hold to CLK	0	–	0	–	0	–	ns

Notes:

1. T_{OFF} is system dependent. MX PCI devices have 7.4 ns turn-off time, reflection is typically an additional 10 ns.
2. REQ# and GNT# are point-to-point signals and have different output valid delay and input setup times than do bussed signals. GNT# has a setup of 10; REW# has a setup of 12.

Timing Characteristics

Table 1-28 • **A40MX02 Timing Characteristics (Nominal 5.0 V Operation)**
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t_{PD1}	Single Module		1.2		1.4		1.6		1.9		2.7	ns
t_{PD2}	Dual-Module Macros		2.7		3.1		3.5		4.1		5.7	ns
t_{CO}	Sequential Clock-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t_{GO}	Latch G-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.4		1.6		1.9		2.7	ns
Logic Module Predicted Routing Delays[1]												
t_{RD1}	FO = 1 Routing Delay		1.3		1.5		1.7		2.0		2.8	ns
t_{RD2}	FO = 2 Routing Delay		1.8		2.1		2.4		2.8		3.9	ns
t_{RD3}	FO = 3 Routing Delay		2.3		2.7		3.0		3.6		5.0	ns
t_{RD4}	FO = 4 Routing Delay		2.9		3.3		3.7		4.4		6.1	ns
t_{RD8}	FO = 8 Routing Delay		4.9		5.7		6.5		7.6		10.6	ns
Logic Module Sequential Timing[2]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t_A	Flip-Flop Clock Input Period	4.8		5.6		6.3		7.5		10.4		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		181		168		154		134		80	MHz
Input Module Propagation Delays												
t_{INYH}	Pad-to-Y HIGH		0.7		0.8		0.9		1.1		1.5	ns
t_{INYL}	Pad-to-Y LOW		0.6		0.7		0.8		1.0		1.3	ns

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

2. *Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.*

3. *The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.*

4. *Delays based on 35pF loading.*

Table 1-28 • **A40MX02 Timing Characteristics (Nominal 5.0 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO = 1 Routing Delay			2.1		2.4		2.2		3.2		4.5	ns
t_{IRD2}	FO = 2 Routing Delay			2.6		3.0		3.4		4.0		5.6	ns
t_{IRD3}	FO = 3 Routing Delay			3.1		3.6		4.1		4.8		6.7	ns
t_{IRD4}	FO = 4 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t_{IRD8}	FO = 8 Routing Delay			5.7		6.6		7.5		8.8		12.4	ns
Global Clock Network													
t_{CKH}	Input Low to HIGH	FO = 16 FO = 128		4.6 4.6		5.3 5.3		6.0 6.0		7.0 7.0		9.8 9.8	ns
t_{CKL}	Input High to LOW	FO = 16 FO = 128		4.8 4.8		5.6 5.6		6.3 6.3		7.4 7.4		10.4 10.4	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 16 FO = 128	2.2 2.4		2.6 2.7		2.9 3.1		3.4 3.6		4.8 5.1		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 16 FO = 128	2.2 2.4		2.6 2.7		2.9 3.01		3.4 3.6		4.8 5.1		ns
t_{CKSW}	Maximum Skew	FO = 16 FO = 128		0.4 0.5		0.5 0.6		0.5 0.7		0.6 0.8		0.8 1.2	ns
t_P	Minimum Period	FO = 16 FO = 128	4.7 4.8		5.4 5.6		6.1 6.3		7.2 7.5		10.0 10.4		ns
f_{MAX}	Maximum Frequency	FO = 16 FO = 128		188 181		175 168		160 154		139 134		83 80	MHz

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

2. *Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.*

3. *The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.*

4. *Delays based on 35pF loading.*

Table 1-28 • **A40MX02 Timing Characteristics (Nominal 5.0 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad HIGH		3.3		3.8		4.3		5.1		7.2	ns
t_{DHL}	Data-to-Pad LOW		4.0		4.6		5.2		6.1		8.6	ns
t_{ENZH}	Enable Pad Z to HIGH		3.7		4.3		4.9		5.8		8.0	ns
t_{ENZL}	Enable Pad Z to LOW		4.7		5.4		6.1		7.2		10.1	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.1	ns
t_{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.02		0.03		0.03		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF
CMOS Output Module Timing[4]												
t_{DLH}	Data-to-Pad HIGH		3.9		4.5		5.1		6.05		8.5	ns
t_{DHL}	Data-to-Pad LOW		3.4		3.9		4.4		5.2		7.3	ns
t_{ENZH}	Enable Pad Z to HIGH		3.4		3.9		4.4		5.2		7.3	ns
t_{ENZL}	Enable Pad Z to LOW		4.9		5.6		6.4		7.5		10.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.0	ns
t_{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d_{TLH}	Delta LOW to HIGH		0.03		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Delta HIGH to LOW		0.02		0.02		0.03		0.03		0.04	ns/pF

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
2. *Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.*
3. *The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.*
4. *Delays based on 35pF loading.*

Table 1-29 • **A40MX02 Timing Characteristics (Nominal 3.3 V Operation)**
(Worst-Case Commercial Conditions, VCC = 3.0 V, T$_J$ = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t$_{PD1}$	Single Module		1.7		2.0		2.3		2.7		3.7	ns
t$_{PD2}$	Dual-Module Macros		3.7		4.3		4.9		5.7		8.0	ns
t$_{CO}$	Sequential Clock-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t$_{GO}$	Latch G-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t$_{RS}$	Flip-Flop (Latch) Reset-to-Q		1.7		2.0		2.3		2.7		3.7	ns
Logic Module Predicted Routing Delays[1]												
t$_{RD1}$	FO = 1 Routing Delay		2.0		2.2		2.5		3.0		4.2	ns
t$_{RD2}$	FO = 2 Routing Delay		2.7		3.1		3.5		4.1		5.7	ns
t$_{RD3}$	FO = 3 Routing Delay		3.4		3.9		4.4		5.2		7.3	ns
t$_{RD4}$	FO = 4 Routing Delay		4.2		4.8		5.4		6.3		8.9	ns
t$_{RD8}$	FO = 8 Routing Delay		7.1		8.2		9.2		10.9		15.2	ns
Logic Module Sequential Timing[2]												
t$_{SUD}$	Flip-Flop (Latch) Data Input Set-Up	4.3		4.9		5.6		6.6		9.2		ns
t$_{HD}$[3]	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{SUENA}$	Flip-Flop (Latch) Enable Set-Up	4.3		4.9		5.6		6.6		9.2		ns
t$_{HENA}$	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{WCLKA}$	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.3		6.0		7.0		9.8		ns
t$_{WASYN}$	Flip-Flop (Latch) Asynchronous Pulse Width	4.6		5.3		6.0		7.0		9.8		ns
t$_A$	Flip-Flop Clock Input Period	6.8		7.8		8.9		10.4		14.6		ns
f$_{MAX}$	Flip-Flop (Latch) Clock Frequency (FO = 128)		109		101		92		80		48	MHz
Input Module Propagation Delays												
t$_{INYH}$	Pad-to-Y HIGH		1.0		1.1		1.3		1.5		2.1	ns
t$_{INYL}$	Pad-to-Y LOW		0.9		1.0		1.1		1.3		1.9	ns

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

2. *Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.*

3. *The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.*

4. *Delays based on 35 pF loading.*

Table 1-29 • **A40MX02 Timing Characteristics (Nominal 3.3 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCC = 3.0 V, T$_J$ = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays1												
t$_{IRD1}$	FO = 1 Routing Delay		2.9		3.4		3.8		4.5		6.3	ns
t$_{IRD2}$	FO = 2 Routing Delay		3.6		4.2		4.8		5.6		7.8	ns
t$_{IRD3}$	FO = 3 Routing Delay		4.4		5.0		5.7		6.7		9.4	ns
t$_{IRD4}$	FO = 4 Routing Delay		5.1		5.9		6.7		7.8		11.0	ns
t$_{IRD8}$	FO = 8 Routing Delay		8.0		9.26		10.5		12.6		17.3	ns
Global Clock Network												
t$_{CKH}$	Input LOW to HIGH FO = 16 FO = 128		6.4 6.4		7.4 7.4		8.3 8.3		9.8 9.8		13.7 13.7	ns
t$_{CKL}$	Input HIGH to LOW FO = 16 FO = 128		6.7 6.7		7.8 7.8		8.8 8.8		10.4 10.4		14.5 14.5	ns
t$_{PWH}$	Minimum Pulse FO = 16 Width HIGH FO = 128	3.1 3.3		3.6 3.8		4.1 4.3		4.8 5.1		6.7 7.1		ns
t$_{PWL}$	Minimum Pulse FO = 16 Width LOW FO = 128	3.1 3.3		3.6 3.8		4.1 4.3		4.8 5.1		6.7 7.1		ns
t$_{CKSW}$	Maximum Skew FO = 16 FO = 128		0.6 0.8		0.6 0.9		0.7 1.0		0.8 1.2		1.2 1.6	ns
t$_P$	Minimum Period FO = 16 FO = 128	6.5 6.8		7.5 7.8		8.5 8.9		10.1 10.4		14.1 14.6		ns
f$_{MAX}$	Maximum FO = 16 Frequency FO = 128		113 109		105 101		96 92		83 80		50 48	MHz
TTL Output Module Timing[4]												
t$_{DLH}$	Data-to-Pad HIGH		4.7		5.4		6.1		7.2		10.0	ns
t$_{DHL}$	Data-to-Pad LOW		5.6		6.4		7.3		8.6		12.0	ns
t$_{ENZH}$	Enable Pad Z to HIGH		5.2		6.0		6.8		8.1		11.3	ns
t$_{ENZL}$	Enable Pad Z to LOW		6.6		7.6		8.6		10.1		14.1	ns
t$_{ENHZ}$	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9	ns
t$_{ENLZ}$	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7	ns
d$_{TLH}$	Delta LOW to HIGH		0.03		0.03		0.04		0.04		0.06	ns/pF
d$_{THL}$	Delta HIGH to LOW		0.04		0.04		0.05		0.06		0.08	ns/pF

Notes:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.

3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.

4. Delays based on 35 pF loading.

Table 1-29 • **A40MX02 Timing Characteristics (Nominal 3.3 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCC = 3.0 V, T$_J$ = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[4]												
t$_{DLH}$	Data-to-Pad HIGH		5.5		6.4		7.2		8.5		11.9	ns
t$_{DHL}$	Data-to-Pad LOW		4.8		5.5		6.2		7.3		10.2	ns
t$_{ENZH}$	Enable Pad Z to HIGH		4.7		5.5		6.2		7.3		10.2	ns
t$_{ENZL}$	Enable Pad Z to LOW		6.8		7.9		8.9		10.5		14.7	ns
t$_{ENHZ}$	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9	ns
t$_{ENLZ}$	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7	ns
d$_{TLH}$	Delta LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d$_{THL}$	Delta HIGH to LOW		0.03		0.03		0.04		0.04		0.06	ns/pF

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

2. *Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.*

3. *The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.*

4. *Delays based on 35 pF loading.*

Table 1-30 • **A40MX04 Timing Characteristics (Nominal 5.0 V Operation)**
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t_{PD1}	Single Module		1.2		1.4		1.6		1.9		2.7	ns
t_{PD2}	Dual-Module Macros		2.3		3.1		3.5		4.1		5.7	ns
t_{CO}	Sequential Clock-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t_{GO}	Latch G-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.4		1.6		1.9		2.7	ns
Logic Module Predicted Routing Delays[1]												
t_{RD1}	FO = 1 Routing Delay		1.2		1.6		1.8		2.1		3.0	ns
t_{RD2}	FO = 2 Routing Delay		1.9		2.2		2.5		2.9		4.1	ns
t_{RD3}	FO = 3 Routing Delay		2.4		2.8		3.2		3.7		5.2	ns
t_{RD4}	FO = 4 Routing Delay		2.9		3.4		3.9		4.5		6.3	ns
t_{RD8}	FO = 8 Routing Delay		5.0		5.8		6.6		7.8		10.9	ns
Logic Module Sequential Timing[2]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	3.1		3.5		4.0		4.7		6.6		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.3		3.8		4.3		5.0		7.0		ns
t_A	Flip-Flop Clock Input Period	4.8		5.6		6.3		7.5		10.4		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		181		167		154		134		80	MHz
Input Module Propagation Delays												
t_{INYH}	Pad-to-Y HIGH		0.7		0.8		0.9		1.1		1.5	ns
t_{INYL}	Pad-to-Y LOW		0.6		0.7		0.8		1.0		1.3	ns

Notes:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.

3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer utility from the Designer software to check the hold time for this macro.

4. Delays based on 35 pF loading.

Table 1-30 • **A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays1													
t$_{IRD1}$	FO = 1 Routing Delay			2.1		2.4		2.2		3.2		4.5	ns
t$_{IRD2}$	FO = 2 Routing Delay			2.6		3.0		3.4		4.0		5.6	ns
t$_{IRD3}$	FO = 3 Routing Delay			3.1		3.6		4.1		4.8		6.7	ns
t$_{IRD4}$	FO = 4 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t$_{IRD8}$	FO = 8 Routing Delay			5.7		6.6		7.5		8.8		12.4	ns
Global Clock Network													
t$_{CKH}$	Input Low to HIGH	FO = 16		4.6		5.3		6.0		7.0		9.8	ns
		FO = 128		4.6		5.3		6.0		7.0		9.8	
t$_{CKL}$	Input High to LOW	FO = 16		4.8		5.6		6.3		7.4		10.4	ns
		FO = 128		4.8		5.6		6.3		7.4		10.4	
t$_{PWH}$	Minimum Pulse Width HIGH	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.1		3.6		5.1		
t$_{PWL}$	Minimum Pulse Width LOW	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.01		3.6		5.1		
t$_{CKSW}$	Maximum Skew	FO = 16		0.4		0.5		0.5		0.6		0.8	ns
		FO = 128		0.5		0.6		0.7		0.8		1.2	
t$_P$	Minimum Period	FO = 16	4.7		5.4		6.1		7.2		10.0		ns
		FO = 128	4.8		5.6		6.3		7.5		10.4		
f$_{MAX}$	Maximum Frequency	FO = 16		188		175		160		139		83	MHz
		FO = 128		181		168		154		134		80	
TTL Output Module Timing[4]													
t$_{DLH}$	Data-to-Pad HIGH			3.3		3.8		4.3		5.1		7.2	ns
t$_{DHL}$	Data-to-Pad LOW			4.0		4.6		5.2		6.1		8.6	ns
t$_{ENZH}$	Enable Pad Z to HIGH			3.7		4.3		4.9		5.8		8.0	ns
t$_{ENZL}$	Enable Pad Z to LOW			4.7		5.4		6.1		7.2		10.1	ns
t$_{ENHZ}$	Enable Pad HIGH to Z			7.9		9.1		10.4		12.2		17.1	ns
t$_{ENLZ}$	Enable Pad LOW to Z			5.9		6.8		7.7		9.0		12.6	ns
d$_{TLH}$	Delta LOW to HIGH			0.02		0.02		0.03		0.03		0.04	ns/pF
d$_{THL}$	Delta HIGH to LOW			0.03		0.03		0.03		0.04		0.06	ns/pF

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

2. *Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.*

3. *The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer utility from the Designer software to check the hold time for this macro.*

4. *Delays based on 35 pF loading.*

Table 1-30 • **A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[1]												
t_{DLH}	Data-to-Pad HIGH		3.9		4.5		5.1		6.05		8.5	ns
t_{DHL}	Data-to-Pad LOW		3.4		3.9		4.4		5.2		7.3	ns
t_{ENZH}	Enable Pad Z to HIGH		3.4		3.9		4.4		5.2		7.3	ns
t_{ENZL}	Enable Pad Z to LOW		4.9		5.6		6.4		7.5		10.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.0	ns
t_{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d_{TLH}	Delta LOW to HIGH		0.03		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Delta HIGH to LOW		0.02		0.02		0.03		0.03		0.04	ns/pF

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

2. *Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.*

3. *The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer utility from the Designer software to check the hold time for this macro.*

4. *Delays based on 35 pF loading.*

Table 1-31 • **A40MX04 Timing Characteristics (Nominal 3.3 V Operation)**
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t_{PD1}	Single Module		1.7		2.0		2.3		2.7		3.7	ns
t_{PD2}	Dual-Module Macros		3.7		4.3		4.9		5.7		8.0	ns
t_{CO}	Sequential Clock-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t_{GO}	Latch G-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.7		2.0		2.3		2.7		3.7	ns
Logic Module Predicted Routing Delays[1]												
t_{RD1}	FO = 1 Routing Delay		1.9		2.2		2.5		3.0		4.2	ns
t_{RD2}	FO = 2 Routing Delay		2.7		3.1		3.5		4.1		5.7	ns
t_{RD3}	FO = 3 Routing Delay		3.4		3.9		4.4		5.2		7.3	ns
t_{RD4}	FO = 4 Routing Delay		4.1		4.8		5.4		6.3		8.9	ns
t_{RD8}	FO = 8 Routing Delay		7.1		8.1		9.2		10.9		15.2	ns
Logic Module Sequential Timing[2]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	4.3		5.0		5.6		6.6		9.2		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	4.3		5.0		5.6		6.6		9.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.3		5.6		7.0		9.8		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.6		5.3		5.6		7.0		9.8		ns
t_A	Flip-Flop Clock Input Period	6.8		7.8		8.9		10.4		14.6		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		109		101		92		80		48	MHz
Input Module Propagation Delays												
t_{INYH}	Pad-to-Y HIGH		1.0		1.1		1.3		1.5		2.1	ns
t_{INYL}	Pad-to-Y LOW		0.9		1.0		1.1		1.3		1.9	ns

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

2. *Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.*

3. *The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.*

4. *Delays based on 35 pF loading.*

Table 1-31 • **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (continued)**
   (Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description			−3 Speed		−2 Speed		−1 Speed		Std Speed		−F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO = 1 Routing Delay			2.9		3.3		3.8		4.5		6.3	ns
t_{IRD2}	FO = 2 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t_{IRD3}	FO = 3 Routing Delay			4.4		5.0		5.7		6.7		9.4	ns
t_{IRD4}	FO = 4 Routing Delay			5.1		5.9		6.7		7.8		11.0	ns
t_{IRD8}	FO = 8 Routing Delay			8.0		9.3		10.5		12.4		17.2	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 16		6.4		7.4		8.4		9.9		13.8	ns
		FO = 128		6.4		7.4		8.4		9.9		13.8	
t_{CKL}	Input HIGH to LOW	FO = 16		6.8		7.8		8.9		10.4		14.6	ns
		FO = 128		6.8		7.8		8.9		10.4		14.6	
t_{PWH}	Minimum Pulse Width HIGH	FO = 16	3.1		3.6		4.1		4.8		6.7		ns
		FO = 128	3.3		3.8		4.3		5.1		7.1		
t_{PWL}	Minimum Pulse Width LOW	FO = 16	3.1		3.6		4.1		4.8		6.7		ns
		FO = 128	3.3		3.8		4.3		5.1		7.1		
t_{CKSW}	Maximum Skew	FO = 16		0.6		0.6		0.7		0.8		1.2	ns
		FO = 128		0.8		0.9		1.0		1.2		1.6	
t_P	Minimum Period	FO = 16	6.5		7.5		8.5		10.1		14.1		ns
		FO = 128	6.8		7.8		8.9		10.4		14.6		
f_{MAX}	Maximum Frequency	FO = 16		113		105		96		83		50	MHz
		FO = 128		109		101		92		80		48	
TTL Output Module Timing[4]													
t_{DLH}	Data-to-Pad HIGH			4.7		5.4		6.1		7.2		10.0	ns
t_{DHL}	Data-to-Pad LOW			5.6		6.4		7.3		8.6		12.0	ns
t_{ENZH}	Enable Pad Z to HIGH			5.2		6.0		6.9		8.1		11.3	ns
t_{ENZL}	Enable Pad Z to LOW			6.6		7.6		8.6		10.1		14.1	ns
t_{ENHZ}	Enable Pad HIGH to Z			11.1		12.8		14.5		17.1		23.9	ns
t_{ENLZ}	Enable Pad LOW to Z			8.2		9.5		10.7		12.6		17.7	ns
d_{TLH}	Delta LOW to HIGH			0.03		0.03		0.04		0.04		0.06	ns/pF
d_{THL}	Delta HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF

Notes:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.

3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.

4. Delays based on 35 pF loading.

Table 1-31 • **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCC = 3.0 V, T$_J$ = 70°C)

Parameter / Description		−3 Speed		−2 Speed		−1 Speed		Std Speed		−F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[4]												
t$_{DLH}$	Data-to-Pad HIGH		5.5		6.4		7.2		8.5		11.9	ns
t$_{DHL}$	Data-to-Pad LOW		4.8		5.5		6.2		7.3		10.2	ns
t$_{ENZH}$	Enable Pad Z to HIGH		4.7		5.5		6.2		7.3		10.2	ns
t$_{ENZL}$	Enable Pad Z to LOW		6.8		7.9		8.9		10.5		14.7	ns
t$_{ENHZ}$	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9	ns
t$_{ENLZ}$	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7	ns
d$_{TLH}$	Delta LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d$_{THL}$	Delta HIGH to LOW		0.03		0.03		0.04		0.04		0.06	ns/pF

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

2. *Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.*

3. *The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.*

4. *Delays based on 35 pF loading.*

Table 1-32 • **A42MX09 Timing Characteristics (Nominal 5.0 V Operation)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		−3 Speed		−2 Speed		−1 Speed		Std Speed		−F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays[1]												
t_{PD1}	Single Module		1.2		1.3		1.5		1.8		2.5	ns
t_{CO}	Sequential Clock-to-Q		1.3		1.4		1.6		1.9		2.7	ns
t_{GO}	Latch G-to-Q		1.2		1.4		1.6		1.8		2.6	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.6		1.8		2.1		2.9	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.7		0.8		0.9		1.0		1.4	ns
t_{RD2}	FO = 2 Routing Delay		0.9		1.0		1.2		1.4		1.9	ns
t_{RD3}	FO = 3 Routing Delay		1.2		1.3		1.5		1.7		2.4	ns
t_{RD4}	FO = 4 Routing Delay		1.4		1.5		1.7		2.0		2.9	ns
t_{RD8}	FO = 8 Routing Delay		2.3		2.6		2.9		3.4		4.8	ns
Logic Module Sequential Timing[3, 4]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.3		0.4		0.4		0.5		0.7		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.4		0.5		0.5		0.6		0.8		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.4		3.8		4.3		5.0		7.0		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.5		4.9		5.6		6.6		9.2		ns
t_A	Flip-Flop Clock Input Period	3.5		3.8		4.3		5.1		7.1		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Set-Up	0.3		0.3		0.4		0.4		0.6		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.3		0.3		0.4		0.4		0.6		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		268		244		224		195		117	MHz

Notes:

1. *For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-32 • **A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		−3 Speed		−2 Speed		−1 Speed		Std Speed		−F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays												
t_{INYH}	Pad-to-Y HIGH		1.0		1.2		1.3		1.6		2.2	ns
t_{INYL}	Pad-to-Y LOW		0.8		0.9		1.0		1.2		1.7	ns
t_{INGH}	G to Y HIGH		1.3		1.4		1.6		1.9		2.7	ns
t_{INGL}	G to Y LOW		1.3		1.4		1.6		1.9		2.7	ns
Input Module Predicted Routing Delays[2]												
t_{IRD1}	FO = 1 Routing Delay		2.0		2.2		2.5		3.0		4.2	ns
t_{IRD2}	FO = 2 Routing Delay		2.3		2.5		2.9		3.4		4.7	ns
t_{IRD3}	FO = 3 Routing Delay		2.5		2.8		3.2		3.7		5.2	ns
t_{IRD4}	FO = 4 Routing Delay		2.8		3.1		3.5		4.1		5.7	ns
t_{IRD8}	FO = 8 Routing Delay		3.7		4.1		4.7		5.5		7.7	ns
Global Clock Network												
t_{CKH}	Input LOW to HIGH	FO = 32	2.4		2.7		3.0		3.6		5.0	ns
		FO = 256	2.7		3.0		3.4		4.0		5.5	ns
t_{CKL}	Input HIGH to LOW	FO = 32	3.5		3.9		4.4		5.2		7.3	ns
		FO = 256	3.9		4.3		4.9		5.7		8.0	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	1.2		1.4		1.5		1.8		2.5		ns
		FO = 256	1.3		1.5		1.7		2.0		2.7		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	1.2		1.4		1.5		1.8		2.5		ns
		FO = 256	1.3		1.5		1.7		2.0		2.7		ns
t_{CKSW}	Maximum Skew	FO = 32		0.3		0.3		0.4		0.5		0.6	ns
		FO = 256		0.3		0.3		0.4		0.5		0.6	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32	2.3		2.6		3.0		3.5		4.9		ns
		FO = 256	2.2		2.4		3.3		3.9		5.5		ns
t_P	Minimum Period	FO = 32	3.4		3.7		4.0		4.7		7.8		ns
		FO = 256	3.7		4.1		4.5		5.2		8.6		ns
f_{MAX}	Maximum Frequency	FO = 32		296		269		247		215		129	MHz
		FO = 256		268		244		224		195		117	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-32 • **A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T$_J$ = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing[5]												
t$_{DLH}$	Data-to-Pad HIGH		2.5		2.7		3.1		3.6		5.1	ns
t$_{DHL}$	Data-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t$_{ENZH}$	Enable Pad Z to HIGH		2.6		2.9		3.3		3.9		5.5	ns
t$_{ENZL}$	Enable Pad Z to LOW		2.9		3.2		3.7		4.3		6.1	ns
t$_{ENHZ}$	Enable Pad HIGH to Z		4.9		5.4		6.2		7.3		10.2	ns
t$_{ENLZ}$	Enable Pad LOW to Z		5.3		5.9		6.7		7.9		11.1	ns
t$_{GLH}$	G-to-Pad HIGH		2.6		2.9		3.3		3.8		5.3	ns
t$_{GHL}$	G-to-Pad LOW		2.6		2.9		3.3		3.8		5.3	ns
t$_{LSU}$	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t$_{LH}$	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{LCO}$	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.2		5.8		6.6		7.7		10.8	ns
t$_{ACO}$	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		7.4		8.2		9.3		10.9		15.3	ns
d$_{TLH}$	Capacity Loading, LOW to HIGH		0.03		0.03		0.03		0.04		0.06	ns/pF
d$_{THL}$	Capacity Loading, HIGH to LOW		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. *For dual-module macros, use t$_{PD1}$ + t$_{RD1}$ + t$_{PDn}$, t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-32 • **A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		2.4		2.7		3.1		3.6		5.1	ns
t_{DHL}	Data-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t_{ENZH}	Enable Pad Z to HIGH		2.7		2.9		3.3		3.9		5.5	ns
t_{ENZL}	Enable Pad Z to LOW		2.9		3.2		3.7		4.3		6.1	ns
t_{ENHZ}	Enable Pad HIGH to Z		4.9		5.4		6.2		7.3		10.2	ns
t_{ENLZ}	Enable Pad LOW to Z		5.3		5.9		6.7		7.9		11.1	ns
t_{GLH}	G-to-Pad HIGH		4.2		4.6		5.2		6.1		8.6	ns
t_{GHL}	G-to-Pad LOW		4.2		4.6		5.2		6.1		8.6	ns
t_{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.2		5.8		6.6		7.7		10.8	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		7.4		8.2		9.3		10.9		15.3	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.03		0.03		0.03		0.04		0.06	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. *For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-33 • **A42MX09 Timing Characteristics (Nominal 3.3 V Operation)**
(Worst-Case Commercial Conditions, VCCA = 3.0 V, T$_J$ = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays[1]												
t$_{PD1}$	Single Module		1.6		1.8		2.1		2.5		3.5	ns
t$_{CO}$	Sequential Clock-to-Q		1.8		2.0		2.3		2.7		3.8	ns
t$_{GO}$	Latch G-to-Q		1.7		1.9		2.1		2.5		3.5	ns
t$_{RS}$	Flip-Flop (Latch) Reset-to-Q		2.0		2.2		2.5		2.9		4.1	ns
Logic Module Predicted Routing Delays[2]												
t$_{RD1}$	FO = 1 Routing Delay		1.0		1.1		1.2		1.4		2.0	ns
t$_{RD2}$	FO = 2 Routing Delay		1.3		1.4		1.6		1.9		2.7	ns
t$_{RD3}$	FO = 3 Routing Delay		1.6		1.8		2.0		2.4		3.3	ns
t$_{RD4}$	FO = 4 Routing Delay		1.9		2.1		2.4		2.9		4.0	ns
t$_{RD8}$	FO = 8 Routing Delay		3.2		3.6		4.1		4.8		6.7	ns
Logic Module Sequential Timing [3, 4]												
t$_{SUD}$	Flip-Flop (Latch) Data Input Set-Up	0.5		0.5		0.6		0.7		0.9		ns
t$_{HD}$	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{SUENA}$	Flip-Flop (Latch) Enable Set-Up	0.6		0.6		0.7		0.8		1.2		ns
t$_{HENA}$	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{WCLKA}$	Flip-Flop (Latch) Clock Active Pulse Width	4.7		5.3		6.0		7.0		9.8		ns
t$_{WASYN}$	Flip-Flop (Latch) Asynchronous Pulse Width	6.2		6.9		7.8		9.2		12.9		ns
t$_A$	Flip-Flop Clock Input Period	5.0		5.6		6.2		7.1		9.9		ns
t$_{INH}$	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{INSU}$	Input Buffer Latch Set-Up	0.3		0.3		0.3		0.4		0.6		ns
t$_{OUTH}$	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{OUTSU}$	Output Buffer Latch Set-Up	0.3		0.3		0.3		0.4		0.6		ns
f$_{MAX}$	Flip-Flop (Latch) Clock Frequency		161		146		135		117		70	MHz

Notes:

1. *For dual-module macros, use t$_{PD1}$ + t$_{RD1}$ + t$_{PDn}$, t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-33 • **A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y HIGH			1.5		1.6		1.8		2.17		3.0	ns
t_{INYL}	Pad-to-Y LOW			1.2		1.3		1.4		1.7		2.4	ns
t_{INGH}	G to Y HIGH			1.8		2.0		2.3		2.7		3.7	ns
t_{INGL}	G to Y LOW			1.8		2.0		2.3		2.7		3.7	ns
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			2.8		3.2		3.6		4.2		5.9	ns
t_{IRD2}	FO = 2 Routing Delay			3.2		3.5		4.0		4.7		6.6	ns
t_{IRD3}	FO = 3 Routing Delay			3.5		3.9		4.4		5.2		7.3	ns
t_{IRD4}	FO = 4 Routing Delay			3.9		4.3		4.9		5.7		8.0	ns
t_{IRD8}	FO = 8 Routing Delay			5.2		5.8		6.6		7.7		10.8	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		4.1		4.5		5.1		6.0		8.4	ns
		FO = 256		4.5		5.0		5.6		6.7		9.3	ns
t_{CKL}	Input HIGH to LOW	FO = 32		5.0		5.5		6.2		7.3		10.2	ns
		FO = 256		5.4		6.0		6.8		8.0		11.2	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	1.7		1.9		2.1		2.5		3.5		ns
		FO = 256	1.9		2.1		2.3		2.7		3.8		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	1.7		1.9		2.1		2.5		3.5		ns
		FO = 256	1.9		2.1		2.3		2.7		3.8		ns
t_{CKSW}	Maximum Skew	FO = 32		0.4		0.5		0.5		0.6		0.9	ns
		FO = 256		0.4		0.5		0.5		0.6		0.9	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32	3.3		3.7		4.2		4.9		6.9		ns
		FO = 256	3.7		4.1		4.6		5.5		7.6		ns
t_P	Minimum Period	FO = 32	5.6		6.2		6.7		7.8		12.9		ns
		FO = 256	6.1		6.8		7.4		8.5		14.2		ns
f_{MAX}	Maximum Frequency	FO = 32		177		161		148		129		77	MHz
		FO = 256		161		146		135		117		70	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-33 • **A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
TTL Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		3.4		3.8		4.3		5.1		7.1	ns
t_{DHL}	Data-to-Pad LOW		4.0		4.5		5.1		6.1		8.3	ns
t_{ENZH}	Enable Pad Z to HIGH		3.7		4.1		4.6		5.5		7.6	ns
t_{ENZL}	Enable Pad Z to LOW		4.1		4.5		5.1		6.1		8.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		6.9		7.6		8.6		10.2		14.2	ns
t_{ENLZ}	Enable Pad LOW to Z		7.5		8.3		9.4		11.1		15.5	ns
t_{GLH}	G-to-Pad HIGH		5.8		6.5		7.3		8.6		12.0	ns
t_{GHL}	G-to-Pad LOW		5.8		6.5		7.3		8.6		12.0	ns
t_{LSU}	I/O Latch Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.7		9.7		10.9		12.9		18.0	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad),64 Clock Loading		12.2		13.5		15.4		18.1		25.3	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.00		0.00		0.00		0.10		0.01	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.09		0.10		0.10		0.10		0.10	ns/pF

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. *Delays based on 35 pF loading.*

Table 1-33 • **A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 3.0 V, T$_J$ = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[5]												
t$_{DLH}$	Data-to-Pad HIGH		3.4		3.8		5.5		6.4		9.0	ns
t$_{DHL}$	Data-to-Pad LOW		4.1		4.5		4.2		5.0		7.0	ns
t$_{ENZH}$	Enable Pad Z to HIGH		3.7		4.1		4.6		5.5		7.6	ns
t$_{ENZL}$	Enable Pad Z to LOW		4.1		4.5		5.1		6.1		8.5	ns
t$_{ENHZ}$	Enable Pad HIGH to Z		6.9		7.6		8.6		10.2		14.2	ns
t$_{ENLZ}$	Enable Pad LOW to Z		7.5		8.3		9.4		11.1		15.5	ns
t$_{GLH}$	G-to-Pad HIGH		5.8		6.5		7.3		8.6		12.0	ns
t$_{GHL}$	G-to-Pad LOW		5.8		6.5		7.3		8.6		12.0	ns
t$_{LSU}$	I/O Latch Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t$_{LH}$	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{LCO}$	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.7		9.7		10.9		12.9		18.0	ns
t$_{ACO}$	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.2		13.5		15.4		18.1		25.3	ns
d$_{TLH}$	Capacity Loading, LOW to HIGH		0.04		0.04		0.05		0.06		0.08	ns/pF
d$_{THL}$	Capacity Loading, HIGH to LOW		0.05		0.05		0.06		0.07		0.10	ns/pF

Notes:

1. *For dual-module macros, use t$_{PD1}$ + t$_{RD1}$ + t$_{PDn}$, t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-34 • **A42MX16 Timing Characteristics (Nominal 5.0 V Operation)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T$_J$ = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays[1]												
t$_{PD1}$	Single Module		1.4		1.5		1.7		2.0		2.8	ns
t$_{CO}$	Sequential Clock-to-Q		1.4		1.6		1.8		2.1		3.0	ns
t$_{GO}$	Latch G-to-Q		1.4		1.5		1.7		2.0		2.8	ns
t$_{RS}$	Flip-Flop (Latch) Reset-to-Q		1.6		1.7		2.0		2.3		3.3	ns
Logic Module Predicted Routing Delays[2]												
t$_{RD1}$	FO = 1 Routing Delay		0.8		0.9		1.0		1.2		1.6	ns
t$_{RD2}$	FO = 2 Routing Delay		1.0		1.2		1.3		1.5		2.1	ns
t$_{RD3}$	FO = 3 Routing Delay		1.3		1.4		1.6		1.9		2.7	ns
t$_{RD4}$	FO = 4 Routing Delay		1.6		1.7		2.0		2.3		3.2	ns
t$_{RD8}$	FO = 8 Routing Delay		2.6		2.9		3.2		3.8		5.3	ns
Logic Module Sequential Timing[3,4]												
t$_{SUD}$	Flip-Flop (Latch) Data Input Set-Up	0.3		0.4		0.4		0.5		0.7		ns
t$_{HD}$	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{SUENA}$	Flip-Flop (Latch) Enable Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t$_{HENA}$	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{WCLKA}$	Flip-Flop (Latch) Clock Active Pulse Width	3.4		3.8		4.3		5.0		7.1		ns
t$_{WASYN}$	Flip-Flop (Latch) Asynchronous Pulse Width	4.5		5.0		5.6		6.6		9.2		ns
t$_A$	Flip-Flop Clock Input Period	6.8		7.6		8.6		10.1		14.1		ns
t$_{INH}$	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{INSU}$	Input Buffer Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t$_{OUTH}$	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{OUTSU}$	Output Buffer Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
f$_{MAX}$	Flip-Flop (Latch) Clock Frequency		215		195		179		156		94	MHz

Notes:

1. *For dual-module macros, use t$_{PD1}$ + t$_{RD1}$ + t$_{PDn}$, t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, point and position whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-34 • **A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			−3 Speed		−2 Speed		−1 Speed		Std Speed		−F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y HIGH			1.1		1.2		1.3		1.6		2.2	ns
t_{INYL}	Pad-to-Y LOW			0.8		0.9		1.0		1.2		1.7	ns
t_{INGH}	G to Y HIGH			1.4		1.6		1.8		2.1		2.9	ns
t_{INGL}	G to Y LOW			1.4		1.6		1.8		2.1		2.9	ns
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			1.8		2.0		2.3		2.7		4.0	ns
t_{IRD2}	FO = 2 Routing Delay			2.1		2.3		2.6		3.1		4.3	ns
t_{IRD3}	FO = 3 Routing Delay			2.3		2.6		3.0		3.5		4.9	ns
t_{IRD4}	FO = 4 Routing Delay			2.6		3.0		3.3		3.9		5.4	ns
t_{IRD8}	FO = 8 Routing Delay			3.6		4.0		4.6		5.4		7.5	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		2.6		2.9		3.3		3.9		5.4	ns
		FO = 384		2.9		3.2		3.6		4.3		6.0	ns
t_{CKL}	Input HIGH to LOW	FO = 32		3.8		4.2		4.8		5.6		7.8	ns
		FO = 384		4.5		5.0		5.6		6.6		9.2	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	3.2		3.5		4.0		4.7		6.6		ns
		FO = 384	3.7		4.1		4.6		5.4		7.6		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	3.2		3.5		4.0		4.7		6.6		ns
		FO = 384	3.7		4.1		4.6		5.4		7.6		ns
t_{CKSW}	Maximum Skew	FO = 32		0.3		0.4		0.4		0.5		0.7	ns
		FO = 384		0.3		0.4		0.4		0.5		0.7	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 384	0.0		0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32	2.8		3.1		5.5		4.1		5.7		ns
		FO = 384	3.2		3.5		4.0		4.7		6.6		ns
t_P	Minimum Period	FO = 32	4.2		4.67		5.1		5.8		9.7		ns
		FO = 384	4.6		5.1		5.6		6.4		10.7		ns
f_{MAX}	Maximum Frequency	FO = 32		237		215		198		172		103	MHz
		FO = 384		215		195		179		156		94	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, point and position whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-34 • **A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T$_J$ = 70°C)

Parameter / Description		−3 Speed		−2 Speed		−1 Speed		Std Speed		−F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing[5]												
t$_{DLH}$	Data-to-Pad HIGH		2.5		2.8		3.2		3.7		5.2	ns
t$_{DHL}$	Data-to-Pad LOW		3.0		3.3		3.7		4.4		6.1	ns
t$_{ENZH}$	Enable Pad Z to HIGH		2.7		3.0		3.4		4.0		5.6	ns
t$_{ENZL}$	Enable Pad Z to LOW		3.0		3.3		3.8		4.4		6.2	ns
t$_{ENHZ}$	Enable Pad HIGH to Z		5.4		6.0		6.8		8.0		11.2	ns
t$_{ENLZ}$	Enable Pad LOW to Z		5.0		5.6		6.3		7.4		10.4	ns
t$_{GLH}$	G-to-Pad HIGH		2.9		3.2		3.6		4.3		6.0	ns
t$_{GHL}$	G-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t$_{LCO}$	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.7		6.3		7.1		8.4		11.9	ns
t$_{ACO}$	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.0		8.9		10.1		11.9		16.7	ns
d$_{TLH}$	Capacitive Loading, LOW to HIGH		0.03		0.03		0.03		0.04		0.06	ns/pF
d$_{THL}$	Capacitive Loading, HIGH to LOW		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. *For dual-module macros, use t$_{PD1}$ + t$_{RD1}$ + t$_{PDn}$, t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, point and position whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-34 • **A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T$_J$ = 70°C)

Parameter / Description		−3 Speed		−2 Speed		−1 Speed		Std Speed		−F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[5]												
t$_{DLH}$	Data-to-Pad HIGH		3.2		3.6		4.0		4.7		6.6	ns
t$_{DHL}$	Data-to-Pad LOW		2.5		2.7		3.1		3.6		5.1	ns
t$_{ENZH}$	Enable Pad Z to HIGH		2.7		3.0		3.4		4.0		5.6	ns
t$_{ENZL}$	Enable Pad Z to LOW		3.0		3.3		3.8		4.4		6.2	ns
t$_{ENHZ}$	Enable Pad HIGH to Z		5.4		6.0		6.8		8.0		11.2	ns
t$_{ENLZ}$	Enable Pad LOW to Z		5.0		5.6		6.3		7.4		10.4	ns
t$_{GLH}$	G-to-Pad HIGH		5.1		5.6		6.4		7.5		10.5	ns
t$_{GHL}$	G-to-Pad LOW		5.1		5.6		6.4		7.5		10.5	ns
t$_{LCO}$	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.7		6.3		7.1		8.4		11.9	ns
t$_{ACO}$	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.0		8.9		10.1		11.9		16.7	ns
d$_{TLH}$	Capacitive Loading, LOW to HIGH		0.03		0.03		0.03		0.04		0.06	ns/pF

Notes:

1. *For dual-module macros, use t$_{PD1}$ + t$_{RD1}$ + t$_{PDn}$, t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, point and position whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-35 • **A42MX16 Timing Characteristics (Nominal 3.3 V Operation)**
(Worst-Case Commercial Conditions, VCCA = 3.0 V, T$_J$ = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays[1]												
t$_{PD1}$	Single Module		1.9		2.1		2.4		2.8		4.0	ns
t$_{CO}$	Sequential Clock-to-Q		2.0		2.2		2.5		3.0		4.2	ns
t$_{GO}$	Latch G-to-Q		1.9		2.1		2.4		2.8		4.0	ns
t$_{RS}$	Flip-Flop (Latch) Reset-to-Q		2.2		2.4		2.8		3.3		4.6	ns
Logic Module Predicted Routing Delays[2]												
t$_{RD1}$	FO = 1 Routing Delay		1.1		1.2		1.4		1.6		2.3	ns
t$_{RD2}$	FO = 2 Routing Delay		1.5		1.6		1.8		2.1		3.0	ns
t$_{RD3}$	FO = 3 Routing Delay		1.8		2.0		2.3		2.7		3.8	ns
t$_{RD4}$	FO = 4 Routing Delay		2.2		2.4		2.7		3.2		4.5	ns
t$_{RD8}$	FO = 8 Routing Delay		3.6		4.0		4.5		5.3		7.5	ns
Logic Module Sequential Timing[3, 4]												
t$_{SUD}$	Flip-Flop (Latch) Data Input Set-Up	0.5		0.5		0.6		0.7		0.9		ns
t$_{HD}$	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{SUENA}$	Flip-Flop (Latch) Enable Set-Up	1.0		1.1		1.2		1.4		2.0		ns
t$_{HENA}$	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{WCLKA}$	Flip-Flop (Latch) Clock Active Pulse Width	4.8		5.3		6.0		7.1		9.9		ns
t$_{WASYN}$	Flip-Flop (Latch) Asynchronous Pulse Width	6.2		6.9		7.9		9.2		12.9		ns
t$_A$	Flip-Flop Clock Input Period	9.5		10.6		12.0		14.1		19.8		ns
t$_{INH}$	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{INSU}$	Input Buffer Latch Set-Up	0.7		0.8		0.9		1.01		1.4		ns
t$_{OUTH}$	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{OUTSU}$	Output Buffer Latch Set-Up	0.7		0.8		0.89		1.01		1.4		ns
f$_{MAX}$	Flip-Flop (Latch) Clock Frequency		129		117		108		94		56	MHz

Notes:

1. *For dual-module macros use t$_{PD1}$ + t$_{RD1}$ + taped, to + t$_{RD1}$ + taped, or t$_{PD1}$ + t$_{RD1}$ + tusk, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-35 • **A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 3.0 V, T$_J$ = 70°C)

Parameter / Description			–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
Input Module Propagation Delays													
t$_{INYH}$	Pad-to-Y HIGH			1.5		1.6		1.9		2.2		3.1	ns
t$_{INYL}$	Pad-to-Y LOW			1.1		1.3		1.4		1.7		2.4	ns
t$_{INGH}$	G to Y HIGH			2.0		2.2		2.5		2.9		4.1	ns
t$_{INGL}$	G to Y LOW			2.0		2.2		2.5		2.9		4.1	ns
Input Module Predicted Routing Delays[2]													
t$_{IRD1}$	FO = 1 Routing Delay			2.6		2.9		3.2		3.8		5.3	ns
t$_{IRD2}$	FO = 2 Routing Delay			2.9		3.2		3.7		4.3		6.1	ns
t$_{IRD3}$	FO = 3 Routing Delay			3.3		3.6		4.1		4.9		6.8	ns
t$_{IRD4}$	FO = 4 Routing Delay			3.6		4.0		4.6		5.4		7.6	ns
t$_{IRD8}$	FO = 8 Routing Delay			5.1		5.6		6.4		7.5		10.5	ns
Global Clock Network													
t$_{CKH}$	Input LOW to HIGH	FO = 32		4.4		4.8		5.5		6.5		9.0	ns
		FO = 384		4.8		5.3		6.0		7.1		9.9	ns
t$_{CKL}$	Input HIGH to LOW	FO = 32		5.3		5.9		6.7		7.8		11.0	ns
		FO = 384		6.2		6.9		7.9		9.2		12.9	ns
t$_{PWH}$	Minimum Pulse Width HIGH	FO = 32	5.7		6.3		7.1		8.4		11.8		ns
		FO = 384	6.6		7.4		8.3		9.8		13.7		ns
t$_{PWL}$	Minimum Pulse Width LOW	FO = 32	5.3		5.9		6.7		7.8		11.0		ns
		FO = 384	6.2		6.9		7.9		9.2		12.9		ns
t$_{CKSW}$	Maximum Skew	FO = 32		0.5		0.5		0.6		0.7		1.0	ns
		FO = 384		2.2		2.4		2.7		3.2		4.5	ns
t$_{SUEXT}$	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 384	0.0		0.0		0.0		0.0		0.0		ns
t$_{HEXT}$	Input Latch External Hold	FO = 32	3.9		4.3		4.9		5.7		8.0		ns
		FO = 384	4.5		4.9		5.6		6.6		9.2		ns
t$_P$	Minimum Period	FO = 32	7.0		7.8		8.4		9.7		16.2		ns
		FO = 384	7.7		8.6		9.3		10.7		17.8		ns
f$_{MAX}$	Maximum Frequency	FO = 32		142		129		119		103		62	MHz
		FO = 384		129		117		108		94		56	MHz

Notes:

1. For dual-module macros use t$_{PD1}$ + t$_{RD1}$ + taped, to + t$_{RD1}$ + taped, or t$_{PD1}$ + t$_{RD1}$ + tusk, whichever is appropriate.

2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.

4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

5. Delays based on 35 pF loading.

Table 1-35 • **A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 3.0 V, T$_J$ = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing5												
t$_{DLH}$	Data-to-Pad HIGH		3.5		3.9		4.4		5.2		7.3	ns
t$_{DHL}$	Data-to-Pad LOW		4.1		4.6		5.2		6.1		8.6	ns
t$_{ENZH}$	Enable Pad Z to HIGH		3.8		4.2		4.8		5.6		7.8	ns
t$_{ENZL}$	Enable Pad Z to LOW		4.2		4.6		5.3		6.2		8.7	ns
t$_{ENHZ}$	Enable Pad HIGH to Z		7.6		8.4		9.5		11.2		15.7	ns
t$_{ENLZ}$	Enable Pad LOW to Z		7.0		7.8		8.8		10.4		14.5	ns
t$_{GLH}$	G-to-Pad HIGH		4.8		5.3		6.0		7.2		10.0	ns
t$_{GHL}$	G-to-Pad LOW		4.8		5.3		6.0		7.2		10.0	ns
t$_{LCO}$	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.0		8.9		10.1		11.9		16.7	ns
t$_{ACO}$	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		11.3		12.5		14.2		16.7		23.3	ns
d$_{TLH}$	Capacitive Loading, LOW to HIGH		0.04		0.04		0.05		0.06		0.08	ns/pF
d$_{THL}$	Capacitive Loading, HIGH to LOW		0.05		0.05		0.06		0.07		0.10	ns/pF
CMOS Output Module Timing5												
t$_{DLH}$	Data-to-Pad HIGH		4.5		5.0		5.6		6.6		9.3	ns
t$_{DHL}$	Data-to-Pad LOW		3.4		3.8		4.3		5.1		7.1	ns
t$_{ENZH}$	Enable Pad Z to HIGH		3.8		4.2		4.8		5.6		7.8	ns
t$_{ENZL}$	Enable Pad Z to LOW		4.2		4.6		5.3		6.2		8.7	ns
t$_{ENHZ}$	Enable Pad HIGH to Z		7.6		8.4		9.5		11.2		15.7	ns
t$_{ENLZ}$	Enable Pad LOW to Z		7.0		7.8		8.8		10.4		14.5	ns
t$_{GLH}$	G-to-Pad HIGH		7.1		7.9		8.9		10.5		14.7	ns
t$_{GHL}$	G-to-Pad LOW		7.1		7.9		8.9		10.5		14.7	ns
t$_{LCO}$	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.0		8.9		10.1		11.9		16.7	ns
t$_{ACO}$	Array Clock-to-Out (Pad-to-Pad),64 Clock Loading		11.3		12.5		14.2		16.7		23.3	ns
d$_{TLH}$	Capacitive Loading, LOW to HIGH		0.04		0.04		0.05		0.06		0.08	ns/pF
d$_{THL}$	Capacitive Loading, HIGH to LOW		0.05		0.05		0.06		0.07		0.10	ns/pF

Notes:

1. *For dual-module macros use t$_{PD1}$ + t$_{RD1}$ + taped, to + t$_{RD1}$ + taped, or t$_{PD1}$ + t$_{RD1}$ + tusk, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-36 • **A42MX24 Timing Characteristics (Nominal 5.0 V Operation)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T$_J$ = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions[1]												
t$_{PD}$	Internal Array Module Delay		1.2		1.3		1.5		1.8		2.5	ns
t$_{PDD}$	Internal Decode Module Delay		1.4		1.6		1.8		2.1		3.0	ns
Logic Module Predicted Routing Delays[2]												
t$_{RD1}$	FO = 1 Routing Delay		0.8		0.9		1.0		1.2		1.7	ns
t$_{RD2}$	FO = 2 Routing Delay		1.0		1.2		1.3		1.5		2.1	ns
t$_{RD3}$	FO = 3 Routing Delay		1.3		1.4		1.6		1.9		2.6	ns
t$_{RD4}$	FO = 4 Routing Delay		1.5		1.7		1.9		2.2		3.1	ns
t$_{RD5}$	FO = 8 Routing Delay		2.4		2.7		3.0		3.6		5.0	ns
Logic Module Sequential Timing[3, 4]												
t$_{CO}$	Flip-Flop Clock-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t$_{GO}$	Latch Gate-to-Output		1.2		1.3		1.5		1.8		2.5	ns
t$_{SUD}$	Flip-Flop (Latch) Set-Up Time	0.3		0.4		0.4		0.5		0.7		ns
t$_{HD}$	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t$_{RO}$	Flip-Flop (Latch) Reset-to-Output		1.4		1.6		1.8		2.1		2.9	ns
t$_{SUENA}$	Flip-Flop (Latch) Enable Set-Up	0.4		0.5		0.5		0.6		0.8		ns
t$_{HENA}$	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{WCLKA}$	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.7		4.2		4.9		6.9		ns
t$_{WASYN}$	Flip-Flop (Latch) Asynchronous Pulse Width	4.4		4.8		5.3		6.5		9.0		ns
Input Module Propagation Delays												
t$_{INPY}$	Input Data Pad-to-Y		1.0		1.1		1.3		1.5		2.1	ns
t$_{INGO}$	Input Latch Gate-to-Output		1.3		1.4		1.6		1.9		2.6	ns
t$_{INH}$	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{INSU}$	Input Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t$_{ILA}$	Latch Active Pulse Width	4.7		5.2		5.9		6.9		9.7		ns

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-36 • **A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			−3 Speed Min.	−3 Speed Max.	−2 Speed Min.	−2 Speed Max.	−1 Speed Min.	−1 Speed Max.	Std Speed Min.	Std Speed Max.	−F Speed Min.	−F Speed Max.	Units
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			1.8		2.0		2.3		2.7		3.8	ns
t_{IRD2}	FO = 2 Routing Delay			2.1		2.3		2.6		3.1		4.3	ns
t_{IRD3}	FO = 3 Routing Delay			2.3		2.5		2.9		3.4		4.8	ns
t_{IRD4}	FO = 4 Routing Delay			2.5		2.8		3.2		3.7		5.2	ns
t_{IRD8}	FO = 8 Routing Delay			3.4		3.8		4.3		5.1		7.1	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		2.6		2.9		3.3		3.9		5.4	ns
		FO = 486		2.9		3.2		3.6		4.3		5.9	ns
t_{CKL}	Input HIGH to LOW	FO = 32		3.7		4.1		4.6		5.4		7.6	ns
		FO = 486		4.3		4.7		5.4		6.3		8.8	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	2.2		2.4		2.7		3.2		4.5		ns
		FO = 486	2.4		2.6		3.0		3.5		4.9		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	2.2		2.4		2.7		3.2		4.5		ns
		FO = 486	2.4		2.6		3.0		3.5		4.9		ns
t_{CKSW}	Maximum Skew	FO = 32		0.5		0.6		0.7		0.8		1.1	ns
		FO = 486		0.5		0.6		0.7		0.8		1.1	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 486	0.0		0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32	2.8		3.1		3.5		4.1		5.7		ns
		FO = 486	3.3		3.7		4.2		4.9		6.9		ns
t_P	Minimum Period (1/f_{MAX})	FO = 32	4.7		5.2		5.7		6.5		10.9		ns
		FO = 486	5.1		5.7		6.2		7.1		11.9		ns

Notes:

1. *For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-36 • **A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T$_J$ = 70°C)

Parameter / Description		−3 Speed		−2 Speed		−1 Speed		Std Speed		−F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing[5]												
t$_{DLH}$	Data-to-Pad HIGH		2.4		2.7		3.1		3.6		5.1	ns
t$_{DHL}$	Data-to-Pad LOW		2.8		3.2		3.6		4.2		5.9	ns
t$_{ENZH}$	Enable Pad Z to HIGH		2.5		2.8		3.2		3.8		5.3	ns
t$_{ENZL}$	Enable Pad Z to LOW		2.8		3.1		3.5		4.2		5.9	ns
t$_{ENHZ}$	Enable Pad HIGH to Z		5.2		5.7		6.5		7.6		10.7	ns
t$_{ENLZ}$	Enable Pad LOW to Z		4.8		5.3		6.0		7.1		9.9	ns
t$_{GLH}$	G-to-Pad HIGH		2.9		3.2		3.6		4.3		6.0	ns
t$_{GHL}$	G-to-Pad LOW		2.9		3.2		3.6		4.3		6.0	ns
t$_{LSU}$	I/O Latch Output Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t$_{LH}$	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{LCO}$	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.6		6.1		6.9		8.1		11.4	ns
t$_{ACO}$	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.6		11.8		13.4		15.7		22.0	ns
d$_{TLH}$	Capacitive Loading, LOW to HIGH		0.04		0.04		0.04		0.05		0.07	ns/pF
d$_{THL}$	Capacitive Loading, HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

Notes:

1. *For dual-module macros, use t$_{PD1}$ + t$_{RD1}$ + t$_{PDn}$, t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-36 • **A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T$_J$ = 70°C)

Parameter / Description		−3 Speed		−2 Speed		−1 Speed		Std Speed		−F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[5]												
t$_{DLH}$	Data-to-Pad HIGH		3.1		3.5		3.9		4.6		6.4	ns
t$_{DHL}$	Data-to-Pad LOW		2.4		2.6		3.0		3.5		4.9	ns
t$_{ENZH}$	Enable Pad Z to HIGH		2.5		2.8		3.2		3.8		5.3	ns
t$_{ENZL}$	Enable Pad Z to LOW		2.8		3.1		3.5		4.2		5.8	ns
t$_{ENHZ}$	Enable Pad HIGH to Z		5.2		5.7		6.5		7.6		10.7	ns
t$_{ENLZ}$	Enable Pad LOW to Z		4.8		5.3		6.0		7.1		9.9	ns
t$_{GLH}$	G-to-Pad HIGH		4.9		5.4		6.2		7.2		10.1	ns
t$_{GHL}$	G-to-Pad LOW		4.9		5.4		6.2		7.2		10.1	ns
t$_{LSU}$	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t$_{LH}$	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{LCO}$	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.5		6.1		6.9		8.1		11.3	ns
t$_{ACO}$	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.6		11.8		13.4		15.7		22.0	ns
d$_{TLH}$	Capacitive Loading, LOW to HIGH		0.04		0.04		0.04		0.05		0.07	ns/pF
d$_{THL}$	Capacitive Loading, HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

Notes:

1. *For dual-module macros, use t$_{PD1}$ + t$_{RD1}$ + t$_{PDn}$, t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-37 • **A42MX24 Timing Characteristics (Nominal 3.3 V Operation)**
(Worst-Case Commercial Conditions, VCCA = 3.0 V, T$_J$ = 70°C)

Parameter / Description		–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
Logic Module Combinatorial Functions[1]												
t_{PD}	Internal Array Module Delay		2.0		1.8		2.1		2.5		3.4	ns
t_{PDD}	Internal Decode Module Delay		1.1		2.2		2.5		3.0		4.2	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		1.7		1.3		1.4		1.7		2.3	ns
t_{RD2}	FO = 2 Routing Delay		2.0		1.6		1.8		2.1		3.0	ns
t_{RD3}	FO = 3 Routing Delay		1.1		2.0		2.2		2.6		3.7	ns
t_{RD4}	FO = 4 Routing Delay		1.5		2.3		2.6		3.1		4.3	ns
t_{RD5}	FO = 8 Routing Delay		1.8		3.7		4.2		5.0		7.0	ns
Logic Module Sequential Timing[3, 4]												
t_{CO}	Flip-Flop Clock-to-Output		2.1		2.0		2.3		2.7		3.7	ns
t_{GO}	Latch Gate-to-Output		3.4		1.9		2.1		2.5		3.4	ns
t_{SUD}	Flip-Flop (Latch) Set-Up Time	0.4		0.5		0.6		0.7		0.9		ns
t_{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		2.0		2.2		2.5		2.9		4.1	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.6		0.6		0.7		0.8		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.2		5.8		6.9		9.6		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.1		6.8		7.7		9.0		12.6		ns
Input Module Propagation Delays												
t_{INPY}	Input Data Pad-to-Y		1.4		1.6		1.8		2.2		3.0	ns
t_{INGO}	Input Latch Gate-to-Output		1.8		1.9		2.2		2.6		3.6	ns
t_{INH}	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t_{ILA}	Latch Active Pulse Width	6.5		7.3		8.2		9.7		13.5		ns

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-37 • **A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 3.0 V, T$_J$ = 70°C)

Parameter / Description			−3 Speed		−2 Speed		−1 Speed		Std Speed		−F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays[2]													
t$_{IRD1}$	FO = 1 Routing Delay			2.6		2.9		3.2		3.8		5.3	ns
t$_{IRD2}$	FO = 2 Routing Delay			2.9		3.2		3.6		4.3		6.0	ns
t$_{IRD3}$	FO = 3 Routing Delay			3.2		3.6		4.0		4.8		6.6	ns
t$_{IRD4}$	FO = 4 Routing Delay			3.5		3.9		4.4		5.2		7.3	ns
t$_{IRD8}$	FO = 8 Routing Delay			4.8		5.3		6.1		7.1		10.0	ns
Global Clock Network													
t$_{CKH}$	Input LOW to HIGH	FO = 32		4.4		4.8		5.5		6.5		9.1	ns
		FO = 486		4.8		5.3		6.0		7.1		10.0	ns
t$_{CKL}$	Input HIGH to LOW	FO = 32		5.1		5.7		6.4		7.6		10.6	ns
		FO = 486		6.0		6.6		7.5		8.8		12.4	ns
t$_{PWH}$	Minimum Pulse Width HIGH	FO = 32	3.0		3.3		3.8		4.5		6.3		ns
		FO = 486	3.3		3.7		4.2		4.9		6.9		ns
t$_{PWL}$	Minimum Pulse Width LOW	FO = 32	3.0		3.4		3.8		4.5		6.3		ns
		FO = 486	3.3		3.7		4.2		4.9		6.9		ns
t$_{CKSW}$	Maximum Skew	FO = 32		0.8		0.8		1.0		1.1		1.6	ns
		FO = 486		0.8		0.8		1.0		1.1		1.6	ns
t$_{SUEXT}$	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 486	0.0		0.0		0.0		0.0		0.0		ns
TTL Output Module Timing[5]													
t$_{DLH}$	Data-to-Pad HIGH			3.4		3.8		4.3		5.0		7.1	ns
t$_{DHL}$	Data-to-Pad LOW			4.0		4.4		5.0		5.9		8.3	ns
t$_{ENZH}$	Enable Pad Z to HIGH			3.6		4.0		4.5		5.3		7.4	ns
t$_{ENZL}$	Enable Pad Z to LOW			3.9		4.4		5.0		5.8		8.2	ns
t$_{ENHZ}$	Enable Pad HIGH to Z			7.2		8.0		9.1		10.7		14.9	ns
t$_{ENLZ}$	Enable Pad LOW to Z			6.7		7.5		8.5		9.9		13.9	ns
t$_{GLH}$	G-to-Pad HIGH			4.8		5.3		6.0		7.2		10.0	ns
t$_{GHL}$	G-to-Pad LOW			4.8		5.3		6.0		7.2		10.0	ns
t$_{LSU}$	I/O Latch Output Set-Up		0.7		0.7		0.8		1.0		1.4		ns

Notes:

1. For dual-module macros, use t$_{PD1}$ + t$_{RD1}$ + t$_{PDn}$, t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.

2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.

4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

5. Delays based on 35 pF loading.

Table 1-37 • **A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing[5] (continued)												
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.7		8.5		9.6		11.3		15.9	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		14.8		16.5		18.7		22.0		30.8	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.04		0.04		0.05		0.06		0.08	ns/pF
CMOS Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		4.8		5.3		5.5		6.4		9.0	ns
t_{DHL}	Data-to-Pad LOW		3.5		3.9		4.1		4.9		6.8	ns
t_{ENZH}	Enable Pad Z to HIGH		3.6		4.0		4.5		5.3		7.4	ns
t_{ENZL}	Enable Pad Z to LOW		3.4		4.0		5.0		5.8		8.2	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.2		8.0		9.0		10.7		14.9	ns
t_{ENLZ}	Enable Pad LOW to Z		6.7		7.5		8.5		9.9		13.9	ns
t_{GLH}	G-to-Pad HIGH		6.8		7.6		8.6		10.1		14.2	ns
t_{GHL}	G-to-Pad LOW		6.8		7.6		8.6		10.1		14.2	ns
t_{LSU}	I/O Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.7		8.5		9.6		11.3		15.9	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		14.8		16.5		18.7		22.0		30.8	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.04		0.04		0.05		0.06		0.08	ns/pF
t_{HEXT}	Input Latch External Hold FO = 32	3.9		4.3		4.9		5.7		8.1		ns
	FO = 486	4.6		5.2		5.8		6.9		9.6		ns
t_P	Minimum Period FO = 32	7.8		8.7		9.5		10.8		18.2		ns
	(1/f_{MAX}) FO = 486	8.6		9.5		10.4		11.9		19.9		ns

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-38 • **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T$_J$ = 70°C)

Parameter / Description		–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
Logic Module Combinatorial Functions[1]												
t$_{PD}$	Internal Array Module Delay		1.3		1.5		1.7		2.0		2.7	ns
t$_{PDD}$	Internal Decode Module Delay		1.6		1.8		2.0		2.4		3.3	ns
Logic Module Predicted Routing Delays[2]												
t$_{RD1}$	FO = 1 Routing Delay		0.9		1.0		1.2		1.4		2.0	ns
t$_{RD2}$	FO = 2 Routing Delay		1.3		1.4		1.6		1.9		2.7	ns
t$_{RD3}$	FO =3 Routing Delay		1.6		1.8		2.0		2.4		3.4	ns
t$_{RD4}$	FO = 4 Routing Delay		2.0		2.2		2.5		2.9		4.1	ns
t$_{RD5}$	FO = 8 Routing Delay		3.3		3.7		4.2		4.9		6.9	ns
t$_{RDD}$	Decode-to-Output Routing Delay		0.3		0.4		0.4		0.5		0.7	ns
Logic Module Sequential Timing[3, 4]												
t$_{CO}$	Flip-Flop Clock-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t$_{GO}$	Latch Gate-to-Output		1.3		1.4		1.6		1.9		2.7	ns
t$_{SUD}$	Flip-Flop (Latch) Set-Up Time	0.3		0.3		0.4		0.5		0.7		ns
t$_{HD}$	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t$_{RO}$	Flip-Flop (Latch) Reset-to-Output		1.6		1.7		2.0		2.3		3.2	ns
t$_{SUENA}$	Flip-Flop (Latch) Enable Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t$_{HENA}$	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{WCLKA}$	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.7		4.2		4.9		6.9		ns
t$_{WASYN}$	Flip-Flop (Latch) Asynchronous Pulse Width	4.4		4.8		5.5		6.4		9.0		ns
Synchronous SRAM Operations												
t$_{RC}$	Read Cycle Time	6.8		7.5		8.5		10.0		14.0		ns
t$_{WC}$	Write Cycle Time	6.8		7.5		8.5		10.0		14.0		ns
t$_{RCKHL}$	Clock HIGH/LOW Time	3.4		3.8		4.3		5.0		7.0		ns
t$_{RCO}$	Data Valid After Clock HIGH/LOW		3.4		3.8		4.3		5.0		7.0	ns
t$_{ADSU}$	Address/Data Set-Up Time	1.6		1.8		2.0		2.4		3.4		ns
Synchronous SRAM Operations (continued)												
t$_{ADH}$	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns

Notes:

1. *For dual-module macros, use t$_{PD1}$ + t$_{RD1}$ + t$_{PDn}$, t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*
4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. *Delays based on 35 pF loading.*

Table 1-38 • **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RENSU}	Read Enable Set-Up	0.6		0.7		0.8		0.9		1.3		ns
t_{RENH}	Read Enable Hold	3.4		3.8		4.3		5.0		7.0		ns
t_{WENSU}	Write Enable Set-Up	2.7		3.0		3.4		4.0		5.6		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{BENS}	Block Enable Set-Up	2.8		3.1		3.5		4.1		5.7		ns
t_{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations												
t_{RPD}	Asynchronous Access Time		8.1		9.0		10.2		12.0		16.8	ns
t_{RDADV}	Read Address Valid	8.8		9.8		11.1		13.0		18.2		ns
t_{ADSU}	Address/Data Set-Up Time	1.6		1.8		2.0		2.4		3.4		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RENSUA}	Read Enable Set-Up to Address Valid	0.6		0.7		0.8		0.9		1.3		ns
t_{RENHA}	Read Enable Hold	3.4		3.8		4.3		5.0		7.0		ns
t_{WENSU}	Write Enable Set-Up	2.7		3.0		3.4		4.0		5.6		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.2		1.3		1.5		1.8		2.5	ns
Input Module Propagation Delays												
t_{INPY}	Input Data Pad-to-Y		1.0		1.1		1.3		1.5		2.1	ns
t_{INGO}	Input Latch Gate-to-Output		1.4		1.6		1.8		2.1		2.9	ns
t_{INH}	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t_{ILA}	Latch Active Pulse Width	4.7		5.2		5.9		6.9		9.7		ns
Input Module Predicted Routing Delays2												
t_{IRD1}	FO = 1 Routing Delay		2.0		2.2		2.5		2.9		4.1	ns
t_{IRD2}	FO = 2 Routing Delay		2.3		2.6		2.9		3.4		4.8	ns
t_{IRD3}	FO = 3 Routing Delay		2.6		2.9		3.3		3.9		5.5	ns
t_{IRD4}	FO = 4 Routing Delay		3.0		3.3		3.8		4.4		6.2	ns
t_{IRD8}	FO = 8 Routing Delay		4.3		4.8		5.5		6.4		9.0	ns

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-38 • **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32		2.7		3.0		3.4		4.0		5.6	ns
		FO = 635		3.0		3.3		3.8		4.4		6.2	ns
t_{CKL}	Input HIGH to LOW	FO = 32		3.8		4.2		4.8		5.6		7.8	ns
		FO = 635		4.9		5.4		6.1		7.2		10.1	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	1.8		2.0		2.2		2.6		3.6		ns
		FO = 635	2.0		2.2		2.5		2.9		4.1		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	1.8		2.0		2.2		2.6		3.6		ns
		FO = 635	2.0		2.2		2.5		2.9		4.1		ns
t_{CKSW}	Maximum Skew	FO = 32		0.8		0.8		0.9		1.0		1.4	ns
		FO = 635		0.8		0.8		0.9		1.0		1.4	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 635	0.0		0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32	2.8		3.2		3.6		4.2		5.9		ns
		FO = 635	3.3		3.7		4.2		4.9		6.9		ns
t_P	Minimum Period $(1/f_{MAX})$	FO = 32	5.5		6.1		6.6		7.6		12.7		ns
		FO = 635	6.0		6.6		7.2		8.3		13.8		ns
f_{MAX}	Maximum Datapath Frequency	FO = 32		180		164		151		131		79	MHz
		FO = 635		166		151		139		121		73	MHz
TTL Output Module Timing[5]													
t_{DLH}	Data-to-Pad HIGH			2.6		2.8		3.2		3.8		5.3	ns
t_{DHL}	Data-to-Pad LOW			3.0		3.3		3.7		4.4		6.2	ns
t_{ENZH}	Enable Pad Z to HIGH			2.7		3.0		3.3		3.9		5.5	ns
t_{ENZL}	Enable Pad Z to LOW			3.0		3.3		3.7		4.3		6.1	ns
t_{ENHZ}	Enable Pad HIGH to Z			5.3		5.8		6.6		7.8		10.9	ns

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-38 • **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing[5] (Continued)												
t_{ENLZ}	Enable Pad LOW to Z		4.9		5.5		6.2		7.3		10.2	ns
t_{GLH}	G-to-Pad HIGH		2.9		3.3		3.7		4.4		6.1	ns
t_{GHL}	G-to-Pad LOW		2.9		3.3		3.7		4.4		6.1	ns
t_{LSU}	I/O Latch Output Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7		6.3		7.1		8.4		11.8	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8		8.6		9.8		11.5		16.1	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.07		0.08		0.09		0.10		0.14	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.07		0.08		0.09		0.10		0.14	ns/pF

Notes:

1. *For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-38 • **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)**
(Worst-Case Commercial Conditions, VCCA = 4.75 V, T$_J$ = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing[5]												
t$_{DLH}$	Data-to-Pad HIGH		3.5		3.9		4.5		5.2		7.3	ns
t$_{DHL}$	Data-to-Pad LOW		2.5		2.7		3.1		3.6		5.1	ns
t$_{ENZH}$	Enable Pad Z to HIGH		2.7		3.0		3.3		3.9		5.5	ns
t$_{ENZL}$	Enable Pad Z to LOW		2.9		3.3		3.7		4.3		6.1	ns
t$_{ENHZ}$	Enable Pad HIGH to Z		5.3		5.8		6.6		7.8		10.9	ns
t$_{ENLZ}$	Enable Pad LOW to Z		4.9		5.5		6.2		7.3		10.2	ns
t$_{GLH}$	G-to-Pad HIGH		5.0		5.6		6.3		7.5		10.4	ns
t$_{GHL}$	G-to-Pad LOW		5.0		5.6		6.3		7.5		10.4	ns
t$_{LSU}$	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t$_{LH}$	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{LCO}$	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7		6.3		7.1		8.4		11.8	ns
t$_{ACO}$	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8		8.6		9.8		11.5		16.1	ns
d$_{TLH}$	Capacitive Loading, LOW to HIGH		0.07		0.08		0.09		0.10		0.14	ns/pF
d$_{THL}$	Capacitive Loading, HIGH to LOW		0.07		0.08		0.09		0.10		0.14	ns/pF

Notes:

1. *For dual-module macros, use t$_{PD1}$ + t$_{RD1}$ + t$_{PDn}$, t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-39 • **A42MX36 Timing Characteristics (Nominal 3.3 V Operation)**
(Worst-Case Commercial Conditions, VCCA = 3.0 V, T$_J$ = 70°C)

Parameter / Description		−3 Speed Min.	−3 Speed Max.	−2 Speed Min.	−2 Speed Max.	−1 Speed Min.	−1 Speed Max.	Std Speed Min.	Std Speed Max.	−F Speed Min.	−F Speed Max.	Units
Logic Module Combinatorial Functions[1]												
t$_{PD}$	Internal Array Module Delay		1.9		2.1		2.3		2.7		3.8	ns
t$_{PDD}$	Internal Decode Module Delay		2.2		2.5		2.8		3.3		4.7	ns
Logic Module Predicted Routing Delays[2]												
t$_{RD1}$	FO = 1 Routing Delay		1.3		1.5		1.7		2.0		2.7	ns
t$_{RD2}$	FO = 2 Routing Delay		1.8		2.0		2.3		2.7		3.7	ns
t$_{RD3}$	FO = 3 Routing Delay		2.3		2.5		2.8		3.4		4.7	ns
t$_{RD4}$	FO = 4 Routing Delay		2.8		3.1		3.5		4.1		5.7	ns
t$_{RD5}$	FO = 8 Routing Delay		4.6		5.2		5.8		6.9		9.6	ns
t$_{RDD}$	Decode-to-Output Routing Delay		0.5		0.5		0.6		0.7		1.0	ns
Logic Module Sequential Timing[3, 4]												
t$_{CO}$	Flip-Flop Clock-to-Output		1.8		2.0		2.3		2.7		3.7	ns
t$_{GO}$	Latch Gate-to-Output		1.8		2.0		2.3		2.7		3.7	ns
t$_{SUD}$	Flip-Flop (Latch) Set-Up Time	0.4		0.5		0.6		0.7		0.9		ns
t$_{HD}$	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t$_{RO}$	Flip-Flop (Latch) Reset-to-Output		2.2		2.4		2.7		3.2		4.5	ns
t$_{SUENA}$	Flip-Flop (Latch) Enable Set-Up	1.0		1.1		1.2		1.4		2.0		ns
t$_{HENA}$	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{WCLKA}$	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.2		5.8		6.9		9.6		ns
t$_{WASYN}$	Flip-Flop (Latch) Asynchronous Pulse Width	6.1		6.8		7.7		9.0		12.6		ns
Synchronous SRAM Operations												
t$_{RC}$	Read Cycle Time	9.5		10.5		11.9		14.0		19.6		ns
t$_{WC}$	Write Cycle Time	9.5		10.5		11.9		14.0		19.6		ns
t$_{RCKHL}$	Clock HIGH/LOW Time	4.8		5.3		6.0		7.0		9.8		ns
t$_{RCO}$	Data Valid After Clock HIGH/LOW		4.8		5.3		6.0		7.0		9.8	ns
t$_{ADSU}$	Address/Data Set-Up Time	2.3		2.5		2.8		3.4		4.8		ns

Notes:

1. *For dual-module macros, use t$_{PD1}$ + t$_{RD1}$ + t$_{PDn}$, t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-39 • **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 3.0 V, T$_J$ = 70°C)

Parameter / Description		−3 Speed		−2 Speed		−1 Speed		Std Speed		−F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous SRAM Operations (continued)												
t$_{ADH}$	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t$_{RENSU}$	Read Enable Set-Up	0.9		1.0		1.1		1.3		1.8		ns
t$_{RENH}$	Read Enable Hold	4.8		5.3		6.0		7.0		9.8		ns
t$_{WENSU}$	Write Enable Set-Up	3.8		4.2		4.8		5.6		7.8		ns
t$_{WENH}$	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{BENS}$	Block Enable Set-Up	3.9		4.3		4.9		5.7		8.0		ns
t$_{BENH}$	Block Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations												
t$_{RPD}$	Asynchronous Access Time		11.3		12.6		14.3		16.8		23.5	ns
t$_{RDADV}$	Read Address Valid	12.3		13.7		15.5		18.2		25.5		ns
t$_{ADSU}$	Address/Data Set-Up Time	2.3		2.5		2.8		3.4		4.8		ns
t$_{ADH}$	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t$_{RENSUA}$	Read Enable Set-Up to Address Valid	0.9		1.0		1.1		1.3		1.8		ns
t$_{RENHA}$	Read Enable Hold	4.8		5.3		6.0		7.0		9.8		ns
t$_{WENSU}$	Write Enable Set-Up	3.8		4.2		4.8		5.6		7.8		ns
t$_{WENH}$	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{DOH}$	Data Out Hold Time		1.8		2.0		2.1		2.5		3.5	ns
Input Module Propagation Delays												
t$_{INPY}$	Input Data Pad-to-Y		1.4		1.6		1.8		2.1		3.0	ns
t$_{INGO}$	Input Latch Gate-to-Output		2.0		2.2		2.5		2.9		4.1	ns
t$_{INH}$	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{INSU}$	Input Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t$_{ILA}$	Latch Active Pulse Width	6.5		7.3		8.2		9.7		13.5		ns

Notes:

1. *For dual-module macros, use t$_{PD1}$ + t$_{RD1}$ + t$_{PDn}$, t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-39 • **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 3.0 V, T$_J$ = 70°C)

Parameter / Description		−3 Speed		−2 Speed		−1 Speed		Std Speed		−F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays2												
t$_{IRD1}$	FO = 1 Routing Delay		2.8		3.1		3.5		4.1		5.7	ns
t$_{IRD2}$	FO = 2 Routing Delay		3.2		3.5		4.1		4.8		6.7	ns
t$_{IRD3}$	FO = 3 Routing Delay		3.7		4.1		4.7		5.5		7.7	ns
t$_{IRD4}$	FO = 4 Routing Delay		4.2		4.6		5.3		6.2		8.7	ns
t$_{IRD8}$	FO = 8 Routing Delay		6.1		6.8		7.7		9.0		12.6	ns
Global Clock Network												
t$_{CKH}$	Input LOW to HIGH	FO = 32	4.6		5.1		5.7		6.7		9.3	ns
		FO = 635	5.0		5.6		6.3		7.4		10.3	ns
t$_{CKL}$	Input HIGH to LOW	FO = 32	5.3		5.9		6.7		7.8		11.0	ns
		FO = 635	6.8		7.6		8.6		10.1		14.1	ns
t$_{PWH}$	Minimum Pulse Width HIGH	FO = 32	2.5		2.7		3.1		3.6		5.1		ns
		FO = 635	2.8		3.1		3.5		4.1		5.7		ns
t$_{PWL}$	Minimum Pulse Width LOW	FO = 32	2.5		2.7		3.1		3.6		5.1		ns
		FO = 635	2.8		3.1		3.5		4.1		5.7		ns
t$_{CKSW}$	Maximum Skew	FO = 32		1.0		1.2		1.3		1.5		2.2	ns
		FO = 635		1.0		1.2		1.3		1.5		2.2	ns
t$_{SUEXT}$	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 635	0.0		0.0		0.0		0.0		0.0		ns
t$_{HEXT}$	Input Latch External Hold	FO = 32	4.0		4.4		5.0		5.9		8.2		ns
		FO = 635	4.6		5.2		5.9		6.9		9.6		ns
t$_P$	Minimum Period (1/f$_{MAX}$)	FO = 32	9.2		10.2		11.1		12.7		21.2		ns
		FO = 635	9.9		11.0		12.0		13.8		23.0		ns
f$_{MAX}$	Maximum Frequency	Datapath FO = 32		108		98		90		79		47	MHz
		FO = 635		100		91		83		73		44	MHz
TTL Output Module Timing5												
t$_{DLH}$	Data-to-Pad HIGH			3.6		4.0		4.5		5.3		7.4	ns
t$_{DHL}$	Data-to-Pad LOW			4.2		4.6		5.2		6.2		8.6	ns
t$_{ENZH}$	Enable Pad Z to HIGH			3.7		4.2		4.7		5.5		7.7	ns
t$_{ENZL}$	Enable Pad Z to LOW			4.1		4.6		5.2		6.1		8.5	ns
t$_{ENHZ}$	Enable Pad HIGH to Z			7.34		8.2		9.3		10.9		15.3	ns

Notes:

1. *For dual-module macros, use t$_{PD1}$ + t$_{RD1}$ + t$_{PDn}$, t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Table 1-39 • **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)**
(Worst-Case Commercial Conditions, VCCA = 3.0 V, T$_J$ = 70°C)

Parameter / Description		−3 Speed		−2 Speed		−1 Speed		Std Speed		−F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing[5]												
t$_{ENLZ}$	Enable Pad LOW to Z		6.9		7.6		8.7		10.2		14.3	ns
t$_{GLH}$	G-to-Pad HIGH		4.9		5.5		6.2		7.3		10.2	ns
t$_{GHL}$	G-to-Pad LOW		4.9		5.5		6.2		7.3		10.2	ns
t$_{LSU}$	I/O Latch Output Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t$_{LH}$	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{LCO}$	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.9		8.8		10.0		11.8		16.5	ns
t$_{ACO}$	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.9		12.1		13.7		16.1		22.5	ns
d$_{TLH}$	Capacitive Loading, LOW to HIGH		0.10		0.11		0.12		0.14		0.20	ns/pF
d$_{THL}$	Capacitive Loading, HIGH to LOW		0.10		0.11		0.12		0.14		0.20	ns/pF
CMOS Output Module Timing[5]												
t$_{DLH}$	Data-to-Pad HIGH		4.9		5.5		6.2		7.3		10.3	ns
t$_{DHL}$	Data-to-Pad LOW		3.4		3.8		4.3		5.1		7.1	ns
t$_{ENZH}$	Enable Pad Z to HIGH		3.7		4.1		4.7		5.5		7.7	ns
t$_{ENZL}$	Enable Pad Z to LOW		4.1		4.6		5.2		6.1		8.5	ns
t$_{ENHZ}$	Enable Pad HIGH to Z		7.4		8.2		9.3		10.9		15.3	ns
t$_{ENLZ}$	Enable Pad LOW to Z		6.9		7.6		8.7		10.2		14.3	ns
t$_{GLH}$	G-to-Pad HIGH		7.0		7.8		8.9		10.4		14.6	ns
t$_{GHL}$	G-to-Pad LOW		7.0		7.8		8.9		10.4		14.6	ns
t$_{LSU}$	I/O Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t$_{LH}$	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{LCO}$	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.9		8.8		10.0		11.8		16.5	ns

Notes:

1. *For dual-module macros, use t$_{PD1}$ + t$_{RD1}$ + t$_{PDn}$, t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*

4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

5. *Delays based on 35 pF loading.*

Pin Descriptions

CLK/A/B, I/O   **Global Clock**

Clock inputs for clock distribution networks. CLK is for 40MX while CLKA and CLKB are for 42MX devices. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK, I/O   **Diagnostic Clock**

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND   **Ground**

Input LOW supply voltage.

I/O   **Input/Output**

Input, output, tristate or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/Os pins are configured by the Designer software as shown in Table 1-40.

Table 1-40 • **Configuration of Unused I/Os**

Device	Configuration
A40MX02, A40MX04	Pulled LOW
A42MX09, A42MX16	Pulled LOW
A42MX24, A42MX36	Tristated

In all cases, it is recommended to tie all unused MX I/O pins to LOW on the board. This applies to all dual-purpose pins when configured as I/Os as well.

LP   **Low Power Mode**

Controls the low power mode of all 42MX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation in 200 µs after the LP pin is driven to a logic LOW.

MODE   **Mode**

Controls the use of multifunction pins (DCLK, PRA, PRB, SDI, TDO). The MODE pin is held HIGH to provide verification capability. The MODE pin should be terminated to GND through a 10kΩ resistor so that the MODE pin can be pulled HIGH when required.

NC   **No Connection**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA, I/O

PRB, I/O   **Probe A/B**

The Probe pin is used to output data from any user-defined design node within the device. Each diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. The Probe pin is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

QCLKA/B/C/D, I/O   **Quadrant Clock**

Quadrant clock inputs for A42MX36 devices. When not used as a register control signal, these pins can function as user I/Os.

SDI, I/O   **Serial Data Input**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDO, I/O   **Serial Data Output**

Serial data output for diagnostic probe and device programming. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW. SDO is available for 42MX devices only.

When Silicon Explorer II is being used, SDO will act as an output while the "checksum" command is run. It will return to user I/O when "checksum" is complete.

TCK, I/O   **Test Clock**

Clock signal to shift the Boundary Scan Test (BST) data into the device. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

TDI, I/O   **Test Data In**

Serial data input for BST instructions and data. Data is shifted in on the rising edge of TCK. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

TDO, I/O   **Test Data Out**

Serial data output for BST instructions and test data. This pin functions as an I/O when "Reserve JTAG" is not checked in the Designer Software. BST pins are only available in A42MX24 and A42MX36 devices.

TMS, I/O   **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI and TDO pins are boundary scan pins. Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications. IEEE JTAG specification recommends a 10kΩ pull-up resistor on the pin. BST pins are only available in A42MX24 and A42MX36 devices.

VCC   **Supply Voltage**

Input supply voltage for 40MX devices

VCCA   **Supply Voltage**

Supply voltage for array in 42MX devices

VCCI   **Supply Voltage**

Supply voltage for I/Os in 42MX devices

WD, I/O   **Wide Decode Output**

When a wide decode module is used in a 42MX device this pin can be used as a dedicated output from the wide decode module. This direct connection eliminates additional interconnect delays associated with regular logic modules. To implement the direct I/O connection, connect an output buffer of any type to the output of the wide decode macro and place this output on one of the reserved WD pins.

Power Matters.™

2 – Package Pin Assignments

PL44

1 44
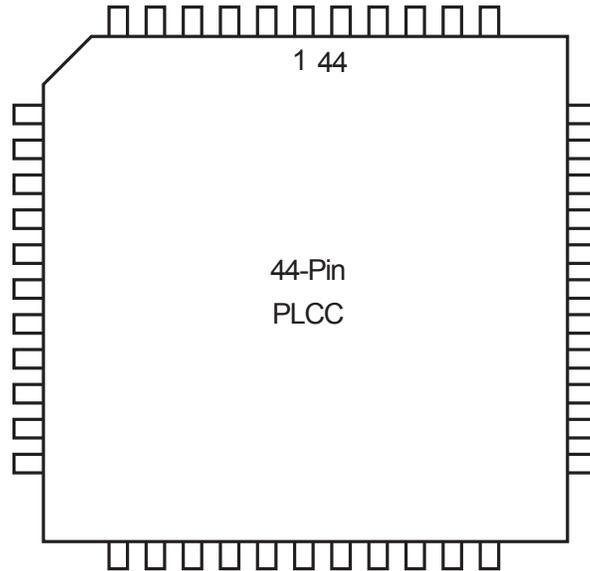
44-Pin
PLCC

PL44		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
1	I/O	I/O
2	I/O	I/O
3	VCC	VCC
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	GND	GND
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	VCC	VCC
15	I/O	I/O
16	VCC	VCC
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	GND	GND
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	VCC	VCC
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	CLK, I/O	CLK, I/O
34	MODE	MODE
35	VCC	VCC
36	SDI, I/O	SDI, I/O

PL44		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
37	DCLK, I/O	DCLK, I/O
38	PRA, I/O	PRA, I/O
39	PRB, I/O	PRB, I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	GND	GND
44	I/O	I/O

PL68

1 68

68-Pin
PLCC

　　　　　　　　　　　　　　　　　　　　Revision 14

PL68			PL68		
Pin Number	A40MX02 Function	A40MX04 Function	Pin Number	A40MX02 Function	A40MX04 Function
1	I/O	I/O	36	I/O	I/O
2	I/O	I/O	37	I/O	I/O
3	I/O	I/O	38	VCC	VCC
4	VCC	VCC	39	I/O	I/O
5	I/O	I/O	40	I/O	I/O
6	I/O	I/O	41	I/O	I/O
7	I/O	I/O	42	I/O	I/O
8	I/O	I/O	43	I/O	I/O
9	I/O	I/O	44	I/O	I/O
10	I/O	I/O	45	I/O	I/O
11	I/O	I/O	46	I/O	I/O
12	I/O	I/O	47	I/O	I/O
13	I/O	I/O	48	I/O	I/O
14	GND	GND	49	GND	GND
15	GND	GND	50	I/O	I/O
16	I/O	I/O	51	I/O	I/O
17	I/O	I/O	52	CLK, I/O	CLK, I/O
18	I/O	I/O	53	I/O	I/O
19	I/O	I/O	54	MODE	MODE
20	I/O	I/O	55	VCC	VCC
21	VCC	VCC	56	SDI, I/O	SDI, I/O
22	I/O	I/O	57	DCLK, I/O	DCLK, I/O
23	I/O	I/O	58	PRA, I/O	PRA, I/O
24	I/O	I/O	59	PRB, I/O	PRB, I/O
25	VCC	VCC	60	I/O	I/O
26	I/O	I/O	61	I/O	I/O
27	I/O	I/O	62	I/O	I/O
28	I/O	I/O	63	I/O	I/O
29	I/O	I/O	64	I/O	I/O
30	I/O	I/O	65	I/O	I/O
31	I/O	I/O	66	GND	GND
32	GND	GND	67	I/O	I/O
33	I/O	I/O	68	I/O	I/O
34	I/O	I/O			
35	I/O	I/O			

PL84

84-Pin
PLCC

1 84

PL84				
Pin Number	**A40MX04 Function**	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
1	I/O	I/O	I/O	I/O
2	I/O	CLKB, I/O	CLKB, I/O	CLKB, I/O
3	I/O	I/O	I/O	I/O
4	VCC	PRB, I/O	PRB, I/O	PRB, I/O
5	I/O	I/O	I/O	WD, I/O
6	I/O	GND	GND	GND
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	WD, I/O
9	I/O	I/O	I/O	WD, I/O
10	I/O	DCLK, I/O	DCLK, I/O	DCLK, I/O
11	I/O	I/O	I/O	I/O
12	NC	MODE	MODE	MODE
13	I/O	I/O	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	I/O	I/O	I/O	I/O
18	GND	I/O	I/O	I/O
19	GND	I/O	I/O	I/O
20	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	VCCA	VCCI	VCCI
23	I/O	VCCI	VCCA	VCCA
24	I/O	I/O	I/O	I/O
25	VCC	I/O	I/O	I/O
26	VCC	I/O	I/O	I/O
27	I/O	I/O	I/O	I/O
28	I/O	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	I/O	I/O	I/O	I/O
31	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	VCC	I/O	I/O	I/O
34	I/O	I/O	I/O	TMS, I/O
35	I/O	I/O	I/O	TDI, I/O
36	I/O	I/O	I/O	WD, I/O

PL84			
Pin Number	**A40MX04 Function**	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	WD, I/O
39	I/O	I/O	I/O	WD, I/O
40	GND	I/O	I/O	I/O
41	I/O	I/O	I/O	I/O
42	I/O	I/O	I/O	I/O
43	I/O	VCCA	VCCA	VCCA
44	I/O	I/O	I/O	WD, I/O
45	I/O	I/O	I/O	WD, I/O
46	VCC	I/O	I/O	WD, I/O
47	I/O	I/O	I/O	WD, I/O
48	I/O	I/O	I/O	I/O
49	I/O	GND	GND	GND
50	I/O	I/O	I/O	WD, I/O
51	I/O	I/O	I/O	WD, I/O
52	I/O	SDO, I/O	SDO, I/O	SDO, TDO, I/O
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	GND	I/O	I/O	I/O
61	GND	I/O	I/O	I/O
62	I/O	I/O	I/O	TCK, I/O
63	I/O	LP	LP	LP
64	CLK, I/O	VCCA	VCCA	VCCA
65	I/O	VCCI	VCCI	VCCI
66	MODE	I/O	I/O	I/O
67	VCC	I/O	I/O	I/O
68	VCC	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	I/O	GND	GND	GND
71	I/O	I/O	I/O	I/O
72	SDI, I/O	I/O	I/O	I/O

PL84				
Pin Number	**A40MX04 Function**	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
73	DCLK, I/O	I/O	I/O	I/O
74	PRA, I/O	I/O	I/O	I/O
75	PRB, I/O	I/O	I/O	I/O
76	I/O	SDI, I/O	SDI, I/O	SDI, I/O
77	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	WD, I/O
79	I/O	I/O	I/O	WD, I/O
80	I/O	I/O	I/O	WD, I/O
81	I/O	PRA, I/O	PRA, I/O	PRA, I/O
82	GND	I/O	I/O	I/O
83	I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O
84	I/O	VCCA	VCCA	VCCA

PQ100

100-Pin
PQFP

100
1

Revision 14
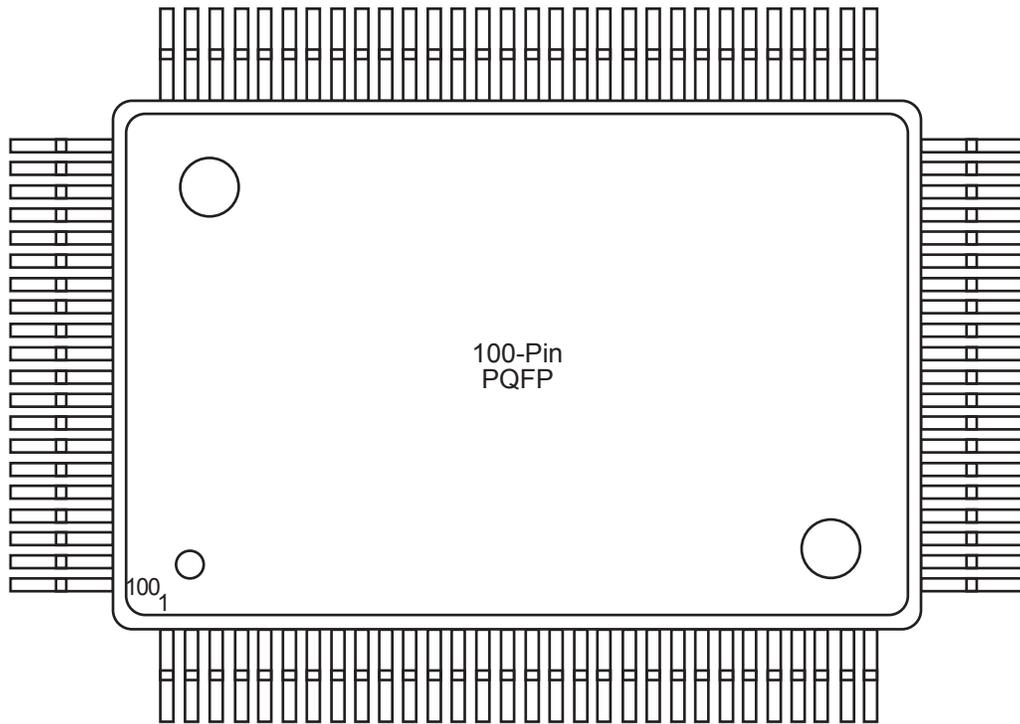
PQ100				
Pin Number	**A40MX02 Function**	**A40MX04 Function**	**A42MX09 Function**	**A42MX16 Function**
1	NC	NC	I/O	I/O
2	NC	NC	DCLK, I/O	DCLK, I/O
3	NC	NC	I/O	I/O
4	NC	NC	MODE	MODE
5	NC	NC	I/O	I/O
6	PRB, I/O	PRB, I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	GND	GND
10	I/O	I/O	I/O	I/O
11	I/O	I/O	I/O	I/O
12	I/O	I/O	I/O	I/O
13	GND	GND	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	VCCA	VCCA
17	I/O	I/O	VCCI	VCCA
18	I/O	I/O	I/O	I/O
19	VCC	V_{CC}	I/O	I/O
20	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	I/O	GND	GND
23	I/O	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	I/O	I/O	I/O	I/O
26	I/O	I/O	I/O	I/O
27	NC	NC	I/O	I/O
28	NC	NC	I/O	I/O
29	NC	NC	I/O	I/O
30	NC	NC	I/O	I/O
31	NC	I/O	I/O	I/O
32	NC	I/O	I/O	I/O
33	NC	I/O	I/O	I/O
34	I/O	I/O	GND	GND
35	I/O	I/O	I/O	I/O
36	GND	GND	I/O	I/O

PQ100				
Pin Number	A40MX02 Function	A40MX04 Function	A42MX09 Function	A42MX16 Function
37	GND	GND	I/O	I/O
38	I/O	I/O	I/O	I/O
39	I/O	I/O	I/O	I/O
40	I/O	I/O	VCCA	VCCA
41	I/O	I/O	I/O	I/O
42	I/O	I/O	I/O	I/O
43	VCC	VCC	I/O	I/O
44	VCC	VCC	I/O	I/O
45	I/O	I/O	I/O	I/O
46	I/O	I/O	GND	GND
47	I/O	I/O	I/O	I/O
48	NC	I/O	I/O	I/O
49	NC	I/O	I/O	I/O
50	NC	I/O	I/O	I/O
51	NC	NC	I/O	I/O
52	NC	NC	SDO, I/O	SDO, I/O
53	NC	NC	I/O	I/O
54	NC	NC	I/O	I/O
55	NC	NC	I/O	I/O
56	VCC	VCC	I/O	I/O
57	I/O	I/O	GND	GND
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	I/O	I/O	I/O	I/O
61	I/O	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	GND	GND	I/O	I/O
64	I/O	I/O	LP	LP
65	I/O	I/O	VCCA	VCCA
66	I/O	I/O	VCCI	VCCI
67	I/O	I/O	VCCA	VCCA
68	I/O	I/O	I/O	I/O
69	VCC	VCC	I/O	I/O
70	I/O	I/O	I/O	I/O
71	I/O	I/O	I/O	I/O
72	I/O	I/O	GND	GND

PQ100				
Pin Number	A40MX02 Function	A40MX04 Function	A42MX09 Function	A42MX16 Function
73	I/O	I/O	I/O	I/O
74	I/O	I/O	I/O	I/O
75	I/O	I/O	I/O	I/O
76	I/O	I/O	I/O	I/O
77	NC	NC	I/O	I/O
78	NC	NC	I/O	I/O
79	NC	NC	SDI, I/O	SDI, I/O
80	NC	I/O	I/O	I/O
81	NC	I/O	I/O	I/O
82	NC	I/O	I/O	I/O
83	I/O	I/O	I/O	I/O
84	I/O	I/O	GND	GND
85	I/O	I/O	I/O	I/O
86	GND	GND	I/O	I/O
87	GND	GND	PRA, I/O	PRA, I/O
88	I/O	I/O	I/O	I/O
89	I/O	I/O	CLKA, I/O	CLKA, I/O
90	CLK, I/O	CLK, I/O	VCCA	VCCA
91	I/O	I/O	I/O	I/O
92	MODE	MODE	CLKB, I/O	CLKB, I/O
93	VCC	VCC	I/O	I/O
94	VCC	VCC	PRB, I/O	PRB, I/O
95	NC	I/O	I/O	I/O
96	NC	I/O	GND	GND
97	NC	I/O	I/O	I/O
98	SDI, I/O	SDI, I/O	I/O	I/O
99	DCLK, I/O	DCLK, I/O	I/O	I/O
100	PRA, I/O	PRA, I/O	I/O	I/O

PQ144

144
1

**144-Pin
PQFP**

PQ144		PQ144		PQ144	
Pin Number	**A42MX09 Function**	**Pin Number**	**A42MX09 Function**	**Pin Number**	**A42MX09 Function**
1	I/O	37	BININ	73	I/O
2	MODE	38	BINOUT	74	I/O
3	I/O	39	I/O	75	I/O
4	I/O	40	I/O	76	I/O
5	I/O	41	I/O	77	I/O
6	I/O	42	I/O	78	I/O
7	I/O	43	I/O	79	GNDQ
8	I/O	44	GNDQ	80	GNDI
9	GNDQ	45	GNDI	81	NC
10	GNDI	46	NC	82	I/O
11	NC	47	I/O	83	I/O
12	I/O	48	I/O	84	I/O
13	I/O	49	I/O	85	I/O
14	I/O	50	I/O	86	I/O
15	I/O	51	I/O	87	I/O
16	I/O	52	I/O	88	VKS
17	I/O	53	I/O	89	VPP
18	VSV	54	VCC	90	VCC
19	VCC	55	VCCI	91	VCCI
20	VCCI	56	NC	92	NC
21	NC	57	I/O	93	VSV
22	I/O	58	I/O	94	I/O
23	I/O	59	I/O	95	I/O
24	I/O	60	I/O	96	I/O
25	I/O	61	I/O	97	I/O
26	I/O	62	I/O	98	I/O
27	I/O	63	I/O	99	I/O
28	GND	64	GND	100	GND
29	GNDI	65	GNDI	101	GNDI
30	NC	66	I/O	102	NC
31	I/O	67	I/O	103	I/O
32	I/O	68	I/O	104	I/O
33	I/O	69	I/O	105	I/O
34	I/O	70	I/O	106	I/O
35	I/O	71	SDO	107	I/O
36	I/O	72	I/O	108	I/O

PQ144	
Pin Number	**A42MX09 Function**
109	I/O
110	SDI
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	GNDQ
117	GNDI
118	NC
119	I/O
120	I/O
121	I/O
122	I/O
123	PROBA
124	I/O
125	CLKA
126	VCC
127	VCCI
128	NC
129	I/O
130	CLKB
131	I/O
132	PROBB
133	I/O
134	I/O
135	I/O
136	GND
137	GNDI
138	NC
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	DCLK

PQ160
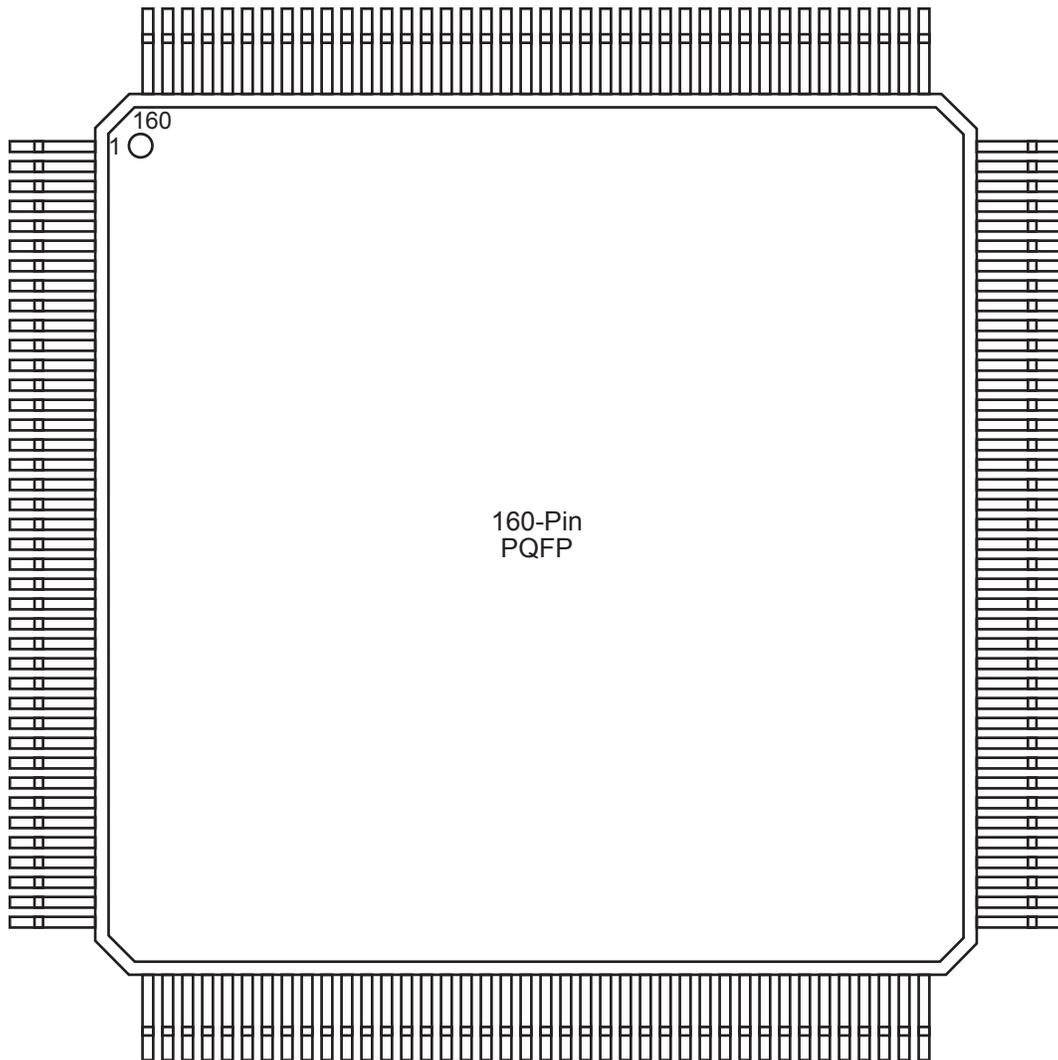
160-Pin
PQFP

PQ160			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
1	I/O	I/O	I/O
2	DCLK, I/O	DCLK, I/O	DCLK, I/O
3	NC	I/O	I/O
4	I/O	I/O	WD, I/O
5	I/O	I/O	WD, I/O
6	NC	VCCI	VCCI
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	NC	I/O	I/O
11	GND	GND	GND
12	NC	I/O	I/O
13	I/O	I/O	WD, I/O
14	I/O	I/O	WD, I/O
15	I/O	I/O	I/O
16	PRB, I/O	PRB, I/O	PRB, I/O
17	I/O	I/O	I/O
18	CLKB, I/O	CLKB, I/O	CLKB, I/O
19	I/O	I/O	I/O
20	VCCA	VCCA	VCCA
21	CLKA, I/O	CLKA, I/O	CLKA, I/O
22	I/O	I/O	I/O
23	PRA, I/O	PRA, I/O	PRA, I/O
24	NC	I/O	WD, I/O
25	I/O	I/O	WD, I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	NC	I/O	I/O
29	I/O	I/O	WD, I/O
30	GND	GND	GND
31	NC	I/O	WD, I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	NC	VCCI	VCCI
36	I/O	I/O	WD, I/O

PQ160			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
37	I/O	I/O	WD, I/O
38	SDI, I/O	SDI, I/O	SDI, I/O
39	I/O	I/O	I/O
40	GND	GND	GND
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	GND	GND	GND
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	NC	I/O	I/O
53	I/O	I/O	I/O
54	NC	VCCA	VCCA
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	VCCA	VCCA	VCCA
58	VCCI	VCCI	VCCI
59	GND	GND	GND
60	VCCA	VCCA	VCCA
61	LP	LP	LP
62	I/O	I/O	TCK, I/O
63	I/O	I/O	I/O
64	GND	GND	GND
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	I/O	I/O	I/O
69	GND	GND	GND
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O

PQ160			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	I/O	I/O	I/O
77	NC	I/O	I/O
78	I/O	I/O	I/O
79	NC	I/O	I/O
80	GND	GND	GND
81	I/O	I/O	I/O
82	SDO, I/O	SDO, I/O	SDO, TDO, I/O
83	I/O	I/O	WD, I/O
84	I/O	I/O	WD, I/O
85	I/O	I/O	I/O
86	NC	VCCI	VCCI
87	I/O	I/O	I/O
88	I/O	I/O	WD, I/O
89	GND	GND	GND
90	NC	I/O	I/O
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	WD, I/O
97	I/O	I/O	I/O
98	VCCA	VCCA	VCCA
99	GND	GND	GND
100	NC	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	NC	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	WD, I/O
107	I/O	I/O	WD, I/O
108	I/O	I/O	I/O

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
109	GND	GND	GND
110	NC	I/O	I/O
111	I/O	I/O	WD, I/O
112	I/O	I/O	WD, I/O
113	I/O	I/O	I/O
114	NC	VCCI	VCCI
115	I/O	I/O	WD, I/O
116	NC	I/O	WD, I/O
117	I/O	I/O	I/O
118	I/O	I/O	TDI, I/O
119	I/O	I/O	TMS, I/O
120	GND	GND	GND
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	NC	I/O	I/O
125	GND	GND	GND
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	NC	I/O	I/O
130	GND	GND	GND
131	I/O	I/O	I/O
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	VCCA	VCCA
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	VCCA	VCCA
139	VCCI	VCCI	VCCI
140	GND	GND	GND
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O

PQ160			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
145	GND	GND	GND
146	NC	I/O	I/O
147	I/O	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	NC	VCCA	VCCA
151	NC	I/O	I/O
152	NC	I/O	I/O
153	NC	I/O	I/O
154	NC	I/O	I/O
155	GND	GND	GND
156	I/O	I/O	I/O
157	I/O	I/O	I/O
158	I/O	I/O	I/O
159	MODE	MODE	MODE
160	GND	GND	GND

PQ208

208-Pin PQFP
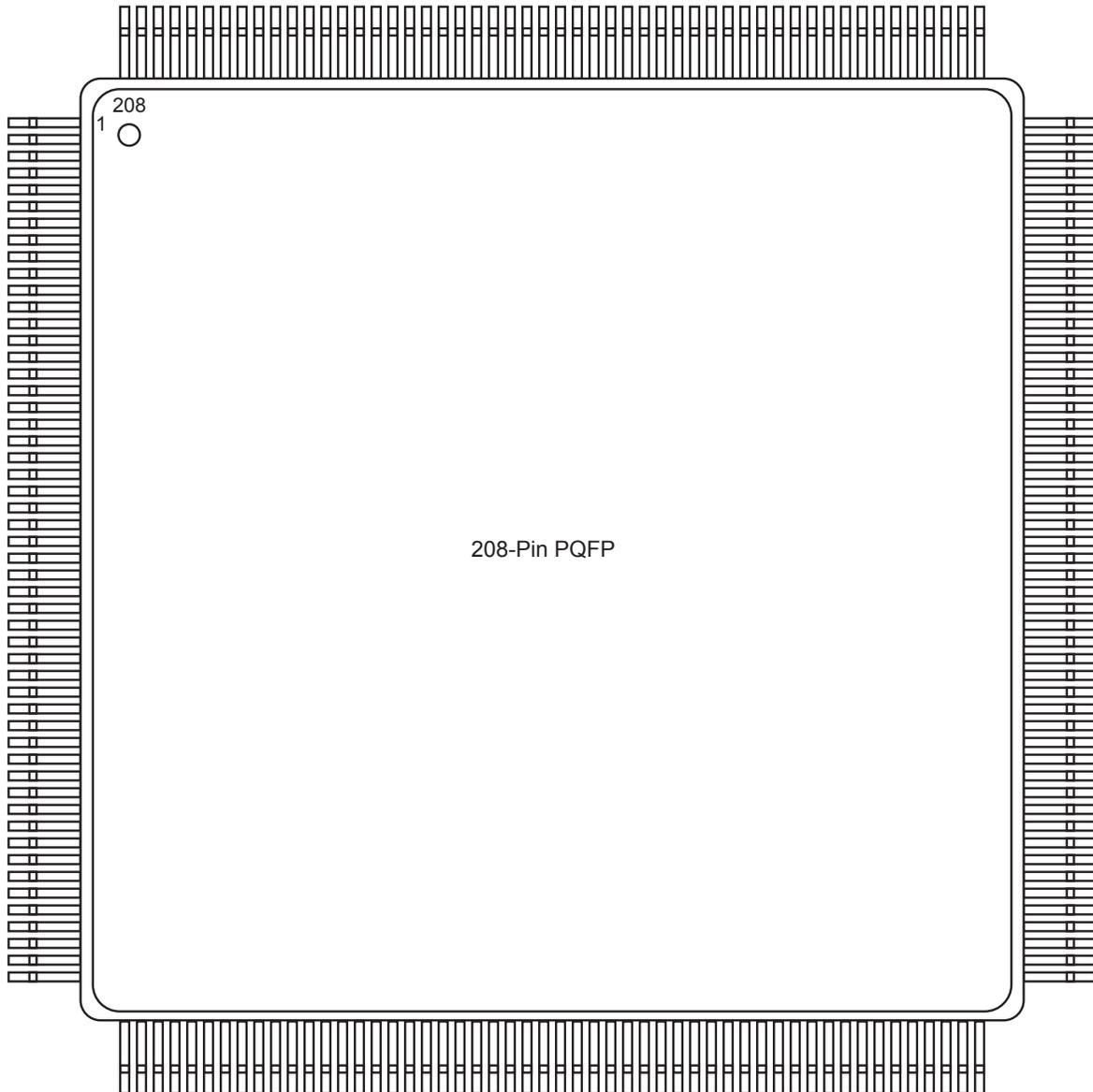
PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
1	GND	GND	GND
2	NC	VCCA	VCCA
3	MODE	MODE	MODE
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	NC	I/O	I/O
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	NC	I/O	I/O
17	VCCA	VCCA	VCCA
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O
21	I/O	I/O	I/O
22	GND	GND	GND
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	GND	GND	GND
28	VCCI	VCCI	VCCI
29	VCCA	VCCA	VCCA
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	VCCA	VCCA	VCCA
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	NC	I/O	I/O
42	NC	I/O	I/O
43	NC	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	NC	I/O	I/O
52	GND	GND	GND
53	GND	GND	GND
54	I/O	TMS, I/O	TMS, I/O
55	I/O	TDI, I/O	TDI, I/O
56	I/O	I/O	I/O
57	I/O	WD, I/O	WD, I/O
58	I/O	WD, I/O	WD, I/O
59	I/O	I/O	I/O
60	VCCI	VCCI	VCCI
61	NC	I/O	I/O
62	NC	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	QCLKA, I/O
66	I/O	WD, I/O	WD, I/O
67	NC	WD, I/O	WD, I/O
68	NC	I/O	I/O
69	I/O	I/O	I/O
70	I/O	WD, I/O	WD, I/O
71	I/O	WD, I/O	WD, I/O
72	I/O	I/O	I/O

PQ208			
Pin Number	**A42MX16 Function**	**A42MX24 Function**	**A42MX36 Function**
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	GND	GND	GND
79	VCCA	VCCA	VCCA
80	NC	VCCI	VCCI
81	I/O	I/O	I/O
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	WD, I/O	WD, I/O
86	I/O	WD, I/O	WD, I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	NC	I/O	I/O
90	NC	I/O	I/O
91	I/O	I/O	QCLKB, I/O
92	I/O	I/O	I/O
93	I/O	WD, I/O	WD, I/O
94	I/O	WD, I/O	WD, I/O
95	NC	I/O	I/O
96	NC	I/O	I/O
97	NC	I/O	I/O
98	VCCI	VCCI	VCCI
99	I/O	I/O	I/O
100	I/O	WD, I/O	WD, I/O
101	I/O	WD, I/O	WD, I/O
102	I/O	I/O	I/O
103	SDO, I/O	SDO, TDO, I/O	SDO, TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	VCCA	VCCA
107	I/O	I/O	I/O
108	I/O	I/O	I/O

PQ208			
Pin Number	**A42MX16 Function**	**A42MX24 Function**	**A42MX36 Function**
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	NC	I/O	I/O
113	NC	I/O	I/O
114	NC	I/O	I/O
115	NC	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	I/O	I/O	I/O
126	GND	GND	GND
127	I/O	I/O	I/O
128	I/O	TCK, I/O	TCK, I/O
129	LP	LP	LP
130	VCCA	VCCA	VCCA
131	GND	GND	GND
132	VCCI	VCCI	VCCI
133	VCCA	VCCA	VCCA
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	VCCA	VCCA	VCCA
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	I/O	I/O	I/O
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O

PQ208			
Pin Number	**A42MX16 Function**	**A42MX24 Function**	**A42MX36 Function**
145	I/O	I/O	I/O
146	NC	I/O	I/O
147	NC	I/O	I/O
148	NC	I/O	I/O
149	NC	I/O	I/O
150	GND	GND	GND
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	I/O	I/O	I/O
156	I/O	I/O	I/O
157	GND	GND	GND
158	I/O	I/O	I/O
159	SDI, I/O	SDI, I/O	SDI, I/O
160	I/O	I/O	I/O
161	I/O	WD, I/O	WD, I/O
162	I/O	WD, I/O	WD, I/O
163	I/O	I/O	I/O
164	VCCI	VCCI	VCCI
165	NC	I/O	I/O
166	NC	I/O	I/O
167	I/O	I/O	I/O
168	I/O	WD, I/O	WD, I/O
169	I/O	WD, I/O	WD, I/O
170	I/O	I/O	I/O
171	NC	I/O	QCLKD, I/O
172	I/O	I/O	I/O
173	I/O	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	I/O	WD, I/O	WD, I/O
177	I/O	WD, I/O	WD, I/O
178	PRA, I/O	PRA, I/O	PRA, I/O
179	I/O	I/O	I/O
180	CLKA, I/O	CLKA, I/O	CLKA, I/O

PQ208			
Pin Number	**A42MX16 Function**	**A42MX24 Function**	**A42MX36 Function**
181	NC	I/O	I/O
182	NC	VCCI	VCCI
183	VCCA	VCCA	VCCA
184	GND	GND	GND
185	I/O	I/O	I/O
186	CLKB, I/O	CLKB, I/O	CLKB, I/O
187	I/O	I/O	I/O
188	PRB, I/O	PRB, I/O	PRB, I/O
189	I/O	I/O	I/O
190	I/O	WD, I/O	WD, I/O
191	I/O	WD, I/O	WD, I/O
192	I/O	I/O	I/O
193	NC	I/O	I/O
194	NC	WD, I/O	WD, I/O
195	NC	WD, I/O	WD, I/O
196	I/O	I/O	QCLKC, I/O
197	NC	I/O	I/O
198	I/O	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	NC	I/O	I/O
202	VCCI	VCCI	VCCI
203	I/O	WD, I/O	WD, I/O
204	I/O	WD, I/O	WD, I/O
205	I/O	I/O	I/O
206	I/O	I/O	I/O
207	DCLK, I/O	DCLK, I/O	DCLK, I/O
208	I/O	I/O	I/O

PQ240

Note: 240-Pin PQFP Package (Top View)

PQ240		PQ240		PQ240	
Pin Number	**A42MX36 Function**	**Pin Number**	**A42MX36 Function**	**Pin Number**	**A42MX36 Function**
1	I/O	37	WD, I/O	73	I/O
2	DCLK, I/O	38	WD, I/O	74	I/O
3	I/O	39	I/O	75	I/O
4	I/O	40	I/O	76	I/O
5	I/O	41	I/O	77	I/O
6	WD, I/O	42	I/O	78	I/O
7	WD, I/O	43	I/O	79	I/O
8	VCCI	44	I/O	80	I/O
9	I/O	45	QCLKD, I/O	81	I/O
10	I/O	46	I/O	82	I/O
11	I/O	47	WD, I/O	83	I/O
12	I/O	48	WD, I/O	84	I/O
13	I/O	49	I/O	85	VCCA
14	I/O	50	I/O	86	I/O
15	QCLKC, I/O	51	I/O	87	I/O
16	I/O	52	VCCI	88	VCCA
17	WD, I/O	53	I/O	89	VCCI
18	WD, I/O	54	WD, I/O	90	VCCA
19	I/O	55	WD, I/O	91	LP
20	I/O	56	I/O	92	TCK, I/O
21	WD, I/O	57	SDI, I/O	93	I/O
22	WD, I/O	58	I/O	94	GND
23	I/O	59	VCCA	95	I/O
24	PRB, I/O	60	GND	96	I/O
25	I/O	61	GND	97	I/O
26	CLKB, I/O	62	I/O	98	I/O
27	I/O	63	I/O	99	I/O
28	GND	64	I/O	100	I/O
29	VCCA	65	I/O	101	I/O
30	VCCI	66	I/O	102	I/O
31	I/O	67	I/O	103	I/O
32	CLKA, I/O	68	I/O	104	I/O
33	I/O	69	I/O	105	I/O
34	PRA, I/O	70	I/O	106	I/O
35	I/O	71	VCCI	107	I/O
36	I/O	72	I/O	108	VCCI

PQ240		PQ240		PQ240	
Pin Number	**A42MX36 Function**	**Pin Number**	**A42MX36 Function**	**Pin Number**	**A42MX36 Function**
109	I/O	145	I/O	181	VCCA
110	I/O	146	I/O	182	GND
111	I/O	147	I/O	183	I/O
112	I/O	148	I/O	184	I/O
113	I/O	149	I/O	185	I/O
114	I/O	150	VCCI	186	I/O
115	I/O	151	VCCA	187	I/O
116	I/O	152	GND	188	I/O
117	I/O	153	I/O	189	I/O
118	VCCA	154	I/O	190	I/O
119	GND	155	I/O	191	I/O
120	GND	156	I/O	192	VCCI
121	GND	157	I/O	193	I/O
122	I/O	158	I/O	194	I/O
123	SDO, TDO, I/O	159	WD, I/O	195	I/O
124	I/O	160	WD, I/O	196	I/O
125	WD, I/O	161	I/O	197	I/O
126	WD, I/O	162	I/O	198	I/O
127	I/O	163	WD, I/O	199	I/O
128	VCCI	164	WD, I/O	200	I/O
129	I/O	165	I/O	201	I/O
130	I/O	166	QCLKA, I/O	202	I/O
131	I/O	167	I/O	203	I/O
132	WD, I/O	168	I/O	204	I/O
133	WD, I/O	169	I/O	205	I/O
134	I/O	170	I/O	206	VCCA
135	QCLKB, I/O	171	I/O	207	I/O
136	I/O	172	VCCI	208	I/O
137	I/O	173	I/O	209	VCCA
138	I/O	174	WD, I/O	210	VCCI
139	I/O	175	WD, I/O	211	I/O
140	I/O	176	I/O	212	I/O
141	I/O	177	I/O	213	I/O
142	WD, I/O	178	TDI, I/O	214	I/O
143	WD, I/O	179	TMS, I/O	215	I/O
144	I/O	180	GND	216	I/O

PQ240	
Pin Number	**A42MX36 Function**
217	I/O
218	I/O
219	VCCA
220	I/O
221	I/O
222	I/O
223	I/O
224	I/O
225	I/O
226	I/O
227	VCCI
228	I/O
229	I/O
230	I/O
231	I/O
232	I/O
233	I/O
234	I/O
235	I/O
236	I/O
237	GND
238	MODE
239	VCCA
240	GND

VQ80

80-Pin
VQFP

VQ80			VQ80			VQ80		
Pin Number	**A40MX02 Function**	**A40MX04 Function**	**Pin Number**	**A40MX02 Function**	**A40MX04 Function**	**Pin Number**	**A40MX02 Function**	**A40MX04 Function**
1	I/O	I/O	28	I/O	I/O	55	NC	I/O
2	NC	I/O	29	I/O	I/O	56	NC	I/O
3	NC	I/O	30	I/O	I/O	57	SDI, I/O	SDI, I/O
4	NC	I/O	31	I/O	I/O	58	DCLK, I/O	DCLK, I/O
5	I/O	I/O	32	I/O	I/O	59	PRA, I/O	PRA, I/O
6	I/O	I/O	33	VCC	VCC	60	NC	NC
7	GND	GND	34	I/O	I/O	61	PRB, I/O	PRB, I/O
8	I/O	I/O	35	I/O	I/O	62	I/O	I/O
9	I/O	I/O	36	I/O	I/O	63	I/O	I/O
10	I/O	I/O	37	I/O	I/O	64	I/O	I/O
11	I/O	I/O	38	I/O	I/O	65	I/O	I/O
12	I/O	I/O	39	I/O	I/O	66	I/O	I/O
13	VCC	VCC	40	I/O	I/O	67	I/O	I/O
14	I/O	I/O	41	NC	I/O	68	GND	GND
15	I/O	I/O	42	NC	I/O	69	I/O	I/O
16	I/O	I/O	43	NC	I/O	70	I/O	I/O
17	NC	I/O	44	I/O	I/O	71	I/O	I/O
18	NC	I/O	45	I/O	I/O	72	I/O	I/O
19	NC	I/O	46	I/O	I/O	73	I/O	I/O
20	VCC	VCC	47	GND	GND	74	VCC	**VCC**
21	I/O	I/O	48	I/O	I/O	75	I/O	I/O
22	I/O	I/O	49	I/O	I/O	76	I/O	I/O
23	I/O	I/O	50	CLK, I/O	CLK, I/O	77	I/O	I/O
24	I/O	I/O	51	I/O	I/O	78	I/O	I/O
25	I/O	I/O	52	MODE	MODE	79	I/O	I/O
26	I/O	I/O	53	VCC	VCC	80	I/O	I/O
27	GND	GND	54	NC	I/O			

VQ100

100

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100-Pin
VQFP

VQ100			VQ100			VQ100		
Pin Number	A42MX09 Function	A42MX16 Function	Pin Number	A42MX09 Function	A42MX16 Function	Pin Number	A42MX09 Function	A42MX16 Function
1	I/O	I/O	36	I/O	I/O	71	I/O	I/O
2	MODE	MODE	37	I/O	I/O	72	I/O	I/O
3	I/O	I/O	38	VCCA	VCCA	73	I/O	I/O
4	I/O	I/O	39	I/O	I/O	74	I/O	I/O
5	I/O	I/O	40	I/O	I/O	75	I/O	I/O
6	I/O	I/O	41	I/O	I/O	76	I/O	I/O
7	GND	GND	42	I/O	I/O	77	SDI, I/O	SDI, I/O
8	I/O	I/O	43	I/O	I/O	78	I/O	I/O
9	I/O	I/O	44	GND	GND	79	I/O	I/O
10	I/O	I/O	45	I/O	I/O	80	I/O	I/O
11	I/O	I/O	46	I/O	I/O	81	I/O	I/O
12	I/O	I/O	47	I/O	I/O	82	GND	GND
13	I/O	I/O	48	I/O	I/O	83	I/O	I/O
14	VCCA	NC	49	I/O	I/O	84	I/O	I/O
15	VCCI	VCCI	50	SDO, I/O	SDO, I/O	85	PRA, I/O	PRA, I/O
16	I/O	I/O	51	I/O	I/O	86	I/O	I/O
17	I/O	I/O	52	I/O	I/O	87	CLKA, I/O	CLKA, I/O
18	I/O	I/O	53	I/O	I/O	88	VCCA	VCCA
19	I/O	I/O	54	I/O	I/O	89	I/O	I/O
20	GND	GND	55	GND	GND	90	CLKB, I/O	CLKB, I/O
21	I/O	I/O	56	I/O	I/O	91	I/O	I/O
22	I/O	I/O	57	I/O	I/O	92	PRB, I/O	PRB, I/O
23	I/O	I/O	58	I/O	I/O	93	I/O	I/O
24	I/O	I/O	59	I/O	I/O	94	GND	GND
25	I/O	I/O	60	I/O	I/O	95	I/O	I/O
26	I/O	I/O	61	I/O	I/O	96	I/O	I/O
27	I/O	I/O	62	LP	LP	97	I/O	I/O
28	I/O	I/O	63	VCCA	VCCA	98	I/O	I/O
29	I/O	I/O	64	VCCI	VCCI	99	I/O	I/O
30	I/O	I/O	65	VCCA	VCCA	100	DCLK, I/O	DCLK, I/O
31	I/O	I/O	66	I/O	I/O			
32	GND	GND	67	I/O	I/O			
33	I/O	I/O	68	I/O	I/O			
34	I/O	I/O	69	I/O	I/O			
35	I/O	I/O	70	GND	GND			

TQ176

176-Pin
TQFP

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
1	GND	GND	GND
2	MODE	MODE	MODE
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	NC	NC	I/O
9	I/O	I/O	I/O
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	NC	VCCA	VCCA
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	GND	GND	GND
19	NC	I/O	I/O
20	NC	I/O	I/O
21	I/O	I/O	I/O
22	NC	I/O	I/O
23	GND	GND	GND
24	NC	VCCI	VCCI
25	VCCA	VCCA	VCCA
26	NC	I/O	I/O
27	NC	I/O	I/O
28	VCCI	VCCA	VCCA
29	NC	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	NC	NC	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O

TQ176			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
37	NC	I/O	I/O
38	NC	NC	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	I/O	I/O	I/O
45	GND	GND	GND
46	I/O	I/O	TMS, I/O
47	I/O	I/O	TDI, I/O
48	I/O	I/O	I/O
49	I/O	I/O	WD, I/O
50	I/O	I/O	WD, I/O
51	I/O	I/O	I/O
52	NC	VCCI	VCCI
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	NC	I/O	WD, I/O
56	I/O	I/O	WD, I/O
57	NC	NC	I/O
58	I/O	I/O	I/O
59	I/O	I/O	WD, I/O
60	I/O	I/O	WD, I/O
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	NC	I/O	I/O
65	I/O	I/O	I/O
66	NC	I/O	I/O
67	GND	GND	GND
68	VCCA	VCCA	VCCA
69	I/O	I/O	WD, I/O
70	I/O	I/O	WD, I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O

TQ176			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
73	I/O	I/O	I/O
74	NC	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	NC	NC	WD, I/O
78	NC	I/O	WD, I/O
79	I/O	I/O	I/O
80	NC	I/O	I/O
81	I/O	I/O	I/O
82	NC	VCCI	VCCI
83	I/O	I/O	I/O
84	I/O	I/O	WD, I/O
85	I/O	I/O	WD, I/O
86	NC	I/O	I/O
87	SDO, I/O	SDO, I/O	SDO, TDO, I/O
88	I/O	I/O	I/O
89	GND	GND	GND
90	I/O	I/O	I/O
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	NC	I/O	I/O
97	NC	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	I/O	I/O	I/O
101	NC	NC	I/O
102	I/O	I/O	I/O
103	NC	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	GND	GND	GND
107	NC	I/O	I/O
108	NC	I/O	TCK, I/O

TQ176			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
109	LP	LP	LP
110	VCCA	VCCA	VCCA
111	GND	GND	GND
112	VCCI	VCCI	VCCI
113	VCCA	VCCA	VCCA
114	NC	I/O	I/O
115	NC	I/O	I/O
116	NC	VCCA	VCCA
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	NC	NC	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	NC	I/O	I/O
125	NC	I/O	I/O
126	NC	NC	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	I/O	I/O	I/O
130	I/O	I/O	I/O
131	I/O	I/O	I/O
132	I/O	I/O	I/O
133	GND	GND	GND
134	I/O	I/O	I/O
135	SDI, I/O	SDI, I/O	SDI, I/O
136	NC	I/O	I/O
137	I/O	I/O	WD, I/O
138	I/O	I/O	WD, I/O
139	I/O	I/O	I/O
140	NC	VCCI	VCCI
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	NC	I/O	I/O
144	NC	I/O	WD, I/O

TQ176			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
145	NC	NC	WD, I/O
146	I/O	I/O	I/O
147	NC	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	I/O	I/O	WD, I/O
151	NC	I/O	WD, I/O
152	PRA, I/O	PRA, I/O	PRA, I/O
153	I/O	I/O	I/O
154	CLKA, I/O	CLKA, I/O	CLKA, I/O
155	VCCA	VCCA	VCCA
156	GND	GND	GND
157	I/O	I/O	I/O
158	CLKB, I/O	CLKB, I/O	CLKB, I/O
159	I/O	I/O	I/O
160	PRB, I/O	PRB, I/O	PRB, I/O
161	NC	I/O	WD, I/O
162	I/O	I/O	WD, I/O
163	I/O	I/O	I/O
164	I/O	I/O	I/O
165	NC	NC	WD, I/O
166	NC	I/O	WD, I/O
167	I/O	I/O	I/O
168	NC	I/O	I/O
169	I/O	I/O	I/O
170	NC	VCCI	VCCI
171	I/O	I/O	WD, I/O
172	I/O	I/O	WD, I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	DCLK, I/O	DCLK, I/O	DCLK, I/O
176	I/O	I/O	I/O

CQ208
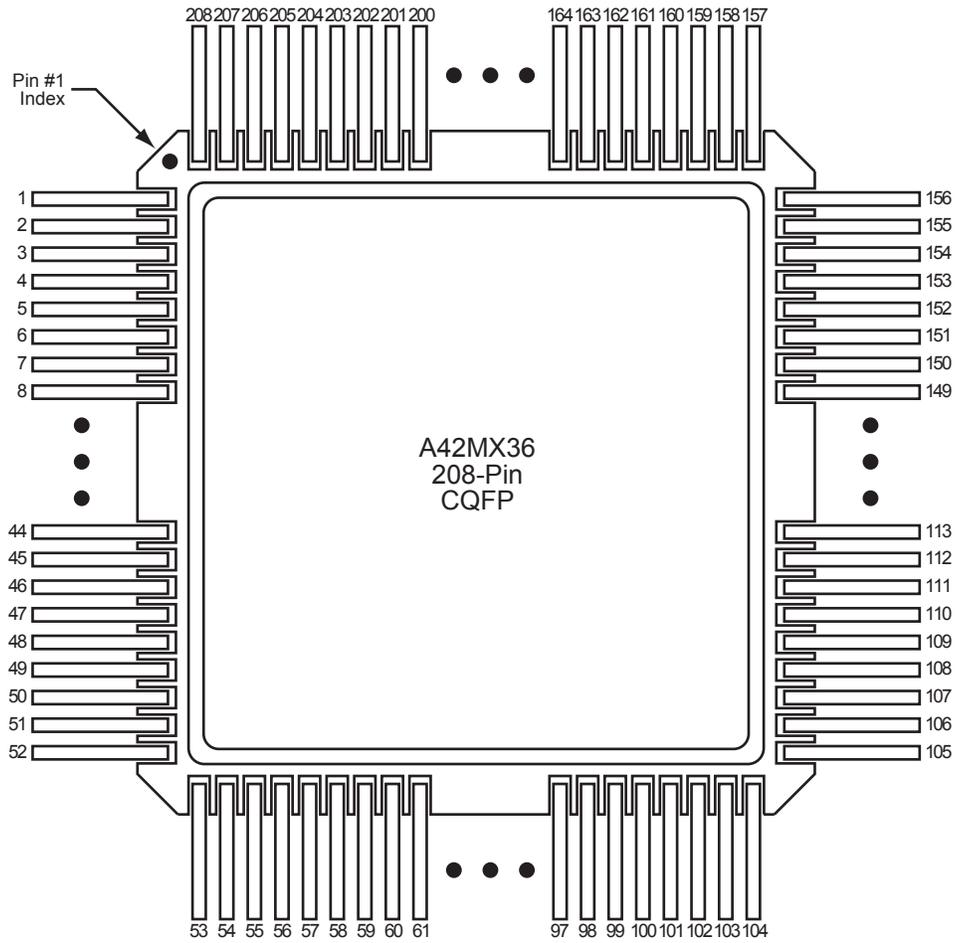
CQ208	
Pin Number	**A42MX36 Function**
1	GND
2	VCCA
3	MODE
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	VCCA
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	VCCI
29	VCCA
30	I/O
31	I/O
32	VCCA
33	I/O
34	I/O
35	I/O
36	I/O

CQ208	
Pin Number	**A42MX36 Function**
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	GND
53	GND
54	TMS, I/O
55	TDI, I/O
56	I/O
57	WD, I/O
58	WD, I/O
59	I/O
60	VCCI
61	I/O
62	I/O
63	I/O
64	I/O
65	QCLKA, I/O
66	WD, I/O
67	WD, I/O
68	I/O
69	I/O
70	WD, I/O
71	WD, I/O
72	I/O

CQ208	
Pin Number	**A42MX36 Function**
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	GND
79	VCCA
80	VCCI
81	I/O
82	I/O
83	I/O
84	I/O
85	WD, I/O
86	WD, I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	QCLKB, I/O
92	I/O
93	WD, I/O
94	WD, I/O
95	I/O
96	I/O
97	I/O
98	VCCI
99	I/O
100	WD, I/O
101	WD, I/O
102	I/O
103	TDO, I/O
104	I/O
105	GND
106	VCCA
107	I/O
108	I/O

CQ208		CQ208		CQ208	
Pin Number	A42MX36 Function	Pin Number	A42MX36 Function	Pin Number	A42MX36 Function
109	I/O	145	I/O	181	I/O
110	I/O	146	I/O	182	VCCI
111	I/O	147	I/O	183	VCCA
112	I/O	148	I/O	184	GND
113	I/O	149	I/O	185	I/O
114	I/O	150	GND	186	CLKB, I/O
115	I/O	151	I/O	187	I/O
116	I/O	152	I/O	188	PRB, I/O
117	I/O	153	I/O	189	I/O
118	I/O	154	I/O	190	WD, I/O
119	I/O	155	I/O	191	WD, I/O
120	I/O	156	I/O	192	I/O
121	I/O	157	GND	193	I/O
122	I/O	158	I/O	194	WD, I/O
123	I/O	159	SDI, I/O	195	WD, I/O
124	I/O	160	I/O	196	QCLKC, I/O
125	I/O	161	WD, I/O	197	I/O
126	GND	162	WD, I/O	198	I/O
127	I/O	163	I/O	199	I/O
128	TCK, I/O	164	VCCI	200	I/O
129	LP	165	I/O	201	I/O
130	VCCA	166	I/O	202	VCCI
131	GND	167	I/O	203	WD, I/O
132	VCCI	168	WD, I/O	204	WD, I/O
133	VCCA	169	WD, I/O	205	I/O
134	I/O	170	I/O	206	I/O
135	I/O	171	QCLKD, I/O	207	DCLK, I/O
136	VCCA	172	I/O	208	I/O
137	I/O	173	I/O		
138	I/O	174	I/O		
139	I/O	175	I/O		
140	I/O	176	WD, I/O		
141	I/O	177	WD, I/O		
142	I/O	178	PRA, I/O		
143	I/O	179	I/O		
144	I/O	180	CLKA, I/O		

CQ256

Pin #1
Index

A42MX36
256-Pin
CQFP

CQ256		CQ256		CQ256	
Pin Number	**A42MX36 Function**	**Pin Number**	**A42MX36 Function**	**Pin Number**	**A42MX36 Function**
1	NC	37	I/O	73	I/O
2	GND	38	I/O	74	I/O
3	I/O	39	I/O	75	I/O
4	I/O	40	I/O	76	WD, I/O
5	I/O	41	I/O	77	GND
6	I/O	42	I/O	78	WD, I/O
7	I/O	43	I/O	79	I/O
8	I/O	44	I/O	80	QCLKB, I/O
9	I/O	45	I/O	81	I/O
10	GND	46	I/O	82	I/O
11	I/O	47	I/O	83	I/O
12	I/O	48	GND	84	I/O
13	I/O	49	I/O	85	I/O
14	I/O	50	I/O	86	I/O
15	I/O	51	I/O	87	WD, I/O
16	I/O	52	I/O	88	WD, I/O
17	I/O	53	I/O	89	I/O
18	I/O	54	I/O	90	I/O
19	I/O	55	I/O	91	I/O
20	I/O	56	I/O	92	I/O
21	I/O	57	I/O	93	I/O
22	I/O	58	I/O	94	I/O
23	I/O	59	I/O	95	VCCI
24	I/O	60	VCCA	96	VCCA
25	I/O	61	GND	97	GND
26	VCCA	62	GND	98	GND
27	I/O	63	NC	99	I/O
28	I/O	64	NC	100	I/O
29	VCCA	65	NC	101	I/O
30	VCCI	66	I/O	102	I/O
31	GND	67	SDO, TDO, I/O	103	I/O
32	VCCA	68	I/O	104	I/O
33	LP	69	WD, I/O	105	WD, I/O
34	TCK, I/O	70	WD, I/O	106	WD, I/O
35	I/O	71	I/O	107	I/O
36	GND	72	VCCI	108	I/O

CQ256	
Pin Number	A42MX36 Function
109	WD, I/O
110	WD, I/O
111	I/O
112	QCLKA, I/O
113	I/O
114	GND
115	I/O
116	I/O
117	I/O
118	I/O
119	VCCI
120	I/O
121	WD, I/O
122	WD, I/O
123	I/O
124	I/O
125	I/O
126	I/O
127	GND
128	NC
129	NC
130	NC
131	GND
132	I/O
133	I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	I/O
139	GND
140	I/O
141	I/O
142	I/O
143	I/O
144	I/O

CQ256	
Pin Number	A42MX36 Function
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	I/O
153	I/O
154	I/O
155	VCCA
156	I/O
157	I/O
158	VCCA
159	VCCI
160	GND
161	I/O
162	I/O
163	I/O
164	I/O
165	GND
166	I/O
167	I/O
168	I/O
169	I/O
170	VCCA
171	I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	I/O
177	I/O
178	I/O
179	I/O
180	GND

CQ256	
Pin Number	A42MX36 Function
181	I/O
182	I/O
183	I/O
184	I/O
185	I/O
186	I/O
187	I/O
188	MODE
189	VCCA
190	GND
191	NC
192	NC
193	NC
194	I/O
195	DCLK, I/O
196	I/O
197	I/O
198	I/O
199	WD, I/O
200	WD, I/O
201	VCCI
202	I/O
203	I/O
204	I/O
205	I/O
206	GND
207	I/O
208	I/O
209	QCLKC, I/O
210	I/O
211	WD, I/O
212	WD, I/O
213	I/O
214	I/O
215	WD, I/O
216	WD, I/O

CQ256	
Pin Number	A42MX36 Function
217	I/O
218	PRB, I/O
219	I/O
220	CLKB, I/O
221	I/O
222	GND
223	GND
224	VCCA
225	VCCI
226	I/O
227	CLKA, I/O
228	I/O
229	PRA, I/O
230	I/O
231	I/O
232	WD, I/O
233	WD, I/O
234	I/O
235	I/O
236	I/O
237	I/O
238	I/O
239	I/O
240	QCLKD, I/O
241	I/O
242	WD, I/O
243	GND
244	WD, I/O
245	I/O
246	I/O
247	I/O
248	VCCI
249	I/O
250	WD, I/O
251	WD, I/O
252	I/O

CQ256	
Pin Number	A42MX36 Function
253	SDI, I/O
254	I/O
255	GND
256	NC

BG272

272-Pin PBGA

BG272		BG272		BG272	
Pin Number	**A42MX36 Function**	**Pin Number**	**A42MX36 Function**	**Pin Number**	**A42MX36 Function**
A1	GND	B17	WD, I/O	D13	I/O
A2	GND	B18	I/O	D14	VCCI
A3	I/O	B19	GND	D15	I/O
A4	WD, I/O	B20	GND	D16	VCCA
A5	I/O	C1	I/O	D17	GND
A6	I/O	C2	MODE	D18	I/O
A7	WD, I/O	C3	GND	D19	I/O
A8	WD, I/O	C4	I/O	D20	I/O
A9	I/O	C5	WD, I/O	E1	I/O
A10	I/O	C6	I/O	E2	I/O
A11	CLKA	C7	QCLKC, I/O	E3	I/O
A12	I/O	C8	I/O	E4	VCCA
A13	I/O	C9	I/O	E17	VCCI
A14	I/O	C10	CLKB	E18	I/O
A15	I/O	C11	PRA, I/O	E19	I/O
A16	WD, I/O	C12	WD, I/O	E20	I/O
A17	I/O	C13	I/O	F1	I/O
A18	I/O	C14	QCLKD, I/O	F2	I/O
A19	GND	C15	I/O	F3	I/O
A20	GND	C16	WD, I/O	F4	VCCI
B1	GND	C17	SDI, I/O	F17	I/O
B2	GND	C18	I/O	F18	I/O
B3	DCLK, I/O	C19	I/O	F19	I/O
B4	I/O	C20	I/O	F20	I/O
B5	I/O	D1	I/O	G1	I/O
B6	I/O	D2	I/O	G2	I/O
B7	WD, I/O	D3	I/O	G3	I/O
B8	I/O	D4	I/O	G4	VCCI
B9	PRB, I/O	D5	VCCI	G17	VCCI
B10	I/O	D6	I/O	G18	I/O
B11	I/O	D7	I/O	G19	I/O
B12	WD, I/O	D8	VCCA	G20	I/O
B13	I/O	D9	WD, I/O	H1	I/O
B14	I/O	D10	VCCI	H2	I/O
B15	WD, I/O	D11	I/O	H3	I/O
B16	I/O	D12	VCCI	H4	VCCA

BG272	
Pin Number	**A42MX36 Function**
H17	I/O
H18	I/O
H19	I/O
H20	I/O
J1	I/O
J2	I/O
J3	I/O
J4	VCCI
J9	GND
J10	GND
J11	GND
J12	GND
J17	VCCA
J18	I/O
J19	I/O
J20	I/O
K1	I/O
K2	I/O
K3	I/O
K4	VCCI
K9	GND
K10	GND
K11	GND
K12	GND
K17	I/O
K18	VCCA
K19	VCCA
K20	LP
L1	I/O
L2	I/O
L3	VCCA
L4	VCCA
L9	GND
L10	GND
L11	GND
L12	GND

BG272	
Pin Number	**A42MX36 Function**
L17	VCCI
L18	I/O
L19	I/O
L20	TCK, I/O
M1	I/O
M2	I/O
M3	I/O
M4	VCCI
M9	GND
M10	GND
M11	GND
M12	GND
M17	I/O
M18	I/O
M19	I/O
M20	I/O
N1	I/O
N2	I/O
N3	I/O
N4	VCCI
N17	VCCI
N18	I/O
N19	I/O
N20	I/O
P1	I/O
P2	I/O
P3	I/O
P4	VCCA
P17	I/O
P18	I/O
P19	I/O
P20	I/O
R1	I/O
R2	I/O
R3	I/O
R4	VCCI

BG272	
Pin Number	**A42MX36 Function**
R17	VCCI
R18	I/O
R19	I/O
R20	I/O
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T17	VCCA
T18	I/O
T19	I/O
T20	I/O
U1	I/O
U2	I/O
U3	I/O
U4	I/O
U5	VCCI
U6	WD, I/O
U7	I/O
U8	I/O
U9	WD, I/O
U10	VCCA
U11	VCCI
U12	I/O
U13	I/O
U14	QCLKB, I/O
U15	I/O
U16	VCCI
U17	I/O
U18	GND
U19	I/O
U20	I/O
V1	I/O
V2	I/O
V3	GND
V4	GND

BG272	
Pin Number	**A42MX36 Function**
V5	I/O
V6	I/O
V7	I/O
V8	WD, I/O
V9	I/O
V10	I/O
V11	I/O
V12	I/O
V13	WD, I/O
V14	I/O
V15	WD, I/O
V16	I/O
V17	I/O
V18	SDO, TDO, I/O
V19	I/O
V20	I/O
W1	GND
W2	GND
W3	I/O
W4	TMS, I/O
W5	I/O
W6	I/O
W7	I/O
W8	WD, I/O
W9	WD, I/O
W10	I/O
W11	I/O
W12	I/O
W13	WD, I/O
W14	I/O
W15	I/O
W16	WD, I/O
W17	I/O
W18	WD, I/O
W19	GND
W20	GND

BG272	
Pin Number	**A42MX36 Function**
Y1	GND
Y2	GND
Y3	I/O
Y4	TDI, I/O
Y5	WD, I/O
Y6	I/O
Y7	QCLKA, I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	I/O
Y13	I/O
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	WD, I/O
Y19	GND
Y20	GND

PG132
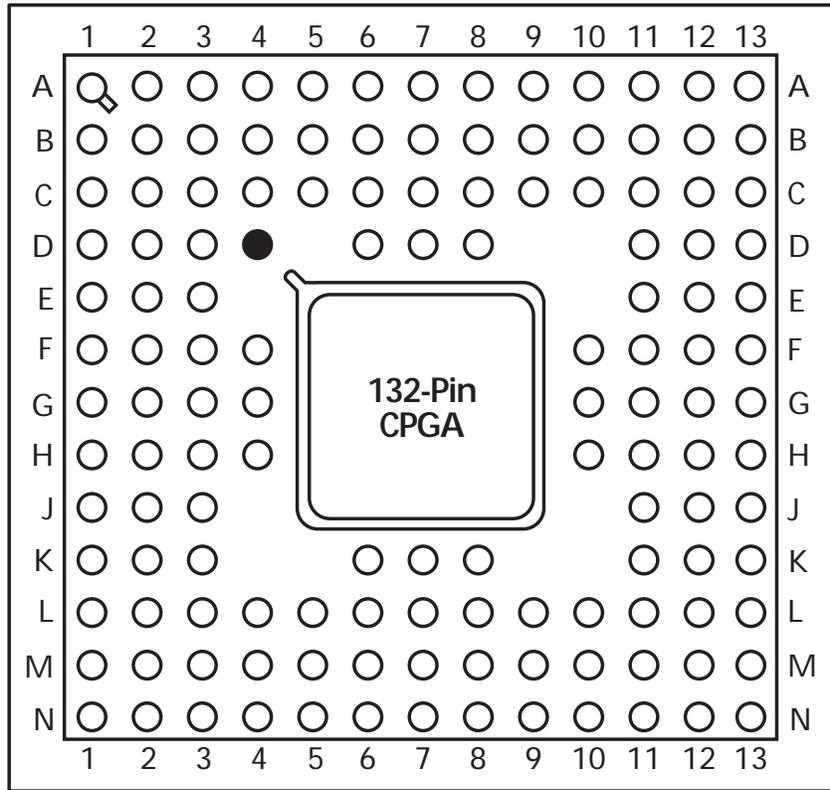
● Orientation Pin

PG132	
Pin Number	A42MX09 Function
–	PMPOUT
B2	I/O
A1	MODE
B1	I/O
D3	I/O
C2	I/O
C1	I/O
D2	I/O
D1	I/O
E2	I/O
E1	I/O
F3	I/O
F2	I/O
F1	I/O
G1	I/O
G4	VSV
H1	I/O
H2	I/O
H3	I/O
H4	I/O
J1	I/O
K1	I/O
L1	I/O
K2	I/O
M1	I/O
K3	I/O
L2	I/O
N1	I/O
L3	BININ
M2	BINOUT
N2	I/O
M3	I/O
L4	I/O
N3	I/O
M4	I/O

PG132	
Pin Number	A42MX09 Function
N4	I/O
M5	I/O
K6	I/O
N5	I/O
N6	I/O
L6	I/O
M6	I/O
M7	I/O
N7	I/O
N8	I/O
M8	I/O
L8	I/O
K8	I/O
N9	I/O
N10	I/O
M10	I/O
N11	I/O
L10	I/O
M11	I/O
N12	SDO
M12	I/O
L11	I/O
N13	I/O
M13	I/O
K11	I/O
L12	I/O
L13	I/O
K13	I/O
H10	I/O
J12	I/O
J13	I/O
H11	I/O
H12	I/O
H13	VKS
G13	VPP

PG132	
Pin Number	A42MX09 Function
G12	VSV
F13	I/O
F12	I/O
F11	I/O
F10	I/O
E13	I/O
D13	I/O
D12	I/O
C13	I/O
B13	I/O
D11	I/O
C12	I/O
A13	I/O
C11	I/O
B12	SDI
B11	I/O
C10	I/O
A12	I/O
A11	I/O
B10	I/O
D8	I/O
A10	I/O
C8	I/O
A9	I/O
B8	PRBA
A8	I/O
B7	CLKA
A7	I/O
B6	CLKB
A6	I/O
C6	PRBB
A5	I/O
D6	I/O
A4	I/O
B4	I/O

PG132	
A42MX09	
Pin Number	**Function**
A3	I/O
C4	I/O
B3	I/O
A2	I/O
C3	DCLK
B5	GNDA
E12	GNDA
J2	GNDA
M9	GNDA
B9	GNDI
C5	GNDI
E11	GNDI
F4	GNDI
J3	GNDI
J11	GNDI
L5	GNDI
L9	GNDI
C9	GNDQ
E3	GNDQ
K12	GNDQ
D7	VCCA
G3	VCCA
G10	VCCA
L7	VCCA
C7	VCCI
G2	VCCI
G11	VCCI
K7	VCCI

CQ172
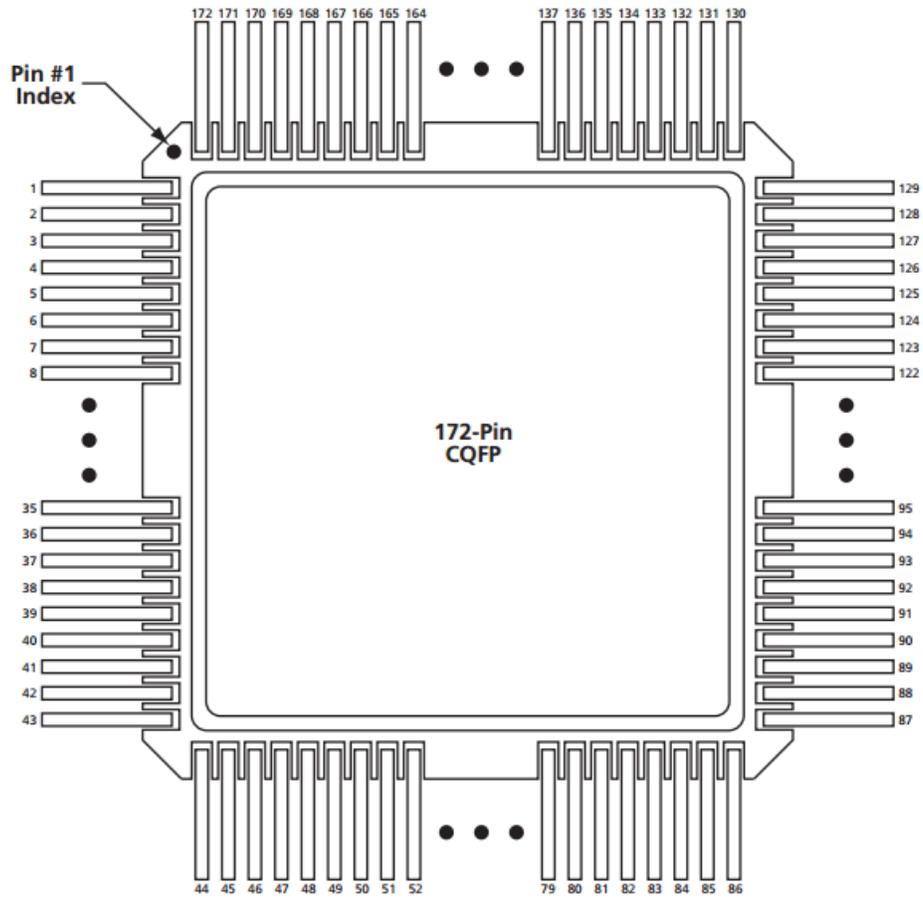
CQ172	
Pin Number	**A42MX16 Function**
1	MODE
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	GND
8	I/O
9	I/O
10	I/O
11	I/O
12	VCC
13	I/O
14	I/O
15	I/O
16	I/O
17	GND
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	VCCI
24	VSV
25	I/O
26	I/O
27	VCC
28	I/O
29	I/O
30	I/O
31	I/O
32	GND
33	I/O
34	I/O
35	I/O
36	I/O
37	GND
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O

CQ172	
Pin Number	**A42MX16 Function**
43	I/O
44	BININ
45	BINOUT
46	I/O
47	I/O
48	I/O
49	I/O
50	VCCI
51	I/O
52	I/O
53	I/O
54	I/O
55	GND
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	GND
66	VCC
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	GND
76	I/O
77	I/O
78	I/O
79	I/O
80	VCCI
81	I/O
82	I/O
83	I/O
84	I/O

CQ172	
Pin Number	**A42MX16 Function**
85	SDO
86	I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	GND
99	I/O
100	I/O
101	I/O
102	I/O
103	GND
104	I/O
105	I/O
106	VKS
107	VPP
108	GND
109	VCCI
110	VSV
111	I/O
112	I/O
113	VCC
114	I/O
115	I/O
116	I/O
117	I/O
118	GND
119	I/O
120	I/O
121	I/O
122	I/O
123	GNDI
124	I/O
125	I/O
126	I/O

CQ172	
Pin Number	**A42MX16 Function**
127	I/O
128	I/O
129	I/O
130	I/O
131	SDI
132	I/O
133	I/O
134	I/O
135	I/O
136	VCCI
137	I/O
138	I/O
139	I/O
140	I/O
141	GND
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	PROBA
149	I/O
150	CLKA
151	VCC
152	GND
153	I/O
154	CLKB
155	I/O
156	PROBB
157	I/O
158	I/O
159	I/O
160	I/O
161	GND
162	I/O
163	I/O
164	I/O
165	I/O
166	VCCI
167	I/O
168	I/O

CQ172	
Pin Number	**A42MX16 Function**
169	I/O
170	I/O
171	DCLK

3 – Datasheet Information

List of Changes

The following table shows the important changes made in this document for each revision.

Revision	Changes	Page
Revision 14 (May 2016)	Added CQFP package information for A42MX16 device in "Product Profile" section and "Ceramic Device Resources" section (SAR 79522).	1-i, 1-iii
	Added Military (M) and MIL-STD-883 Class B (B) grades for CPGA 132 Package and added Commercial (C), Military (M), and MIL-STD-883 Class B (B) grades for CQFP 172 Package in "Temperature Grade Offerings" section (SAR 79519).	1-iii
	Changed Silicon Sculptor II to Silicon Sculptor in "Programming" section (SAR 38754).	1-8
	Added "CQ172" package (SAR 79522).	2-57
Revision 13 (August 2015)	Added "PQ144" Package for A42MX09 device (SAR 69776).	2-13
	Added "PG132" Package for A42MX09 device (SAR 69776).	2-54
Revision 12 (March 2014)	Added information on power-up behavior for A42MX24 and A42MX36 devices to the "Power Supply" section (SAR 42096).	1-9
	Corrected the inadvertent mistake in the naming of the PL68 pin assignment table (SARs 48999, 49793).	2-4
Revision 11 (May 2012)	The FuseLock logo and accompanying text was removed from the "User Security" section. This marking is no longer used on Microsemi devices (PCN 0915).	1-8
	The "Development Tool Support" section was updated (SAR 38512).	1-16
Revision 10 (April 2012)	"Ordering Information" was updated to include lead-free package ordering codes (SAR 21968).	ii
	The "User Security" section was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34673).	1-8
	The "Transient Current" section is new (SAR 36930).	1-9
	Package names were revised according to standards established in *Package Mechanical Drawings* (SAR 34774).	2-1
Revision 9 (v6.1, April 2009)	In Table 1-14 • Absolute Maximum Ratings*, the limits in VI were changed from -0.5 to VCCI + 0.5 to -0.5 to VCCA + 0.5.	1-21
	In Table 1-16 • Mixed 5.0V/3.3V Electrical Specifications, V_{OH} was changed from 3.7 to 2.4 for the min in industrial and military. V_{IH} had V_{CCI} and that was changed to VCCA.	1-22

Revision	Changes	Page
v6.0 (January 2004)	The "Ease of Integration" section was updated.	1-i
	The "Temperature Grade Offerings" section is new.	1-iii
	The "Speed Grade Offerings" section is new.	1-iv
	The "General Description" section was updated.	1-1
	The "MultiPlex I/O Modules" section was updated.	1-7
	The "User Security" section was updated.	1-8
	Table 1-1 • Voltage Support of MX Devices was updated.	1-9
	The "Power Dissipation" section was updated.	1-10
	The "Static Power Component" section was updated.	1-10
	The "Equivalent Capacitance" section was updated.	1-10
	Figure 1-12 • Silicon Explorer II Setup with 42MX was updated.	1-12
	Table 1-4 • Supported BST Public Instructions was updated.	1-14
	Figure 1-13 • 42MX IEEE 1149.1 Boundary Scan Circuitry was updated.	1-14
	Table 1-5 • Boundary Scan Pin Configuration and Functionality was updated.	1-15

Revision	Changes	Page
v6.0 (continued)	The "Development Tool Support" section was updated.	1-16
	The Table 1-7 • Absolute Maximum Ratings for 42MX Devices* and the Table 1-6 • Absolute Maximum Ratings for 40MX Devices* were updated.	1-17
	The Table 1-9 • 5V TTL Electrical Specifications was updated.	1-18
	The Table 1-13 • 3.3V LVTTL Electrical Specifications was updated.	1-20
	In the "Mixed 5.0V/3.3V Electrical Specifications" section, Table 1-14 • Absolute Maximum Ratings*, Table 1-15 • Recommended Operating Conditions, and Table 1-16 • Mixed 5.0V/3.3V Electrical Specifications were updated.	1-21
	Table 1-17 • DC Specification (5.0 V PCI Signaling)[1] was updated.	1-23
	Table 1-19 • DC Specification (3.3 V PCI Signaling)[1] was updated.	1-24
	The "Junction Temperature (T_J)" section, "Package Thermal Characteristics" section, and the tables were updated.	1-26
	Figure 1-16 • 40MX Timing Model* was updated.	1-27
	Figure 1-18 • 42MX Timing Model (Logic Functions Using Quadrant Clocks) was updated.	1-28
	Figure 1-19 • 42MX Timing Model (SRAM Functions) was updated.	1-29
	Figure 1-26 • Output Buffer Latches was updated.	1-32
	Table 1-22 • 42MX Temperature and Voltage Derating Factors is new.	1-36
	Table 1-23 • 40MX Temperature and Voltage Derating Factors is new.	1-36
	The "Pin Descriptions" section was updated.	1-83
	In the "PQ100" table, Pin 64 (42MX09 and 42MX16) has changed to LP.	2-10
	In the "PQ160" table, Pin 61 (42MX09, 42MX16, and 42MX64) has changed to LP.	2-17
	In the "PQ208" table, the following pins changed: Pin 129 (42MX09, 42MX16, and 42MX64) has changed to LP. Pin 198 (42MX09) has changed to I/O.	2-23
	The n the "PQ240" table, Pin 91 (42MX36) has changed to LP.	2-30
	In the "VQ100" table, Pin 62 (42MX09 and 42MX16) has changed to LP.	2-36
	In the "TQ176" table, Pin 109 (42MX09 and 42MX16) has changed to LP.	2-38
	In the "BG272" table, Pin K20 (42MX36) has changed to LP.	2-51
v5.1	The "Low Power Mode" section was updated.	1-9
	Footnote 8 in Table 1-9 • 5V TTL Electrical Specifications was updated.	1-18
	Footnote 8 in Table 1-13 • 3.3V LVTTL Electrical Specifications was updated.	1-20
v5.0	Because the changes in this data sheet are extensive and technical in nature, this should be viewed as a new document. Please read it as you would a datasheet that is published for the first time.	ALL
	Note that the "Package Characteristics and Mechanical Drawings" section has been eliminated from the datasheet. The mechanical drawings are now contained in a separate document, *Package Mechanical Drawings,* available on the Microsemi SoC Products Group website.	

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In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

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The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advance

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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