ChargePump™

General Description

The AAT3190 charge pump controller provides the regulated positive and negative voltage biases required by active matrix thin-film transistor (TFT) liquid-crystal displays (LCDs), charge-coupled device (CCD) sensors, and organic light emitting diodes (OLEDs). Two low-power charge pumps convert input supply voltages ranging from 2.7V to 5.5V into two independent output voltages.

The dual low-power charge pumps independently regulate a positive (V_{POS}) and negative (V_{NEG}) output voltage. These outputs use external diode and capacitor multiplier stages (as many stages as required) to regulate output voltages up to ±25V. Built-in soft-start circuitry prevents excessive inrush current during start-up. A high switching frequency enables the use of small external capacitors. The device's shutdown feature disconnects the load from V_{IN} and reduces quiescent current to less than 1.0µA.

The AAT3190 is available in a Pb-free MSOP-8 or TSOPJW-12 package and is specified over the -40°C to +85°C operating temperature range.

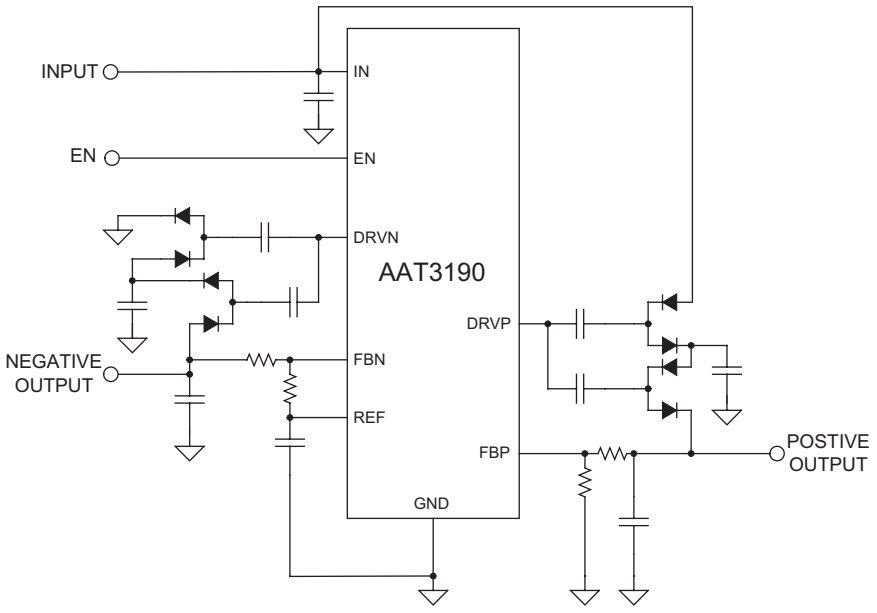
Features

- V_{IN} Range: 2.7V to 5.5V
- Adjustable ± Dual Charge Pump
- Positive Supply Output Up to +25V
- Negative Supply Output Down to -25V
- Up to 30mA Output Current
- 1.0MHz Switching Frequency
- <1.0µA Shutdown Current
- Internal Power MOSFETs
- Internally Controlled Soft Start
- Fast Transient Response
- Ultra-Thin Solution (No Inductors)
- -40°C to +85°C Temperature Range
- Available in 8-Pin MSOP or 12-Pin TSOPJW Package

Applications

- CCD Sensor Voltage Bias
- OLEDs
- Passive-Matrix Displays
- Personal Digital Assistants (PDAs)
- TFT Active-Matrix LCDs

Typical Application

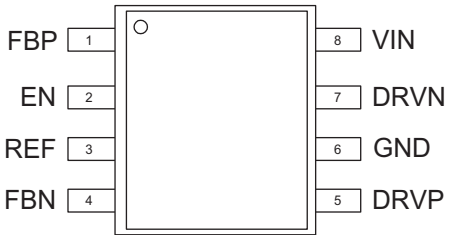


Pin Description

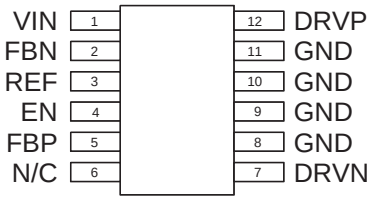
Pin #		Symbol	Function
MSOP-8	TSOPJW-12		
1	5	FBP	Positive charge pump feedback input. Regulates to 1.2V nominal. Connect feedback resistive divider to analog ground (GND).
2	4	EN	Enable input. When EN is pulled low, the device shuts off and draws only 1.0µA. When high, it is in normal operation. Drive EN through an external resistor.
3	3	REF	Internal reference bypass terminal. Connect a 0.1µF capacitor from this terminal to analog ground (GND). External load capability to 50µA. REF is disabled in shutdown.
4	2	FBN	Negative charge pump regulator feedback input. Regulates to 0V nominal. Connect feedback resistive divider to the reference (REF).
5	12	DRVP	Positive charge pump driver output. Output high level is V_{IN} and low level is PGND.
6	8, 9, 10, 11	GND	Ground.
7	7	DRVN	Negative charge pump driver output. Output high level is V_{IN} and low level is PGND.
8	1	VIN	Input voltage: 2.7V to 5.5V.

Pin Configuration

MSOP-8
(Top View)



TSOPJW-12
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}	Input Voltage	-0.3 to 6	V
V_{EN}	EN to GND	-0.3 to 6	V
V_{N_CH}	DRVN to GND	-0.3V to (V_{IN} + 0.3V)	V
V_{P_CH}	DRVP to GND	-0.3V to (V_{IN} + 0.3V)	V
Other Inputs	REF, FBN, FBP to GND	-0.3V to (V_{IN} + 0.3V)	V
I_{MAX}	Continuous Current Into DRVN, DRVP	±200	mA
	All Other Pins	±10	
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information[2]

Symbol	Description		Value	Units
Θ_{JA}	Thermal Resistance	MSOP-8	150	°C/W
		TSOPJW-12	160	
P_D	Maximum Power Dissipation (T_A = 25°C)	MSOP-8[3]	667	mW
		TSOPJW-12[4]	625	

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board.
3. Derate 6.7mW/°C above 25°C.
4. Derate 6.25mW/°C above 25°C.

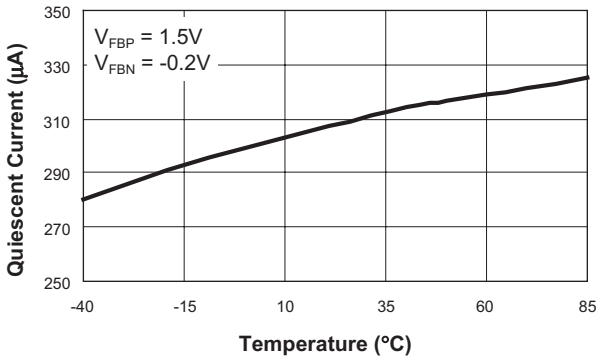
Electrical Characteristics

V_{IN} = 5.0V, C_{REF} = 0.1µF, T_A = -40°C to +85°C. Unless otherwise noted, typical values are T_A = 25°C.

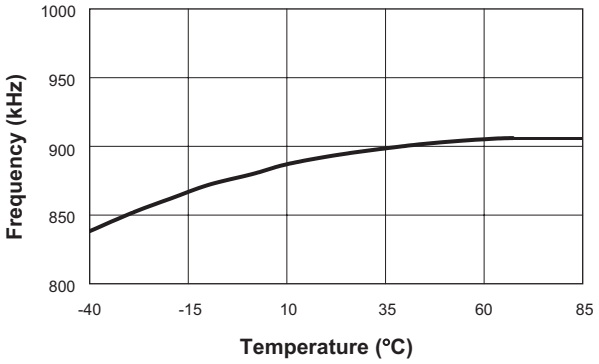
Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Supply Range		2.7		5.5	V
UVLO	Input Under-Voltage Threshold	V_{IN} Rising		1.8		V
		V_{IN} Falling, 40mV Hysteresis (typ)		1.6		
I_{IN}	Input Quiescent Supply Current	V_{FBP} = 1.5V, V_{FBN} = -0.2V, No Load on DRVN and DRVP		400	800	µA
I_{SD}	Shutdown Supply Current	V_{EN} = 0V		0.1	1.0	µA
F_{OSC}	Operating Frequency		0.8	1.0	1.2	MHz
Negative Low-Power Charge Pump						
V_{FBN}	FBN Regulation Voltage		-100	0	+100	mV
I_{FBN}	FBN Input Bias Current	V_{FBN} = -50mV	-100		+100	nA
R_{DSNCHN}	DRVN NCH On-Resistance			1.5	5.0	Ω
$R_{DSPCHMIN}$	MIN DRVN PCH On-Resistance	V_{FBN} = 100mV, V_{IN} = 4V		1.0	5.0	Ω
$R_{DSPCHMAX}$	MAX DRVN PCH On-Resistance	V_{FBN} = -100mV, V_{IN} = 4V		20		kΩ
Positive Low-Power Charge Pump						
V_{FBP}	FBP Regulation Voltage		1.15	1.2	1.25	V
I_{FBP}	FBP Input Bias Current	V_{FBP} = 1.5V	-60		+100	nA
R_{DSPCHP}	DRVP PCH On-Resistance			1.0	5.0	Ω
$R_{DSNCHMIN}$	MIN DRVP NCH On-Resistance	V_{FBP} = 1.15V, V_{IN} = 4V		3	15	Ω
$R_{DSNCHMIN}$	MAX DRVP NCH On-Resistance	V_{FBP} = 1.25V, V_{IN} = 4V		20		kΩ
Reference						
V_{REF}	Reference Voltage	-2.0µA < I_{REF} < 50µA	1.18	1.2	1.22	V
	Reference Under-Voltage Threshold	V_{REF} Rising		0.8		V
Logic Signals						
V_{IL}	Input Low Voltage				0.5	V
V_{IH}	Input High Voltage		1.5			V
I_{IL}	Enable Input Low Current	V_{IN} = 5.0V, F_{BP} = 1.5V, F_{BN} = -0.2V			1	µA
I_{IH}	Enable Input High Current	V_{IN} = 5.0V, F_{BP} = 1.5V, F_{BN} = -0.2V			1	µA
Thermal Limit						
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYST}	Over-Temperature Shutdown Hysteresis			15		°C

Typical Characteristics

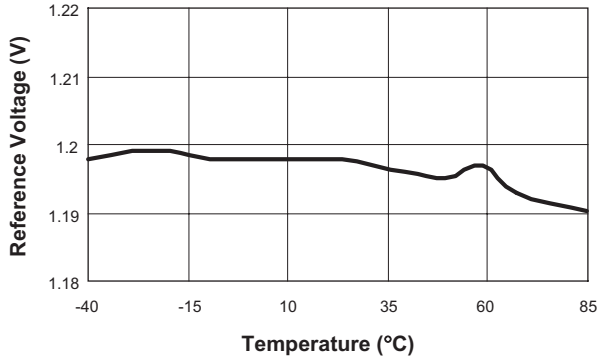
Quiescent Current vs. Temperature



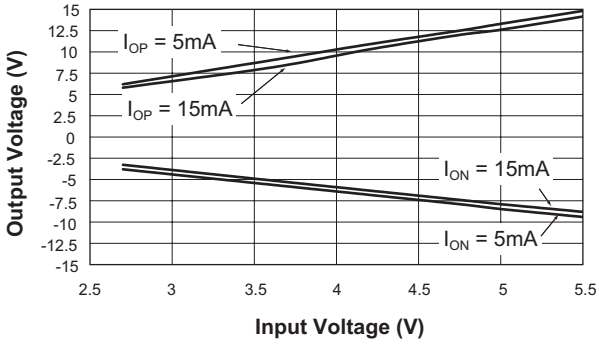
Switching Frequency vs. Temperature



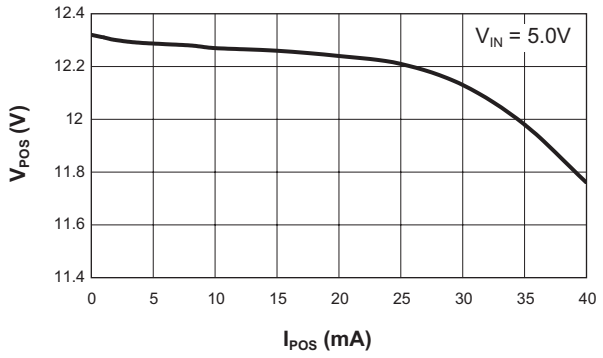
Reference Voltage vs. Temperature



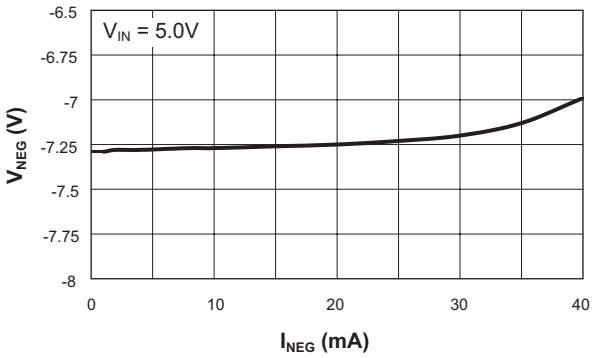
Maximum V_{OUT} vs. V_{IN}
(I_{OUT} = 5mA and 15mA)



Positive Output Voltage vs. Load Current
(T_A = 25°C)

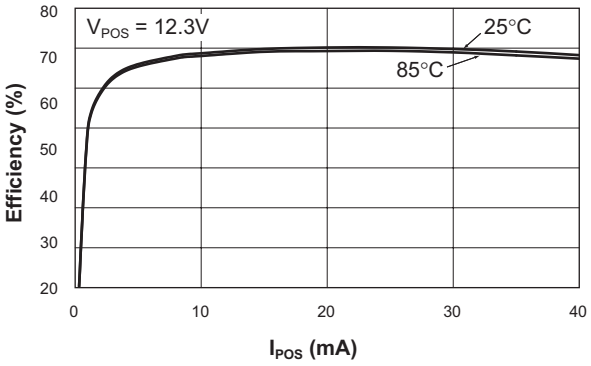


Negative Output Voltage vs. Load Current
(T_A = 25°C)

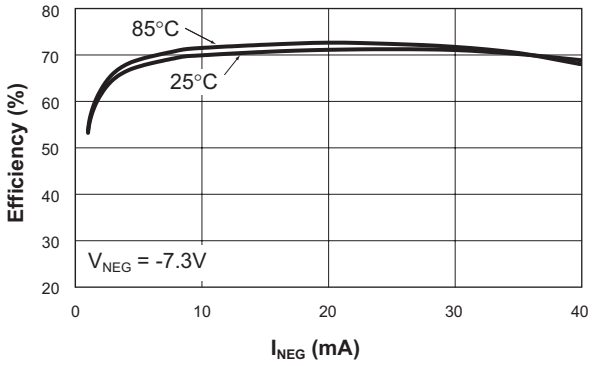


Typical Characteristics

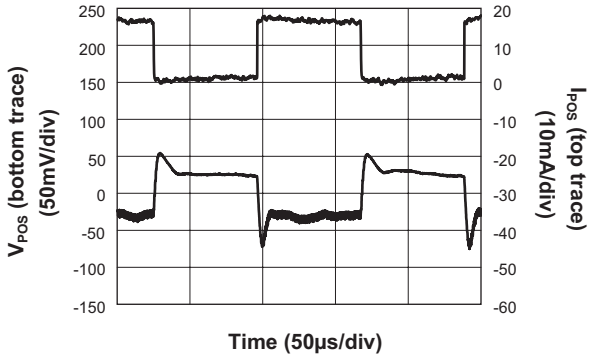
Positive Output Efficiency vs. Load Current
(V_{IN} = 5.0V)



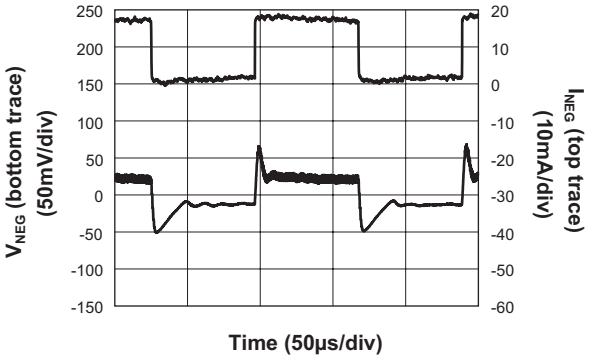
Negative Output Efficiency vs. Load Current
(V_{IN} = 5.0V)



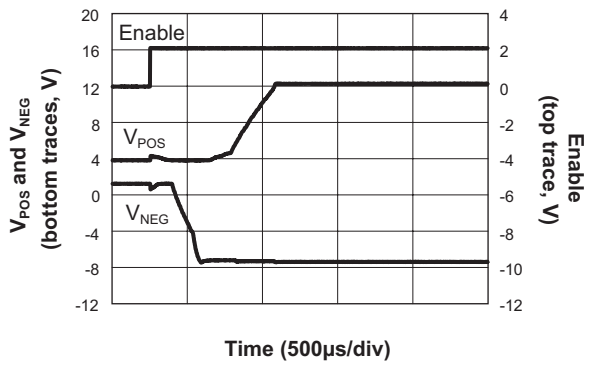
V_{POS} Load Transient



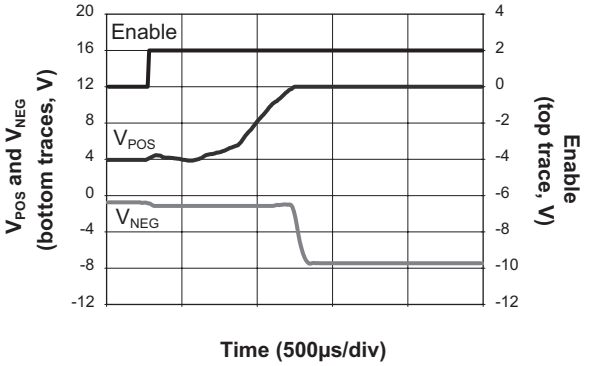
V_{NEG} Load Transient



AAT3190 Power-Up Sequence

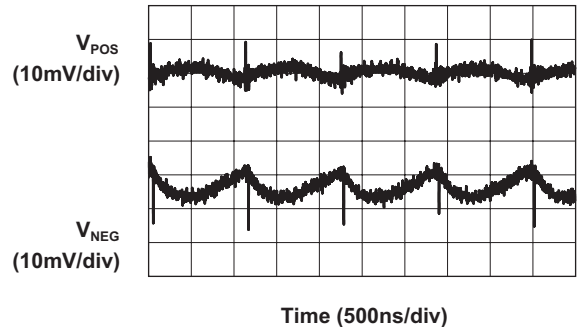


AAT3190-1 Power-Up Sequence

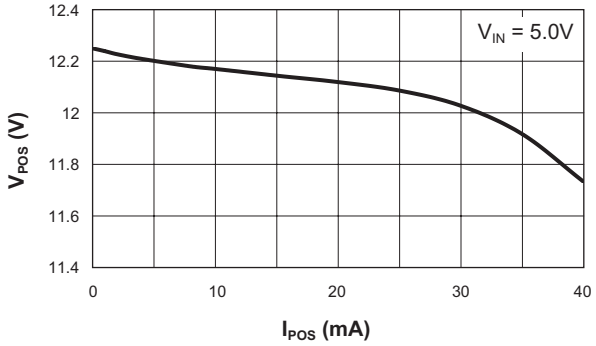


Typical Characteristics

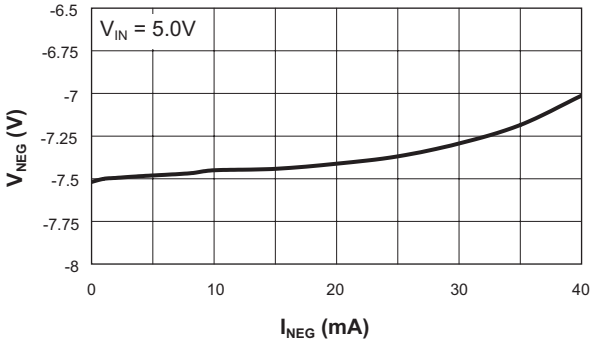
Output Ripple
(V_{POS} = 12.3V; I_{POS} = 5mA; V_{NEG} = 7.2V; I_{NEG} = 10mA)



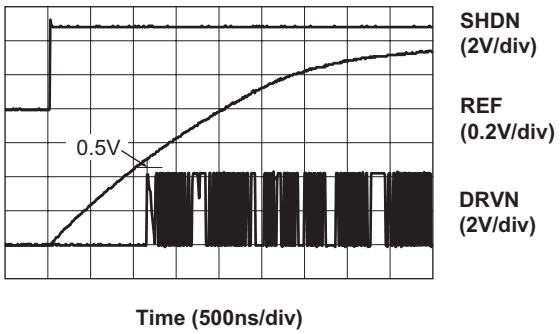
Positive Output Voltage vs. Load Current
(T = 85°C)



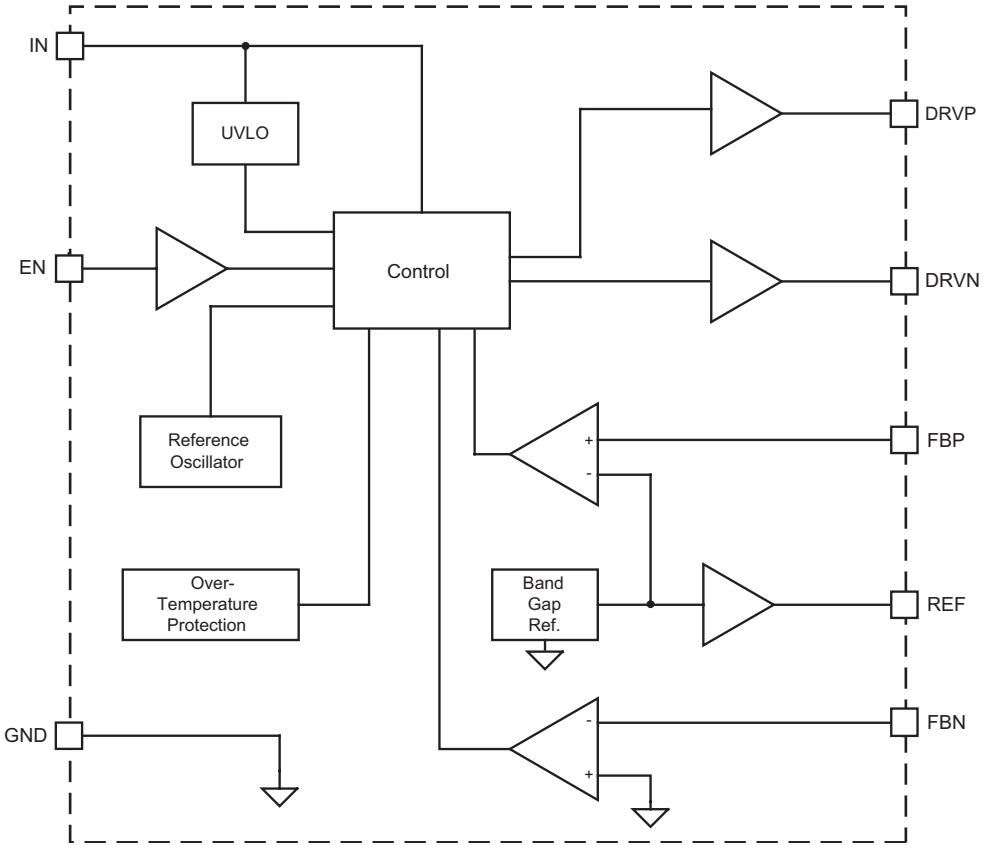
Negative Output Voltage vs. Load Current
(T = 85°C)



AAT3190 Reference Under-Voltage Threshold
(120µF capacitor placed across REF to limit rate of rise of REF for test purposes only)



Functional Block Diagram



Functional Description

Dual Charge Pump Regulators

The AAT3190 provides low-power regulated output voltages from two individual charge pumps. Using a single stage, the first charge pump inverts the supply voltage (V_{IN}) and provides a regulated negative output voltage. The second charge pump doubles V_{IN} and provides a regulated positive output voltage. These outputs use external Schottky diodes and capacitor multiplier stages (as many as required) to regulate up to ±25V. A constant switching frequency of 1MHz minimizes the output ripple and capacitor size.

Negative Charge Pump

During the first half-cycle, the P-channel MOSFET turns on and the flying capacitor C7 charges to V_{IN} minus a diode drop (Figure 1). During the second half-cycle, the P-channel MOSFET turns off and the N-channel MOSFET turns on, level shifting C7. This connects C7 in parallel with the output reservoir capacitor C10. If the voltage across C10 minus a diode drop is less than the voltage across C7, current flows from C7 to C10 until the diode turns off.

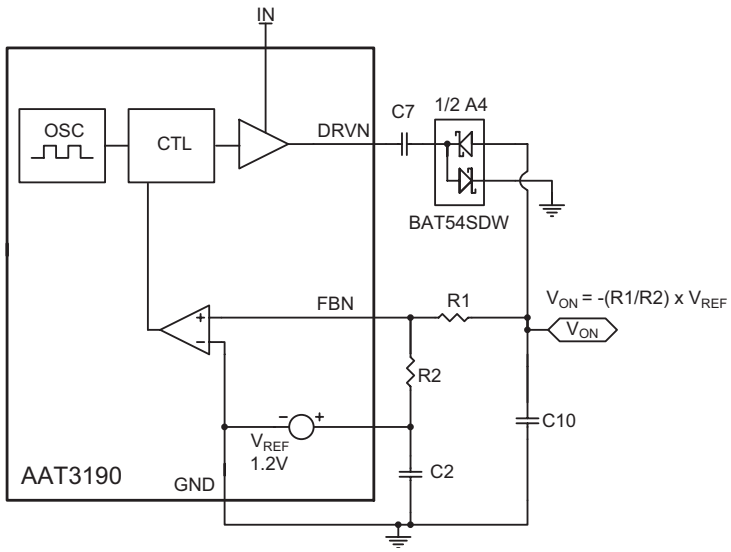


Figure 1: Negative Charge Pump Block Diagram.

Positive Charge Pump

During the first half-cycle, the N-channel MOSFET turns on and charges the flying capacitor C4 (Figure 2). During the second half-cycle, the N-channel MOSFET turns off and the P-channel MOSFET turns on, level shifting C4 by the input voltage. This connects C4 in parallel with the reservoir capacitor C5. If the voltage across C5 plus a diode drop is less than the level shifted flying capacitor (C4 + V_{IN}), charge is transferred from C4 to C5 until the diode turns off.

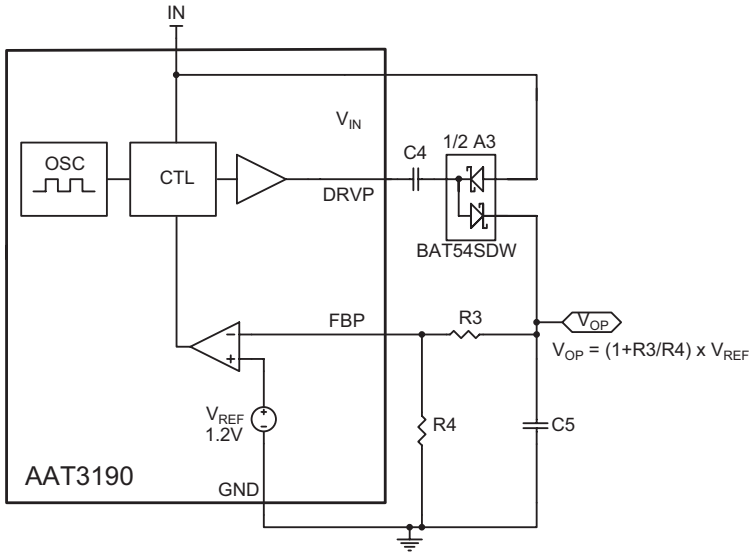


Figure 2: Positive Charge Pump Block Diagram.

Voltage Reference

The voltage reference is a simple band gap with an output voltage equal to V_{BE} + K*V_T. The band gap reference amplifier has an additional compensation capacitor from the negative input to the output. This capacitor serves to slow down the circuit during startup and soft starts the voltage reference and the regulator output from overshoot. The reference circuit amplifier also increases the overall PSRR of the device. An 80kΩ resistor serves to isolate and buffer the amplifier from a small internal filter capacitor and an optional large external filter capacitor.

Enable and Start-up

The AAT3190 is disabled by pulling the EN pin low. The threshold levels lie between 0.5V and 1.5V. Even though the quiescent current of the IC during shutdown is less than 1µA, the positive output voltage (V_{OP}) and any load current associated with it does not disappear without the complete removal of the input voltage. This is due to the fact that with no switching of the DRVP pin, the input voltage simply forward biases the Schottky diodes associated with the V_{OP} charge pump, providing a path for load current to be drawn from the input voltage.

Depending on the application, the supplies must be sequenced properly to avoid damage or latch-up. The AAT3190 start-up sequence ramps up the V_{OP} output 200µs after the V_{ON} output is present. The AAT3190-1 ramps up the positive supply before the negative supply.

Over-Temperature Protection

A logic control circuit will shut down both charge pumps in the case of an over-temperature condition.

Under-Voltage Lockout

A UVLO circuit disables the AAT3190 when the input voltage supply is lower than 1.8V nominal.

Design Procedure and Component Selection

Output Voltage

The number of charge pump stages required for a given output varies with the input voltage applied. The number of stages required can be estimated by:

$$n_p = \frac{V_{OP} - V_{IN}}{V_{IN} - 2V_F}$$

for the positive output and

$$n_n = \frac{V_{ON}}{2V_F - V_{IN}}$$

for the negative output.

When solving for n_p and n_n, round up the solution to the next highest integer to determine the number of stages required.

V_{ON}

The negative output voltage is adjusted by a resistive divider from the output (V_{ON}) to the FBN and REF pin.

The maximum reference voltage current is 50µA; therefore, the minimum allowable value for R2 of Figure 1 is 24kΩ. It is best to select the smallest value possible for R2, as this will keep R1 to a minimum. This limits errors due to the FBN input bias current. The FBN input has a maximum input bias current of 100nA. Using the full 50µA reference current for programming V_{ON}:

$$I_{PGM} = \frac{V_{REF}}{R2} = \frac{1.2}{24.1k} = 50\mu A$$

will limit the error due to the input bias current at FBN to less than 0.2%:

$$\frac{I_{FBN}}{I_{PGM}} = \frac{0.1\mu A}{50\mu A} = 0.2\%$$

With R2 selected, R1 can be determined:

$$R1 = \frac{V_{NEG} \cdot R2}{-V_{REF}}$$

V_{OP}

The positive output voltage is set by way of a resistive divider from the output (V_{OP}) to the FBP and ground pin. Limiting the size of R4 reduces the effect of the FBP bias current. For less than 0.1% error, limit R4 to less than 12kΩ.

$$I_{PGM} = \frac{V_{REF}}{R4} = \frac{1.2V}{12k\Omega} = 100\mu A$$

$$\frac{I_{FBP}}{I_{PGM}} = \frac{0.1\mu A}{100\mu A} = 0.1\%$$

Once R4 has been determined, solve for R3:

$$R3 = R4 \cdot \left(\frac{V_O}{V_{REF}} - 1\right)$$

Flying and Output Capacitor

The flying capacitor minimum value is limited by the output power requirement, while the maximum value is set by the bandwidth of the power supply. If C_{FLY} is too small, the output may not be able to deliver the power demanded, while too large of a capacitor may limit the bandwidth and time required to recover from load and line transients. A 0.1µF X7R or X5R ceramic capacitor is typically used. The voltage rating of the flying and reservoir output capacitors varies with the number of charge pump stages. The reservoir output capacitor should be roughly 10 times the flying capacitor. Use larger capacitors for reduced output ripple.

Positive Output Capacitor Voltage Ratings

The absolute steady-state maximum output voltage (neglecting the internal $R_{DS(ON)}$ drop of the internal MOSFETs) for the nth stage is:

$$V_{BULK(n)} = (n + 1) \cdot V_{IN} - 2 \cdot n \cdot V_{FWD}$$

where V_{FWD} is the estimated forward drop of the Schottky diode. This is also the voltage rating required for the nth bulk capacitor in the positive output charge pump.

The voltage rating for the nth flying capacitor in the positive stage is:

$$V_{FLY(n)} = V_{BULK(n+1)} - V_{FWD}$$

where $V_{BULK(0)}$ is the input voltage (see Table 1).

V_{IN} = 5.0V, V_{FWD} = 0.3V		
Stages (n)	**$V_{BULK(n)}$**	**$V_{FLY(n)}$**
1	9.4V	4.7V
2	13.8V	9.1V
3	18.2V	13.5V
4	22.6V	17.9V
5	27.0V	22.3V
6	31.4V	26.7V

Table 1: Positive Output Capacitor Voltages.

Negative Output Capacitor Voltage Ratings

The absolute steady-state maximum output voltage (neglecting the internal $R_{DS(ON)}$ drop of the internal MOSFETs) for the nth stage is:

$$V_{BULK(n)} = -n \cdot V_{IN} + 2 \cdot n \cdot V_{FWD}$$

This is also the voltage rating required for the nth bulk capacitor in the negative output charge pump.

The voltage rating for the nth flying capacitor in the negative stage (see Table 2) is:

$$V_{FLY(n)} = V_{FWD} - V_{BULK(n)}$$

V_{IN} = 5.0V, V_{FWD} = 0.3V		
Stages (n)	**$V_{BULK(n)}$**	**$V_{FLY(n)}$**
1	-4.4V	4.7V
2	-8.8V	9.1V
3	-13.2V	13.5V
4	-17.6V	17.9V
5	-22.0V	22.3V
6	-26.4V	26.7V

Table 2: Negative Output Capacitor Voltages.

Single Output Operation

If only one of the two channels is needed, it is possible to disable either output. Connect the respective FB pin to V_{IN} to disable the output (e.g., connect FBN to V_{IN} in order to disable the negative output).

Input Capacitors

Input Capacitor

The primary function of the input capacitor is to provide a low impedance loop for the edges of pulsed current drawn by the IC. A low ESL X7R or X5R type ceramic capacitor is ideal for this function. The size required will vary depending on the load, output voltage, and input voltage characteristics. Typically, the input capacitor should be 5 to 10 times the flying capacitor. If the source impedance of the input supply is high, a larger capacitor may be required. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing radiated and conducted EMI.

Rectifier Diodes

For the rectifiers, use Schottky diodes with a voltage rating of 1.5 times the input voltage. The maximum steady-state voltage seen by the rectifier diodes for both the positive and negative charge pumps (regardless of the number of stages) is:

$$V_{REVERSE} = V_{IN} - V_F$$

The BAT54S dual Schottky is offered in a SOT23 package that provides a convenient pin-out for the voltage doubler configuration. The BAT54SDW quad Schottky in a SOT363 (2x2mm) package is a good choice for multiple-stage charge pump configuration (see Figure 3, Evaluation Board Schematic).

PC Board Layout

The input and reference capacitor should be placed as close to the IC as possible. Place the programming resistors (R1-R4) close to the IC, minimizing trace length to FBN and FBP. Figures 4 and 5 display the evaluation board layout with the TSOPJW-12 package.

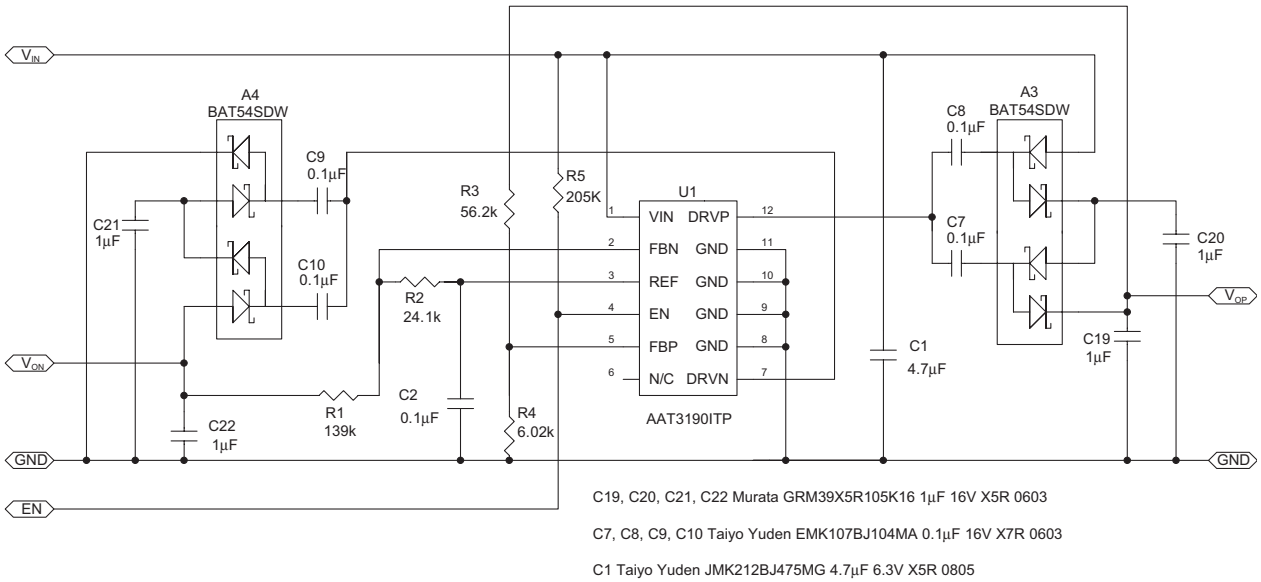


Figure 3: AAT3190 Evaluation Board Schematic (shown with two stages)
V_{OP} = 12V, V_{ON} = -7V.

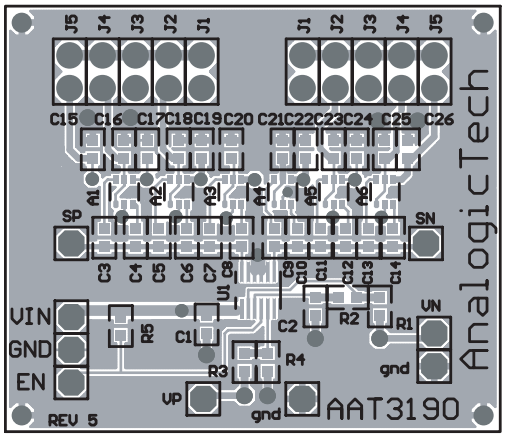


Figure 4: AAT3190 Evaluation Board Top Side.

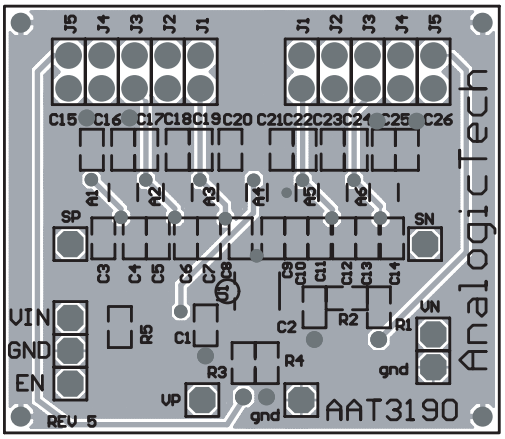


Figure 5: AAT3190 Evaluation Board Bottom Side.

Ordering Information

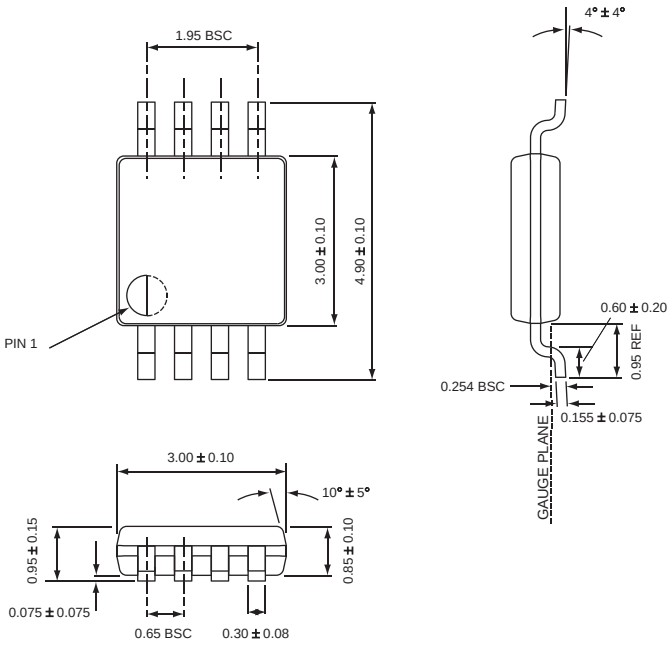
Package	Power-Up Sequence	Marking[1]	Part Number (Tape and Reel)[2]
MSOP-8	-, +	JDXYY	**AAT3190IKS-T1**
TSOPJW-12	-, +	JDXYY	**AAT3190ITP-T1**
TSOPJW-12	+, -	LKXYY	**AAT3190ITP-1-T1**

Pb-free

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/pbfree.

Package Information

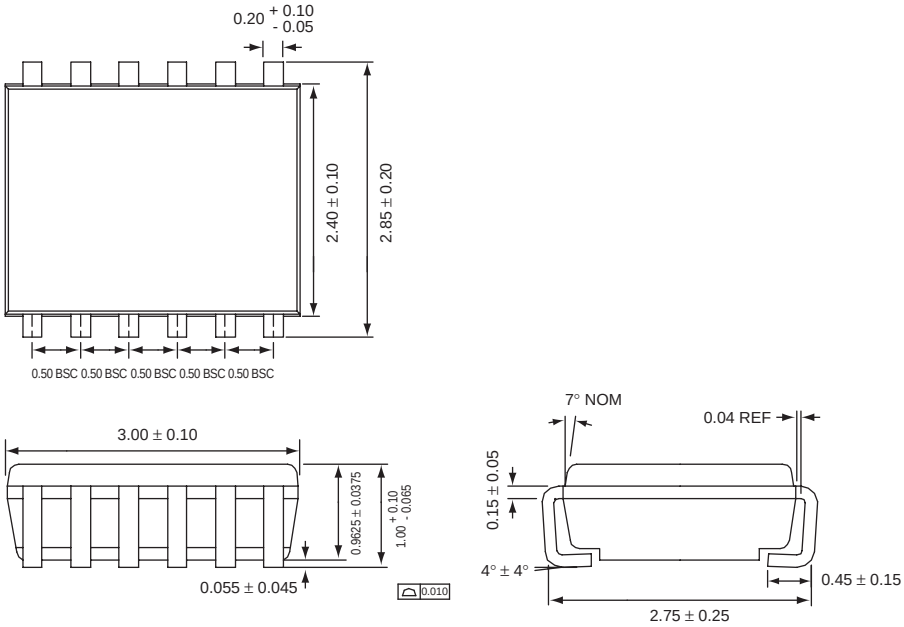
MSOP-8



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

TSOPJW-12



All dimensions in millimeters.

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