ACPL-K33T

Automotive 2.5 A Peak High Output Current SiC MOSFET and IGBT Gate Drive Optocoupler with Rail-to-Rail Output Voltage in Stretched SO-8

Data Sheet

Description

Avago Technologies' 2.5 Amp Automotive R²Coupler Gate Drive Optocoupler contains an AlGaAs LED, which is optically coupled to an integrated circuit with a power output stage. The ACPL-K33T features fast propagation delay and tight timing skew, is ideally designed for driving SiC MOSFET and IGBTs used in AC-DC and DC-DC converters. The high operating voltage range of the output stage provides the drive voltages required by gate-controlled devices. The voltage and high peak output current supplied by this optocoupler make it ideally suited for direct driving SiC MOSFET and IGBTs at high frequency for high efficiency conversion.

Avago R²Coupler isolation products provide reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high-temperature industrial applications.

Functional Diagram

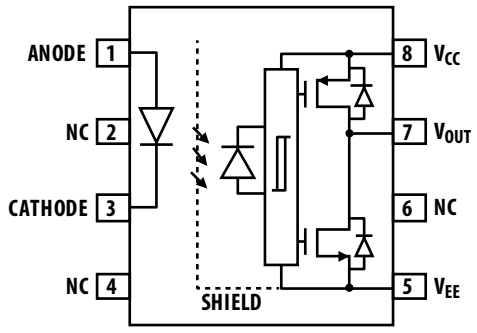


Figure 1. ACPL-K33T Functional Diagram

Note: Minimum 1 µF bypass capacitor must be connected between pins V_{CC} and V_{EE}.

Truth Table

LED	$V_{CC} - V_{EE}$	V_{OUT}
OFF	0 – 30 V	LOW
ON	< V_{UVLO-}	LOW
ON	> V_{UVLO+}	HIGH

Features

- Qualified to AEC-Q100 Grade 1 Test Guidelines
- Automotive temperature range: -40 °C to +125 °C
- Peak output current: 2.0 A min.
- Rail-to-rail output voltage
- Propagation delay: 120 ns max.
- Dead time distortion: +50 ns/-40 ns
- LED input threshold current hysteresis
- Common Mode Rejection (CMR): 50 kV/µs min. at V_{CM} = 1500 V
- Low supply current allow bootstrap half-bridge topology: I_{CC} = 4.2 mA max.
- Under Voltage Lock-Out (UVLO) protection with hysteresis for SiC MOSFET and IGBT
- Wide operating VCC range: 15 V to 30 V
- Safety Approvals:
  - UL Recognized 5000 V_{RMS} for 1 min
  - CSA
  - IEC/EN/DIN EN 60747-5-5 V_{IORM} = 1140 V_{peak}

Applications

- Hybrid Power Train DC/DC Converter
- EV/PHEV Charger
- Automotive Isolated IGBT Gate Drive
- AC and Brushless DC Motor Drives

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Ordering Information

Part number	Option (RoHS Compliant)	Package	Surface Mount	Tape & Reel	UL 5000 Vrms/ 1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-K33T	-000E	Stretched SO-8	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel

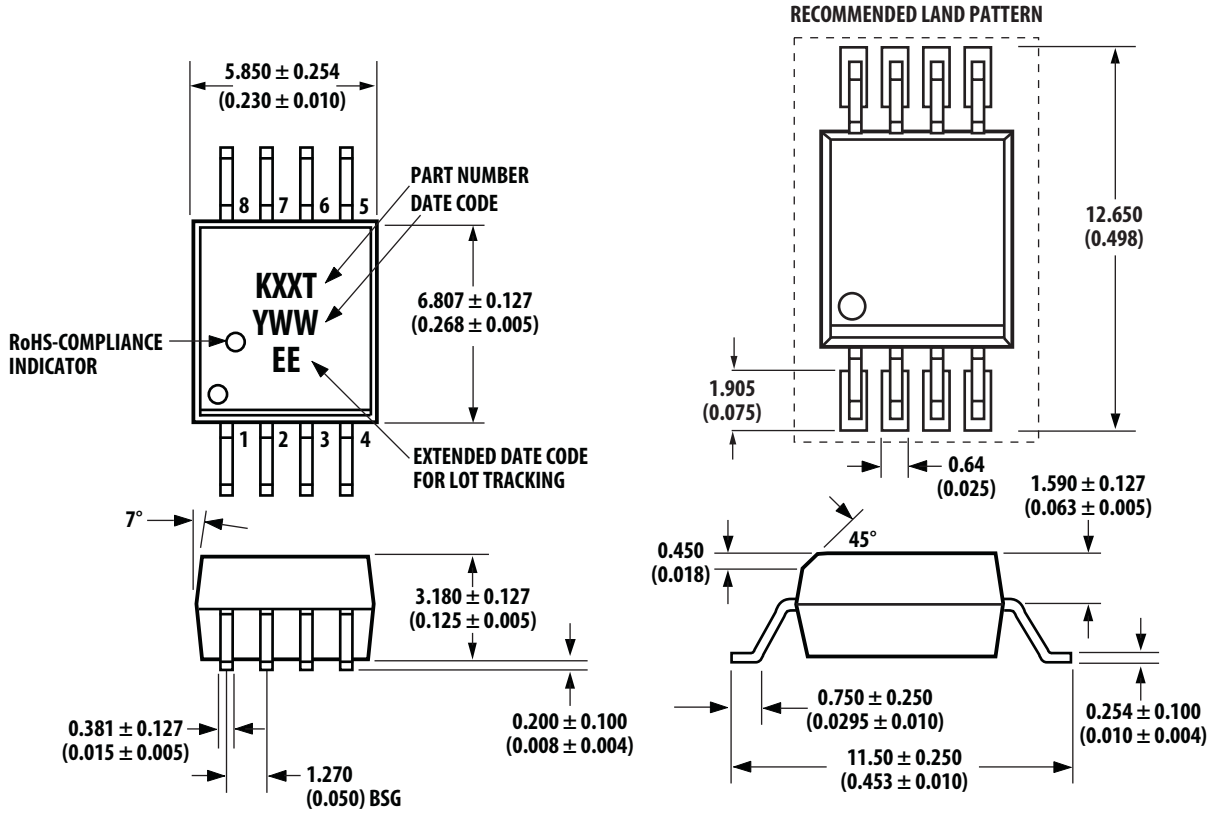
To order, choose a part number from the Part Number column and combine it with the desired option from the Option column to form an order entry.

Example 1:

ACPL-K33T-560E to order product of SSO-8 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval and is RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings (Stretched SO-8)



Dimensions in millimeters (inches).

Notes:
1. Lead coplanarity = 0.1 mm (0.004 inches).
2. Floating lead protrusion = 0.25 mm (10 mils) max.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

Note: Non-halide flux should be used.

Regulatory Information

The ACPL-K33T is approved by the following organizations:

UL	UL 1577, component recognition program up to V_{ISO} = 5 kV_{RMS}
CSA	CSA Component Acceptance Notice #5
IEC/EN/DIN EN 60747-5-5	IEC/EN/DIN EN 60747-5-5

IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristic (Option 060 and 560 only)

Description	Symbol	Option 060 and 560	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage < 600 V_{RMS} for rated mains voltage < 1000 V_{RMS}		 I - IV I - III	
Climatic Classification*		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1140	V_{peak}
Input to Output Test Voltage, Method b $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	2137	V_{peak}
Input to Output Test Voltage, Method a $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test with t_m=10 sec, Partial discharge < 5 pC	V_{PR}	1824	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure Case Temperature Input Current Output Power	 T_S $I_{S, INPut}$ $P_{S,OUTPUT}$	 175 230 600	 °C mA mW
Insulation Resistance at T_S, V_{IO}=500 V	Rs	$> 10^9$	Ω

* Climatic classification denotes <Minimum ambient temperature of operation>/<Maximum ambient temperature of operation>/<Number of days of the damp heat, steady state test>.

Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-K33T	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (DIN VDE0109)		IIIa		Material Group (DIN VDE 0109)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-55	150	°C	
Operating Temperature	T_A	-40	125	°C	
IC Junction Temperature	T_J		150	°C	3
Average Input Current	$I_{F(AVG)}$		20	mA	
Peak Input Current (50% duty cycle, < 1 ms pulse width)	$I_{F(PEAK)}$		40	mA	
Peak Transient Input Current (<1 μs pulse width, 300 pps)	$I_{F(TRAN)}$		1	A	
Reverse Input Voltage	V_R		6	V	
"High" Peak Output Current	$I_{OH(PEAK)}$		2.5	A	1
"Low" Peak Output Current	$I_{OL(PEAK)}$		2.5	A	1
Total Output Supply Voltage	$(V_{CC} - V_{EE})$	0	35	V	
Output Voltage	$V_{O(PEAK)}$	-0.5	V_{CC}	V	
Output IC Power Dissipation	P_O		500	mW	2
Total Power Dissipation	P_T		550	mW	3

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Operating Temperature	T_A	- 40	125	°C	
Output Supply Voltage	$(V_{CC} - V_{EE})$	15	30	V	
Input Current (ON)	$I_{F(ON)}$	7	13	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	-5.5	0.8	V	

Electrical Specifications (DC)

Unless otherwise noted, all Minimum/Maximum specifications are at Recommended Operating Conditions. All typical values are at T_A = 25 °C, V_{CC} - V_{EE} = 15 V, V_{EE} = Ground.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
High Level Peak Output Current	I_{OH}		-3.5	-2.0	A	$V_{CC} - V_O$ = 15 V	3	
Low Level Peak Output Current	I_{OL}	2.0	4		A	$V_O - V_{EE}$ = 15 V	4	
High Output Transistor RDS(ON)	$R_{DS,OH}$		2.2	4.0	Ω	I_{OH} = -2.0 A		4
Low Output Transistor RDS(ON)	$R_{DS,OL}$		1.0	2.0	Ω	I_{OL} = 2.0 A		4
High Level Output Voltage	V_{OH}	Vcc –0.45	Vcc –0.2		V	I_F = 10 mA, I_O = -100 mA		5, 6
Low Level Output Voltage	V_{OL}		0.1	0.25	V	I_O = 100 mA		
High Level Supply Current	I_{CCH}		2.65	4.2	mA	I_F = 10 mA	5	
Low Level Supply Current	I_{CCL}		2.55	4.2	mA	V_F = 0 V	6	
Threshold Input Current Low to High	I_{FLH}		2.6	5.5	mA	V_O > 5 V	7	
Threshold Input Voltage High to Low	V_{FHL}	0.8			V			
Input Forward Voltage	V_F	1.25	1.5	1.85	V	I_F = 10 mA	7	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$		-1.5		mV/ °C			
Input Reverse Breakdown Voltage	BV_R	6			V	I_R = 100 μA		
Input Capacitance	C_{IN}		90		pF	f = 1 MHz, V_F = 0 V		
UVLO Threshold	V_{UVLO+}	12.1	13	13.9	V	V_O > 5 V, I_F = 10 mA	8	
	V_{UVLO-}	11.1	12	12.9			8	
UVLO Hysteresis	$UVLO_{HYS}$	0.5	1.0		V			

Switching Specifications (AC)

Unless otherwise noted, all Minimum/Maximum specifications are at Recommended Operating Conditions. All typical values are at T_A = 25 °C, V_{CC} - V_{EE} = 15 V, V_{EE} = Ground.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Propagation Delay Time to High Output Level	t_{PLH}	30	65	120	ns	V_{CC} = 15 V R_G = 7.5 Ω C_L = 10 nF f = 20 kHz Duty Cycle = 50% V_{in} = 4.5 V to 5.5 V R_{in} = 350 Ω	9,12,14	7
Propagation Delay Time to Low Output Level	t_{PHL}	30	65	120	ns		10,12,14	
Pulse Width Distortion (t_{PHL} – t_{PLH})	PWD	-40	0	40	ns		11	8
Dead Time Distortion Caused by Any Two Parts (t_{PLH} – t_{PHL})	DTD	-40		50	ns			9
Rise Time	t_R		15		ns	V_{CC} = 15 V C_L = 1 nF f = 20 kHz Duty Cycle = 50% V_{in} = 4.5 V to 5.5 V R_{in} = 350 Ω	13,14	
Fall Time	t_F		15		ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	50	>75		kV/μs	T_A = 25 °C V_{CC} = 30 V, V_{CM}=1500 V, with split resistors	15	10,11
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	50	>75		kV/μs			10,12

Package Characteristics

Unless otherwise noted, all Minimum/Maximum specifications are at Recommended Operating Conditions. All typical values are at T_A = 25 °C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Input-Output Momentary Withstand Voltage*	V_{ISO}	5000			V_{RMS}	RH < 50%, t = 1 min T_A = 25 °C		13, 14
Input-Output Resistance	R_{I-O}	10^9	10^{14}		Ω	V_{I-O} = 500 V_{DC}		14
Input-Output Capacitance	C_{I-O}		0.6		pF	f =1 MHz		

* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Avago Technologies Application Note 1074 "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Maximum pulse width = 100 ns, Duty cycle = 2%.
2. Derate linearly above 110 °C free-air temperature at a rate of 13 mW/°C. Refer to Figure 2 from Output IC Power Dissipation Derating Chart.
3. Total power dissipation is derated linearly above 110 °C free-air temperature at a rate of 13 mW/°C. The maximum LED and IC junction temperature should not exceed 150 °C.
4. Output is source at -2.0 A or 2.0 A with a maximum pulse width of 10 μs.
5. In this test, V_{OH} is measured with a DC load current. When driving capacitive loads V_{OH} will approach V_{CC} as I_{OH} approaches zero amperes.
6. Maximum pulse width = 1 ms.
7. This load condition approximates the gate load of a 600 V/50 A power devices.
8. Pulse Width Distortion (PWD) is defined as tPHL – tPLH for any given device.
9. Dead Time Distortion (DTD) is defined as tPLH – tPHLbetween any two parts under the same test condition. A negative DTD reduces original system dead time; while a positive DTD increases original system dead time.
10. Pin 2 and Pin 4 need to be connected to LED common.
11. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to ensure that the output will remain in the high state, (i.e., V_O > 15 V).
12. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to ensure that the output will remain in a low state (i.e., V_O < 1.0 V).
13. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second.
14. Device considered a two-terminal device: pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

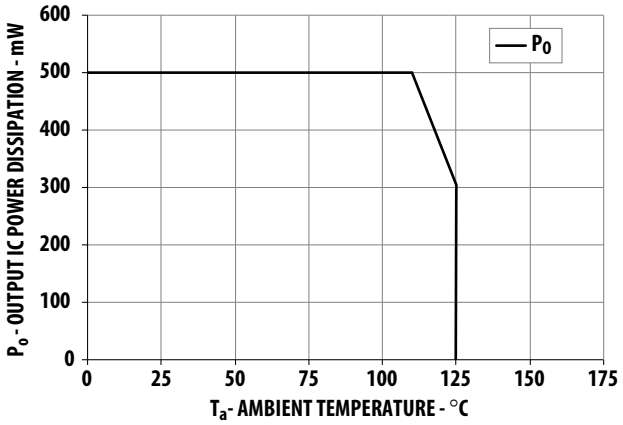


Figure 2. Output IC Power Dissipation Derating Chart

Typical Performance Plots

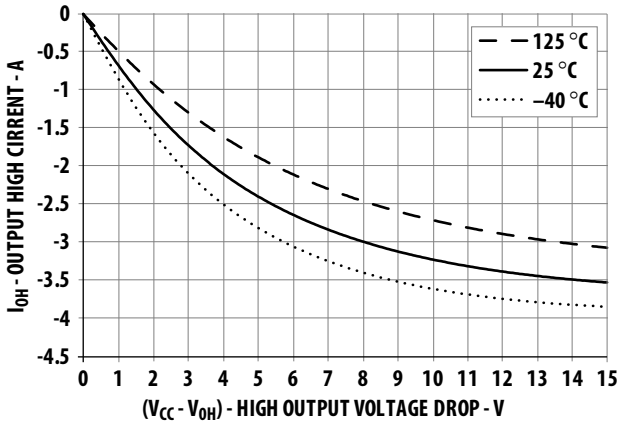


Figure 3. I_{OH} vs. (V_{CC}-V_{OH})

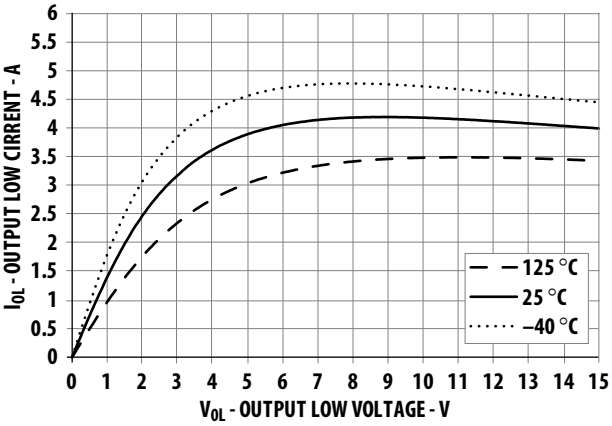


Figure 4. I_{OL} vs. V_{OL}

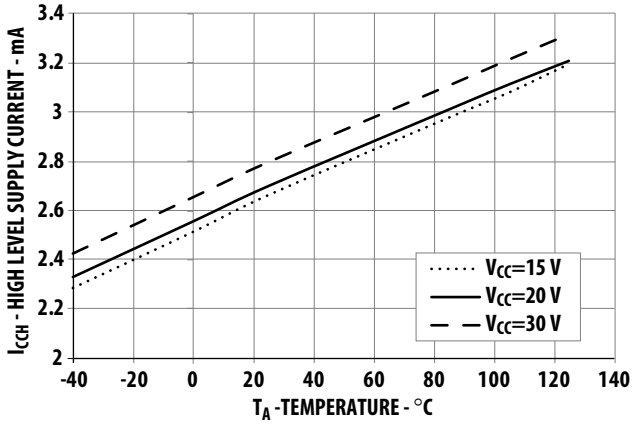


Figure 5. I_{CCH} vs. Temperature

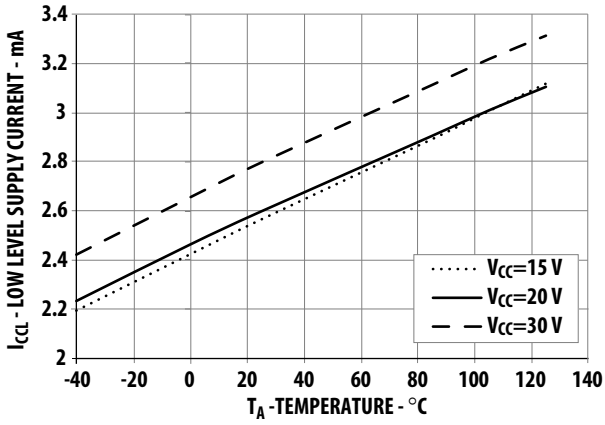


Figure 6. I_{CCL} vs. Temperature

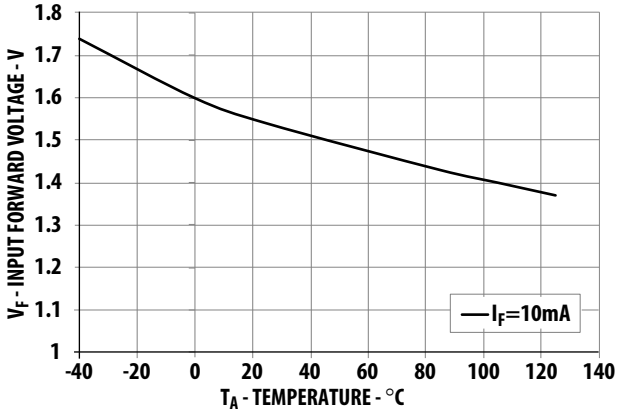


Figure 7. V_F vs. Temperature

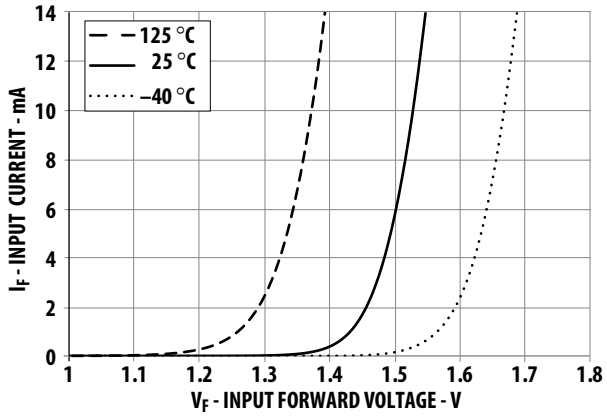


Figure 8. I_F vs. V_F

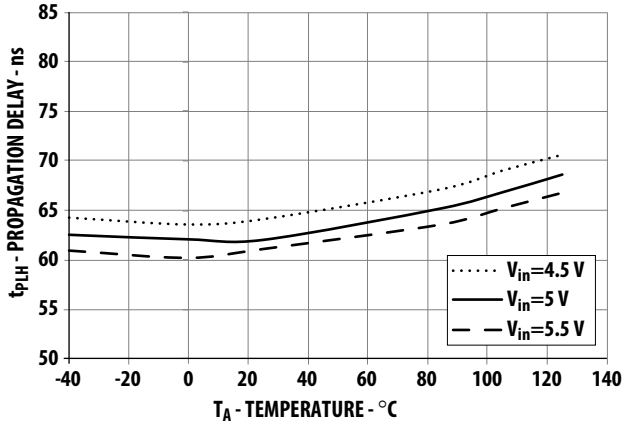


Figure 9. t_{PLH} vs. Temperature

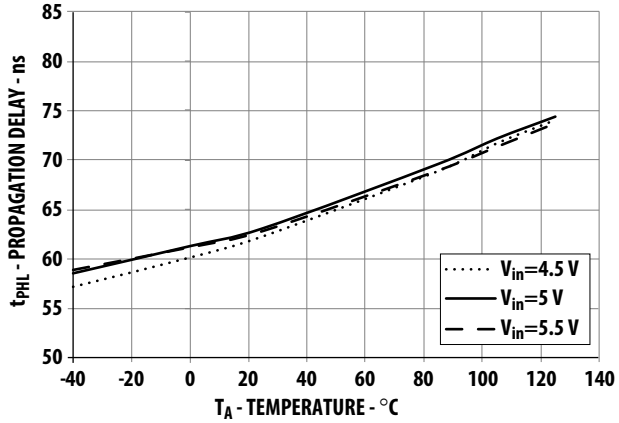


Figure 10. t_{PHL} vs. Temperature

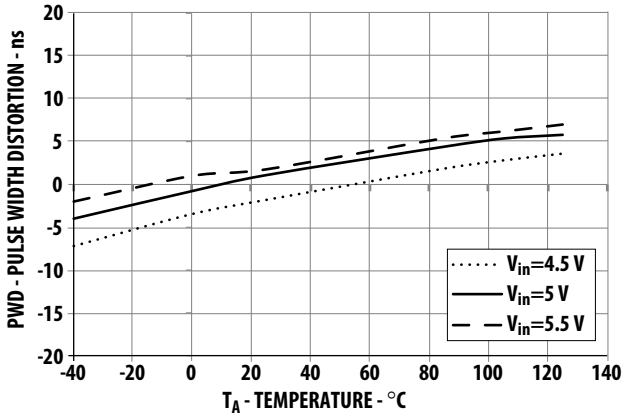


Figure 11. PWD vs. Temperature

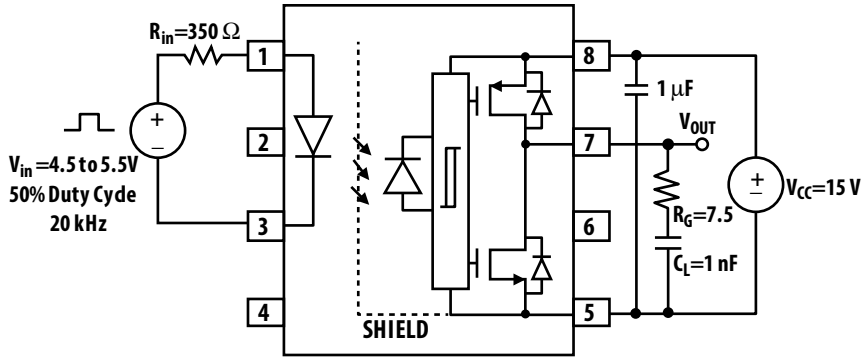


Figure 12. t_{PLH} and t_{PHL} test circuit

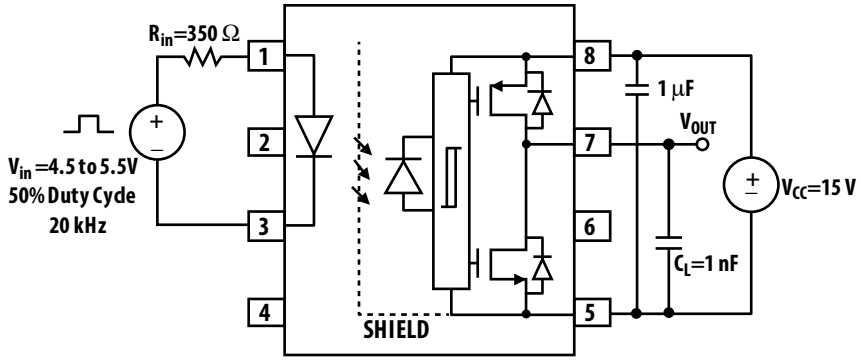


Figure 13. t_r and t_f test circuit

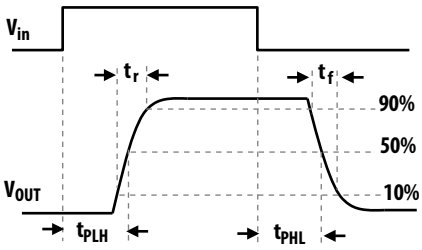


Figure 14. t_{PLH}, t_{PHL}, t_r and t_f reference waveforms

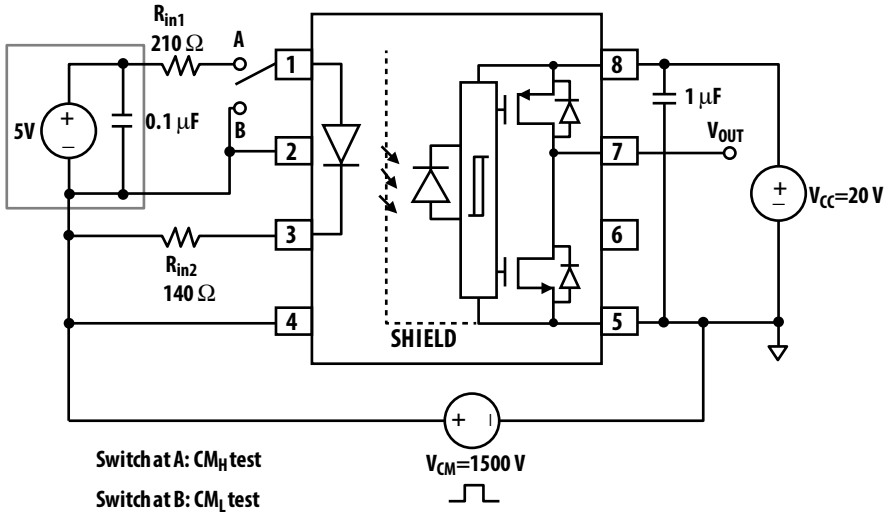


Figure 15. CMR test circuit

Typical High Speed SiC MOSFET/IGBT Gate Drive Circuit

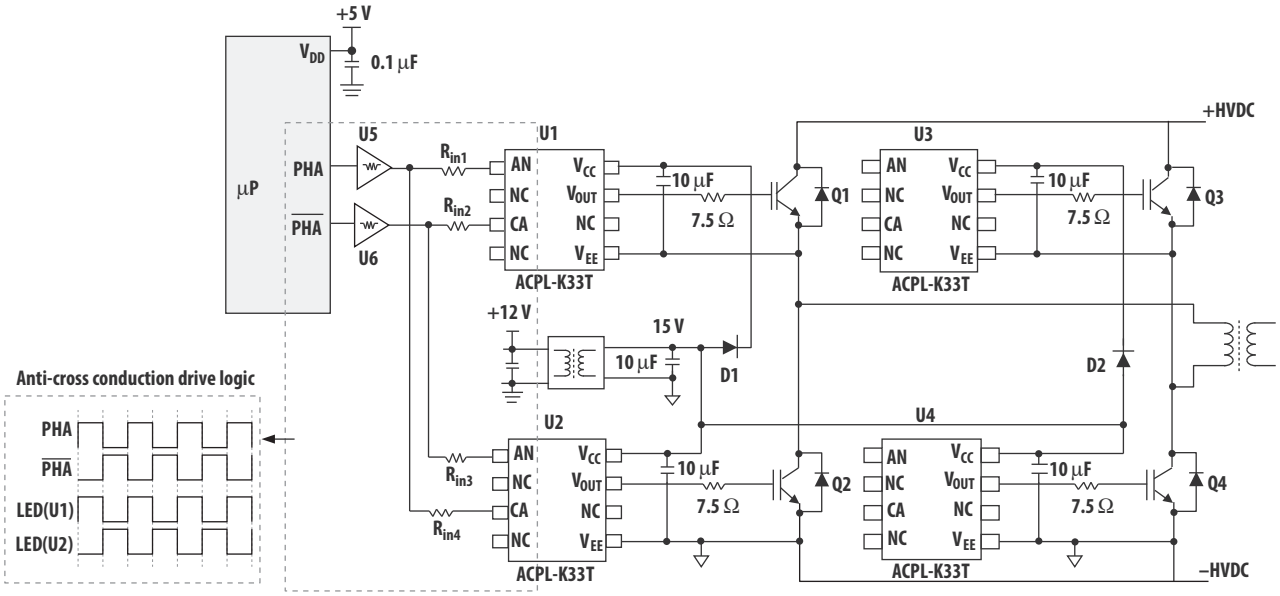


Figure 16. Typical high speed SiC MOSFET/IGBT gate drive circuit

Anti-Cross Conduction Drive

One of the many benefits of using ACPL-K33T is the ease of implementing anti-cross conduction drive between the high side and the low side gate drivers to prevent a shoot-through event. This safety interlock drive can be realized by interlocking the output of buffer U5 and U6 to both the high and the low side gate drivers, as shown in Figure 16. Due to the difference in propagation delay between optocouplers, however, a certain amount of dead time has to be added to ensure sufficient dead time at the MOSFET gate. For more details, see the "Dead Time and Propagation Delay" section.

Recommended LED Drive Circuits

There will be common mode noise whenever there is a difference in the ground level of the optocoupler's input control circuitry and that of the output control circuitry. Figure 17 and Figure 18 show the recommended LED drive circuits that use logic gate (CMOS buffer) for high common mode rejection (CMR) performance of the optocoupler gate driver. Split limiting resistors are used to balance the impedance at both anode and cathode of the input LED for high common mode noise rejection. The output impedance of the CMOS buffer (shown as R_O in Figure 17 and Figure 18) has to be included in the calculation for LED drive current.

On the other hand, Figure 19 shows the recommended LED drive circuits that use a single transistor. During the LED off state, M1 and Q1 in Figure 19 will shunt current, which results in greater power consumption. It is not recommended to have open drain and open collector drive circuits, as shown in Figure 20. This is because during the off state of the MOSFET/transistor, the cathode of the input LED sees high impedance and becomes sensitive to noise.

Drive Power

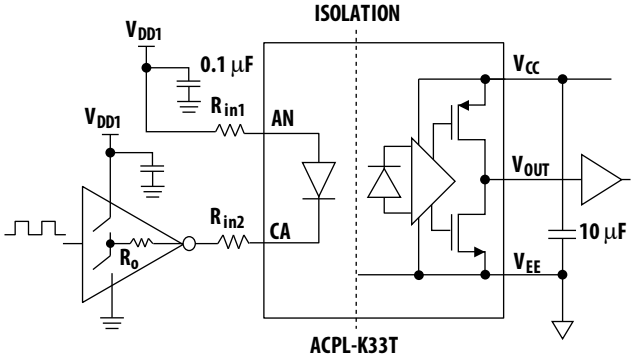
If a CMOS buffer is used to drive the LED, it is recommended that you connect the CMOS buffer at the LED cathode. This is because the sinking capability of the NMOS is usually greater than the driving capability of the PMOS in a CMOS buffer.

Drive Logic

The designer can configure LED drive circuits for non-inverting and inverting logic as recommended in Figure 17 and Figure 18. For the inverting and non-inverting logic to work, the external power supply V_{DD1} must be connected to the CMOS buffer. If the V_{DD1} supply is lost, the LED will be permanently off and output will be low.

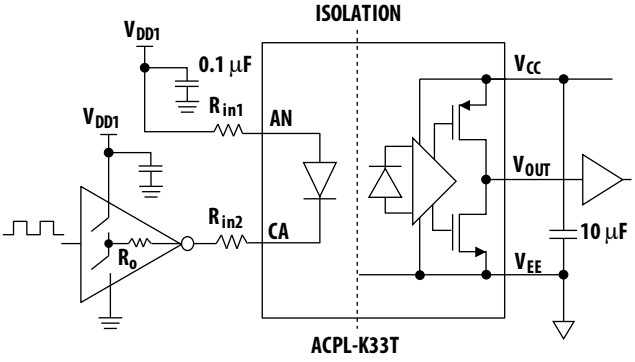
Bypass and Reservoir Capacitors

Supply bypass capacitors are necessary at the input buffer and ACPL-K33T output supply pin. A ceramic capacitor with the value of 0.1 µF is recommended at the input buffer to provide high frequency bypass, which also helps to improve CMR performance. At the output supply pin (V_{CC} – V_{EE}), it is recommended to use a 10 µF, low ESL capacitor as a charge reservoir to supply instant driving current to IGBT at V_{OUT} during switching.



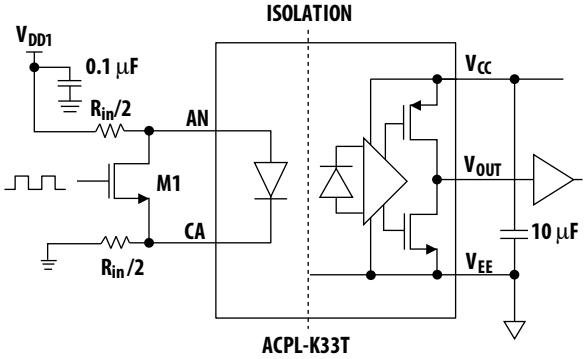
V_{DD1}= 5 V ± 10%
Ratio Rin1: (R_{in2}+R_o) = 1.5:1
Recommended R_o+R_{in1}+R_{in2} = 350 Ω

Figure 17. Recommended non-inverting logic gate drive circuit



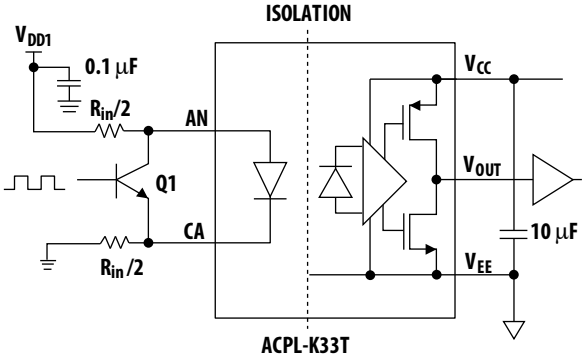
V_{DD1}= 5 V ± 10%
Ratio Rin1: (R_{in2}+R_o) = 1.5:1
Recommended R_o+R_{in1}+R_{in2} = 350 Ω

Figure 18. Recommended inverting logic gate drive circuit



V_{DD1}= 5 V ± 10%
Ratio Rin1: R_{in2} = 1.5:1
Recommended R_{in1}+R_{in2} = 350 Ω

Figure 19a. Recommended single transistor drive circuit



V_{DD1}= 5 V ± 10%
Ratio Rin1: R_{in2} = 1.5:1
Recommended R_{in1}+R_{in2} = 350 Ω

Figure 19b. Recommended single transistor drive circuit

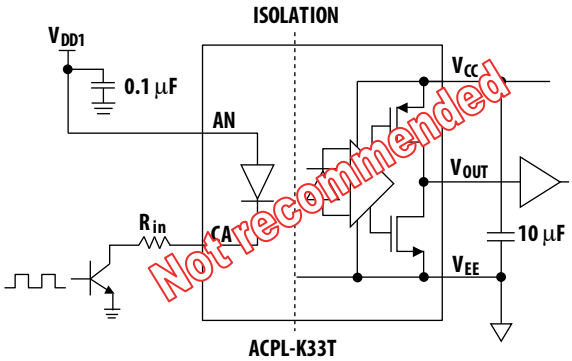


Figure 20a. Not recommended – Open drain/open collector drive circuit

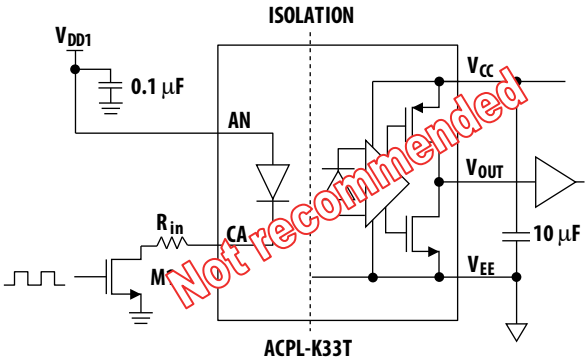


Figure 20b. Not recommended – Open drain/open collector drive circuit

Initial Power Up and UVLO Operation

Insufficient gate voltage to IGBT can increase IGBT turn-on resistance, resulting in a large power loss and damage to IGBT due to high heat dissipation. ACPL-K33T constantly monitors the output power supply. During initial power up, the ACPL-K33T requires a maximum of 50 µs initial startup time for the internal bias and circuitry to get ready. The gate driver output (V_{OUT}) is held at off state during initial startup time. Thereafter, when the output power supply is lower than the under voltage lockout (V_{UVLO-}) threshold, the gate driver output will shut off to protect IGBT from low voltage bias. When the output power supply is more than the V_{UVLO+} threshold, V_{OUT} is released from low state and it follows the input LED drive signal, as shown in Figure 21.

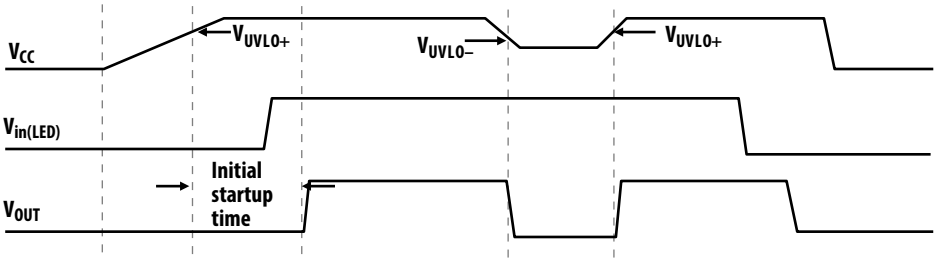


Figure 21. ACPL-K33T initial power-up and UVLO operation

Dead Time Distortion and Propagation Delay

Dead time is the period of time during which both high side and low side power transistors (shown as Q1 and Q2 in Figure 16) are off. Originally, the system is required to design in some amount of dead time to compensate for the turn-off delay needed for the MOSFET to discharge the input capacitance after the gate is switched off. In this application note, this amount of dead time is called system original dead time. When an optocoupler is used, the designer has to consider the effect of the optocoupler's dead time distortion (DTD) toward system original dead time. The optocoupler's negative DTD decreases system original dead time; on the other hand, the optocoupler's positive DTD increases system original dead time. Therefore, the designer must add extra dead time to system original dead time to compensate for the optocoupler's negative DTD. Figure 22 illustrates the effect of the optocoupler's DTD to system original dead time.

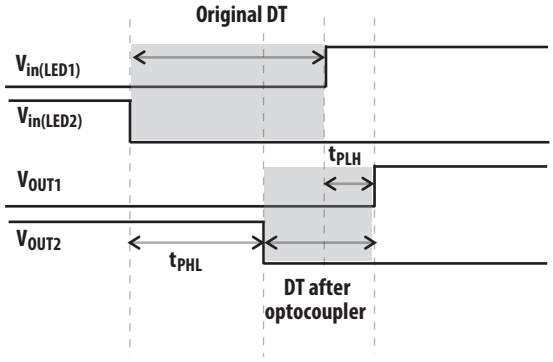


Figure 22a. Negative DTD reduces original DT

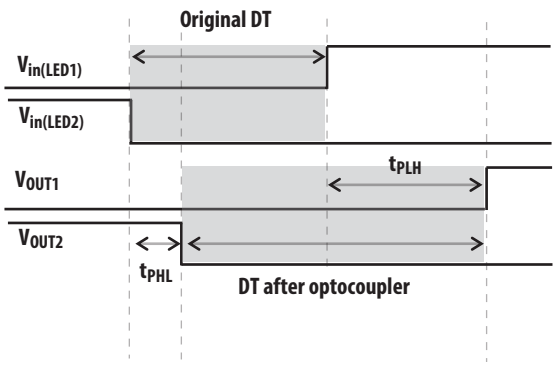


Figure 22b. Positive DTD increases original DT

Figure 22. Dead Time and Propagation Delay Waveforms

Here is an example of total dead time calculation for a typical optocoupler drive circuit for MOSFET.

Total dead time required = System original dead time + |optocoupler's negative DTD|

= System original dead time + |40 ns|

where system original dead time = MOSFET turn-off delay

Note:

The propagation delays used to calculate dead time distortion (DTD) are taken at equal temperatures and test conditions as the optocouplers used under consideration are typically mounted in close proximity to each other and are switching same type of MOSFETs.

Programmable Dead Time

Programmable dead time can be introduced to an optocoupler gate driver by adding an external capacitor (C_{DT}) across the input LED (Anode and Cathode) as shown in Figure 23. This simple circuitry offers you the flexibility to optimize gate drive switching timing for various MOSFETs and applications through hardware configuration.

The value of the external capacitor (C_{DT}) can be calculated based on the minimum dead time requirement for the system, as shown in the following equation. The added dead time will delay the turn-on timing of the gate signal, as shown in Figure 24.

$$C_{DT(min)} = - \frac{DT_{(min)}}{R_{in(min)} \ln\left(1 - \frac{V_{F(min)} - V_{in(off)}}{V_{in(on)} - V_{in(off)}}\right)}$$

where

DT: Total dead time required for a system, inclusive of original dead time and the optocoupler's negative DTD

R_{in}: Total input LED current-limiting resistor

C_{DT}: External Dead time programming capacitor

V_F: Input LED forward voltage

V_{in}: Input PWM voltage

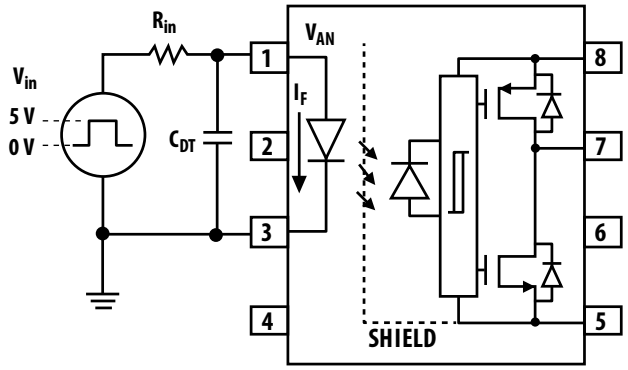


Figure 23. Add C_{DT} for dead time programming

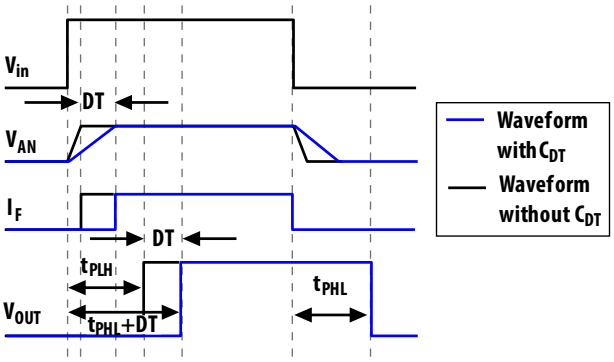


Figure 24. Timing diagram with and without C_{DT}

Thermal Resistance Model for ACPL-K33T

The diagram for measurement is shown in Figure 25. Here, one die is first heated and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the second die is heated and all the dice temperatures are recorded. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 2 by 2 matrix for our case of two heat sources.

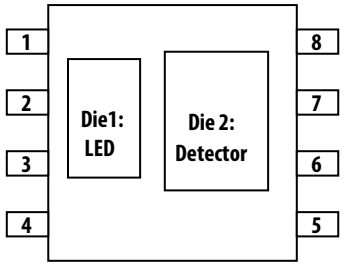


Figure 25. Diagram of ACPL-K33T for measurement

$$\begin{vmatrix} R11 & R12 \\ R21 & R22 \end{vmatrix} \cdot \begin{vmatrix} P1 \\ P2 \end{vmatrix} = \begin{vmatrix} \Delta T1 \\ \Delta T2 \end{vmatrix}$$

R11: Thermal Resistance of Die1 due to heating of Die1 (°C/W)

R12: Thermal Resistance of Die1 due to heating of Die2 (°C/W)

R21: Thermal Resistance of Die2 due to heating of Die1 (°C/W)

R22: Thermal Resistance of Die2 due to heating of Die2 (°C/W)

P1: Power dissipation of Die1 (W)

P2: Power dissipation of Die2 (W)

T1: Junction temperature of Die1 due to heat from all dice (°C)

T2: Junction temperature of Die2 due to heat from all dice (°C)

T_a: Ambient temperature (°C)

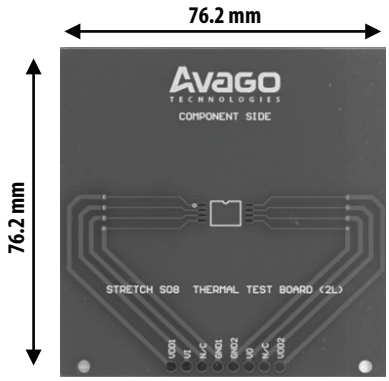
ΔT1: Temperature difference between Die1 junction and ambient (°C)

ΔT2: Temperature deference between Die2 junction and ambient (°C)

$T1 = (R11 \times P1 + R12 \times P2) + T_a$ ----------(1)

$T2 = (R21 \times P1 + R22 \times P2) + T_a$ ----------(2)

Measurement is done on both low and high conductivity boards as shown in the following:

Layout	Measurement data	
	Low conductivity board per JEDEC 51-3: R11 = 191 °C/W R12 = R21 = 68.5 °C/W R22 = 77 °C/W	High conductivity board per JEDEC 51-7: R11 = 155 °C/W R12 = R21 = 64 °C/W R22=41 °C/W

Note: These thermal resistances R11, R12, R21 and R22 can be improved by increasing the ground plane/copper area.

Application and environment design for ACPL-K33T needs to ensure that the junction temperature of the internal IC and LED within the gate drive optocoupler do not exceed 150 °C. Use equation (1) and equation (2) to estimate the junction temperatures. For example:

Calculation of LED and output IC power dissipation:

LED power dissipation, P_E = $I_{F(LED)}$ (Recommended Max) * $V_{F(LED)}$ (at 125 °C) * Duty Cycle
= 13 mA * 1.25 V * 50%
= 8.125 mW

Output IC power dissipation, P_O = V_{CC} (Recommended Max) * I_{CC}(Max) + P_{HS} + P_{LS}
= 30 V * 4.2 mA + 60 mW + 34.3 mW
= 220.3 mW

where P_{HS} = High side switching power dissipation
= $(V_{CC} * Q_G * f_{PWM}) * R_{DS,OH(MAX)}/(R_{DS,OH(MAX)} + R_{GH})/2$
= (30 V * 80 nC * 200 kHz) * 4 Ω/(4 Ω+12 Ω)/2
= 60 mW

P_{LS} = Low side switching power dissipation
= $(V_{CC} * Q_G * f_{PWM}) * R_{DS,OL(MAX)}/(R_{DS,OL(MAX)} + R_{GL})/2$
= (30 V * 80 nC * 200 kHz) * 2 Ω/(2 Ω+12 Ω)/2
= 34.3 mW

Q_G = Gate charge at supply voltage

f_{PWM} = LED switching frequency

R_{GH} = Gate charging resistance

R_{GL} = Gate discharging resistance

Calculation of LED junction temperature and output IC junction temperature at T_a=125 °C based on a high conductivity board thermal resistance model:

LED junction temperature, T1 = $(R11 \times P_E + R12 \times P_O) + T_a$
= (155 °C/W * 8.125 mW + 64 °C/W * 220.3 mW) + 125 °C
= 140 °C < T_J(absolute max) of 150 °C

Output IC junction temperature, T2 = $(R21 \times P_E + R22 \times P_O) + T_a$
= (64 °C/W * 8.125 mW + 41 °C/W * 220.3 mW) + 125 °C
= 135 °C < T_J(absolute max) of 150 °C

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