FEDL7396A/B/E-07
Issue Date: Jan. 15, 2015

ML7396A/B/E

Sub GHz band short range wireless transceiver IC

■Overview

The ML7396 family (ML7396A (915MHz band), ML7396B (920MHz band), and ML7396E (868MHz band)) are ICs for transmitting/receiving data which integrate the RF, IF, MODEM and HOST interface sections into one chip for the specified low power radio communication. The ML7396 family is used for FCC PART15, ARIB STD-108(specified low-power radio station, 920MHz-band telemeter, telecontrol and data transmission radio equipment), ETSI EN 300 220 compliant radio station, and uses a packet transmission function of IEEE802.15.4d and IEEE802.15.4g.

■Features

- Compliant to ARIB STD T-108 (ML7396B)
- Compliant to FCC Part15 (ML7396A)
- Compliant to ETSI EN 300-220 (ML7396E)
- High resolution modulation by using fractional-N PLL direct modulation.
- Modulation: GFSK / GMSK, FSK / MSK
  (MSK is FSK transmission of modulation index: m=0.5)
- Data rates: 10 / 20 / 40 / 50 / 100 / 150 / 200 kbps and 400 kbps (option)
- Data coding: NRZ and Manchester codes
- Programable channel filter suited to data rates
- Programmable frequency deviation function
- TX and RX data inverse function
- 36MHz oscillator circuit
- TCXO direct inputs available
- Oscillator capacitance fine tuning function
- Frequency fine tuning function (using fractional-N PLL)
- Synchronous serial peripheral interface (SPI)
- On chip TX PA (20mW/10mW/1mW selectable)
- External TX PA control function
- RSSI indicator and threshold judgement function
- AFC function
- Antenna diversity function
- Test pattern generator (PN9, CW, 01 pattern, all”1”, all“0”)
- FEC function
- CRC32 (Note: This function is not compliant to IEEE802.15.4g.)
- IEEE802.15.4d/g support
    - Two 256-byte FIFOs (TX/RX common use)
    - Max packet length 2047 byte (IEEE802.15.4g mode)
    - RX Preamble pattern detection function (Programmable between 1 to 15 byte)
    - Programmable TX preamble length (Max 255 byte)
    - SFD generation and detection function (Max 4 byte)
    - Programmable CRC function (CRC32, CRC16-IBM, CRC16, CRC8 or no-CRC)
    - Whitening function
    - Address filtering function
    - Automatic Acknowledge (Ack TX or RX) function
    - FEC function (IEEE802.15.4g mode)
      Note; Interleaving mode is not compliant to IEEE802.15.4g.

- Supply voltage: 1.8 to 3.6V (TX power 1mW mode)
  2.3 to 3.6V (TX power 10mW mode)
  2.6 to 3.6V (TX power 20mW mode)
- Operating temperature: -40 to +85 ˚C
- Current consumption (920MHz)

Sleep mode		0.6 µA (Typ.) (registor value retention)
Idle mode		1.4mA (Typ.)
TX	20mW	32 mA (Typ.)
	10mW	24 mA (Typ.)
	1mW	13 mA (Typ.)
RX		15 mA (Typ.) (@100kbps)

- Package
  40 pin WQFN P-WQFN40-0606-0.50
  Pb free, RoHS compliant

■Description Convention

1) Numbers description
‘0xnn’ indicates hexa decimal. ‘0bnn’ indicates binary.

Example: 0x11= 17(decimal), 0b11= 3(decimal)

2) Registers description
[<register name>: B<Bank No> <register address>] register

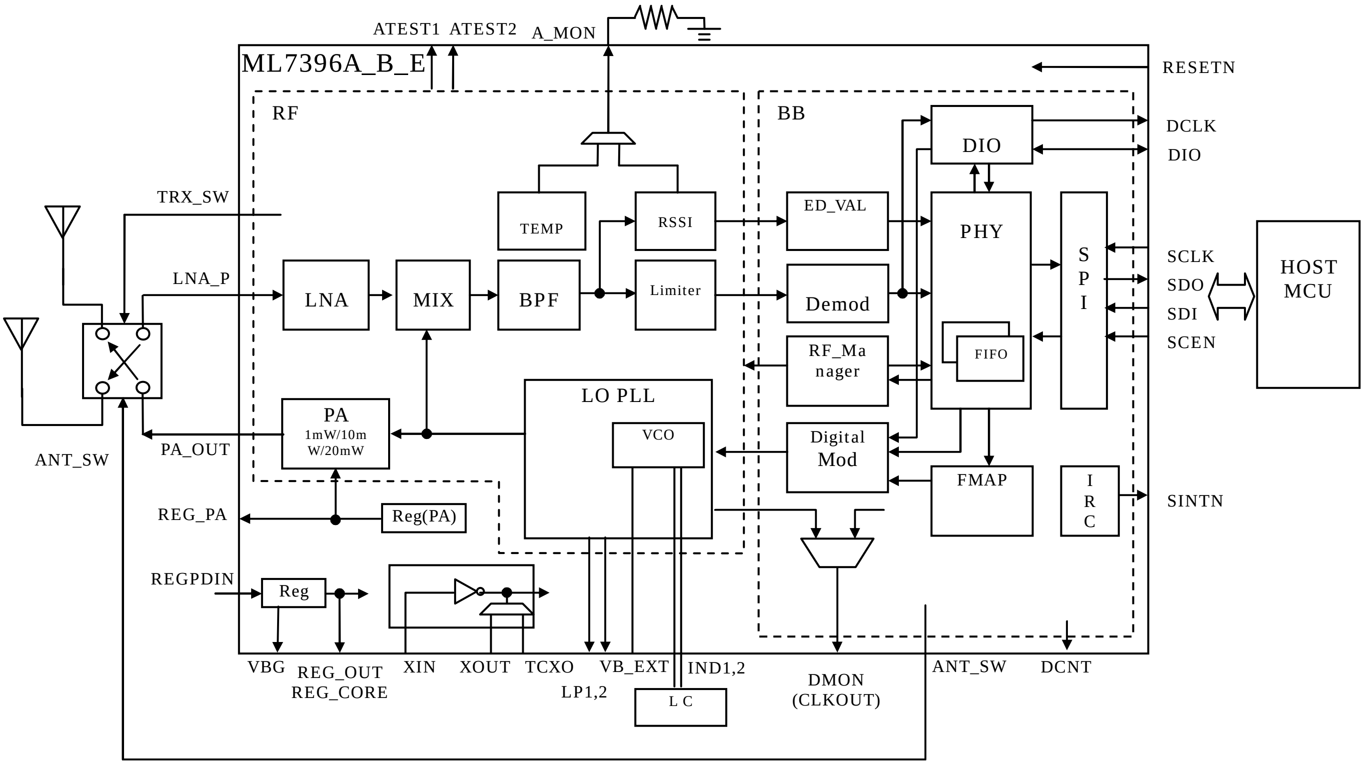
Example: **[CLK_SET:B0 0x02] register**
Register name: CLK_SET
Bank No: 0
Register address: 0x02

3) Bir name description
<bit name> ([<register name>: B<Bank No> <register address>(<bit location>)])

Example: **RATE[2:0] ([DATA_SET:B0 0x47(2-0)])**
Bit name: RATE[2:0]
Register name: DATA_SET
Bank No: 0
Register address: 0x47
Bit location: bit2 to bit0

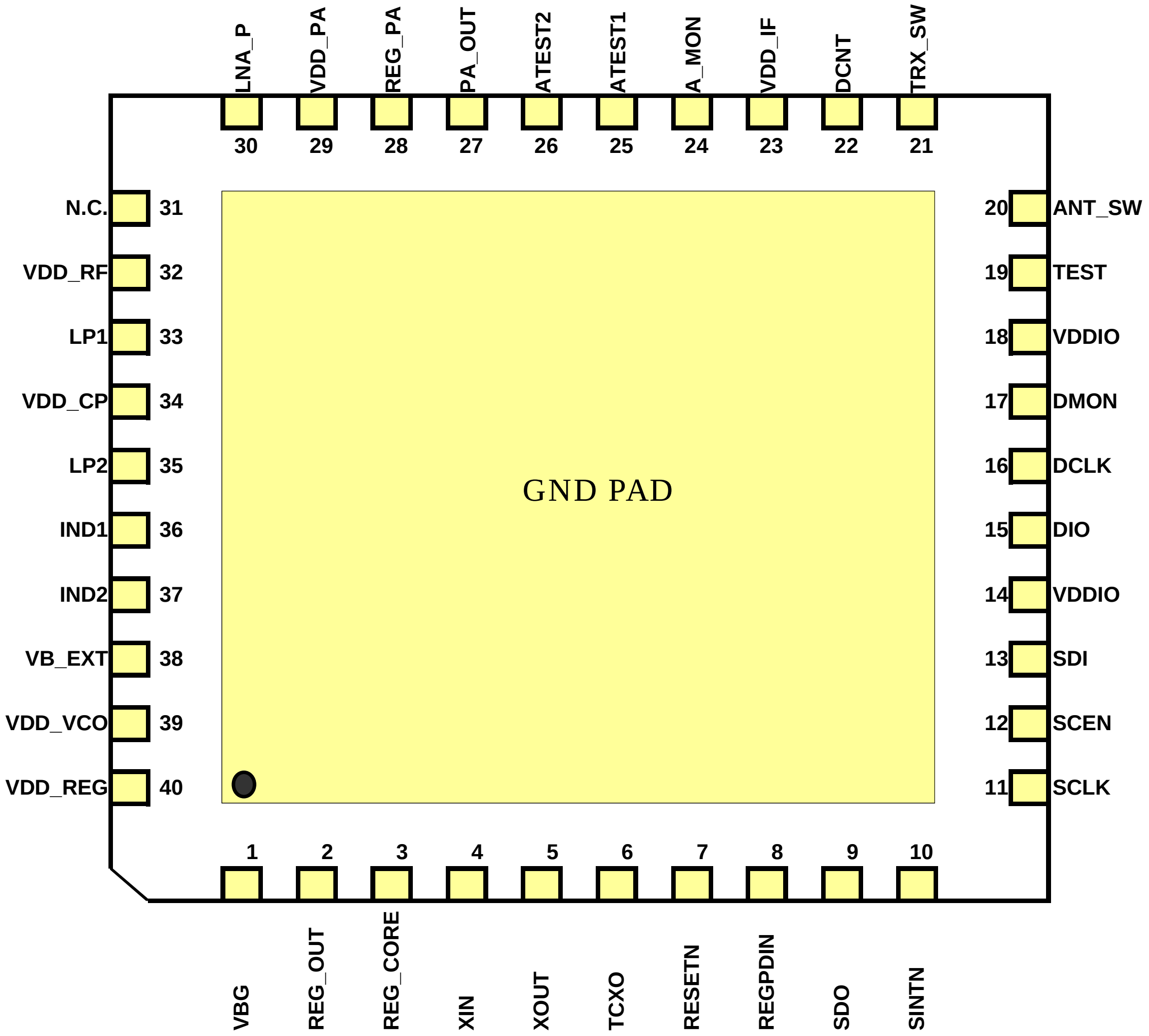
4) In this document
“TX” stands for transmittion.
“RX” stands for reception.

■Block Diagram


ATEST1
ATEST2
A_MON
ML7396A_B_E
RESETN
RF
BB
DIO
DCLK
DIO
TRX_SW
TEMP
RSSI
ED_VAL
PHY
S P I
SCLK
SDO
SDI
SCEN
HOST MCU
LNA_P
LNA
MIX
BPF
Limiter
Demod
FIFO
RF_Manager
PA
1mW/10mW/20mW
LO PLL
VCO
Digital Mod
ANT_SW
PA_OUT
REG_PA
Reg(PA)
FMAP
I R C
SINTN
REGPDIN
Reg
VBG
REG_OUT
REG_CORE
XIN
XOUT
TCXO
VB_EXT
LP1,2
IND1,2
L C
DMON (CLKOUT)
ANT_SW
DCNT

■PIN Configuration

40 Pin WQFN


LNA_P
VDD_PA
REG_PA
PA_OUT
ATEST2
ATEST1
A_MON
VDD_IF
DCNT
TRX_SW
30
29
28
27
26
25
24
23
22
21
N.C. 31
VDD_RF 32
LP1 33
VDD_CP 34
LP2 35
IND1 36
IND2 37
VB_EXT 38
VDD_VCO 39
VDD_REG 40
20 ANT_SW
19 TEST
18 VDDIO
17 DMON
16 DCLK
15 DIO
14 VDDIO
13 SDI
12 SCEN
11 SCLK
GND PAD
1
2
3
4
5
6
7
8
9
10
VBG
REG_OUT
REG_CORE
XIN
XOUT
TCXO
RESETN
REGPDIN
SDO
SINTN

NOTE) GND pad in the middle of the IC is reverse side (name: GND PAD)

■PIN Definitions

Symbols

I_{RF}	: RF input
O_{RF}	: RF output
I_A	: Analog input
I_{OS}	: Oscillator input
O_{OS}	: Oscillator output
I	: Digital input
O	: Digital output
I/O	: Digital inout
Is	: Schmitt Trigger input

●RF and Analog pins

Pin No	Pin name	Reset state	I/O	Active Level	Detail function
30	LNA_P	I	I_{RF}	-	RF antenna input
27	PA_OUT	O	O_{RF}	-	RF antenna output
36	IND1	-	-	-	Pin for VCO inductor
37	IND2	-	-	-	Pin for VCO inductor
33	LP1	-	-	-	Pin for PLL loop filter
38	VB_EXT	-	-	-	Pin for smoothing capacitor for internal bias
25	ATEST1	Hi-Z	O_{RF}	-	Test pin for analog circuit. *Left open when in normal use
26	ATEST2	Hi-Z	O_{RF}	-	Test pin for analog circuit. *Left open when in normal use
24	A_MON	Hi-Z	O_{RF}	-	Analog monitor pin (*1)

[Description]

*1 Analog monitor signal can be configured by [RSSI/TEMP_OUT:B1 0x03] register, no signal assigned as default condition.

PIN DEFINITION(continued)

●SPI interface pins

Pin No	Pin name	Reset state	I/O	Active Level	Detail function
9	SDO	O/L	O	H or L	SPI data output
13	SDI	I	Is	H or L	SPI data input
11	SCLK	I	Is	P or N	SPI clock input
12	SCEN	I	Is	L	SPI chip enable L: enable H: disable
10	SINTN	O/H	O	L	SPI interrupt output L: interrupt occurs H: -

●DIO interface pins

Pin No	Pin name	Reset state	I/O	Active Level	Detail function
15	DIO	O/L	I/O	H or L	DIO data input/output
16	DCLK	O/L	O	P or N	DIO clock output

●Regulator pins

Pin No	Pin name	Reset state	I/O	Active Level	Detail function
2	REG_OUT	-	-	-	Regulator output (typ.1.5V) (Cap 10uF) Note: This pin will output 0V in the sleep state
3	REG_CORE	-	-	-	Monitor pin for power supply to digital core(typ.1.5V) (Cap 10uF)
1	VBG	-	-	-	Pin for decoupling capacitor pin (Cap 0.1uF)
8	REGPDIN	I	I	H	Power down pin for regulator * Fix to “L” for normal use
28	REG_PA	-	-	-	Regulator output for PA block Note: This pin will output 0V in the sleep state

PIN DEFINITION(continued)

●Miscellaneous pins

Pin No	Pin name	Reset state	I/O	Active Level	Detail function
7	RESETN	I	Is	L	Hardware reset L: Hardware reset enable H: normal operation
4	XIN	I	Ios	P or N	36MHz crystal pin1 *Fixed to GND in case of using external clock
5	XOUT	O	Oos	P or N	36MHzcristal pin2 *Fixed to GND in case of using external clock
6	TCXO	I	I_A	-	External clock (TCXO) input pin. *Fixed to GND in case of using crystal oscillator
20	ANT_SW	O/L	O	H or L or OD	Diversity control signal
21	TRX_SW	O/L	O	H or L or OD	TX-RX switch signal
19	TEST	I	I	H	Test mode input Fixed to “L” for normal use
17	DMON*1	O	O	H	Digital monitor pin Primary function: Clock output (6MHz) Secondary function: PLL_LD output Third function: FIFO trigger output
22	DCNT	O/L	O	H or L or OD	External TX PA control signal
31,35	N.C.	-	-	-	Non connection

[Description]

*1 Function of DMON pin can be selected by following condition. Clock output as a default.
If clock output is not used, please select another function. Please refer to each register description for more details.
Primary function will have higher priority when multiple function are configured simultaneously.

Configuration of DMON output

Function Name	Configuration register name	Address	Bit position (bit symbol)
CLK output	CLK_SET	B0 0x02	bit4 (CLKOUT_EN)
PLL_LD output	PLL_MON/DIO_SEL	B0 0x69	bit4 (PLL_LD)
FIFO trigger output	CRC_AREA/FIFO_TRG	B0 0x77	bit0 (FIFO_TRG_EN)

●Power supply pins

Pin No	Pin name	Reset state	I/O	Active Level	Detail function
14,18	VDDIO	-/-	PWR	-	Power supply for digital IOs (Input voltage: 1.8V to 3.3V)
40	VDD_REG	-/-	PWR	-	Power supply for regulator input (Input voltage: 1.8V to 3.3V)
29	VDD_PA	-/-	PWR	-	Power supply for PA block (Input voltage: 1.8V to.3.3V, depending on TX mode)
32	VDD_RF	-/-	PWR	-	Power supply for RF blocks (REG_OUT is connected, typ.1.5V)
23	VDD_IF	-/-	PWR	-	Power supply for IF block (REG_OUT is connected, typ.1.5V)
34	VDD_CP	-/-	PWR	-	Power supply for charge pump (REG_OUT is connected, typ.1.5V)
39	VDD_VCO	-/-	PWR	-	Power supply for VCO (REG_OUT is connected, typ.1.5V)
EL	-	-/-	GND	-	GND PAD

●Unused pins

Unused pins treatments are as follows:

Pin Name	Pin number	Recommended treatment
XIN	4	Fixed to GND (When TCXO is used)
XOUT	5	Fixed to GND (When TCXO is used)
TCXO	6	Fixed to GND (When crystal OSC is used)
ATEST1	25	Left OPEN
ATEST2	26	Left OPEN
A_MON	24	Left OPEN
ANT_SW	20	Left OPEN
DMON	17	Left OPEN *1
DCNT	22	Left OPEN

*1 If not using DMON, it is necessary to stop clock out (default output on DMON) by CLKOUT_EN ([CLK_SET:B0 0x02(4)]). Left open with enableing clock out causes the perfoemance down on RX sensitivity.

Note: If input pins are high-impedence state and leave open, excess current could be drawn. Care must be taken that unused input pins and unused I/O pins should not be left open.

■Electrical Characteristics

●Absolute maximum ratings

Item	Symbol	Condition	Rating	Unit
Power Supply (I/O) (*1)	V_{DDIO}	Ta=-40 to 85 ˚C GND=0V	-0.3 to +4.6	V
Power Supply (RF) (*2)	V_{DDRF}		-0.3 to +2.0	V
Digital Input Voltage	V_{DIN}		-0.3 to V_{DDIO}+0.3	V
RF Input Voltage	V_{RFIN}		-1.0 to +2.0	V
Analog Input Voltage	V_{AIN}		-0.3 to V_{DDIO}+0.3	V
Analog Input Voltage2 (*3)	V_{AIN2}		-0.3 to V_{DDRF}+0.3	V
TCXO Input Voltage	VTCXO		-0.3 to +1.75	V
Digital Output Voltage	V_{DO}		-0.3 to V_{DDIO}+0.3	V
RF Output Voltage	V_{RFO}		-0.3 to V_{DDRF}+1.9	V
Analog Output Voltage	V_{AO}		-0.3 to V_{DDIO}+0.3	V
Analog Output Voltage2 (*4)	V_{AO2}		-0.3 to V_{DDRF}+0.3	V
Digital Input Current	I_{DI}		-10 to +10	mA
RF Input Current	I_{RF}		-2 to +2	mA
Analog Input Current	I_{AI}		-2 to +2	mA
Analog Input Current2 (*3)	I_{AI2}		-2 to +2	mA
TCXO Input Current	ITCXO		-2 to +2	mA
Digital Output Current	I_{DO}		-8 to +8	mA
RF Output Current	I_{RFO}		-2 to +60	mA
Analog Output Current	I_{AO}		-2 to +2	mA
Analog Output Current2 (*4)	I_{AO2}		-2 to +2	mA
Power Dissipation	P_d	Ta=+25 ˚C	300	mW
Storage Temperature	T_{stg}	-	-55 to +150	˚C

*1 VDD_IO, VDD_REG, VDD_PA pins
*2 VDD_RF, VDD_IF, VDD_VCO, VDD_CP pins
*3 XIN, TCXO pins
*4 XOUT pin

- Recommended operating conditions

Item	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply (I/O)	V_{DDIO}	VDD_IO, VDD_REG pins	1.8	3.3	3.6	V
Power Supply (PA)	V_{DDPA}	VDD_PA pin TX power 1mW mode	1.8	3.3	3.6	V
		VDD_PA pin TX power 10mW mode	2.3	3.3	3.6	V
		VDD_PA pin TX power 20mW mode	2.6	3.3	3.6	V
Power Supply (RF) (*2)	V_{DDRF}	VDD_RF, VDD_IF, VDD_VCO, VDD_CP pins	1.4	1.5	1.6	V
Operating Temperature	T_a	-	-40	+25	+85	˚C
Digital Input Rising Time	T_{IR}	Digital input pins (*1)	-	-	20	ns
Digital Input Falling Time	T_{IF}	Digital Input pins (*1)	-	-	20	ns
Digital Output Loads	C_{DL}	All Digital Output pins	-	-	20	pF
Master Clock1 Accuracy (Crystal)	F_{MCK1}	XIN, XOUT pins	-20ppm (*3)	36	+20ppm (*3)	MHz
Master Clock2 Accuracy (TCXO)	F_{MCK2}	TCXO pin	-20ppm (*3)	36	+20ppm (*3)	MHz
TCXO Input Voltage	V_{TCXO}	DC cut	0.8	-	1.5	Vpp
SPI clock frequency	F_{SCLK}	SCLK pin	0.032	2	16	MHz
SPI clock duty ratio	D_{SCLK}	SCLK pin	45	50	55	%
RF channel frequency	F_{RF}	LNA_P,PA_OUT pins	863	-	960	MHz

*1 Those pins with symbol I, Is at pin definition section
*2 Use REG_OUT output of this LSI.
*3 It’s max.+10ppm and min.-10ppm at 10kbps setting.

[Note]
Electrical characteristics are in the above recommended operating conditions without special instruction.

* Following "Typ" value is not guaranteed value studied variation of IC but typical centre value.

●Power consumption

Item	Symbol	Conditions	Min	Typ (*2)	Max	Unit
Power Consumption (*1)	IDD1	Sleep state (Retaining register values)	-	0.6	3.0(*3)	µA
	IDD2	Idle state	-	1.4	3.0	mA
	IDD3	RF RX state (*4)	-	15.0	20.0	mA
	IDD4	RF TX state (1mW) (*4)	-	13.0	20.0	mA
	IDD5	RF TX state (10mW) (*4)	-	24.0	35.0	mA
	IDD6	RF TX state (20mW) (*4)	-	32.0	43.0	mA

*1 Power consumption is sum of current consumption of all power supply pins
*2 "Typ" value is centre value under condition of VDDIO=3.3V, 25 ˚C.
*3 This "Max" value is under condition of 25 ˚C. Other "Max" values are defind under recommended operating coditions.
*4 Current consumption when the data rate is 100kbps and the RF frequency is 920MHz.

●DC characteristics

Item	Symbol	Conditions	Min	Typ (*2)	Max	Unit
Voltage Input High	VIH1	Digital input/inout pins	V_{DDIO} * 0.75	-	V_{DDIO}	V
	VIH2	XIN pin	V_{DDRF} *0.9	-	V_{DDRF}	V
Voltage Input Low	VIL1	Digital input/inout pins	0	-	V_{DDIO} *0.18	V
	VIL2	XIN pin	0	-	V_{DDRF} *0.1	V
Schmitt trigger Threshold High level	VT+	RESETN pin SDI, SCLK, SCEN pins	-	1.2	V_{DDIO} *0.75	V
Schmitt Trigger Threshold Low level	VT-	ESETN pin SDI, SCLK, SCEN pins	V_{DDIO} *0.18	0.8	-	V
Input Leakage Current	IIH1	Digital input/inout pins	-1	-	1	µA
	IIH2	XIN pin	-0.3	-	0.3	µA
	IIL1	Digital input/inout pins	-1	-	1	µA
	IIL2	XIN pin	-0.3	-	0.3	µA
Tri-state Output Leakage Current	IOZH1	Digital inout pins	-1	-	1	µA
	IOZL1	Digital inout pins	-1	-	1	µA
Voltage Output Level H	VOH	IOH=-4mA /-2mA (*1)	V_{DDIO} *0.8	-	V_{DDIO}	V
Voltage Output Level L	VOL	IOL=4mA /2mA (*1)	0	-	0.3	V
Regulator output Voltage	REG_CORE (*2)	Sleep state	0.95	1.3	1.65	V
		Other states	1.40	1.5	1.60	V
Pin Capacitance	CIN	Input pins	-	6	-	pF
	COUT	Output pins	-	9	-	pF
	CRFIO	RF inout pins	-	9	-	pF
	CAI	Analog input pins	-	9	-	pF

*1 DMON pin is IOH=-2mA/2mA
*2 REG_CORE pin and REG_OUT pin. REG_OUT pin becomes 0V when in sleep state.

●RF characteristics

Data Rate	:	10kbps/ 20kbps/ 40kbps/ 50kbps/100kbps/ 150kbps/200kbps/ 400kbps
Modulation scheme	:	GFSK
Channel spacing	:	200kHz/400kHz/600kHz
Frequency	:	Support 750MHz to 1GHz by changing L/C components between IND1 and IND2 pins
Others		Definition point is a antenna connector in the reference circuit.
	:	RF characteristics out of below table include 400kbps (option) are available as reference data separately.

[TX]

Item	Condition	Min	Typ	Max	Unit
TX Power	20mW (13dBm) mode	9	13	15	dBm
	10mW (10dBm) mode	6	10	12	dBm
	1mW (0dBm) mode	-4	0	2	dBm
Frequency deviation setting range [Fdev] (*1)		-	-	2,250	kHz
920MHz band (920.5MHz to 928.1MHz)					
Occupied bandwidth	n : number of channel	-	-	200 * n	kHz
Power at channel edge	20mW mode (920.5MHz to 922.3MHz)	-	-	-7	dBm
	10mW mode	-	-	-10	dBm
	1mW mode	-	-	-20	dBm
Adjacent Channel Power	20mW mode ±1ch, bandwidth 200kHz)	-	-33	-15	dBm
	10mW mode +/-1ch bandwidth: 200kHz	-	-39	-18	dBm
	1mW mode +/-1ch bandwidth: 200kHz	-	-47	-26	dBm
Spurious emission level (20mW mode)	710MHz or lower, 100kHz band	-	-65	-36	dBm
	Higher than 710MHz to 900MHz, 1MHz band	-	-70	-55	dBm
	Higher than 900MHz to 915MHz, 100kHz band	-	-72	-55	dBm
	Higher than 915MHz to 930MHz, 100kHz band (Excluding within 200 + 100*n kHz above and below the channel frequency, however, within 100 + 100*n kHz above and below for 920.5MHz to 922.3MHz. n is the number of concurrently used channels)	-	-51	-36	dBm
	Higher than 930MHz to 1000MHz, 100kHz band	-	-70	-55	dBm
	Higher than 1000MHz to 1215MHz, 1MHz band	-	-75	-45	dBm
	Higher than 1215MHz, 1MHz band (2nd harmonics or higher)	-	-40	-30	dBm
915MHz band (902MHz to 928MHz)					
6dB bandwidth	Frequency deviation=171kHz	500	-	-	kHz
Power spectrum density	20mW mode, frequency deviation = 171kHz, 3kHz band	-	-	8	dBm
Spurious emission level (20mW mode)	900MHz or lower	-	-65	-56	dBm
	Higher than 960MHz (2nd harmonics or higher)	-	-50	-41	dBm
868MHz band (863MHz to 870MHz) (*2)					
Spurious emission level (10mW mode)	Higher than 1000MHz (2nd harmonics or higher)	-	-35	-30	dBm

*1 While the setting range is described as above, the possible maximum value depends on the RF channel frequency to be used. RF channel frequency ± frequency deviation should not include a multiple of 36MHz (864MHz, 900MHz, 936MHz, and so on).
Example) For 902MHz, 2,000kHz is a possible maximum frequency deviation value.

*2 863.5MHz to 866.2MHz cannot be used. For details, refer section "Programing Channel Frequency."

[RX]

Item	Condition	Min	Typ	Max	Unit
920MHz band (920.5MHz to 928.1MHz)					
Minimum RX sensitivity BER<0.1%	50kbps mode (*1)	-	-108	-102	dBm
	100kbps mode (*1)	-	-106	-100	dBm
	200kbps mode (*1)	-	-102	-97	dBm
Maximum input level	50kbps mode/100kbps mode/200kbps mode	0	-	-	dBm
Adjacent channel selectivity	50kbps mode	20	35	-	dB
	100kbps mode	20	35	-	dB
	200kbps mode	20	35	-	dB
Alternate channel selectivity	50kbps mode	30	45	-	dB
	100kbps mode	30	45	-	dB
	200kbps mode	30	45	-	dB
Minimum energy detection level [ED value]		-	-	-100	dBm
Energy detection range	Dynamic range	60	70	-	dB
Energy detection accuracy		-6	-	+6	dB
Spurious emission level ARIB T108 measurement condition 915.9MHz~916.9MHz 920.5MHz~929.7MHz	710MHz or lower, 100kHz band	-	<-93	-54	dBm
	Higher than 710MHz to 900MHz, 1MHz band	-	<-83	-55	dBm
	Higher than 900MHz to 915MHz, 100kHz band	-	<-93	-55	dBm
	Higher than 915MHz to 930MHz, 100kHz band	-	-63	-54	dBm
	Higher than 930MHz to 1000MHz, 100kHz band	-	<-93	-55	dBm
	Higher than 1000MHz	-	-57	-47	dBm
915MHz band (902MHz to 928MHz)					
Minimum receiver sensitivity BER<0.1%	100kbps mode (modulation index = 1) (*1)	-	-106	-99	dBm
	150kbps mode (modulation index = 0.5) (*1)	-	-102	-96	dBm
	200kbps mode (modulation index = 1) (*1)	-	-102	-96	dBm
	100kbps mode (frequency shift: 171kHz)	-	-100	-87	dBm
	150kbps mode (frequency shift: 171kHz)	-	-97.5	-84	dBm
	200kbps mode (frequency shift: 171kHz)	-	-96.5	-83	dBm
868MHz band (863MHz to 870MHz) (*2)					
Minimum receiver sensitivity BER<0.1%	50kbps mode (*1)	-	-108	-102	dBm
	100kbps mode (*1)	-	-106	-100	dBm
	200kbps mode (*1)	-	-102	-97	dBm
Collateral emission level	1000MHz or lower (local frequency)	-	-63	-57	dBm
	Higher than 1000MHz	-	-57	-47	dBm

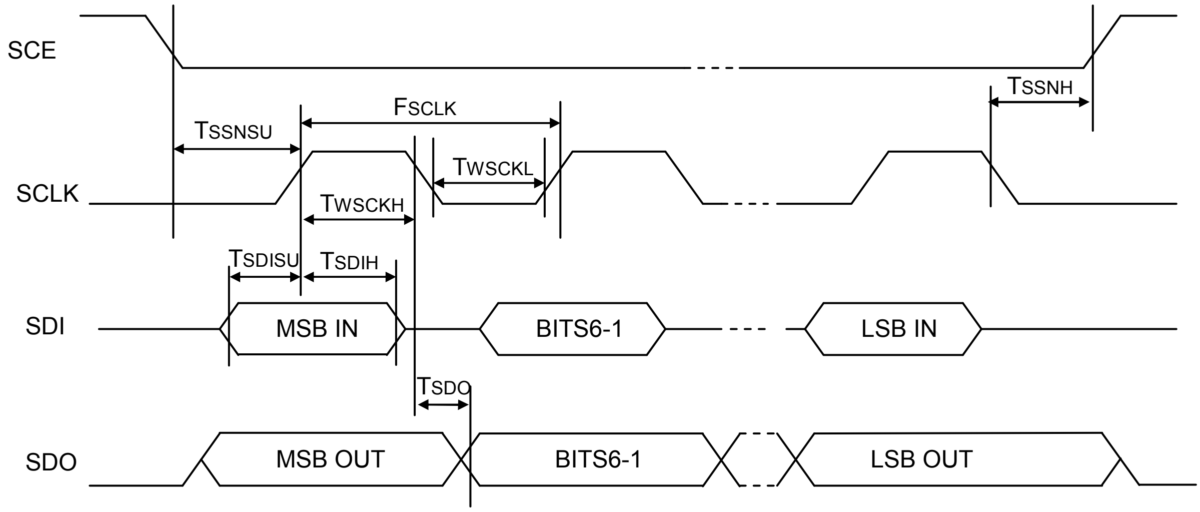
*1 When NBO_SEL([DATA_SET:B0 0x47(7)])=0b0.

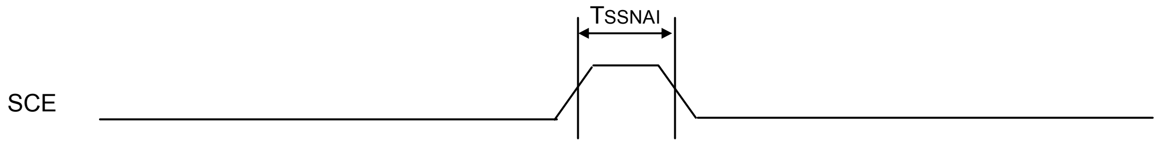
*2 863.5MHz to 866.2MHz cannot be used. For details, refer section "Programing Channel Frequency."

- SPI interface characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
SCLK clock frequency	FSCLK	Load capacitance CL=20pF	0.032	2	16	MHz
SCEN input setup time	TSSNSU		30	-	-	ns
SCEN input hold time	TSSNH		30	-	-	ns
SCLK high pulse width	TWSCKH		28	-	-	ns
SCLK low pulse width	TWSCKL		28	-	-	ns
SDI input setup time	TSDISU		5	-	-	ns
SDI input hold time	TSDIH		15	-	-	ns
SCEN negate interval	TSSNAI		60	-	-	ns
SDO output delay time	TSDO		-	-	22	ns

[Note]
All timing parameter is defined at voltage level of V_{DDIO} * 20% and V_{DDIO} * 80%.


SCE
TSSNH
FSCLK
TSSNSU
TWSCKL
SCLK
TWSCKH
TSDISU
TSDIH
SDI
MSB IN
BITS6-1
LSB IN
TSDO
SDO
MSB OUT
BITS6-1
LSB OUT

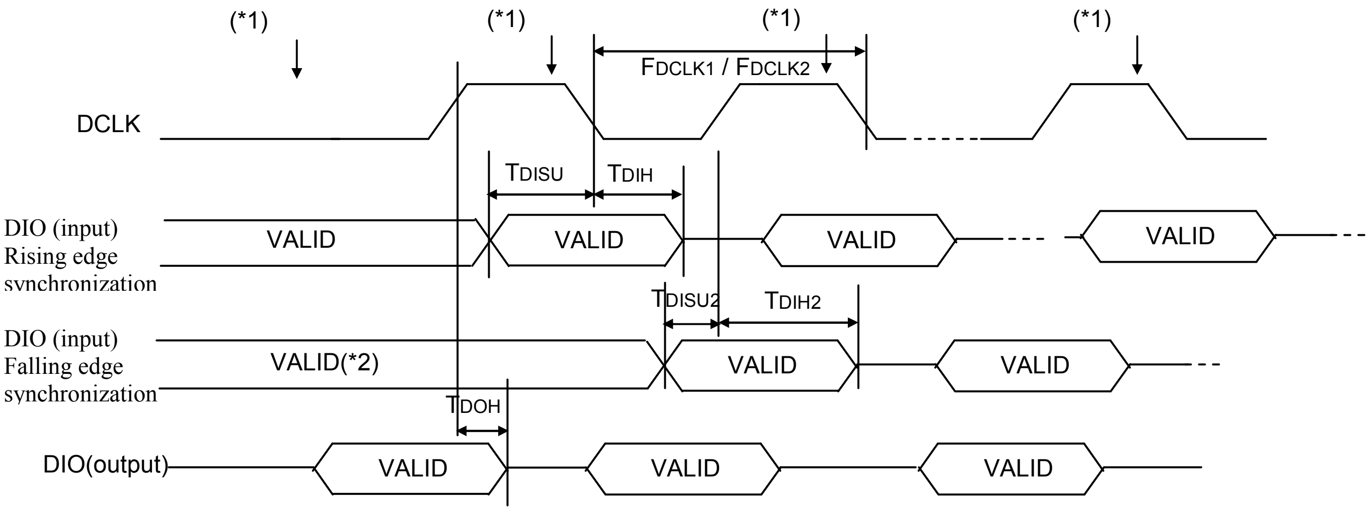


●DIO interface characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
DIO input setup time (Rising edge synchronization)	TDISU	Load capacitance CL=20pF	1	-	-	µs
DIO input setup time (Falling edge synchronization)	TDISU2		0	-	-	µs
DIO input hold time (Rising edge synchronization)	TDIH		0	-	-	ns
DIO input hold time (*3) (Falling edge synchronization)	TDIH2		10 5 2.5	-	-	µs
DIO Output hold time	T_{DOH}		20	-	-	ns
DCLK frequency (*1) (*3) (TX)	F_{DCLK1}		-20ppm	50 100 200	+20ppm	kHz
DCLK frequency (*2) (*3) (RX)	F_{DCLK2}		-4%	50 100 200	+4%	kHz
DCLK output duty ratio (TX)	D_{DCLK}		-	50	-	%
DCLK output duty ratio (RX)	D_{DCLK}		40	-	60	%

*1 DCLK clock frequency in TX mode will be varied depending on the variance of master clock frequency.
*2 DCLK clock frequency in RX mode will be varied by reproduced clock and its jitter.
*3 These characteristics are depend on the setting to the RATE [2:0] ([DATA_SET:B0 0x47(2-0)].
(upper: 50kbps, mid: 100kbps, lower: 200kbps)

[Note]
All timing parameter is defined at voltage level of V_{DDIO} * 20% and V_{DDIO} * 80%


(*1)
(*1)
(*1)
(*1)
FDCLK1 / FDCLK2
DCLK
TDISU
TDIH
DIO (input)
Rising edge
synchronization
VALID
VALID
VALID
VALID
TDISU2
TDIH2
DIO (input)
Falling edge
synchronization
VALID(*2)
VALID
VALID
TDOH
DIO(output)
VALID
VALID
VALID

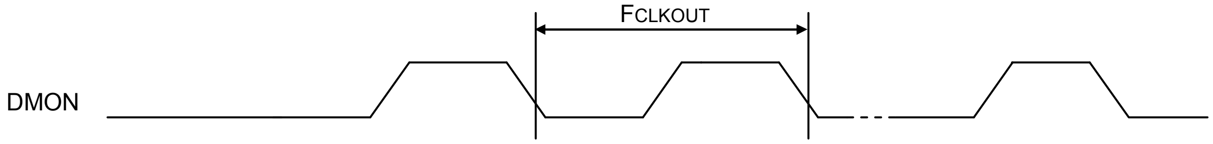
(*1) Timing when ML7396 takes the DIO input.
(*2) For the falling edge synchronization, the first two bits of DIO input have the same data, refer section “TX mode (with DIO mode)”

●Clock output characteristics

Clock output can be controled by [CLK_SET:B0 0x02] register (Initial value:enable), Clock output from DMON pin.

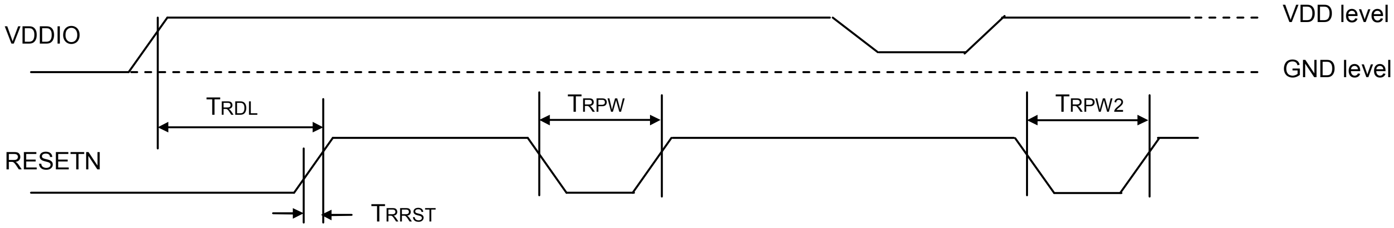
Item	Symbol	Condition		Min	Typ	Max	Unit
Clock output frequency	F_{CLKOUT}	Load capacitance CL=20pF	-	0.0088	6	36	MHz
Clock output duty ratio (*1)	D_{CLKOUT}		12MHz	30	-	70	%
			Other than above	48	50	52	%

*1 Duty ratio will be H:L = 1:2 when output frequency is 12MHz.. Refer [CLK_OUT: B0 0x03] register ().



●Reset

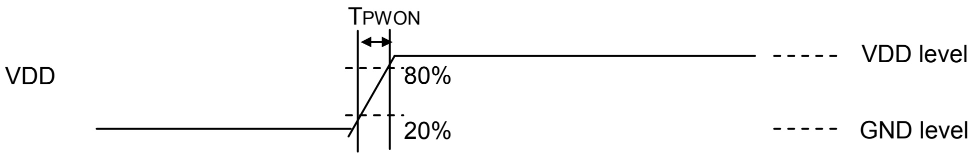
Item	Symbol	Condition	Min	Typ	Max	Unit
RESETN delay time (Power on)	T_{RDL}	All power supply pins (After power on)	1.5	-	-	ms
RESETN pulse period (When starting from VDDIO=0V)	T_{RPW}		200	-	-	ns
RESETN pulse period 2 (*1) (When starting from VDDIO≠0V)	TRPW2	VDD>1.8V	1.5	-	-	ms
RESETN rising period	TRRST		-	-	1	ms



(*1) When starting from VDDIO≠.0V, input a pulse to the RESETN signal after VDDIO exceeds 1.8V.

●Power on sequence

Item	Symbol	Condition	Min	Typ	Max	Unit
Power on time	T_{PWON}	Power on state (All power supply pins)	-	-	5	ms


TPWON
VDD
80%
20%
VDD level
GND level

■Registers

●Register map

It is consist of 3bank, BANK0, BANK1, BANK2. Each BANK has address space of 0x00 to 0x7F, 128 byte in total.
The space shown as gray highlighted part is not implemented in LSI or reserved bits. TX/RX FIFO is implemented in PHY block, those register except for FIFO is implemented in SPI block. The address not exist in the memory map is not accessible. Also, the address is not accessible during the VCO calibration.

In each BANK, there are some registers that can not be access unless give access allowance by TST_ACEN ([BANK_SEL: B0/B1/B2 0x00(7)] =0b1. Such registers are marked with "#" in the following list. The TST_ACEN enable setting is required in the initial setting or test mode setting, but it is recommended to set disable when in normal operation to avoid miss-setting.

For registers whose setting value is specified by the "ML7396Family_InitialRegisterSetting" file, please set the value shown in the file.

☐ : Implemented as functionable register
▨ : Implemented as reserved bits

BANK0

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x00	BANK_SEL		▨	▨	▨	▨	▨			Register access bank selection
0x01	RST_SET									Software reset setting
0x02	CLK_SET									Clock configuration
0x03	CLKOUT									CLKOUT frequency setting
0x04	RATE_SET1									Data rate conversion setting 1
0x05	RATE_SET2									Data rate conversion setting 2
0x06-0x07	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x08	#ADC_CLK_SET	▨	▨	▨		▨	▨	▨	▨	RSSI ADC clock frequency setting
0x09-0x0a	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x0b	#OSC_ADJ	▨								Load capacitor adjustment for oscillation circuit
0x0c	#RF_TEST_MODE		▨							TX test pattern setting
0x0d-0x0e	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x0f	# PHY_STATE	▨	▨							PHY status indication
0x10	#FIFO_BANK	▨	▨	▨	▨					FIFO bank indication
0x11	#PLL_LOCK_DETECT									PLL lock detection configuration
0x12	CCA_IGNORE_LEVEL									ED threshold level setting for excluding CCA judgement
0x13	CCA_LEVEL									CCA threshold level setting
0x14	CCA_ABORT									Timing setting for forced termincation of CCA operation
0x15	CCA_CNTRL									CCA control setting and result indication
0x16	ED_RSLT									ED (Energy Detection) value indication
0x17	IDLE_WAIT_L									IDLE detection period setting during CCA (low 8bits)
0x18	IDLE_WAIT_H	▨	▨	▨	▨	▨	▨			IDLE detection period setting during CCA (high 2bits)
0x19	CCA_PROG_L									IDLE judgement elapsed time indication during CCA (low byte)
0x1a	CCA_PROG_H	▨	▨	▨	▨	▨	▨			IDLE judgement elapsed time indication during CCA (high 2bits)
0x1b	ED_CNTRL		▨	▨		▨				ED detection control setting
0x1c	GAIN_MtoL	▨	▨							Threshold level setting for switching middle gain to low gain
0x1d	GAIN_LtoM	▨	▨							Threshold level setting for switching low gain to middle gain
0x1e	GAIN_HtoM		▨							Gain update setting and threshold level setting for switching high gain to middle gain
0x1f	GAIN_MtoH	▨	▨							Threshold level setting for switching middle gain to high gain
0x20	RSSI_ADJ_M	▨	▨							RSSI offset value setting during middle gain operation
0x21	RSSI_ADJ_L	▨	▨							RSSI offset value setting during low gain operation
0x22	RSSI_STABLE_TIME	▨	▨							Time parameter for RSSI value become stable after gain switch
0x23	RSSI_VAL_ADJ									RSSI scale factor setting for ED value conversion.
0x24	INT_SOURCE_GRP1									FIFO clear setting and interrupt status for INT00 to INT05
0x25	INT_SOURCE_GRP2									Interrupt status for INT08 to INT15
0x26	INT_SOURCE_GRP3									Interrupt status for INT16 to INT23
0x27	INT_SOURCE_GRP4	▨	▨	▨	▨	▨	▨			Interrupt status for INT24 and INT25
0x28	PD_DATA_REQ	▨	▨			▨	▨			Data transmission request status indication
0x29	PD_DATA_IND	▨	▨			▨	▨			Data reception status indication
0x2a	INT_EN_GRP1	▨	▨							Interrupt mask for INT00 to INT05
0x2b	INT_EN_GRP2									Interrupt mask for INT08 to INT15
0x2c	INT_EN_GRP3									Interrupt mask for INT16 to INT23
0x2d	INT_EN_GRP4	▨	▨	▨	▨	▨	▨			Interrupt mask for INT24 and INT25
0x2e	CH_EN_L									RF channel enable setting for low 8ch
0x2f	CH_EN_H									RF channel enable setting for high 8ch
0x30	IF_FREQ_AFC_H									IF frequency setting during AFC operation (high byte)
0x31	IF_FREQ_AFC_L									IF frequency setting during AFC operation (low byte)
0x32	BPF_AFC_ADJ_H	▨	▨	▨	▨	▨	▨			Bandpass filter capacitance adjustment during AFC operation (high 2bits)
0x33	BPF_AFC_ADJ_L									Bandpass filter capacitance adjustment during AFC operation (low byte)
0x34	AFC_CNTRL	▨				▨	▨	▨		AFC control setting
0x35	TX_ALARM_LH									TX FIFO full level setting
0x36	TX_ALARM_HL									TX FIFO empty level setting
0x37	RX_ALARM_LH									RX FIFO full level setting

BANK0 (continued)

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x38	RX_ALARM_HL									RX FIFO empty level setting
0x39	PREAMBLE_SET									Preamble pattern setting
0x3a	SFD1_SET1									SFD pattern #1 1st byte setting (max 4byte)
0x3b	SFD1_SET2									SFD pattern #1 2nd byte setting (max 4byte)
0x3c	SFD1_SET3									SFD pattern #1 3rd byte setting (max 4byte)
0x3d	SFD1_SET4									SFD pattern #1 4th byte setting (max 4byte)
0x3e	SFD1_SET1									SFD pattern #2 1st byte setting (max 4byte
0x3f	SFD2_SET2									SFD pattern #2 2nd byte setting (max 4byte)
0x40	SFD2_SET3									SFD pattern #2 3rd byte setting (max 4byte)
0x41	SFD2_SET4									SFD pattern #2 4th byte setting (max 4byte)
0x42	TX_PR_LEN									TX preamble length setting
0x43	RX_PR_LEN/SFD_LEN									RX preamble setting and SFD length setting
0x44	SYNC_CONDITION									Bit error tolerance setting in RX preamble and SFD detection
0x45	PACKET_MODE_SET									Packet configuration
0x46	FEC/CRC_SET									FEC and CRC configuration
0x47	DATA_SET									Data configuration
0x48	CH0_FL									Channel #0 frequency (F-counter) setting (low byte)
0x49	CH0_FM									Channel #0 frequency (F-counter) setting (middle byte)
0x4a	CH0_FH	▨	▨	▨	▨					Channel #0 frequency (F-counter) setting (high 4bits)
0x4b	CH0_NA					▨	▨			Channel #0 frequency (N-counter and A-counter) setting
0x4c	CH_SPACE_L									Channel space setting (low byte)
0x4d	CH_SPACE_H									Channel space setting (high byte)
0x4e	F_DEV_L									GFSK frequency deviation setting (low byte)
0x4f	F_DEV_H									GFSK frequency deviation setting (high byte)
0x50	ACK_TIMER_L									Ack timer setting (low byte)
0x51	ACK_TIMER_H									Ack timer setting (high byte)
0x52	ACK_TIMER_EN	▨	▨			▨	▨	▨		Ack timer control setting
0x53	ACK_FRAME1									Ack Frame Control Field (2bytes) setting (low byte)
0x54	ACK_FRAME2									Ack Frame Control Field (2bytes) setting (high byte)
0x55	AUTO_ACK_SET			▨		▨	▨			Auto_Ack function setting
0x56-x58	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x59	GFIL00 / FSK_FDEV1									Gaussian filter coefficient setting 1 / FSK 1st frequency deviation setting
0x5a	GFIL01 / FSK_FDEV2									Gaussian filter coefficient setting 2 / FSK 2nd frequency deviation setting
0x5b	GFIL02 / FSK_FDEV3									Gaussian filter coefficient setting 3 / FSK 3rd frequency deviation setting
0x5c	GFIL03 / FSK_FDEV4									Gaussian filter coefficient setting 4 / FSK 4th frequency deviation setting
0x5d	GFIL04									Gaussian filter coefficient setting 5
0x5e	GFIL05									Gaussian filter coefficient setting 6
0x5f	GFIL06									Gaussian filter coefficient setting 7
0x60	GFIL07									Gaussian filter coefficient setting 8
0x61	GFIL08									Gaussian filter coefficient setting 9
0x62	GFIL09									Gaussian filter coefficient setting 10
0x63	GFIL10									Gaussian filter coefficient setting 11
0x64	GFIL11									Gaussian filter coefficient setting 12
0x65	FSK_TIME1									FSK 3rd frequency deviation (FDEV3) hold time setting
0x66	FSK_TIME2									FSK 2nd frequency deviation (FDEV2) hold time setting
0x67	FSK_TIME3									FSK 1st frequency deviation (FDEV1) hold time setting
0x68	FSK_TIME4									FSK no-deviation frequency (carrier frequency) hold time setting

BANK0 (continued)

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x69	PLL_MON/DIO_SEL	▨		▨		▨	▨			PLL lock detection signal output control and DIO mode configuration
0x6a	FAST_TX_SET									TX trigger level setting in FAST_TX mode
0x6b	CH_SET	▨	▨	▨	▨					RF channel setting
0x6c	RF_STATUS									RFstate setting and status indication
0x6d	2DIV_ED_AVG	▨	▨	▨	▨	▨				Average number setting for ED calculation during 2 diversity
0x6e	2DIV_GAIN_CNTRL									Gain control setting during 2 diversity
0x6f	2DIV_SEARCH									2 diversity search mode and search time setting
0x70	2DIV_FAST_LV									ED threshold level setting during 2 diversity FAST mode
0x71	2DIV_CNTRL	▨	▨							2 diversity setting
0x72	2DIV_RSLT		▨			▨	▨			2 diversity resurt indication and forced antenna control setting
0x73	ANT1_ED									Acquired ED value by antenna 1
0x74	ANT2_ED									Acquired ED value by antenna 2
0x75	RF_CNTRL_SET	▨				▨				RF control pin configuration (ANT_SW, TRX_SW,DCNT)
0x76	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x77	CRC_AREA/FIFO_TRG	▨	▨	▨	▨	▨	▨			CRC calculation field and FIFO trigger setting
0x78	RSSI_MON	▨	▨							RSSI value indication
0x79	TEMP_MON									Temperature indication
0x7a	PN9_SET_L									PN9 initialized status setting / randum number indication (low byte)
0x7b	PN9_SET_H		▨	▨	▨	▨	▨	▨		PN9 initialized status setting / randum number indication (high 1bit) and PN9 enable control
0x7c	RD_ FIFO_LAST									FIFO remaining size or FIFO address indication
0x7d	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x7e	WR_TX_FIFO									TX FIFO
0x7f	RD_RX_FIFO									RX FIFO

BANK1

Address	Symbol	Bit								Description
		7	6	5	4	3	2	1	0	
0x00	BANK_SEL		▨	▨	▨	▨	▨			Register access bank selection
0x01	DEMOD_SET		▨	▨	▨					Demodulator setting
0x02	RSSI_ADJ		▨	▨						RSSI value adjustment
0x03	RSSI/TEMP_OUT	▨	▨			▨	▨	▨		RSSI and Temperature data output setting
0x04	PA_ADJ1									PA adjustment 1st setting
0x05	PA_ADJ2									PA adjustment 2nd setting
0x06	PA_ADJ3									PA adjustment 3rd setting
0x07	PA_CNTRL					▨	▨			External PA control and PA mode setting
0x08	SW_OUT/RAMP_ADJ			▨						ANT_SW/TRX_SW configuration and PA ramping up adjustment
0x09	PLL_CP_ADJ	▨				▨				PLL charge pump current adjustment
0x0a	IF_FREQ_H									IF frequency setting (high byte)
0x0b	IF_FREQ_L									IF frequency setting (low byte)
0x0c	IF_FREQ_CCA_H									IF frequency setting during CCA operation (high byte)
0x0d	IF_FREQ_CCA_L									IF frequency setting during CCA operation (low byte)
0x0e	BPF_ADJ_H	▨	▨	▨	▨	▨	▨			Bandpass filter bandwidth adjustment (high 2bits)
0x0f	BPF_ADJ_L									Bandpass filter bandwidth adjustment (low byte)
0x10	BPF_CCA_ADJ_H	▨	▨	▨	▨	▨	▨			Bandpass filter bandwidth adjustment during CCA operation (high 2bits)
0x11	BPF_CCA_ADJ_L									Bandpass filter bandwidth adjustment during CCA operation (low byte)
0x12	RSSI_LPF_ADJ	▨	▨							RSSI lowpass filter adjustment
0x13	PA_REG_FINE_ADJ	▨	▨	▨						PA regulator fine adjustment
0x14	IQ_MAG_ADJ	▨	▨							IF I/Q amplitude balance adjustment
0x15	IQ_PHASE_ADJ	▨	▨							IF I/Q phase balance adjustment
0x16	VCO_CAL_MIN_FL									VCO calibration low limit frequency setting (low byte)

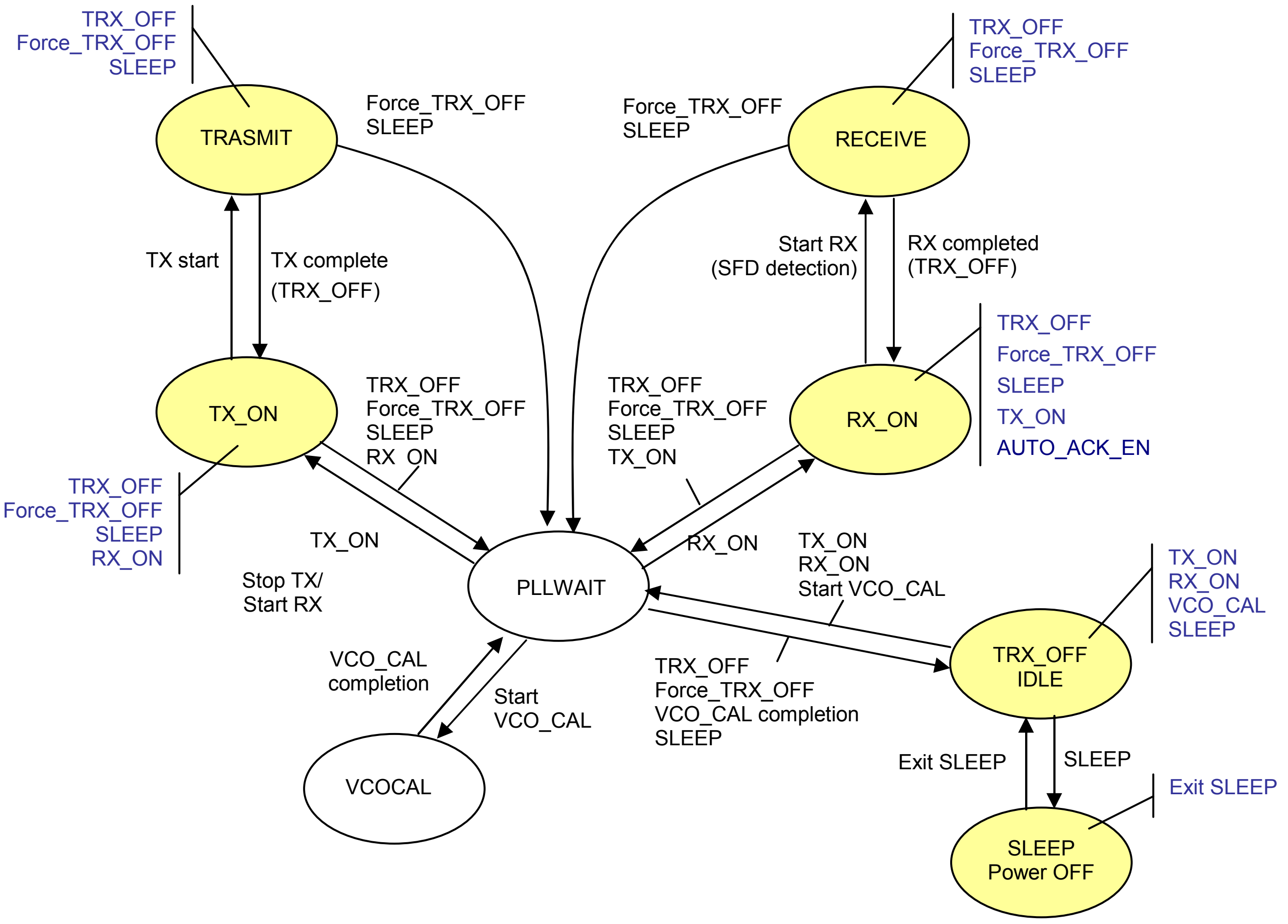
BANK1 (continued)

Address	Symbol	Bit								Description
		7	6	5	4	3	2	1	0	
0x17	VCO_CAL_MIN_FM									VCO calibration low limit frequency setting (middle byte)
0x18	VCO_CAL_MIN_FH	▨	▨	▨	▨					VCO calibration low limit frequency setting (high 4bits)
0x19	VCO_CAL_MAX_N	▨	▨	▨						VCO calibration upper limit frequency setting
0x1a	VCO_CAL_MIN	▨								VCO calibration low limit value indication and setting
0x1b	VCO_CAL_MAX	▨								VCO calibration upper limit value indication and setting
0x1c	VCO_CAL									VCO calibration value indication and setting
0x1d	VCO_CAL_START	▨	▨	▨	▨	▨	▨	▨		VCO calibration execution
0x1e	BPF_ADJ_OFFSET									BPF adjustment offset value indication
0x1f-0x2a	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x2b	# ID_CODE									ID code indication
0x2c-0x32	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x33	# PA_REG_ADJ1	▨	▨	▨	▨	▨				PA regulator adjustment (1st setting)
0x34	# PA_REG_ADJ2	▨	▨	▨	▨	▨				PA regulator adjustment (2nd setting)
0x35	# PA_REG_ADJ3	▨	▨	▨	▨	▨				PA regulator adjustment (3rd setting)
0x36-0x39	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x3a	# PLL_CTRL	▨	▨	▨		▨	▨	▨	▨	PLL setting
0x3b-0x3e	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x3f	# RX_ON_ADJ2	▨				▨	▨	▨	▨	RX_ON timing adjustment #2
0x40-0x48	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x49	# LNA_GAIN_ADJ_M	▨	▨							LNA gain adjustment during middle gain operation
0x4a	# LNA_GAIN_ADJ_L	▨	▨							LNA gain adjustment during low gain operation
0x4b-0x4c	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x4d	# MIX_GAIN_ADJ_H									Mixer gain adjustment during high gain operation
0x4e	# MIX_GAIN_ADJ_M									Mixer gain adjustment during middle gain operation
0x4f	# MIX_GAIN_ADJ_L									Mixer gain adjustment during low gain operation
0x50-0x54	Reserved	▨						▨	▨	Reserved
0x55	#TX_OFF_ADJ1									TX_OFF ramping down adjustment
0x56-0x59	Reserved	▨						▨	▨	Reserved
0x5a	# RSSI_SLOPE_ADJ	▨								RSSI slope adjustment
0x5b-0x7f	Reserved	▨						▨	▨	Reserved

BANK2

Address	Symbol	Bit								Description
		7	6	5	4	3	2	1	0	
0x00	BANK_SEL		▨	▨	▨	▨	▨	▨		Register access bank selection
0x01-0x11	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x12	# SYNC_MODE	▨	▨	▨	▨	▨		▨	▨	Bit synchronization mode setting
0x13-0x1d	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x1e	# PA_ON_ADJ									PA_ON timing adjustment
0x1f	# DATA_IN_ADJ	▨	▨	▨	▨	▨	▨	▨	▨	DATA enable timing adjustment
0x20-0x21	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x22	# RX_ON_ADJ									RX_ON timing adjustment
0x23	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x24	# RXD_ADJ									RXD timing adjustment
0x25-0x29	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x2a	RATE_ADJ1									Demodulator adjustment for optional data rate (low byte)
0x2b	RATE_ADJ2	▨	▨	▨		▨	▨			Demodulator adjustment for optional data rate (high 2 bits)
0x2c	#RAMP_CNTRL	▨	▨	▨		▨	▨	▨	▨	Ramp control enable setting
0x2d-0x5f	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved
0x60	ADDFILCNTRL									Address filtering function setting
0x61	PANID_L									PANID setting for address filtering function (low byte)
0x62	PANID_H									PANID setting for address filtering function (high byte)
0x63	64ADDR1									64bit address setting for address filtering function (1st byte)
0x64	64ADDR2									64bit address setting for address filtering function (2nd byte)
0x65	64ADDR3									64bit address setting for address filtering function (3rd byte)
0x66	64ADDR4									64bit address setting for address filtering function (4th byte)
0x67	64ADDR5									64bit address setting for address filtering function (5th byte)
0x68	64ADDR6									64bit address setting for address filtering function (6th byte)
0x69	64ADDR7									64bit address setting for address filtering function (7th byte)
0x6a	64ADDR8									64bit address setting for address filtering function (8th byte)
0x6b	SHT_ADDR0_L									Short address #0 setting for address filtering function (low byte)
0x6c	SHT_ADDR0_H									Short address #0 setting for address filtering function (high byte)
0x6d	SHT_ADDR1_L									Short address #1 setting for address filtering function (low byte)
0x6e	SHT_ADDR1_H									Short address #1 setting for address filtering function (high byte)
0x6f	DISCARD_COUNT_L									Discarded packet number indication by address filtering (low byte)
0x70	DISCARD_COUNT_H									Discarded packet number indication by address filtering (high byte)
0x71-0x7f	Reserved	▨	▨	▨	▨	▨	▨	▨	▨	Reserved

■State Diagram


TRX_OFF
Force_TRX_OFF
SLEEP
TRASMIT
Force_TRX_OFF
SLEEP
Force_TRX_OFF
SLEEP
RECEIVE
TRX_OFF
Force_TRX_OFF
SLEEP
TX start
TX complete
(TRX_OFF)
Start RX
(SFD detection)
RX completed
(TRX_OFF)
TRX_OFF
Force_TRX_OFF
SLEEP
TX_ON
AUTO_ACK_EN
TX_ON
TRX_OFF
Force_TRX_OFF
SLEEP
RX_ON
TRX_OFF
Force_TRX_OFF
SLEEP
TX_ON
RX_ON
TRX_OFF
Force_TRX_OFF
SLEEP
RX_ON
TX_ON
Stop TX/
Start RX
PLLWAIT
RX_ON
TX_ON
RX_ON
Start VCO_CAL
TX_ON
RX_ON
VCO_CAL
SLEEP
VCO_CAL
completion
Start
VCO_CAL
TRX_OFF
Force_TRX_OFF
VCO_CAL completion
SLEEP
TRX_OFF
IDLE
VCOCAL
Exit SLEEP
SLEEP
Exit SLEEP
SLEEP
Power OFF

[State]
SLEEP/Power OFF :SLEEP
TRX_OFF/IDLE :IDLE (TX-RX stand-by)
PLL_WAIT :PLL stand-by
TX_ON :TX ready (TX data waiting)
TRANSMIT :TX on-going
RX_ON :RX readt (RX data waiting)
RECEIVE :RX in process
VCO_CAL :VCO calibration on going

—| State Transition instruction

← Normal sequence
(State transition)

⬭ Control from upper layer

⬭ ML7396 self controlled
state transition

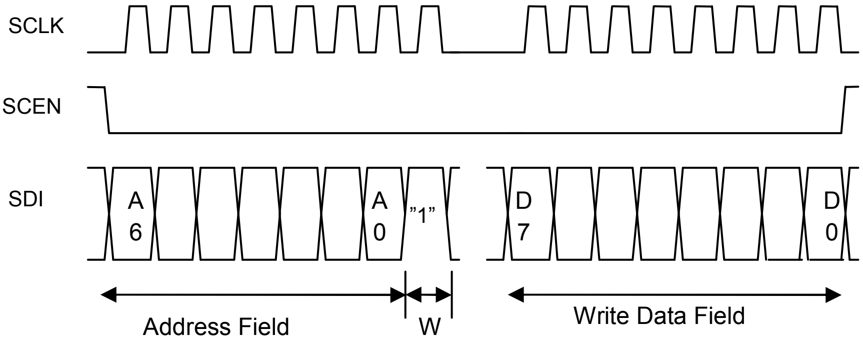
■Functional Description

●SPI

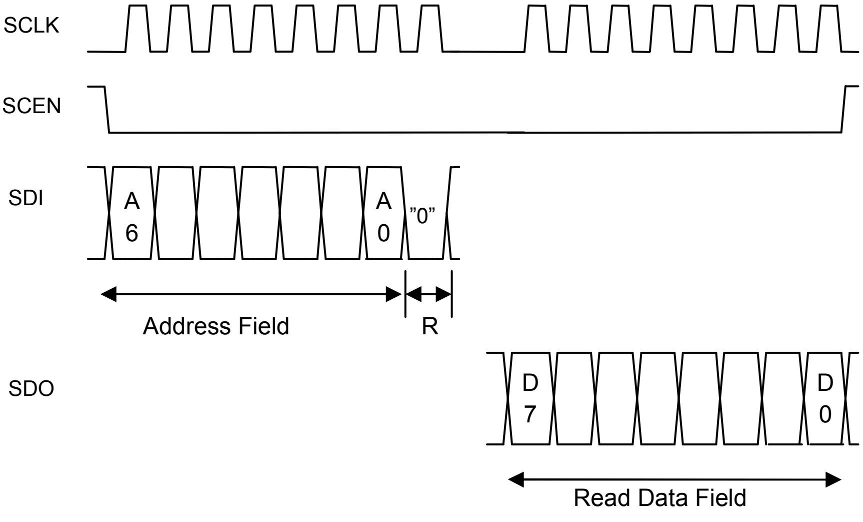
ML7396 family has a Serial Peripheral Interface (SPI), which supports slave mode. Host MCU can read/write to the ML7396 registers and on-chip FIF using MCU clock. Single access mode and burst access mode are also supported.

[Single access mode]
In write operation, data will be stored into internal register at rising edge of clock which is capturing D0 data. During write operation, if setting SCEN line to “H”, the data will not be sotred into register.

[Write]


SCLK
SCEN
SDI
A 6
A 0
”1”
D 7
D 0
Address Field
W
Write Data Field

[Read]


SCLK
SCEN
SDI
A 6
A 0
”0”
Address Field
R
SDO
D 7
D 0
Read Data Field

[Note]
When using IEEE802.15.4d mode, it is need to read “Length+1” bytes of data from RX FIFO for switching the FIFO banks correctly. After reading Lngth bytes of data, need to access [RD_RX_FIFO:B0 0x7F] register once more. (The last byte is invalid data.)

[Burst access mode]

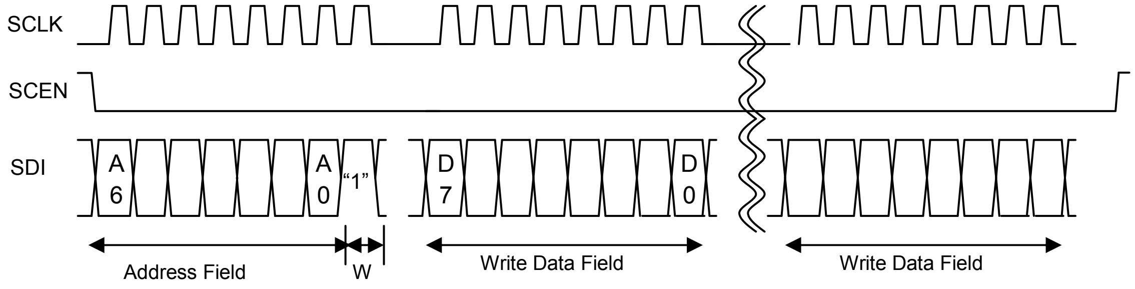
By maintaining SCEN as L, Burst access mode will be active. By setting SCEN line to "H", exiting from the burst access mode. During burst access mode, address will be automatically incremented.

When SCEN become H before Clock for D0 is input, data transaction will be aborted.

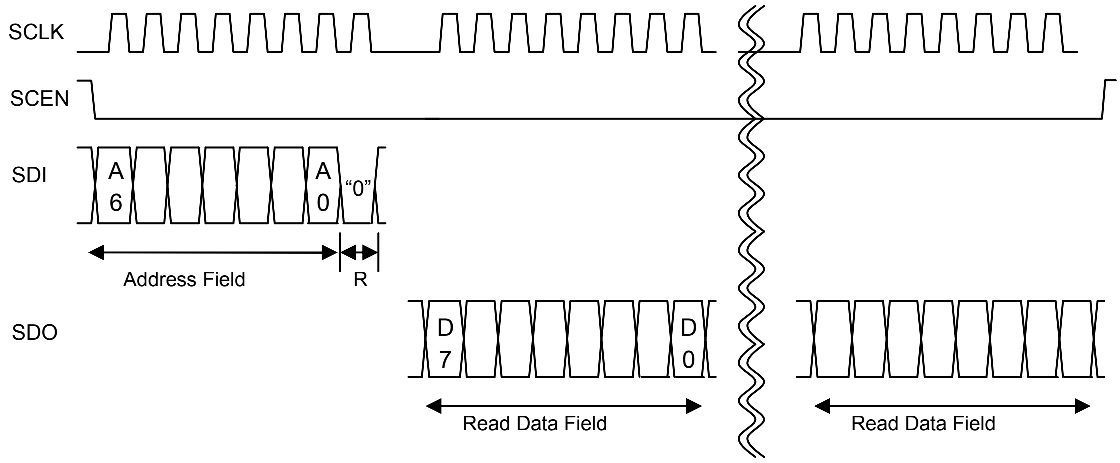
[Note]

If destination is [WR_TX_FIFO:B0 0x7E] or [RD_RX_FIFO:B0 0x7F] register, address will not be incremented. And continuous FIFO access is possible.

[Write]


SCLK
SCEN
SDI
A 6
A 0
"1"
D 7
D 0
Address Field
W
Write Data Field
Write Data Field

[Read]


SCLK
SCEN
SDI
A 6
A 0
"0"
Address Field
R
SDO
D 7
D 0
Read Data Field
Read Data Field

[Note]

When using IEEE802.15.4d mode, it is need to read "Length+1" bytes of data from RX FIFO for switching the FIFO banks correctly. (The last byte is invalid data.)

●AFC function

ML7396 family supports AFC function during RX operation. Frequency deviation (max +/- 20ppm) between remote device and local device can be compensated by this function. Using this function, stable RX sensitivity and interference blocking performance can be achieved.

This function can be activated by setting AFC_EN ([AFC_CNTRL:B0 0x34(0)]) =0b1

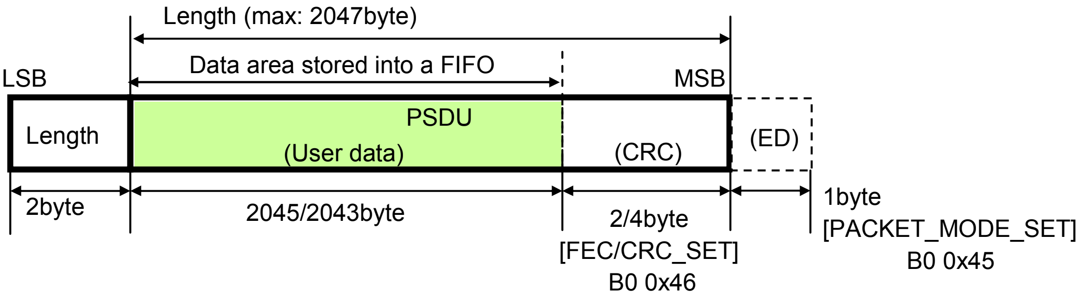
This is not supported for optional data rate. (other than 50/100/150/200/400kbps) When using optional data rate, AFC_EN should be set to 0b0.

●FIFO

ML7396 family has on-chio two 256byte FIFOs as TX -RX buffer. However, one FIFO can store only one packet. (one packet cannot use two FIFOs).
During RX, RX data is stored in a FIFO (byte by byte), and the host MCU wil read RX data through SPI. Duting TX, the host MCU write TX data to a FIFO (byte by byte) through SPI and tenasmitting through RF.

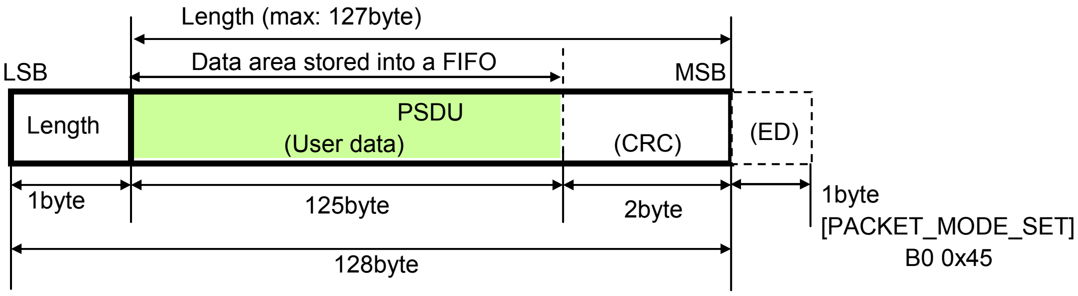
Followings show the data format stored in FIFO.
As described below, input data format will be different according to the setting value to IEEE_MODE ([PACKET MODE_SET:B0 0x45(1)]). (Regardless of IEEE_MODE, preamble and SFD bits are not stored into FIFOs)

[IEEE802.15.4g mode] (IEEE_MODE =0b1)


Length (max: 2047byte)
Data area stored into a FIFO
LSB
MSB
Length
PSDU
(User data)
(CRC)
(ED)
2byte
2045/2043byte
2/4byte
[FEC/CRC_SET]
B0 0x46
1byte
[PACKET_MODE_SET]
B0 0x45

[Note; Length, CRC and ED value will be stored into data strage area other than FIFO.]

[IEEE802.15.4d mode] (IEEE_MODE =0b0)


Length (max: 127byte)
Data area stored into a FIFO
LSB
MSB
Length
PSDU
(User data)
(CRC)
(ED)
1byte
125byte
2byte
128byte
1byte
[PACKET_MODE_SET]
B0 0x45

[Note; Length, CRC and ED value will be stored into data strage area other than FIFO.]

Writeing or reading FIFO will be done through SPI with burst access. TX data is written to [WR_TX_FIFO:B0 0x7E] register, and RX data is read from [RD_RX_FIFO:B0 0x7F] register. Continuous access increments internal FIFO address automatically. If burst access is suspended during write or read operation, address will be kept until the packet will beagain.

Two FIFOs (bank0, bank1) will be accessed one by another. If the host MCU writes TX data to a FIFO during RX, RX FIFO will use only single FIFO. Control of switching FIFO banks will be done automatically. FIFO status can be checked by [PD_DATA_REQ:B0 0x28] or [PD_DATA_IND:B0 0x29] register.

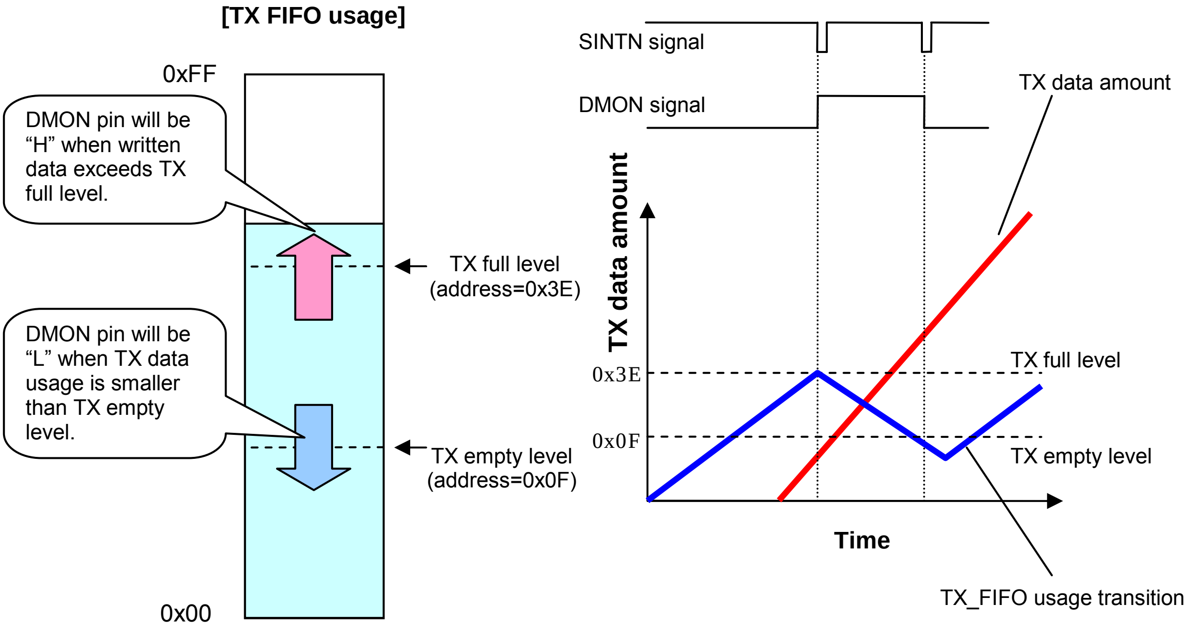
[Note]

1. When using IEEE802.15.4d mode, it is need to read “Length+1” bytes of data from RX FIFO for switching the FIFO banks correctly. (The last byte is invalid data.)
2. In both TX and RX, Length indicates PSDU length including CRC field. (not including ED fieled if selected)
   However during TX, the host MCU writes PSDU excluding CRC field to a FIFO. During RX, the host MCU should read Lngth field, user data field and CRC fieled from a FIFO.

○TX FIFO usage notification function

This function is to notice un-transmitted data in TX_FIFO (FIFO usage) to the MCU using SINTN (interrupt) pin (#10) and/or DMON pin (#17). If un-transmitted data in TX_FIFO (FIFO usage) exceeds the full level threshold set by [TX_ALARM_LH:B0 0x35] register, SINTN pin will become "L" (FIFO-Full interrupt) and/or DMON pin will become "H". And if the TX_FIFO usage is equal to or less than the empty threshold level set by [TX_ALARM_HL:B0 0x36] register, SINTN will become "L" (FIFO-Empty interrupt) and/or DMON pin will become "L".

If re-generating the FIFO-Full interrupr (INT[05], group1), after clearing the interrupt, once the TX_FIFO usage should be equal or less than the empty level. If re-generating the FIFO-Empty interrupt (INT[04], group1), after clearing the interrupt, one the TX_FIFO usage excceds the full level threshold.

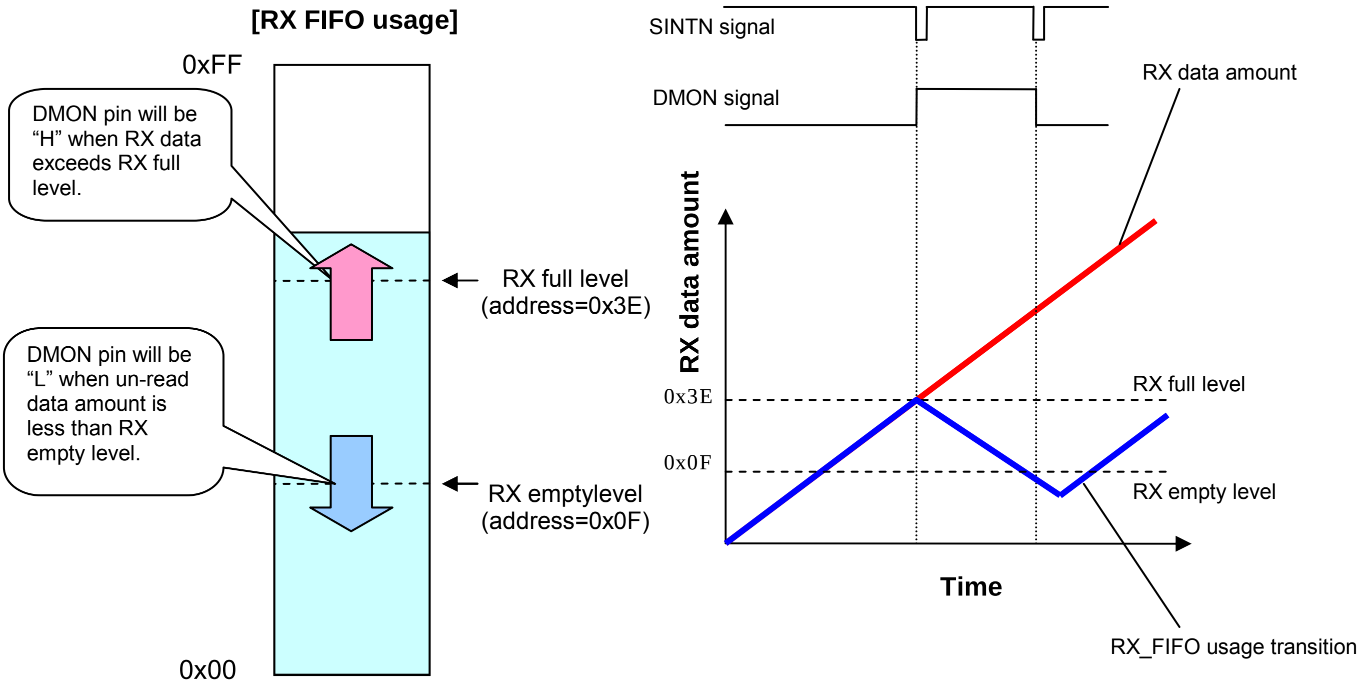

[TX FIFO usage]
0xFF
DMON pin will be "H" when written data exceeds TX full level.
TX full level (address=0x3E)
DMON pin will be "L" when TX data usage is smaller than TX empty level.
TX empty level (address=0x0F)
0x00
SINTN signal
DMON signal
TX data amount
TX data amount
0x3E
0x0F
TX full level
TX empty level
Time
TX_FIFO usage transition

[Note]
1. At default setting, DMON pin is configured as CLKOUT output. If using DMON pin as this function, CLKOUT_EN ([CLK_SET:B0 0x02(4)]) =0b0 and FIFO_TRG_EN ([CRC_AREA/FIFO_TRG:B0 0x77(0)])=0b1 are required.
2. Each threshold should set as [TX_ALARM_LH:B0 0x35] (full level) > [TX_ALARM_HL:B0 0x36] (empty level).

○RX FIFO usage notification function

This function is to notice un-read data in RX_FIFO (FIFO usage) to the MCU using SINTN (interrupt) pin (#10) and/or DMON pin (#17). If un-read data in RX_FIFO (FIFO usage) exceeds the full level threshold set by [RX_ALARM_LH:B0 0x37] register, SINTN pin will become "L" (FIFO-Full interrupt) and/or DMON pin will become "H". And if the RX_FIFO usage is equal to or less than the empty threshold level set by [RX_ALARM_HL:B0 0x38] register, SINTN will becom "L" (FIFO-Empty interrupt) and/or DMON pin will become "L".

If re-generating the FIFO-Full interrupr (INT[05], group1), after clearing the interrupt, once the RX_FIFO usage should be equal or less than the empty level. If re-generating the FIFO-Empty interrupt (INT[04], group1), after clearing the interrupt, one the RX_FIFO usage excceds the full level threshold.


[RX FIFO usage]
0xFF
DMON pin will be "H" when RX data exceeds RX full level.
RX full level (address=0x3E)
DMON pin will be "L" when un-read data amount is less than RX empty level.
RX emptylevel (address=0x0F)
0x00
SINTN signal
DMON signal
RX data amount
RX data amount
0x3E
0x0F
RX full level
RX empty level
Time
RX_FIFO usage transition

[Note]

1. At default setting, DMON pin is configured as CLKOUT output. If using DMON pin as this function, CLKOUT_EN ([CLK_SET:B0 0x02(4)]) =0b0 and FIFO_TRG_EN ([CRC_AREA/FIFO_TRG:B0 0x77(0)]) =0b1 are required.
2. Each threshold should set as [RX_ALARM_LH:B0 0x37] (full level) > [RX_ALARM_HL:B0 0x38] (empty level).
3. If reading a portion of RX data from a FIFO before receiving RX completion interrupt (INT[18]/INT[19] group3), please keep the FIFO remaining size indicated by [RD_FIFO_LAST:B0 0x7C] should be more than 0x01.
4. This function is valid only when data receiving. After RX completion, FIFO-Empty interrupt (INT[04] group1) is not generated.

○FIFO control method when using FIFO address

(1) TX

Condition: AUTO_TX ([PACKET_MODE_SET:B0 0x45(2)]) =0b1 and FIFO access size is 128 bytes.① Set [FAST_TX_SET;B0 0x6A] register and FIFO_ADR_EN ([PACKET_MODE_SET:B0 0x45(7)]) =0b1.

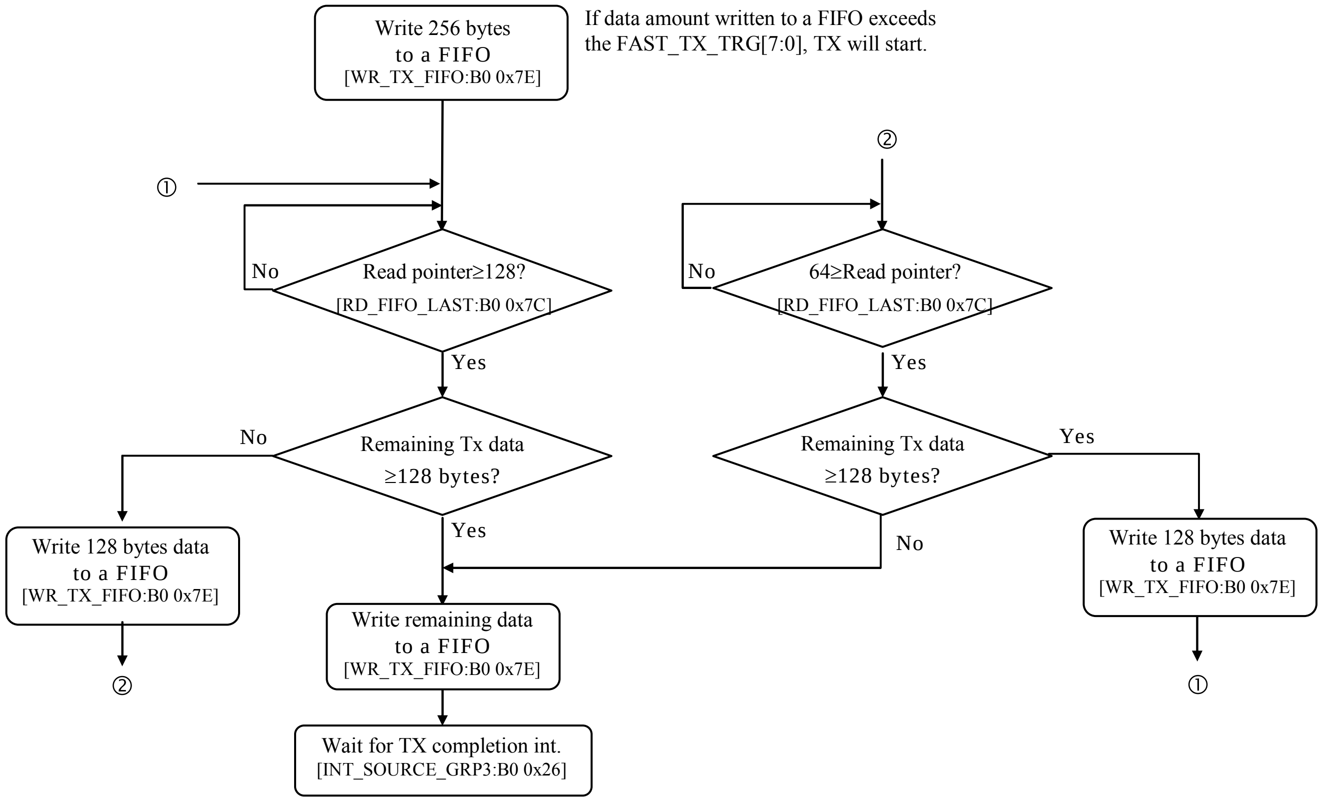
② Write256 bytesdata to FIFO ([WR_TX_FIFO:B0 0x7E] register) via SPI interface.

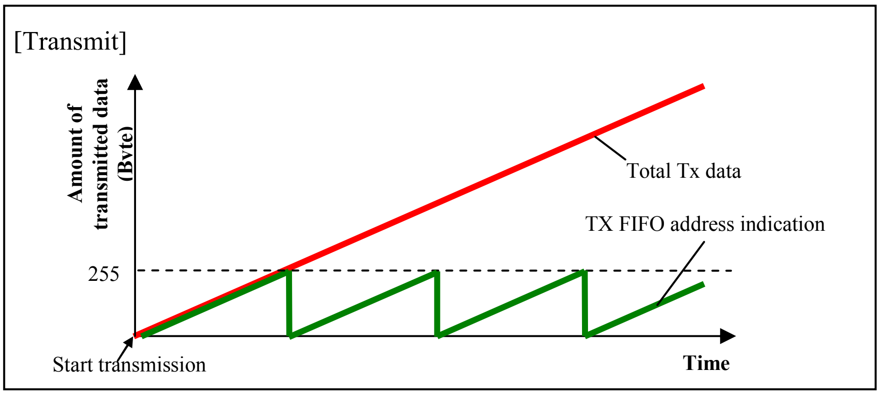
* When the amount of written data reaches [FIFO_TX_SET:B0 0x6A] register, transmission starts.③ Read [RD_FIFO_LAST:B0 0x7C] register. When FIFO address indication (hereafter, Read pointer) is 128 or more and the remaining TX data is 128 bytes or more, writing 128 bytes data to FIFO. If remaining TX data is less than 128 bytes, go to ⑥.

④ Read [RD_FIFO_LAST] register. When Read pointer is 64 or less and the remaining Tx data is 128 bytes or more, writing 128 bytes data to FIFO. If remaining TX data is less than 128 bytes, go to ⑥.

⑤ Repeat ③ and ④ until for the necessary amount of TX data.

⑥ Writing whole remaining data to FIFO and wait TX completion interrupt (INT[16] / INT[17], group3) notification.


Write 256 bytes
to a FIFO
[WR_TX_FIFO:B0 0x7E]
If data amount written to a FIFO exceeds
the FAST_TX_TRG[7:0], TX will start.
①
②
No
Read pointer≥128?
[RD_FIFO_LAST:B0 0x7C]
No
64≥Read pointer?
[RD_FIFO_LAST:B0 0x7C]
Yes
Yes
No
Remaining Tx data
≥128 bytes?
Remaining Tx data
≥128 bytes?
Yes
Yes
No
Write 128 bytes data
to a FIFO
[WR_TX_FIFO:B0 0x7E]
Write remaining data
to a FIFO
[WR_TX_FIFO:B0 0x7E]
Write 128 bytes data
to a FIFO
[WR_TX_FIFO:B0 0x7E]
②
①
Wait for TX completion int.
[INT_SOURCE_GRP3:B0 0x26]



TX FIFO address indication (read pointer) increments after Tx start.
After transimitting 256th byte data, the address indication is turned to 0 and increments again.

(2) RX (FIFO access size is 128 bytes)

① Set FIFO_ADR_EN ([PACKET_MODE_SET:B0 0x45(7)]) =0b1, and issuing RX_ON by [RF_STATUS:B0 0x6C] register. (RX start)

② Read [RD_FIFO_LAST:B0 0x7C] register. When FIFO address indication (hereafter, Write pointer) is 5 or more, read 5 bytes from FIFO ([RD_RX_FIFO:B0 0x7F] register). At this time, if the Length field is less than 5, this paclet does not meet IEEE802.15.4 requirement of the minimum packet length, the the packet might be discarded. (* It is not applied when using an original packet format other than IEEE802.15.4.) When it is equal to or more than 5 and less than 128, wait RX completion interrupt (INT[18]/[19] group3) and then read out the remaining data from FIFO.

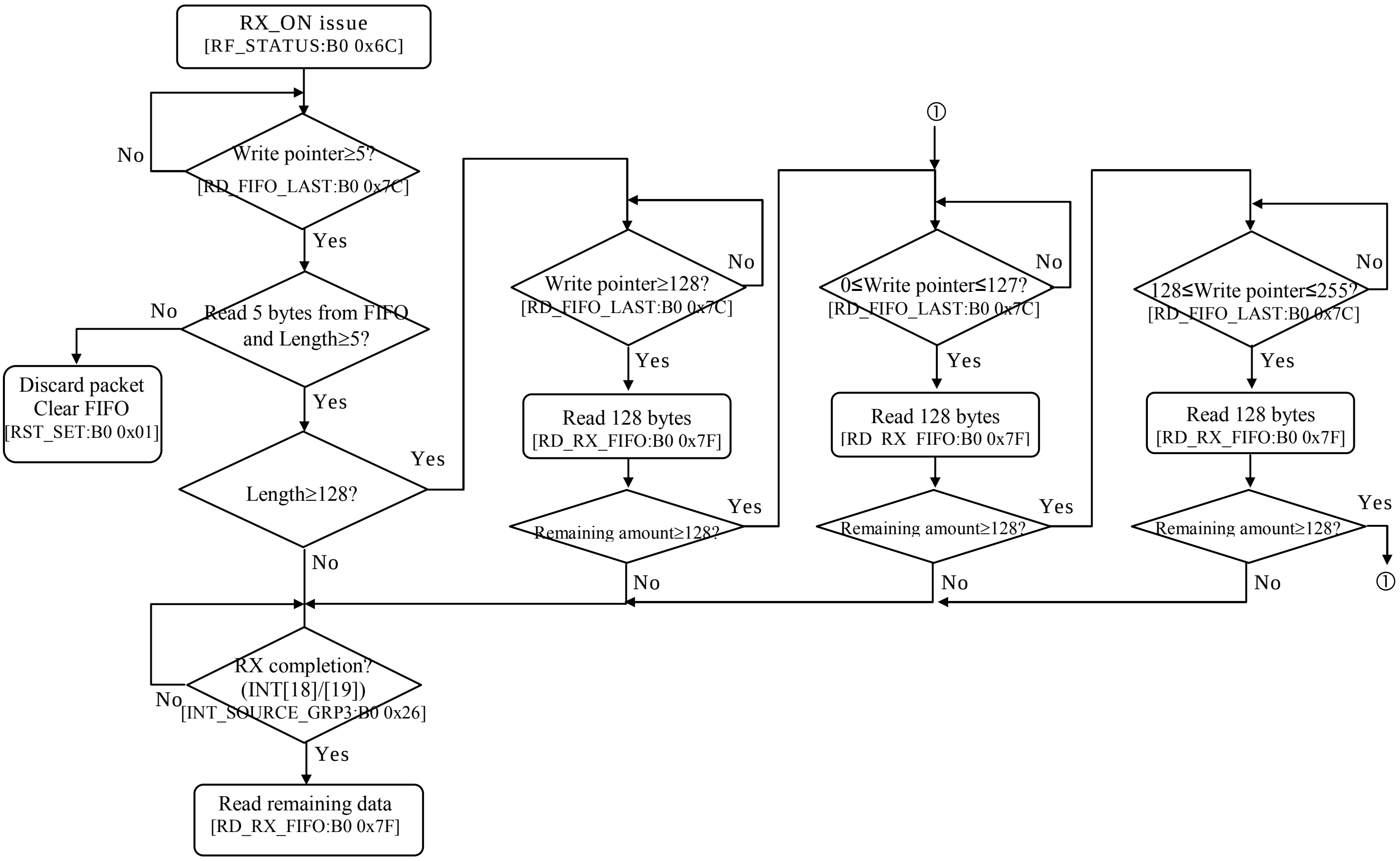
③ At ②, if the Length field is 128 or more, after Write pointer is 128 or more, read 123 bytes from FIFO. After that, if the remaining RX data size is less than 128, go to ⑦.

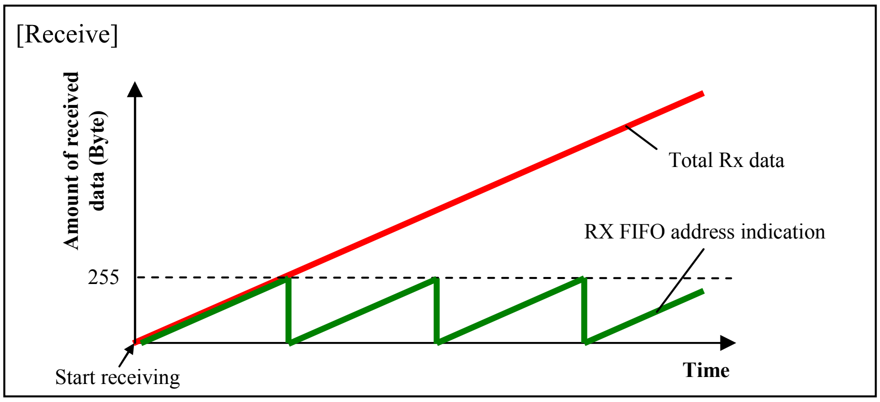
④ At ③, if the remaining RX data size is 128 or more, after Write pointer is 0 to 127, read 128 bytes from FIFO. After that, if the remaining RX data size is less than 128, go to ⑦.

⑤ At ④, if the remaining RX data size is 128 or more, after Write pointer is 128 to 255, read 128 bytes from FIFO. After that, if the remaining RX data size is less than 128, go to ⑦.

⑥ Repeat ④ and ⑤ until for the necessary amount of Rx data.

⑦ After RX completion interrupt (INT[18]/INT[19], group3) notification, read out the remaining RX data from FIFO.


RX_ON issue
[RF_STATUS:B0 0x6C]
No
Write pointer≥5?
[RD_FIFO_LAST:B0 0x7C]
Yes
No
Read 5 bytes from FIFO
and Length≥5?
Discard packet
Clear FIFO
[RST_SET:B0 0x01]
Yes
Length≥128?
Yes
No
Write pointer≥128?
[RD_FIFO_LAST:B0 0x7C]
No
Yes
Read 128 bytes
[RD_RX_FIFO:B0 0x7F]
Remaining amount≥128?
Yes
No
①
0≤Write pointer≤127?
[RD_FIFO_LAST:B0 0x7C]
No
Yes
Read 128 bytes
[RD_RX_FIFO:B0 0x7F]
Remaining amount≥128?
Yes
No
128≤Write pointer≤255?
[RD_FIFO_LAST:B0 0x7C]
No
Yes
Read 128 bytes
[RD_RX_FIFO:B0 0x7F]
Remaining amount≥128?
Yes
No
①
RX completion?
(INT[18]/[19])
[INT_SOURCE_GRP3:B0 0x26]
No
Yes
Read remaining data
[RD_RX_FIFO:B0 0x7F]

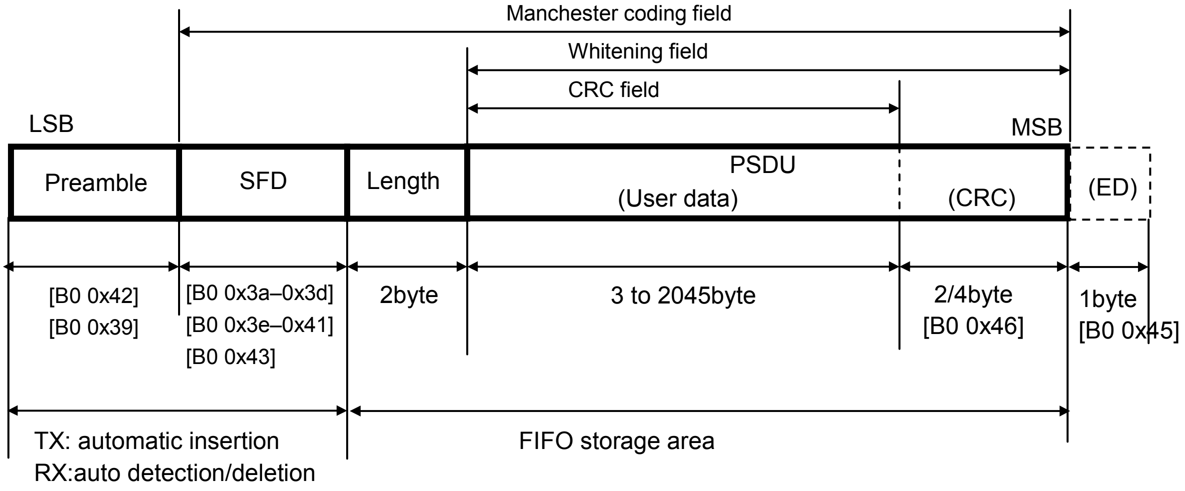


RX FIFO address indication (read pointer) increments after Rx start.
After receiving 256th byte data, the address indication is turned to 0 and increments again.

●Packet format

ML7396 family supports following packet format. (In DIO mode, the packet format is Preamble, SFD+DIO data)
Preamble and SFD field are automatically inserted in TX, and automatically detected and deleted in RX. The host MCU need not concern those packet handling.

[IEEE802.15.4g mode] (IEEE_MODE ([PACKET_MODE_SET:B0 0x45(1)]) =0b1)


Manchester coding field
Whitening field
CRC field
LSB
MSB
Preamble
SFD
Length
PSDU
(User data)
(CRC)
(ED)
[B0 0x42]
[B0 0x39]
[B0 0x3a–0x3d]
[B0 0x3e–0x41]
[B0 0x43]
2byte
3 to 2045byte
2/4byte
[B0 0x46]
1byte
[B0 0x45]
TX: automatic insertion
RX:auto detection/deletion
FIFO storage area

[Note]
1. The following shows the bit assignment of Length field (PHR) in IEEE802.15.4g format. It is different from IEEE802.15.4d format. User dara fieled (after 3rd byte) will be output with LSB first.
2. When using CRC32, the minimum user data length is 4 bytes. When transmitting/receiving 3-bytes data, CRC16 should be used. ACK packet cannot be received under CRC32 setting.

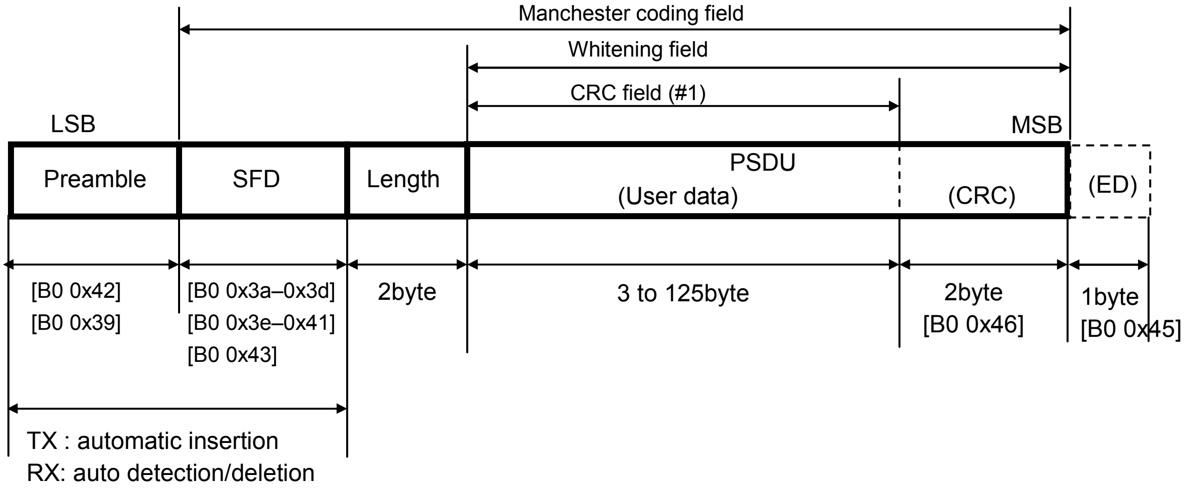
	1st byte								2nd byte							
Input from SPI	Mode Switch	Reserved	Reserved	FCS Length	Whitening	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0
Output to Air	Mode Switch	Reserved	Reserved	FCS Length	Whitening	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0

↑
TX starting bit

After 3rd byte

L7	L6	L5	L4	L3	L2	L1	L0
L0	L1	L2	L3	L4	L5	L6	L7

[IEEE802.15.4d mode] (IEEE_MODE ([PACKET_MODE_SET:B0 0x45(1)]) =0b0)


Manchester coding field
Whitening field
CRC field (#1)
LSB
MSB
Preamble
SFD
Length
PSDU
(User data)
(CRC)
(ED)
[B0 0x42]
[B0 0x39]
[B0 0x3a–0x3d]
[B0 0x3e–0x41]
[B0 0x43]
2byte
3 to 125byte
2byte
[B0 0x46]
1byte
[B0 0x45]
TX : automatic insertion
RX: auto detection/deletion

[Note]

#1 When in 802.15.4d mode, if setting CRC_AREA ([CRC_AREA/FIFO_TRG:B0 0x77(1)] bit (PHYSET101 bit1) =0b1, CRC calculationn area will be extended to Length field (Length+PSDU).

1. The following shows the bit assignment of Length field (PHR) in IEEE802.15.4d format. It is different from IEEE802.15.4g format. User dara fieled (after 2nd byte) will be output with LSB first.

Input from SPI	L7	L6	L5	L4	L3	L2	L1	L0
Output to Air	L0	L1	L2	L3	L4	L5	L6	L7

↑
TX starting bit

●Data whitening function

ML7396 family supports data whitening function specified in IEEE 802.15.4g standard. The following figure shows the PN9 pattern generator. The generated pattern will be "XOR" with data located in PSDU area.
Initialization value can be configured by [PN9_SET_L:B0 0x7A] and [PN9_SET_H:B0 0x7B] registers.
When setting PN9_EN ([PN9_SET_H:B0 0x7B(7)]) =0b1, this generator can be used as random number generator.
When WHITENING ([PACKET_MODE_SET:B0 0x45(4)]) =0b1, whitening condition is set by IEEE_MODE ([PACKET_MODE_SET:B0 0x45(1)] setting. Please refer to the "Packet format".

- In IEEE802.15.4d mode (IEEE_MODE=0b0), data whitening applied to every TX or RX packet
- In IEEE802.15.4g mode (IEEE_MODE=0b1), data whitening will be applied to the packet which whitening bit in PHR fieled is set to 0b1

[Note]

1. The PN9 pattern generator shares setting with the Whitening function. While the Whitening function is running, PN9_EN should be set to 0b0.

TX: $En = Rn \oplus PN9n$
RX: $Rn = REn \oplus PN9n$

En:	Whitening bits as TX data
Rn:	data bits
REn:	Whitening bits as RX data
PN9n:	PN9 pattern (Initialization value 0b111111111)

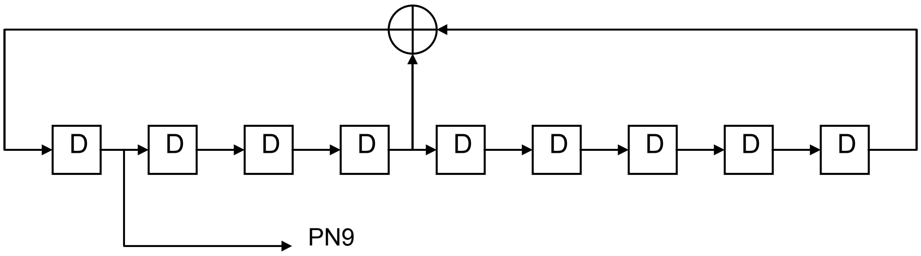
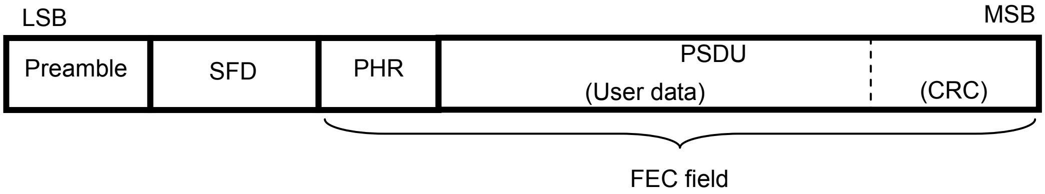


Fig. PN9 pattern generator

●FEC function

ML7396 family supports FEC function. FEC function will be applied to PHR and PSDU field as shown in below.



[Note]

1. Length in PHR fieled should be set the length before FEC encoding.
2. When using whitening function at same time, whitening will apply to the FEC encoded data. For more details of whitening field, please refer to the "Packet format".
3. Inrerleaving mode is not compliant to IEEE802.15.4g.

●Energy Detection value (ED value) Function

ML7396 family supports calculating Energy detection value (here in after ED value) based on Received signal strength indicator (RSSI). ED value acquisition can be enabled by ED_CALC_EN ([ED_CNTRL:B0 0x1B(7)])=0b1, and as soon as transition to RX_ON state. And acquired ED value will be indicate at [ED_RSLT:B0 0x16] register. When ED_CALC_EN=1, ED value will be updated constantly during RX_ON state. Even if ED_CALC_EN=1, While CCA operation or diversity search operation, ED value will not be updated. After completion of CCA operation, diversity search, ED value will be updated.

ED value is not RSSI value at given timing, but average values. The number of average times can be specified by register ED_AVG[2:0] ([ED_CNTRL:B0 0x1B(2-0)]). During diversity operation, 2DIV_ED_AVG[2:0] ([2DIV_ED_AVG:B0 0x6D(2-0)]) is used for setting. After acquiring specified average ED value, ED_DONE [ED_CNTRL:B0 0x1B(4)] becomes “0b1”, and [ED_RSLT:B0 0x16] register is updated.

ED_DONE bit will be cleared if one of the following conditions is met.

1. Gain is switched.
2. Suspend ED value acquisition and then resume it.
3. Antenna is switched. (When diversity is enabled)

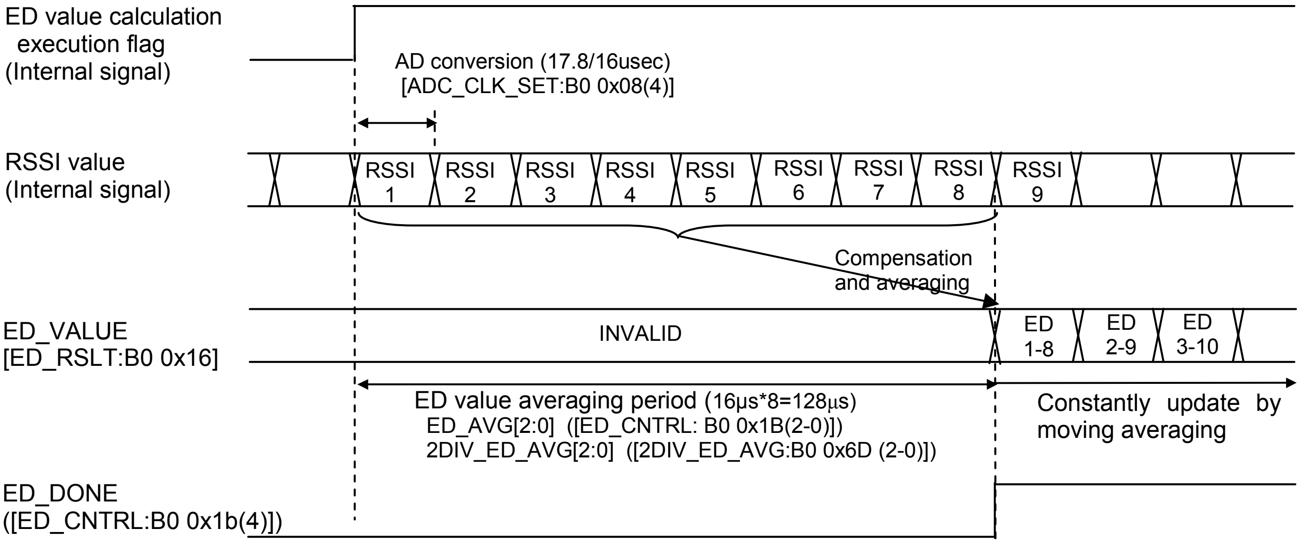
Timing from ED value starting point ot ED value acquisition is calculated as following formula.

ED value averaging time = AD conversion time (17.7µs/16µs) * number of average times

Note; AD conversion time can be set by ADC_CLK_SET ([ADC_CLK_SET:B0 0x08(4)])
Default value is 1.8MHz and SDC conversion time is 17.7µs

[Timechart]

[Condition]
Set ADC_CLK_SET([ADC_CLK_SET: B1 0x08(4)])=0b1 (2MHz)
Set ED_AVG[2:0] ([ED_CTRL: B0 0x1B(2-0)])=0b011 (8 times averaging)


ED value calculation execution flag (Internal signal)
AD conversion (17.8/16usec) [ADC_CLK_SET:B0 0x08(4)]
RSSI value (Internal signal)
RSSI 1
RSSI 2
RSSI 3
RSSI 4
RSSI 5
RSSI 6
RSSI 7
RSSI 8
RSSI 9
Compensation and averaging
ED_VALUE [ED_RSLT:B0 0x16]
INVALID
ED 1-8
ED 2-9
ED 3-10
ED value averaging period (16µs*8=128µs)
ED_AVG[2:0] ([ED_CNTRL: B0 0x1B(2-0)])
2DIV_ED_AVG[2:0] ([2DIV_ED_AVG:B0 0x6D (2-0)])
Constantly update by moving averaging
ED_DONE ([ED_CNTRL:B0 0x1b(4)])

○ED value calculation

Input level and ED value are descrived in the following formula. During CCA operation, ED value is bigger than normal case, since the BPF setting is modified. Therefore, CCA compensation value should be attached to the normal case.

Input level is defined at antenna connector in the ciruit described in the “Application Circuit Example”. And antenna SW loss is assumed 0.5dB.

[≤200kbps]
ED value = 255/70 * (107 + input level [dBm] - variation - other loss) + CCA cpmpensation

[400kbps]
ED value = 255/62 * (99 + input level [dBm] - variation - other loss)

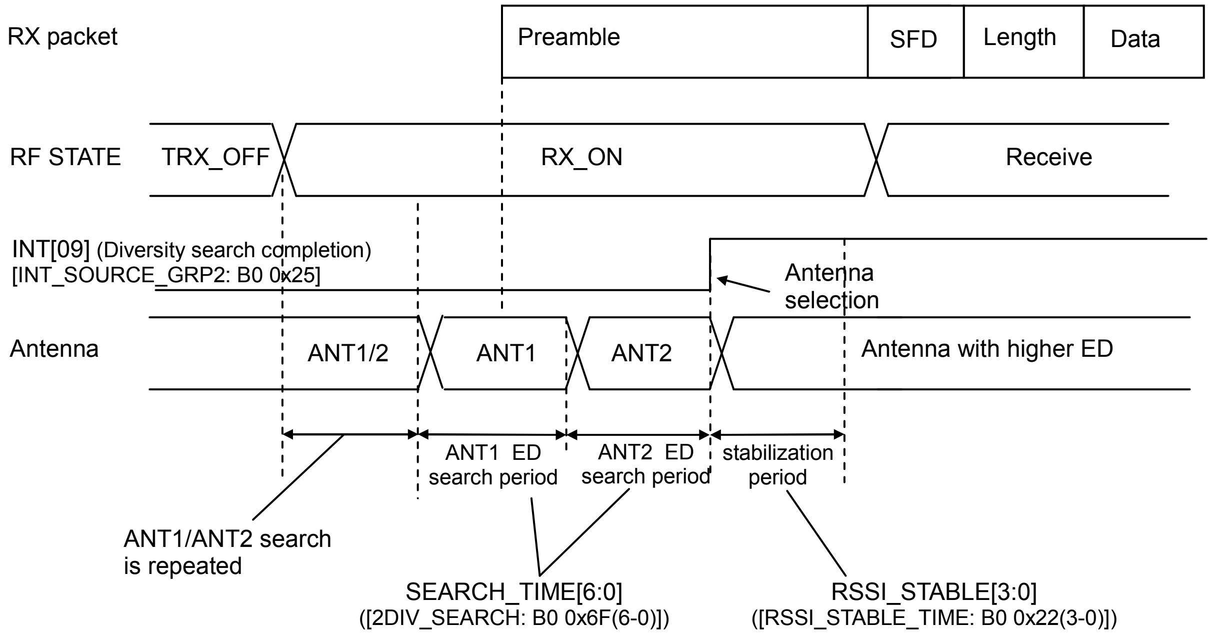
Parameter	Value
Variations (individual, temp.)	6dB
Other loss	Antenna, matching circuit loss
CCA compensation	12@100kbps, 16@200kbps, 0@other rates

●Diversity Function

ML7396 family supports two antenna diversity function.

While setting 2DIV_EN ([2DIV_CNTRL: B0 0x71(0)])=0b1, as soon as RX_ON is set, diversity mode will start. When diversity mode is started, and upon RX data detection, each ED value will be acquired by switching two antennas. And then antenna with higher ED value will be selected automatically. As diversity uses preamble data for ED value acquisition, longer preamble length is desirable. If preamble is too short, accurate ED values may not be obtained.

The timing example is as below.


RX packet
Preamble
SFD
Length
Data
RF STATE
TRX_OFF
RX_ON
Receive
INT[09] (Diversity search completion)
[INT_SOURCE_GRP2: B0 0x25]
Antenna selection
Antenna
ANT1/2
ANT1
ANT2
Antenna with higher ED
ANT1 ED search period
ANT2 ED search period
stabilization period
ANT1/ANT2 search is repeated
SEARCH_TIME[6:0]
([2DIV_SEARCH: B0 0x6F(6-0)])
RSSI_STABLE[3:0]
([RSSI_STABLE_TIME: B0 0x22(3-0)])

ED values and antenna diversity result will be cleared when as below:

1. Diversity search completion interrupt (INT[09] group2) is cleard.
2. FIFO* RX competion interrupt (INT[18] or INT[19] group3) is cleared
3. Diversity resume by errounous detection

ED values and diversity result should be read before clearing Diversity search completion or FIFO* RX completion interrupt.

During receiving state, clearing Diversity search completion interrupt causes the data error since diversity operation wlll resume by the interrupt clearance. Diverstiy search completion interrupt should be cleared at same timing of FIFO* RX completion interrupt clearance.

ML7396 supports recovering function from incorrect diversity completion caused by errornous detection due to thermal noize, After dicersity search completion, if preamble can not be detected until antenna search timer expiration, ML7396 judges the previous diversity search completion is incorrect and resume diversity operation automatically.

When resume diversity operation for next packet receiving, please clear RX completion interrupt and Diversity search completion interrupt.

(Note)

1. When an incorrect diversity completion caused by errornous detection due to thermal noize, ML7396 resume antenna diversity automatically. But when receiving a desired signal during the process of errounous detection, ED value obtained by [ANT1_ED:B0 0x73] or [ANT2_ED:B0 0x74] may indicate a low value different from the actual input level.
   If this event occures, the actual ED value of desired signal can be achibed by reading [ED_RSLT:B0 0x16] registers after SFD detection interrupt (INT[11] group2) generation.
2. When RF state is changed to TX_ON state immediately after an incorrect diversity completion caused by errornous detection, ML7396 judges Diversity search is done. Then, Diversity search is not operated at next receiving. In this case, please clear Diversity search completion interrupt (INT[09] group2) by next receiving.

○Antenna switching function

By using [2DIV_CTRL: B0 0x71], [RF_CTRL_SET: B0 0x75] registers, ML7396 can support both SPDT and DPDT antena swith control. ANT_SW pin (#20) and TRX_SW pin (#21) output considion for each antenna switch are explained below.

DPDT switch

Set 2PORT_SW([2DIV_CTRL:B0 0x71(1)])=0b1, ANT_CTRL1([2DIV_CTRL: B0 0x71(5)])=0b0. ANT_SW, TRX_SW output condition of each Idle, TX, RX state are as follow. (default setting) If INV_TRX_SW([2DIV_CTRL:B0 0x71(2)])=0b1, polarity of ANT_SW pin (#20) and TRX_SW pin (#21) are reversed.

TX/RX state	INV_TRX_SW=0b0 (default setting)		INV_TRX_SW=0b1 (reversed polarity)		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	H	L	L	H	Idle state
TX	L	H	H	L	TX state
RX	H	L	L	H	When Diversity disable or initial condition when diversity enable is set ([2DIV_CTRL: B0 0x71(0)]=0b1).
	L/H	H/L	H/L	L/H	If diversity enable is set, during searching, (ANT_SW=H, TRX_SW=L) and (ANT_SW=L, TRX_SW=H) are switched alternatively. After diversity completion, fix to one of the condition.

SPDT switch

Set 2PORT_SW([2DIV_CTRL:B0 0x71(1)])=0b0, ANT_CTRL1([2DIV_CTRL: B0 0x71(5)])=0b0. ANT_SW, TRX_SW output condition of each Idle, TX, RX state are as follow. (default setting) If INV_TRX_SW([2DIV_CTRL: B0 0x71(2)])=0b1, polarity of TRX_SW pin (#21) is reversed.

TX/RX condition	INV_TRX_SW=0b0 (default setting)		INV_TRX_SW=0b1 (polarity reverse)		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	L	L	L	H	Idel state
TX	L	H	L	L	TX state
RX	L	L	L	H	When diversity disable or initial condition when diversity enable is set ([2DIV_CTRL: B0 0x71(0)]=0b1).
	H/L	L	H/L	H	If diversity enable is set,during searching (TRX_SW=H) and (TRX_SW=L) is switched alternatively. After diversity completion , fix to one of the condition.

In the above setting, If INV_ANT_SW([2DIV_CTRL: B0 0x71(3)])=0b1, ANT_CTRL1([2DIV_CTRL: B0 0x71(5)])=0b1 are set, polarity of ANT_SW pin (#20)is reversed.

TX/RX state	INV_ANT_SW=0b0 ANT_CTRL1=any (default setting)		INV_ANT_SW=0b1 ANT_CTRL1=0b1		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	L	L	H	L	Idle state
TX	L	H	H	H	TX state
RX	L	L	H	L	When diversity disable or intial codition when diversity enable is set ([2DIV_CTRL: B0 0x71(0)]=0b1).
	H/L	L	L/H	L	If diversity enable is set, during searching (ANT_SW=H) and (ANT_SW=L) is switched alternatively. After diversity completion, fix to one of the condition.

○Antenna switch forced setting

ANT_SW pin (#20) and TRX_SW pin (#21) output conditions can be set to fix by [RF_CNTRL_SET: B0 0x75] register, or 2DIV_RSLT2 ([2DIV_RSLT:B0 0x72(1)]) and INV_TRX_SW ([2DIV_CNTRL:B0 0x71(2)]) when diversity fuction is diabled.

1. Forced setting by [RF_CNTRL_SET] register

   ANT_SW pin: By ANT_SW_EN (bit1)=0b1, ANT_SW_SET (bit5) condition will be output.
   TRX_SW pin: By TRX_SW_EN (bit0)=0b1, TRX_SW_SET (bit4) condition will be output.

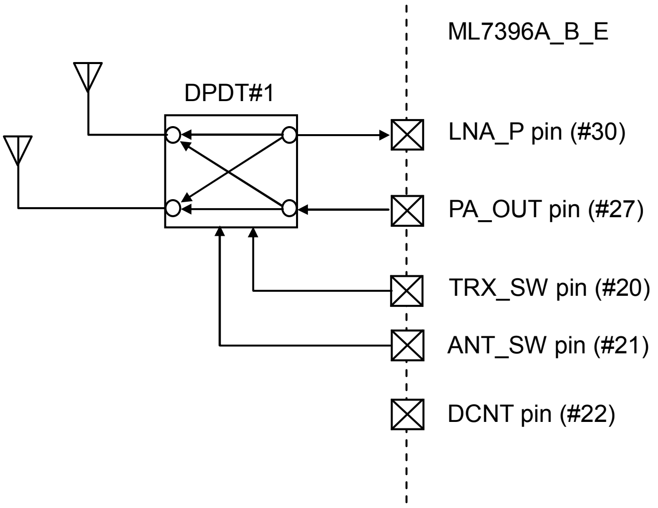
2. Forced setting by 2DIV_RSLT2 bit and INV_TRX_SW bit when diversity function is disabled
   (2DIV_EN ([2DIV_CNTRL:B0 0x71(0)])=0b0)

   ANT_SW pin: When 2DIV_RSLT2=0b0, output “L”. When 0b1, output “H”.
   TRX_SW pin: When INV_TRX_SW=0b0, output “L”. When 0b1, output “H”.

Output defined by [RF_CNTRL_SET:B0 0x75] registers setting has higer priority.
When diversity is enable (2DIV_EN=0b1), output defined by 2DIV_RSLT2 and INV_TRX_SW are ignored.
Any antenna switch setting is inhibited to avoid out-of-synchronization during RECEIVE state.

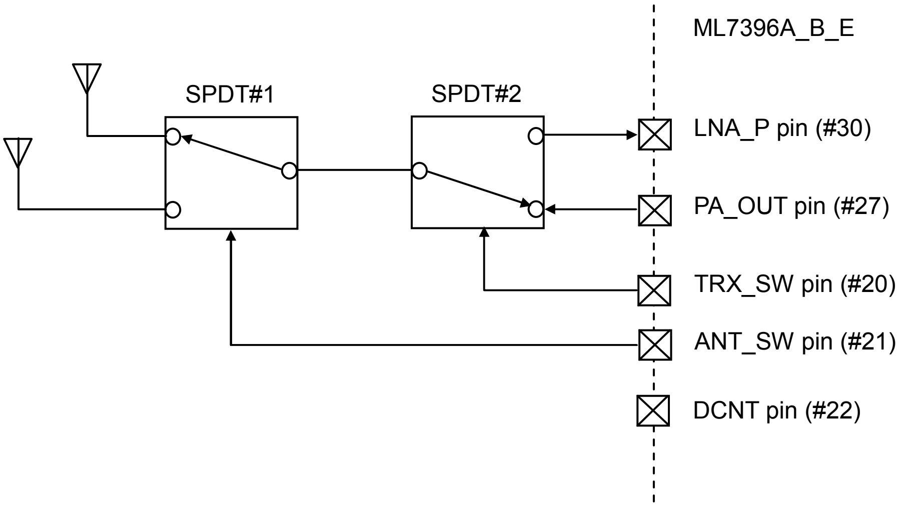
Antenna switching control signals can be also used as below.

Example 1) using one DPDT switch
Please set 2PORT_SW([2DIV_CTRL: B0 0x71(1)])=0b1.


ML7396A_B_E
DPDT#1
LNA_P pin (#30)
PA_OUT pin (#27)
TRX_SW pin (#20)
ANT_SW pin (#21)
DCNT pin (#22)

(Note) altenate external PA control signal exists (DCNT pin).
(Note) external circuits around LNA_P pin, PA_OUT pin and antenna switch (DPDT#1) are omitted in this example.

Example 2) using 2 SPDT switches
Please set 2PORT_SW([2DIV_CTRL: B0 0x71(1)])=0b0.


ML7396A_B_E
SPDT#1
SPDT#2
LNA_P pin (#30)
PA_OUT pin (#27)
TRX_SW pin (#20)
ANT_SW pin (#21)
DCNT pin (#22)

(Note) altenate external PA control signal exsits. (DCNT pin)
(Note) external circuits around LNA_P pin, PA_OUTpin and antenna switch(SPDT#2) are omitted in this example.

●CCA (Clear Channel Assessment) Function

ML7396 family has CCA function that will check availability of certain channel. 3 type of modes are available, normal mode, continuous mode, IDLE detection mode.

[CCA mode setting]
At normal operation

CCA mode	[CCA_CNTRL:B0 0x15]		
	Bit4 (CCA_EN)	Bit3 (CCA_IDLE_EN)	Bit5 (CCA_LOOP_START)
Normal mode	0b1	0b0	0b0
Continuous mode	0b1	0b0	0b1
IDLE detection mode	0b1	0b1	0b0

When using AUTO_ACK

CCA mode	[AUTO_ACK_SET:B0 0x55]	[CCA_CNTRL:B0 0x15]
	Bit4 (AUTO_ACK_EN)	Bit7 (CCA_AUTO_EN)
IDLE detection mode	0b1	0b1

When using address filtering

CCA mode	[ADDFIL_CNTRL:B2 0x60]	[PACKET_MODE_SET:B0 0x45]
	Bit0 to Bit4	Bit0 (ADDFIL_IDLE_DET)
IDLE detection mode	Set 0b1 to any bits	0b1

○Normal mode

Normal mode determines IDLE or BUSY. CCA (normal mode) will be executed when RX_ON is issued while CCA_EN ([CCA_CNTRL:B0 0x15(4)])=0b1, CCA_IDLE_EN ([CCA_CNTRL:B0 0x15(3)])=0b0 and CCA_LOOP_START ([CCA_CNTRL:B0 0x15(5)])=0b0 are set.

The judgement of CCA is determined by average ED value in [ED_RSLT:B0 0x16] and threshold value defined by [CCA_LEVEL:B0 0x13] register. If average ED value exceeds CCA threshold value, it is determined as “BUSY”. And set CCA_RSLT[1:0] ([CCA_CNTRL:B0 0x15(1-0)]) =0b01 is set. If ED value is smaller than CCA threshold, and maintains IDLE detection period which is defined by IDLE_WAIT[9:0] of the [IDLE_WAIT_L:B0 0x17], [IDLE_WAIT_H:B0 0x18] resisters, it is determined as “IDLE”. And CCA_RSLT[1:0] = 0b00 is set. For details operation of IDLE_WAIT[9:0], please refer to “IDLE detection for long period”.

If “BUSY” or “IDLE” is determined, CCA_DONE [CCA_CNTRL:B0 0x15(2)] will become 0b1 and CCA completion interrupt (INT[08] group2) is generated. CCA_EN bit will be cleared to 0b0 automatically.
When CCA completion interrupt is cleared, CCA_RSLT[1:0] are reset to 0b00. Therefore CCA_RSLT[1:0] need to be read before clearing CCA completion interrupt.

If an ED value exceeds the value defined by [CCA_IGNORE_LEVEL:B0 0x12] register, and as long as a given ED value is included in the averaging target of ED value calculation, IDLE judgment is not performed. In this case, if average ED value exceeds CCA threshold value, it is determined as “BUSY” and CCA operation is terminated. However, if average ED value is smaller than CCA threshold value, IDLE judgment is not determined. And CCA_RSLT[1:0] indicates 0b11. CCA operation continues until “BUSY” is ditermined or the given ED value is out of the averaging target and “IDLE” is determined. For detail operation of ED value exceeding [CCA_IGNORE_LEVEL:B0 0x12] register, please refer to "IDLE determination exclusion under strong signal input".

Timing from CCA command issue to the CCA completion is calculated as the following formula.

[IDLE detection]
CCA execution time = (ED value average times + IDLE_WAIT setting) * A/D conversion time +
filter stabilization time (A/D conversion time* 2)

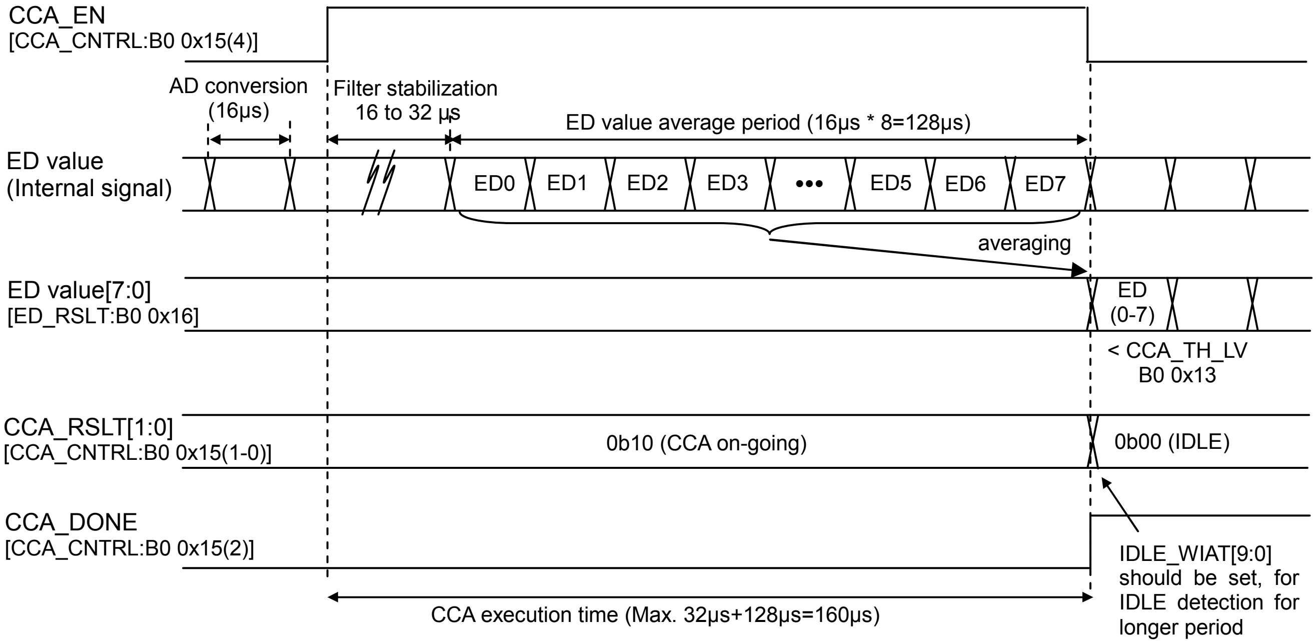
[BUSY detection]
CCA execution time = ED value average times * A/D conversion time+ filter stabilization time (A/D conversion time* 2)

[Note]
1. Above formula does not consider IDLE judgment exclusion based on [CCA_IGNORE_LEVEL:B0 0x12] register.
   For details, please refer to "DLE determination exclusion under strong signal input ".
2. A/D conversion time can be selected by ADC_CLK_SET ([ADC_CLK_SET:B0 0x08(4)]).
   ADC_CLK_SET=0b0: 17.8μs, 0b1: 16μs

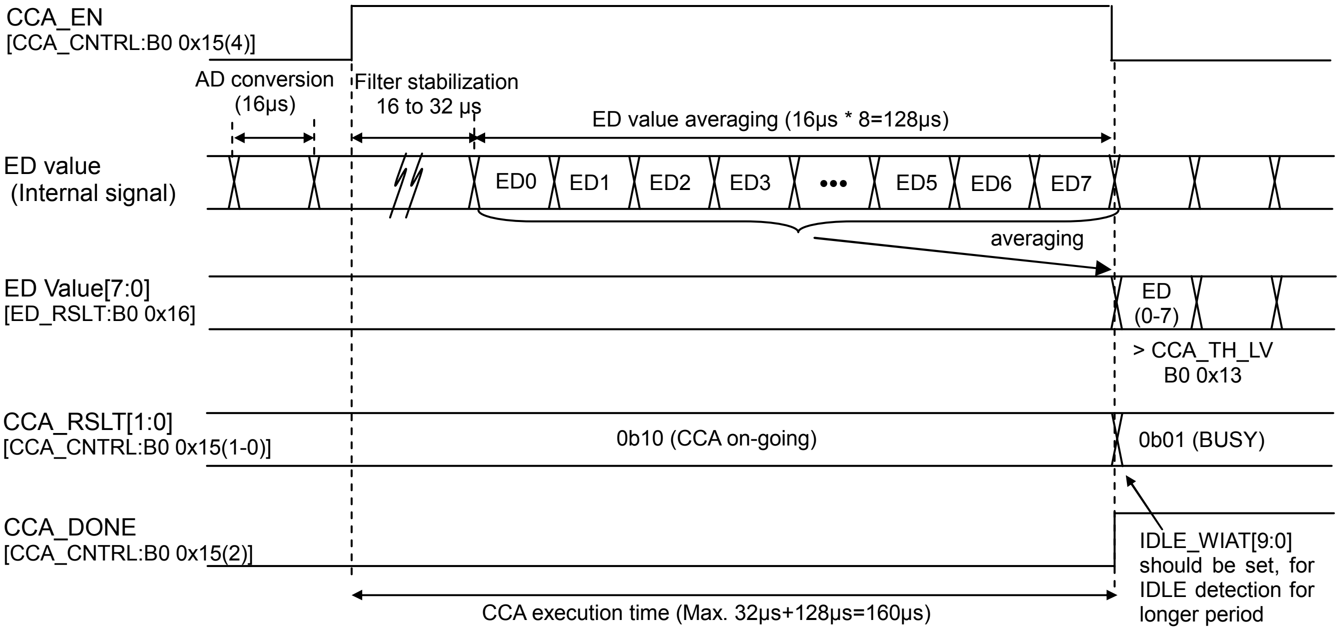
The following is timing chart for normal mode.

[Conditions]
ADC_CK_SET ([ADC_CLK_SET:B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0] ([ED_CNTRL:B0 0x1B(2-0)])=0b011 (ED value 8 times average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H:B0 0x17/0x18(1-0)])=0b00_0000_0000 (IDLE detection 0µs)

[IDLE detection case]


CCA_EN
[CCA_CNTRL:B0 0x15(4)]
AD conversion (16µs)
Filter stabilization 16 to 32 µs
ED value average period (16µs * 8=128µs)
ED value
(Internal signal)
ED0
ED1
ED2
ED3
•••
ED5
ED6
ED7
averaging
ED value[7:0]
[ED_RSLT:B0 0x16]
ED (0-7)
< CCA_TH_LV B0 0x13
CCA_RSLT[1:0]
[CCA_CNTRL:B0 0x15(1-0)]
0b10 (CCA on-going)
0b00 (IDLE)
CCA_DONE
[CCA_CNTRL:B0 0x15(2)]
IDLE_WIAT[9:0] should be set, for IDLE detection for longer period
CCA execution time (Max. 32µs+128µs=160µs)

[BUSY detection case]


CCA_EN
[CCA_CNTRL:B0 0x15(4)]
AD conversion (16µs)
Filter stabilization 16 to 32 µs
ED value averaging (16µs * 8=128µs)
ED value
(Internal signal)
ED0
ED1
ED2
ED3
•••
ED5
ED6
ED7
averaging
ED Value[7:0]
[ED_RSLT:B0 0x16]
ED (0-7)
> CCA_TH_LV B0 0x13
CCA_RSLT[1:0]
[CCA_CNTRL:B0 0x15(1-0)]
0b10 (CCA on-going)
0b01 (BUSY)
CCA_DONE
[CCA_CNTRL:B0 0x15(2)]
IDLE_WIAT[9:0] should be set, for IDLE detection for longer period
CCA execution time (Max. 32µs+128µs=160µs)

[Note]

1. After issuing CCA command, transit into no-input state, and exit this state after filter stbilization.
2. When the iput level chnge from no-input to -80dBm, it takes around 32 µs for indicating -80dBm ED value.

○Continuous mode

Continuous mode continues CCA operation until terminated by the host MCU. CCA continuous mode will be executed when RX_ON is issued while CCA_EN ([CCA_CNTRL:B0 0x15(4)])=0b1, CCA_IDLE_EN ([CCA_CNTRL:B0 0x15(3)])=0b0 and CCA_LOOP_START ([CCA_CNTRL:B0 0x15(5)])=0b1 are set.

Like normal mode, CCA is determined by average ED value in [ED_RSLT:B0 0x16] register and threshold value defined by [CCA_LEVEL:B0 0x13] register. If average ED value exceeds CCA threshold, it is determined as “BUSY”, set CCA_RSLT[1:0] ([CCA_CNTRL:B0 0x15(1-0)]) =0b01. If ED value is smaller than CCA threshold, and maintains IDLE detection period which is defined by IDLE_WAIT[9:0] of the [IDLE_WAIT_L:B0 0x17], [IDLE_WAIT_H:B0 0x18] resisters, it is determined as “IDLE”. And CCA_RSLT[1:0] = 0b00 is set. For details operation of IDLE_WAIT[9:0], please refer to “IDLE detection for long period”.

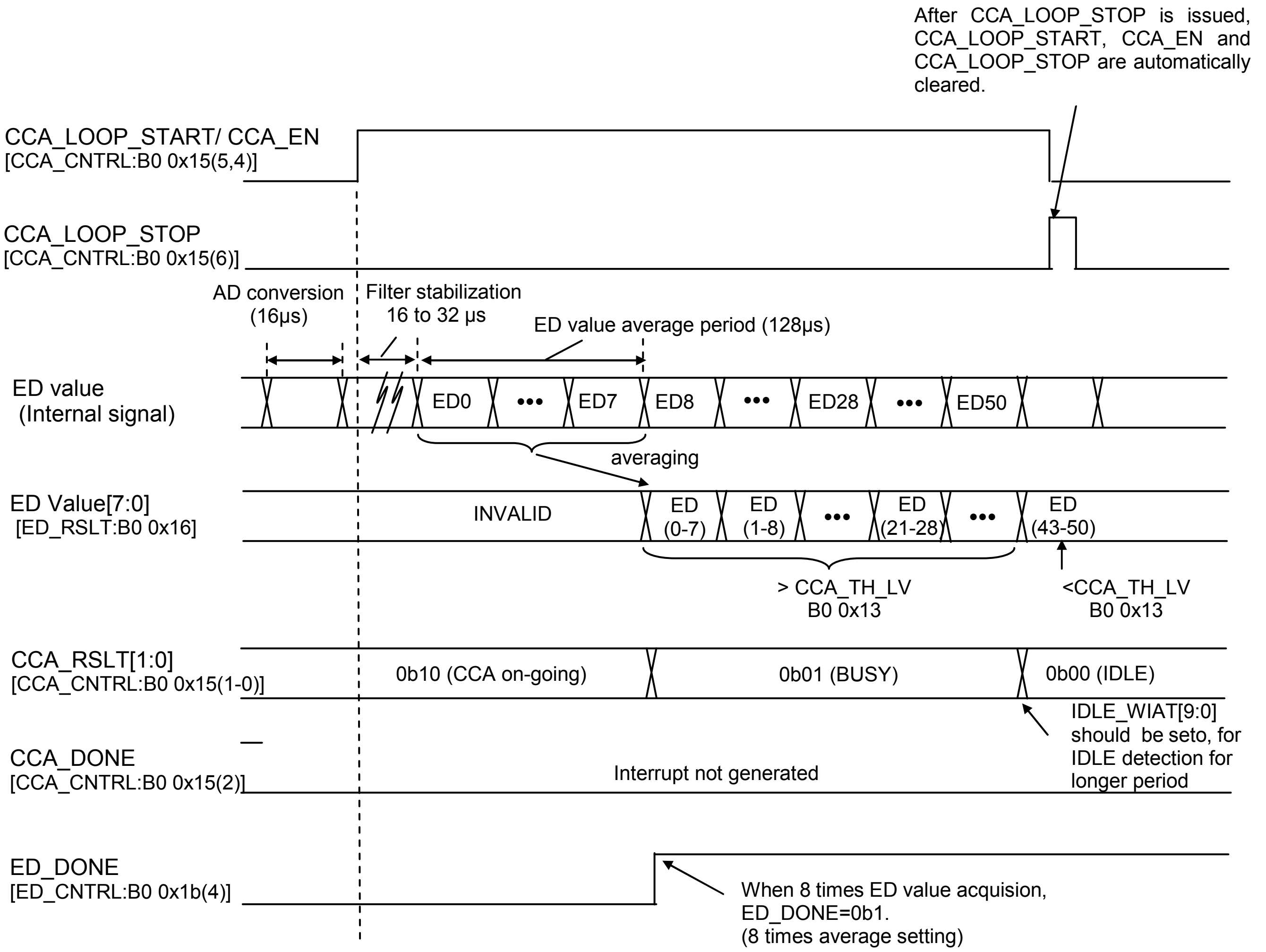
If an ED value exceeds the value defined by [CCA_IGNORE_LEVEL:B0 0x12] register, and as long as a given ED value is included in the averaging target of ED value calculation, IDLE judgment is not performed. In this case, if average ED value exceeds CCA threshold value, it is determined as “BUSY” and CCA operation is terminated. However, if average ED value is smaller than CCA threshold value, IDLE judgment is not determined. And CCA_RSLT[1:0] indicates 0b11. For detail operation of ED value exceeding [CCA_IGNORE_LEVEL:B0 0x12] register, please refer to "IDLE determination exclusion under strong signal input".

Continuous mode does not stop when “BUSY” or “IDLE” is determined. CCA operation continues until 0b1 is set to CCA_LOOP_STOP ([CCA_CNTRL:B0 0x15(6)]). Result is updated every time ED value is acquired. CCA_DONE ([CCA_CNTRL:B0 0x15(2)]) will not be 0b1, and CCA completion interrupt (INT[08] group2) will not be generated.

The following is timing chart for continuous mode.

[Conditions]
ADC_CK_SET ([ADC_CLK_SET:B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0] ([ED_CNTRL:B0 0x1B(2-0)])=0b011 (ED value 8 times average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H:B0 0x17/0x18(1-0)])=0b00_0000_0000 (IDLE detection 0μs)

[BUST to IDLE transitions, terminated with CCA_LOOP_STOP]


After CCA_LOOP_STOP is issued, CCA_LOOP_START, CCA_EN and CCA_LOOP_STOP are automatically cleared.
CCA_LOOP_START/ CCA_EN
[CCA_CNTRL:B0 0x15(5,4)]
CCA_LOOP_STOP
[CCA_CNTRL:B0 0x15(6)]
AD conversion (16μs)
Filter stabilization 16 to 32 μs
ED value average period (128μs)
ED value
(Internal signal)
ED0
•••
ED7
ED8
•••
ED28
•••
ED50
averaging
ED Value[7:0]
[ED_RSLT:B0 0x16]
INVALID
ED (0-7)
ED (1-8)
•••
ED (21-28)
•••
ED (43-50)
> CCA_TH_LV B0 0x13
<CCA_TH_LV B0 0x13
CCA_RSLT[1:0]
[CCA_CNTRL:B0 0x15(1-0)]
0b10 (CCA on-going)
0b01 (BUSY)
0b00 (IDLE)
IDLE_WIAT[9:0] should be seto, for IDLE detection for longer period
CCA_DONE
[CCA_CNTRL:B0 0x15(2)]
Interrupt not generated
ED_DONE
[ED_CNTRL:B0 0x1b(4)]
When 8 times ED value acquision, ED_DONE=0b1.
(8 times average setting)

[Note]

1. After issuing CCA command, transit into no-input state, and exit this state after filter stbilization.
2. When the iput level chnge from no-input to -80dBm, it takes around 32 μs for indicating -80dBm ED value.

○IDLE detection mode

IDLE detection mode continues CCA until IDLE detection. IDLE detection CCA will be executed when RX_ON is issued while CCA_EN ([CCA_CNTRL:B0 0x15(4)])=0b1, CCA_IDLE_EN ([CCA_CNTRL:B0 0x15(3)])=0b1 and CCA_LOOP_START ([CCA_CNTRL:B0 0x15(5)])=0b0 are set.

When AUTO_ACK function is enabled by AUTO_ACK_EN ([AUTO_ACK_SET:B0 0x55(4)])=0b1, if CCA_AUTO_EN ([CCA_CTRL:B0 0x15(7)]) =0b1, CCA IDLE detection mode is performed before transsmitting ACK packet.
And when Address filtering function is enable by setting 0b1 to any bit0 to bit4 of [ADDFIL_CNTRL:B2 0x60] register, if ADDFIL_IDLE_DET ([PACKET_MODE_SET:B0 0x45(0)])=0b1, CCA IDLE detection mode is performed after address mismatch detection.

Like normal mode, CCA is determined by average ED value in [ED_RSLT:B0 0x16] register and threshold value defined by [CCA_LEVEL:B0 0x13] register. If average ED value exceeds CCA threshold, it is determined as “BUSY”, set CCA_RSLT[1:0] ([CCA_CNTRL:B0 0x15(1-0)]) =0b01. If ED value is smaller than CCA threshold, and maintains IDLE detection period which is defined by IDLE_WAIT[9:0] of the [IDLE_WAIT_L:B0 0x17], [IDLE_WAIT_H:B0 0x18] resisters, it is determined as “IDLE”. And CCA_RSLT[1:0] = 0b00 is set. For details operation of IDLE_WAIT[9:0], please refer to “IDLE detection for long period”.

In IDLE detection mode, only when IDLE is detected, CCA_DONE ([CCA_CNTRL:B0 0x15(2)]) wil be set to 0b1 and CCA completion interrupt (INT[08] group2) is generated. If CCA operation is performed by CCA_EN=0b1, after IDLE detection, CCA_EN and CCA_IDLE_EN are reset to 0b0.

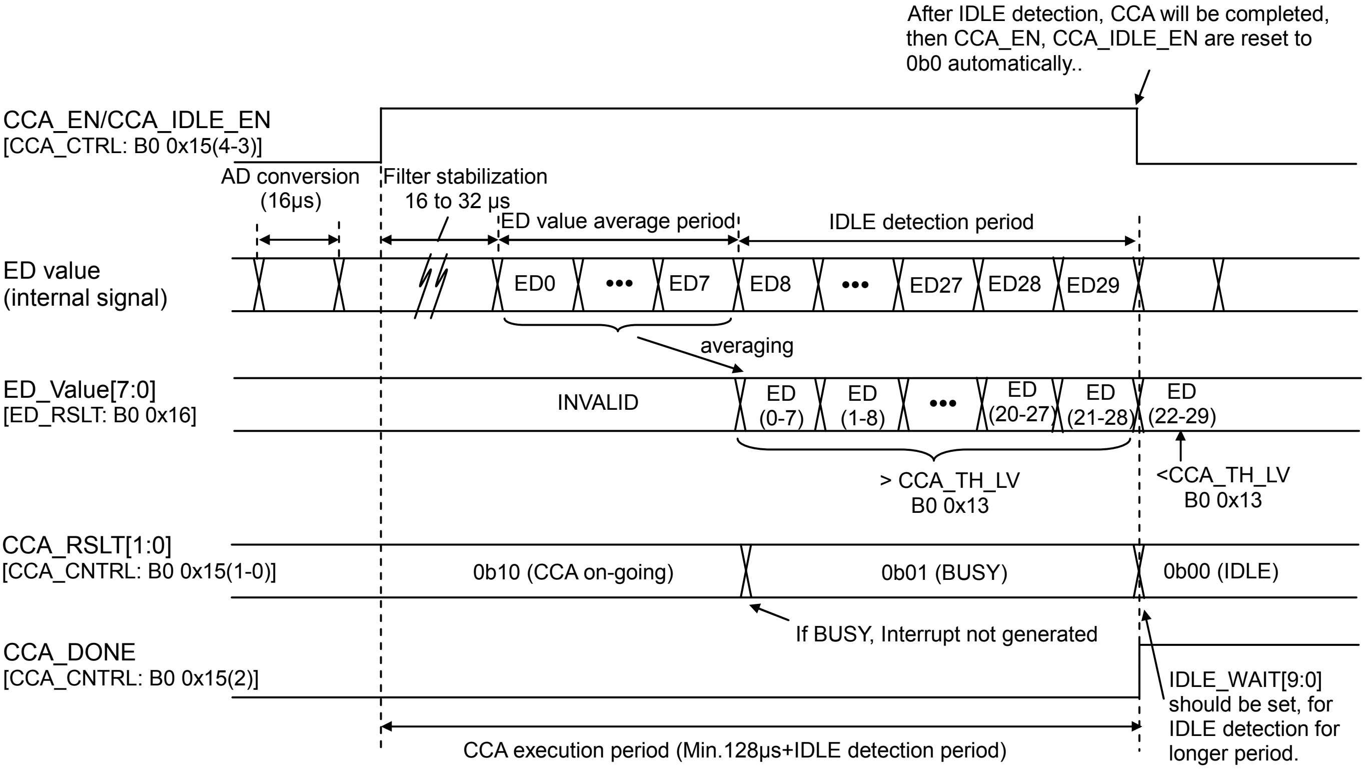
Upon clearing CCA completion interrupt, CCA_RSLT[1:0] are reset to 0b00. CCA_RSLT[1:0] should be read before clearing CCA completion interrupt.

If an ED value exceeds the value defined by [CCA_IGNORE_LEVEL:B0 0x12] register, and as long as a given ED value is included in the averaging target of ED value calculation, IDLE judgment is not performed. In this case, if average ED value is smaller than CCA threshold value, IDLE judgment is not determined. And CCA_RSLT[1:0] indicates 0b11. CCA operation continues until given ED value is out of averaging target and “IDLE” is determined. For details of ED value exceeding [CCA_IGNORE_LEVEL: B0 0x12] register, please refer to ”IDLE determination exclusion under strong signal input”.

The follwing is timing chart for IDLE detection.

[Upon BUSY detection, continue CCA and IDLE detection case]

[Conditions]
ADC_CK_SET ([ADC_CLK_SET:B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0] ([ED_CNTRL:B0 0x1B(2-0)])=0b011 (ED value 8 times average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H:B0 0x17/0x18(1-0)])=0b00_0000_0000 (IDLE detection 0µs)


After IDLE detection, CCA will be completed, then CCA_EN, CCA_IDLE_EN are reset to 0b0 automatically..
CCA_EN/CCA_IDLE_EN
[CCA_CTRL: B0 0x15(4-3)]
AD conversion (16µs)
Filter stabilization 16 to 32 µs
ED value average period
IDLE detection period
ED value (internal signal)
ED0
ED7
ED8
ED27
ED28
ED29
averaging
ED_Value[7:0]
[ED_RSLT: B0 0x16]
INVALID
ED (0-7)
ED (1-8)
ED (20-27)
ED (21-28)
ED (22-29)
> CCA_TH_LV B0 0x13
<CCA_TH_LV B0 0x13
CCA_RSLT[1:0]
[CCA_CNTRL: B0 0x15(1-0)]
0b10 (CCA on-going)
0b01 (BUSY)
0b00 (IDLE)
If BUSY, Interrupt not generated
CCA_DONE
[CCA_CNTRL: B0 0x15(2)]
IDLE_WAIT[9:0] should be set, for IDLE detection for longer period.
CCA execution period (Min.128µs+IDLE detection period)

[Note]

1. After issuing CCA command, transit into no-input state, and exit this state after filter stbilization.
2. When the iput level chnge from no-input to -80dBm, it takes around 32 µs for indicating -80dBm ED value.

○IDLE determination exclusion under strong signal input

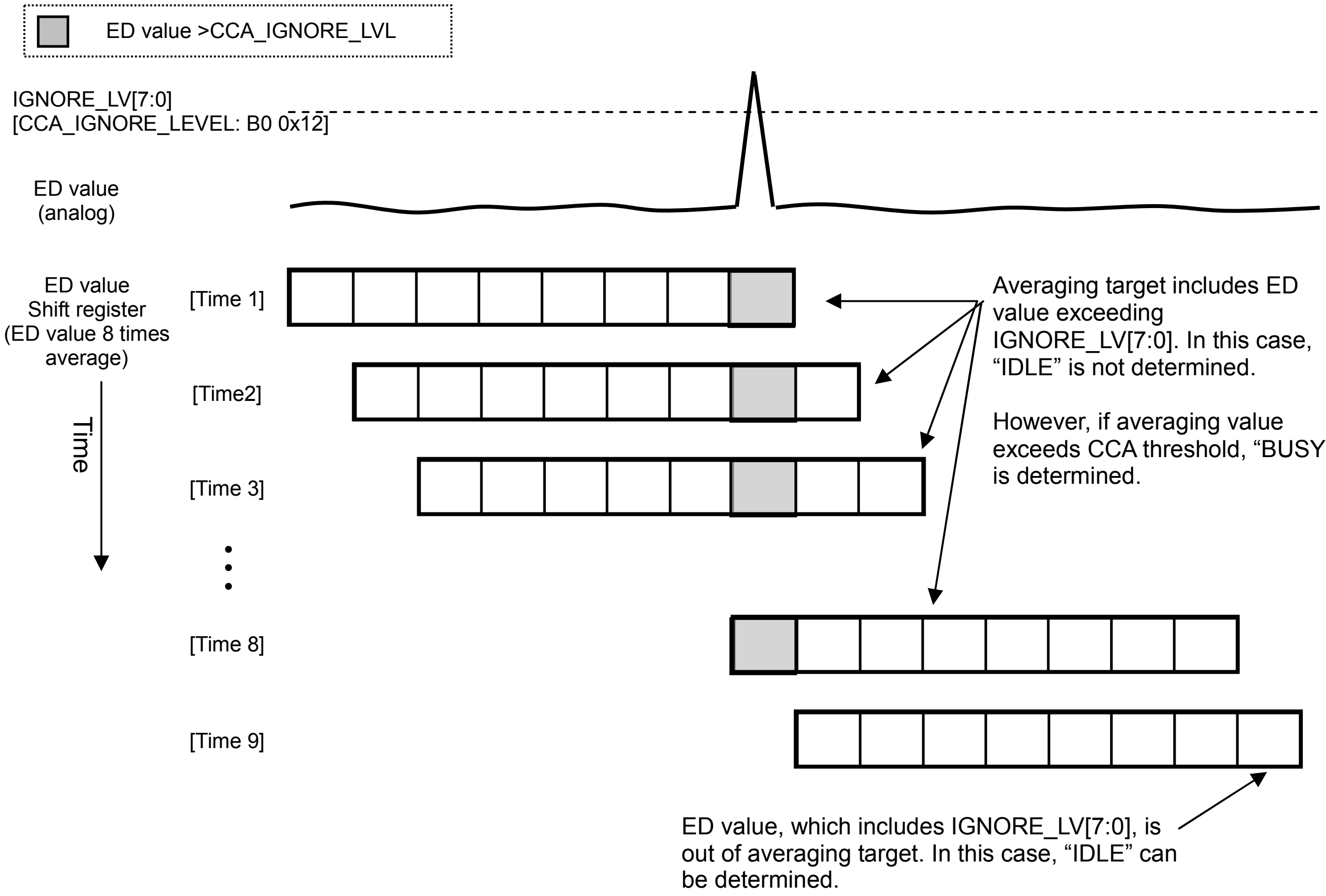
If acquired ED value exceeds [CCA_IGNORE_LVL: B0 0x12] register, IDLE dertermination is not performed as lon as a given ED value is included in the averaging target range. If average ED value including this strong ED value indicated in [ED_RSLT: B0 0x16] register exceeds the CCA threshold value defined by [CCA_LEVEL: B0 0x13] register, it is considered as "BUSY". And CCA_RSLT[1:0]([CCA_CTRL: B0 0x15(1-0)])=0b01 is set.

If average ED value is smaller than CCA threshold value, IDLE determination is not performed and CCA_RSLT[1:0] indicates 0b11 "CCA evaluation on-going (ED value excluding CCA judgement acquisition)". CCA will continue until "IDLE" or "BUSY" determination (in case of IDLE detection mode, "IDLE2 is determined. In case of continuous mode, CCA_LOOP_STOP([CCA_CTRL: B0 0x15(6)]) is issued.)

[Note]

CCA completion interrupt (INT[08] group2) is generated only when "IDLE" or "BUSY" is determined. Therefore, if data whose ED value exceeds IGNORE_LV[7:0] ([CCA_IGNORE_LEVEL:B0 0x12(7-0)]) are input intermittently, neither "IDLE" or "BUSY" can be determined and CCA may continues.

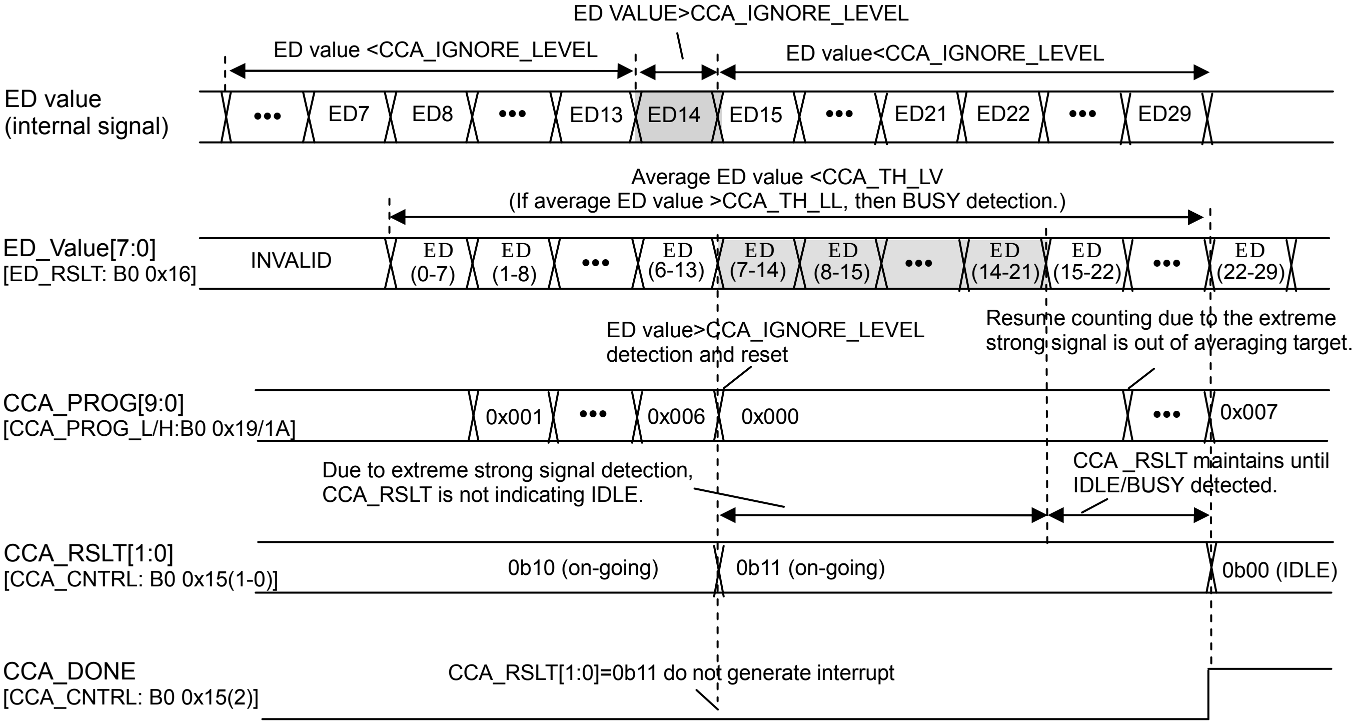
[ED value acquisition under extrem strong signal]


▨ ED value >CCA_IGNORE_LVL
IGNORE_LV[7:0]
[CCA_IGNORE_LEVEL: B0 0x12]
ED value
(analog)
ED value
Shift register
(ED value 8 times
average)
Time
[Time 1]
[Time2]
[Time 3]
[Time 8]
[Time 9]
Averaging target includes ED value exceeding IGNORE_LV[7:0]. In this case, "IDLE" is not determined.
However, if averaging value exceeds CCA threshold, "BUSY" is determined.
ED value, which includes IGNORE_LV[7:0], is out of averaging target. In this case, "IDLE" can be determined.

The follwing is timing chart for CCA determination exclusion under strong signal.

[During IDLE_WAIT counting, detected extremly strong signal. After the given signal is out of averaging target, IDLE detection case]

[Condition]
CCA normal mode
ADC_CK_SEL ([ADC_CLK_SET: B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0] ([ED_CTRL: B0 0x1B(2-0)])=0b011 (ED value 8 times average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H: B0 0x17/18(1-0)])=0b00_0000_0111(IDLE detection period 112μs)


ED VALUE>CCA_IGNORE_LEVEL
ED value <CCA_IGNORE_LEVEL
ED value<CCA_IGNORE_LEVEL
ED value
(internal signal)
•••
ED7
ED8
•••
ED13
ED14
ED15
•••
ED21
ED22
•••
ED29
Average ED value <CCA_TH_LV
(If average ED value >CCA_TH_LL, then BUSY detection.)
ED_Value[7:0]
[ED_RSLT: B0 0x16]
INVALID
ED (0-7)
ED (1-8)
•••
ED (6-13)
ED (7-14)
ED (8-15)
•••
ED (14-21)
ED (15-22)
•••
ED (22-29)
ED value>CCA_IGNORE_LEVEL
detection and reset
Resume counting due to the extreme
strong signal is out of averaging target.
CCA_PROG[9:0]
[CCA_PROG_L/H:B0 0x19/1A]
0x001
•••
0x006
0x000
•••
0x007
Due to extreme strong signal detection,
CCA_RSLT is not indicating IDLE.
CCA _RSLT maintains until
IDLE/BUSY detected.
CCA_RSLT[1:0]
[CCA_CNTRL: B0 0x15(1-0)]
0b10 (on-going)
0b11 (on-going)
0b00 (IDLE)
CCA_DONE
[CCA_CNTRL: B0 0x15(2)]
CCA_RSLT[1:0]=0b11 do not generate interrupt

[Note]

1. After issuing CCA command, transit into no-input state, and exit this state after filter stbilization.
2. When the iput level chnge from no-input to -80dBm, it takes around 32 μs for indicating -80dBm ED value.

○IDLE detection for long period

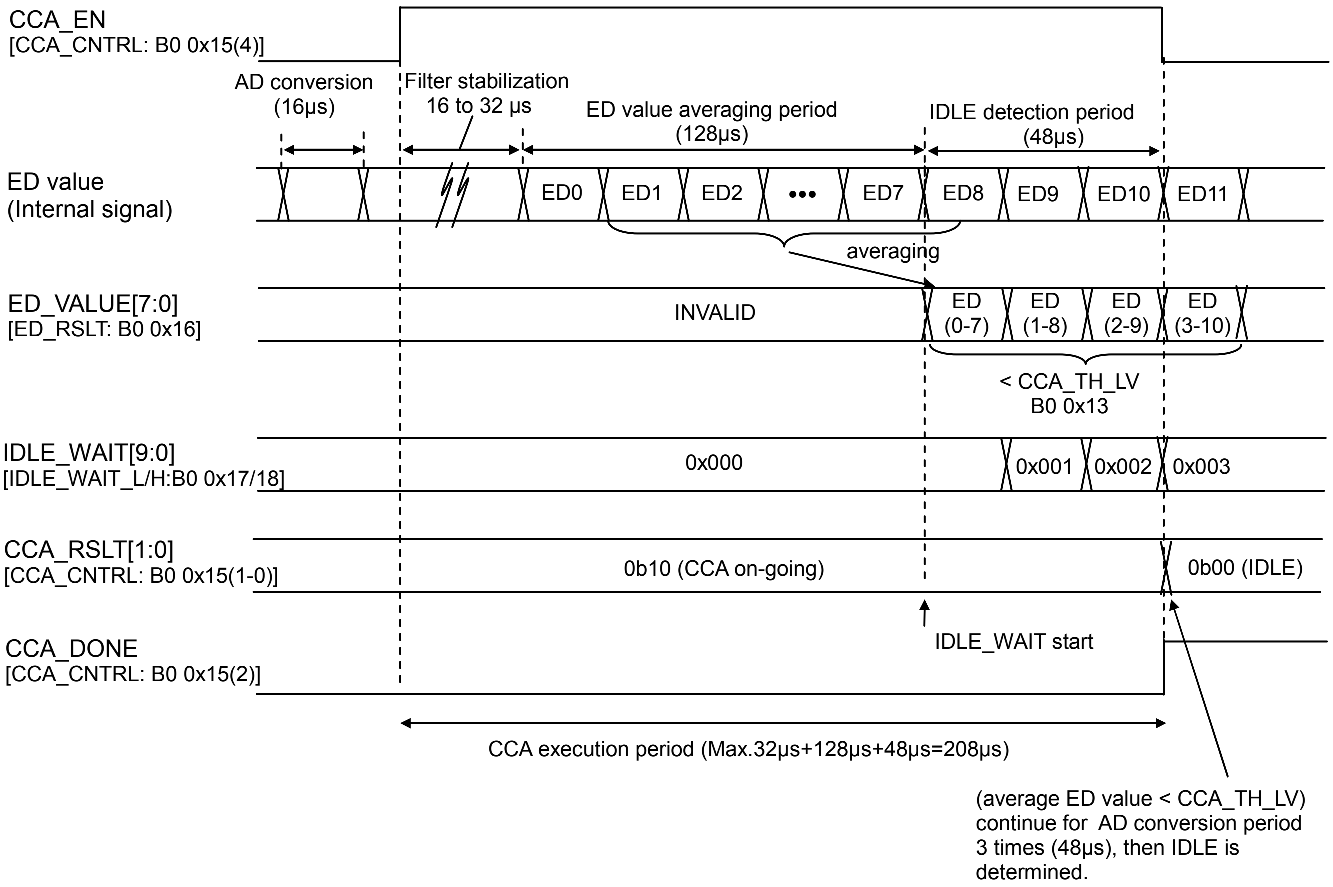
When CCA IDLE detection is performed for longer time period, IDLE_WAIT[9:0]([IDLE_WAIT_L/H:B0 0x17/18(1-0)] can be used. By setting IDLE_WAIT [9:0], averaging period longer than the period (for example, AD conversion16μs, 8 times average setting 128μs) can be possible.

This function can be used for IDLE determination – by counting times when average ED value becomes smaller than CCA threshold defined by [CCA_LEVEL: B0 0x13] register. When counting exceed IDLE_WAIT [9:0], IDLE is determined. If average ED value exceeds CCA threshold level, imemediately "Busy" is determined without wait for IDLE_WAIT [9:0] period.

The following timing chart is IDLE detection setting IDLE_WAIT[9:0].

[ED value 8 timesv average IDLE detection case]

[Condition]
CCA normal mode
ADC_CK_SEL ([ADC_CLK_SET: B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0] ([ED_CTRL: B0 0x1B(2-0)])=0b011 (ED value 8 times average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H: B0 0x17/18(1-0)])=0b00_0000_0011 (IDLE detection period 48μs)

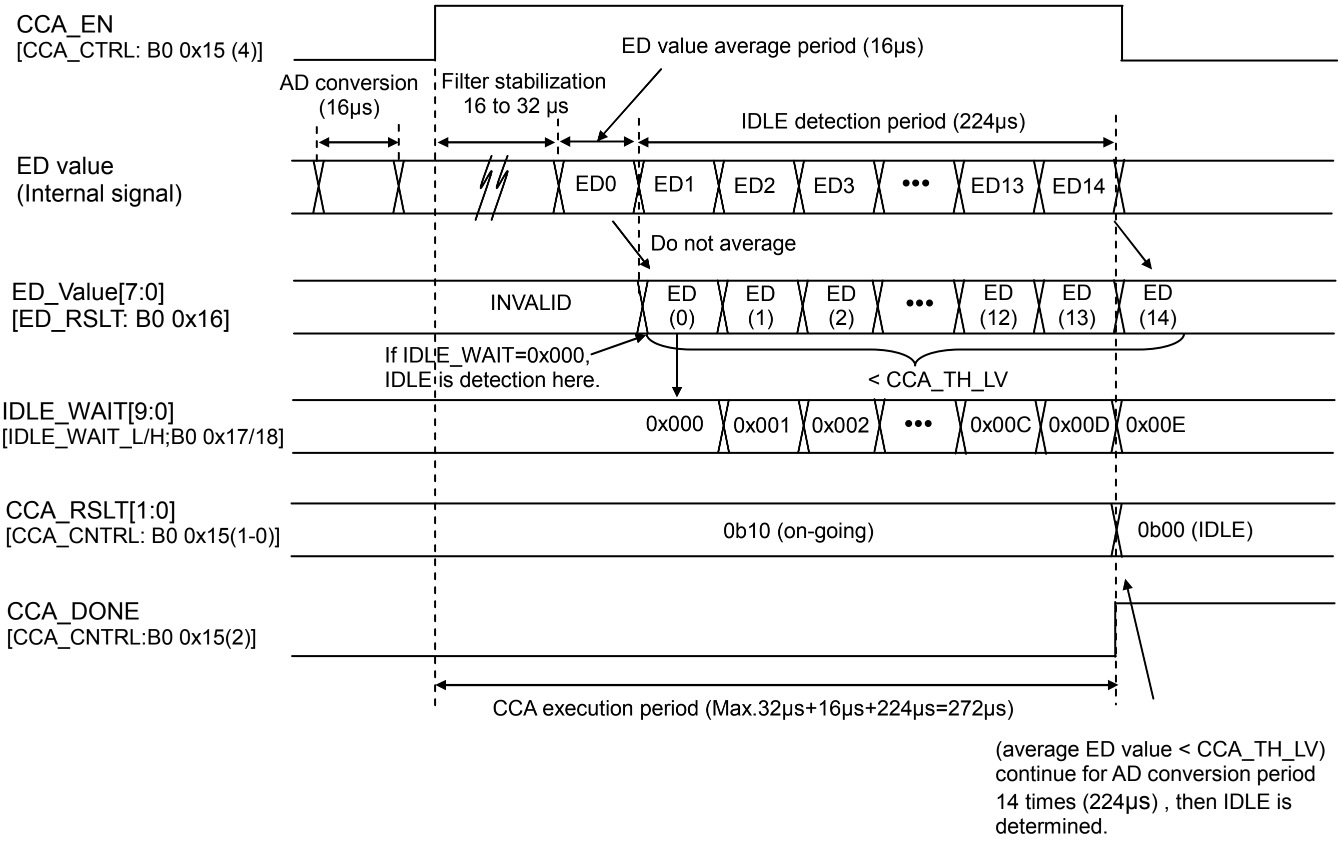

CCA_EN
[CCA_CNTRL: B0 0x15(4)]
AD conversion
(16μs)
Filter stabilization
16 to 32 μs
ED value averaging period
(128μs)
IDLE detection period
(48μs)
ED value
(Internal signal)
ED0
ED1
ED2
•••
ED7
ED8
ED9
ED10
ED11
averaging
ED_VALUE[7:0]
[ED_RSLT: B0 0x16]
INVALID
ED (0-7)
ED (1-8)
ED (2-9)
ED (3-10)
< CCA_TH_LV
B0 0x13
IDLE_WAIT[9:0]
[IDLE_WAIT_L/H:B0 0x17/18]
0x000
0x001
0x002
0x003
CCA_RSLT[1:0]
[CCA_CNTRL: B0 0x15(1-0)]
0b10 (CCA on-going)
0b00 (IDLE)
IDLE_WAIT start
CCA_DONE
[CCA_CNTRL: B0 0x15(2)]
CCA execution period (Max.32μs+128μs+48μs=208μs)
(average ED value < CCA_TH_LV) continue for AD conversion period 3 times (48μs), then IDLE is determined.

[Note]

1. After issuing CCA command, transit into no-input state, and exit this state after filter stbilization.
2. When the iput level chnge from no-input to -80dBm, it takes around 32 μs for indicating -80dBm ED value.

[ED value 1time IDLE detection case]

[Condition]
CCA normal mode
ADC_CK_SEL ([ADC_CLK_SET: B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)])=0b000 (ED value 1 time average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H:B0 0x1718(1-0)])=0b00_0000_1110 (IDLE detection period 224μs)


CCA_EN
[CCA_CTRL: B0 0x15 (4)]
ED value average period (16μs)
AD conversion (16μs)
Filter stabilization 16 to 32 μs
IDLE detection period (224μs)
ED value
(Internal signal)
ED0
ED1
ED2
ED3
•••
ED13
ED14
Do not average
ED_Value[7:0]
[ED_RSLT: B0 0x16]
INVALID
ED (0)
ED (1)
ED (2)
ED (12)
ED (13)
ED (14)
If IDLE_WAIT=0x000, IDLE is detection here.
< CCA_TH_LV
IDLE_WAIT[9:0]
[IDLE_WAIT_L/H;B0 0x17/18]
0x000
0x001
0x002
0x00C
0x00D
0x00E
CCA_RSLT[1:0]
[CCA_CNTRL: B0 0x15(1-0)]
0b10 (on-going)
0b00 (IDLE)
CCA_DONE
[CCA_CNTRL:B0 0x15(2)]
CCA execution period (Max.32μs+16μs+224μs=272μs)
(average ED value < CCA_TH_LV) continue for AD conversion period 14 times (224μs) , then IDLE is determined.

○CCA operation during diversity

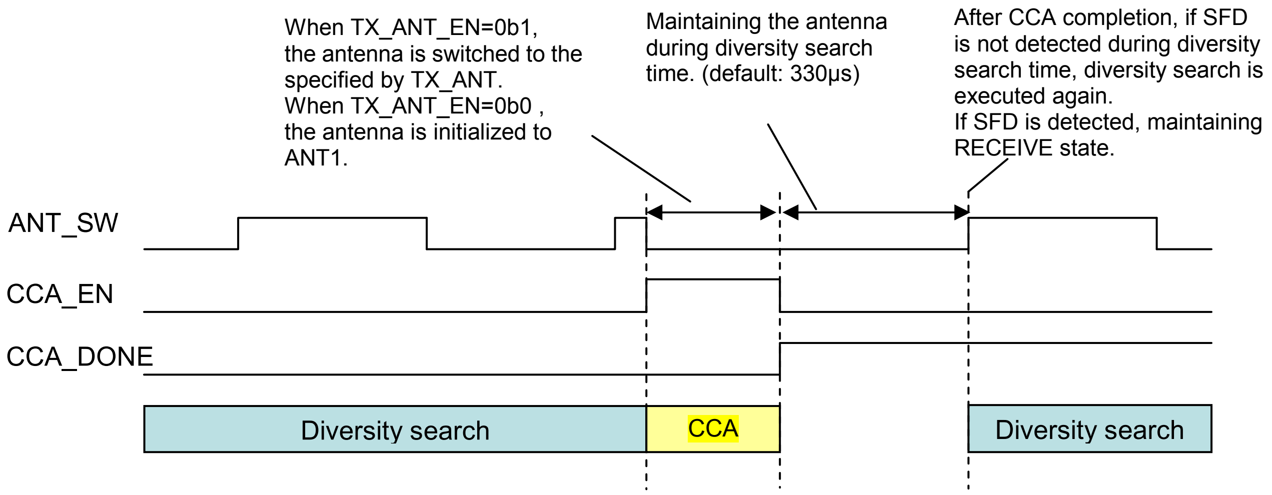
(1) CCA operation during diversity search

During diversity search, If CCA command is issued, diversity terminated and CCA starts.

Upon CCA starting, antenna is fixed to the default value (*1), maintaining until next diversity search. However, if TX_ANT_EN ([2DIV_RSLT:B0 0x72(5)])=0b1 is set, antenna is specified by TX_ANT ([2DIV_RSLT:B0 0x72(4)]) and maintaining until next diversity search.

After CCA completion, if SFD is not detected during diversity search time specified by SEARCH_TIME[6:0] ([2DIV_SEARCH:B0 0x6F(6-0)]) (default approx. 330µs), diversity search will be executed again. If SFD is detected during CCA or after CCA completion, continuing RECEIVE state and diversity search is not executed.

* 1 : Please refer the each table of “Antenna switching function” in “Diversity Function”.
(Upper setting in the "RX" state column)


When TX_ANT_EN=0b1, the antenna is switched to the specified by TX_ANT.
When TX_ANT_EN=0b0 , the antenna is initialized to ANT1.
Maintaining the antenna during diversity search time. (default: 330µs)
After CCA completion, if SFD is not detected during diversity search time, diversity search is executed again.
If SFD is detected, maintaining RECEIVE state.
ANT_SW
CCA_EN
CCA_DONE
Diversity search
CCA
Diversity search

[Note]

When executing CCA during diversity search, set the waiting taimer for waiting for CAA completion interrupt (INT[08] group2). Since CCA executing timing is same as the diversity search completion, CCA completion interrupt may not be notified. When timeout occurs, the latest result is stored into CCA_RSLT[1:0] ([CCA_CNTRL:B0 0x15(1-0)]). In this case, if executing CCA again, set CCA_LOOP_STOP ([CCA_CNTRL:B0 0x15(6)])=0b1 before issuing CCA command.

For waiting timer setting, please refer to the CCA execution time described in "Normal mode".

For details of the CCA execution flow during diversity search, please refer to "CCA operation during diversity" in the “Flow Charts”.

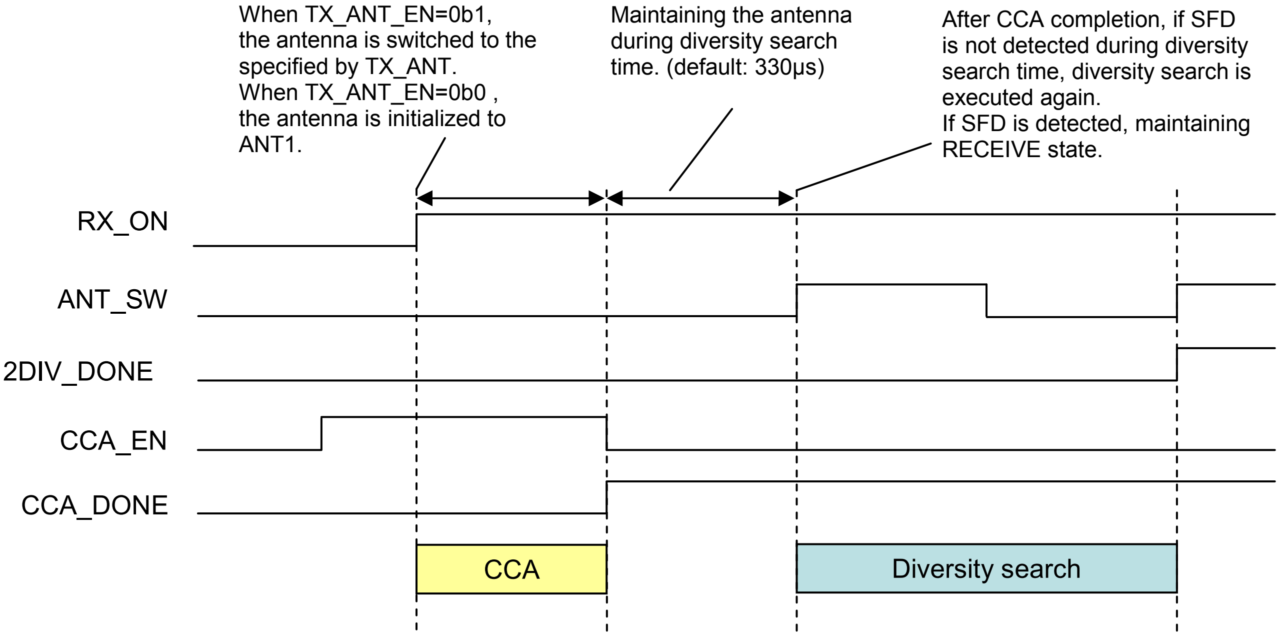
During CCA operarion, RX operation is performed at the same time. Even if CCA_DONE is not notified, SFD detection interrupt (INT[11] group2), RX FIFO access error interruption (INT[14] group2), FIFO-Full interrupt (INT[05] group1), FIFO0/1 RX completion interrupt (INT[18]/[19] group3), or FIFO0/1 CRC error interrupt (INT[20]/[21] group3) may be notified.

For details of the diversity function, please refer to "Diversity Function".

(2) During diversity search, before RX_ON state, CCA is performed

If diversity ON setting and CCA operation setting are enabled before RX_ON state, after RX_ON state transition, diversity search will not perform, but CCA will start.

After CCA completion, if SFD is not detected during diversity search time specified by SEARCH_TIME[6:0] ([2DIV_SEARCH:B0 0x6F(6-0)]) (default approx. 330µs), diversity search wil be executed. If SFD is detected during CCA or after CCAcompletion, continuing RECEIVE state and diversity search is not executed.


When TX_ANT_EN=0b1, the antenna is switched to the specified by TX_ANT. When TX_ANT_EN=0b0 , the antenna is initialized to ANT1.
Maintaining the antenna during diversity search time. (default: 330µs)
After CCA completion, if SFD is not detected during diversity search time, diversity search is executed again. If SFD is detected, maintaining RECEIVE state.
RX_ON
ANT_SW
2DIV_DONE
CCA_EN
CCA_DONE
CCA
Diversity search

●SFD detection function

ML7396 family supports the "Start Frame of Delimiter" (SFD) recognition function. By having 2 sets of SFD pattern strage area, it is possible to detect IEEE 802.15.4g SFD patterns valied by "MRFSKFSD setting" and "FEC scheme". For more details, please refer to IEEE 802.15.4g standard.

Note: The default value of both SFD#1 and SFD#2 (Bank0 0x3A to 0x41) are set to the IEEE 802.15.4d SFD (1byte:0xA7).

In IEEE802.15.4g standard, 4 SFD pattern (each 2 bytes) is defined according to SFD group defined by phyMRFSKSFD and FEC scheme (coded, uncoded).
According to the setting to MRFSKSFD ([PACKET_MODE_SET:B0 0x45(6)]) and FEC_EN ([FEC_CRC_SET:B0 0x46(6)]), SFD pattern to be added TX packet and SFD pattern to be received in RX packet are selected from SDF pattern #1 and SFD pattern #2 as following tables. SFD pattern #1 is defined by [SFD1_SET1:B0 0x3A] to [SFD1_SET4:B0 0x3D] registers and SFD pattern #2 is defined by [SFD2_SET1:B0 0x3E] to [SFD2_SET4:B0 0x41] registers.

(1) TX

①SFD length is shorter than or equal to 2 bytes. (IEEE 802.15.4g format)

FEC_EN	MRFSKSFD	
	0	1
0	SFD1[15:0]	SFD2[15:0]
1	SFD1[31:16]	SFD2[31:16]

②SFD length is longer than or equal to 3 bytes. (Original format

FEC_EN	MRFSKSFD	
	0	1
0/1	SFD1 [31:0]	SFD2 [31:0]

(2) RX

If SFD length is shorter than or equal to 2 bytes and FEC_EN=0b1, it is possible to serach two SFD patterns. According to the matching pattern, FEC is performed. Otherwise serach one pattern and the data following SFD are processed as uncoded.

①SFD length shorter than or equal to 2bytes. (IEEE 802.15.4g format)

FEC_EN	MRFSKSFD	SFD pattern		SFD detect	Data process after SFD
		uncoded	coded		
1	0	SFD1 [15:0]	SFD1 [31:16]	Uncoded or coded	If pattern match with coded pattern, FEC is performed. If pattern match with uncoded pattern, FEC is not performed
1	1	SFD2 [15:0]	SFD2 [31:16]	Uncoded or coded	If pattern match with coded pattern, FEC is performed. If pattern match with uncoded pattenr, FEC is not performed.
0	0	SFD1 [15:0]	-	Uncoded	Determined as uncoded
0	1	SFD2 [15:0]	-	Uncoded	Determined as uncoded

②SFD length is longer than or equal to 3bytes. (Original format)

FEC_EN	MRFSKSFD	SFD pattern		SFD detect	Process following to SFD
		uncoded	Coded		
1	0	SFD1 [31:0]	-	Uncoded	Determined as uncoded
1	1	SFD2 [31:0]	-	Uncoded	Determined as uncoded
0	0	SFD1 [31:0]	-	Uncoded	Determined as uncoded
0	1	SFD2 [31:0]	-	Uncoded	Determined as uncoded

When using IEEE 802.15.4g (2bytes SFD), recommended configuration will be as following table.

Register name	Address (Bank 0)	Setting value
SFD1_SET1	0x3a	0x09
SFD1_SET2	0x3b	0x72
SFD1_SET3	0x3c	0xF6
SFD1_SET4	0x3d	0x72
SFD2_SET1	0x3e	0x5E
SFD2_SET2	0x3f	0x70
SFD2_SET3	0x40	0xC6
SFD2_SET4	0x41	0xB4

●AUTO_ACK function

ML7396 family supports AUTO_ACK function to assist MCU operation in acknowledge packet (hereafter Ack packet) transmission. Followings are detail of the AUTO_ACK function.

[Notes when using AUTO_ACK function]

1. AUTO_ACK function can not be used with FEC function, please set FEC_EN ([FEC/CRC_SET:B0 0x46(6)])=0b1. When MCU handls Ack packet, FEC function can be used.
2. When TX packet and RX packet use diferent FCS length, especially note on the following; If transmissting Ack packet before reading out RX data from FIFO, TX packet FCS length will be applied to the unread RX data stored into FIFO. Therefore, RX data can not be read out correctly. Under this case, before start to read RX data, forcibly set RX packet FCS length by using [FEC/CRC_SET:B0 0x46] register.
   (Above condition will meet when the data packet uses 32bit FCS and Ack packet uses 16bit FCS. Since ML7396 fammily does not support 32bit FCS Ack packet.)

*Ack transmission (MCU requests transmitting Ack packet)

1) Analyzing Frame Control Field in RX data, and if Ack request bit is set to 0b1, then obtain Sequence Number from RX data.

2) After RX completion, performing CRC check and if FCS is OK, then transit to TX_ON state automatically for Ack packet transmission preparation. (At this time, RX completion interrupt (INT[18]/[19] group3) will be generated.)

3) MCU analyzes Address field and Pending data in received data, and it decide to transmit Ack packet, set Ack packet to [ACK_FRAME1:B0 0x53] and [ACK_FRAME2:B0 0x54] registers.
Note: It is dpossible to determine Ack packet transmittion by reading MAC header. Therefore Ack packet setting is possible before RX completion.
If there is a Pending data, the Frame Pending bit should be set to 0b1 by [ACK_FRAME1:B0 0x53] register.

4) After completing TX_ON state transition, Auto_Ack ready interrupt (INT[24] group4) will be generated.
After confirming Ack_ready interrupt, set ACK_SEND ([AUTO_ACK_SET:B0 0x55(1)])=0b1 .

5) Transmitting Ack packet
Frame Control Field is filled with the setting data into [ACK_FRAME1:B0 0x53] and [ACK_FRAME2:B0 0x54] registers.
Sequence Number Field is automatically filled with sequence number obtained from received data.

6) After Ack packet transmission is completed, TX completion interrupt (INT[16]/[17] group 3) will be generated.
Note: RF status keeps TX_ON state, If return to IDLE state, set SET_TRX ([RF_STATUS:B0 0x6C(3-0)]) =0b1000 (TRX_OFF).

*Ack transmission (MCU requests to stop Ack packet transmission)

1) Analyzing Frame Control Field in RX data, and if Ack request bit is set to 0b1, then obtain Sequence Number from RX data.

2) After RX completion, performing CRC check and if FCS is OK, then transit to TX_ON state automatically for Ack packet transmission preparation. (At this time, RX completion interrupt (INT[18]/[19] group3) will be generated.)

3) After completing TX_ON state transition, Auto_Ack ready interrupt (INT[24] group4) will be generated.

4) MCU analyzes Address field and Pending data in received data, and it decide not to send Ack packet, issuing PHY reset by [RST_SET:B0 0x01]=0x88 and then set ACK_STOP ([AUTO_ACK_SET:B0 0x55(0)])=0b1.
ML7396 family aborts Ack packet and RF status will be back to TRX_OFF state automatically.

5) Set ACK_STOP ([AUTO_ACK_SET:B0 0x46(0)])=0b0. If AckAuto_Ack ready interrupt (INT[24] group4) is already generated, please clear the interrupt.

*Ack Transmission (Ack packet transmission using Ack timer)
Condition: AUTO_TIMER_EN ([ACK_TIMER_EN:B0 0x52(0)])=0b1.

1) Analyzing Frame Control Field in RX data, and if Ack request bit is set to 0b1, then obtain Sequence Number from RX data.

2) After RX completion, performing CRC check and if FCS is OK, then transit to TX_ON state automatically for Ack packet transmission preparation. (At this time, RX completion interrupt (INT[18]/[19]) will be generated.)

3) After Completing TX_ON state transition, Ack timer starts counting and Auto_Ack ready interrupt (INT[24] group4) will be generated.

4) After elapsing the period defined by [ACK_TIMER_L/H:B0 0x50/51] registers, Ack packet will be transmitted.

5) After Ack packet trnasumission is completed, TX completion interrupt (INT[]16)/[17] group3) will be generated.
Note: RF status keeps TX_ON state, If return to IDLE state, set SET_TRX ([RF_STATUS:B0 0x6C(3-0)]) =0b1000 (TRX_OFF).

[Additional Function]

- By setting CCA_AUTO_EN ([CCA_CNTRL:B0 0x15(7)])=0b1, it is possible to execute CCA operation automatically for Ack packet transmission.

*Ack Reception
Condition: AUTO_RX_EN ([AUTO_ACK_SET:B0 0x55(6)])=0b1.

1) After competing transmission of data packet with Ack request, TX completion interrupt (INT[16]/[17] group3) will be generated, then transit to RX_ON state automatically for Ack packet to reception.

2) After RX completion for Ack packet, RX completion interrupt (INT[18]/[19]) will be generated.
Note: RF status keeps RX_ON state, If return to IDLE state, set SET_TRX ([RF_STATUS:B0 0x6C(3-0)]) =0b1000 (TRX_OFF).

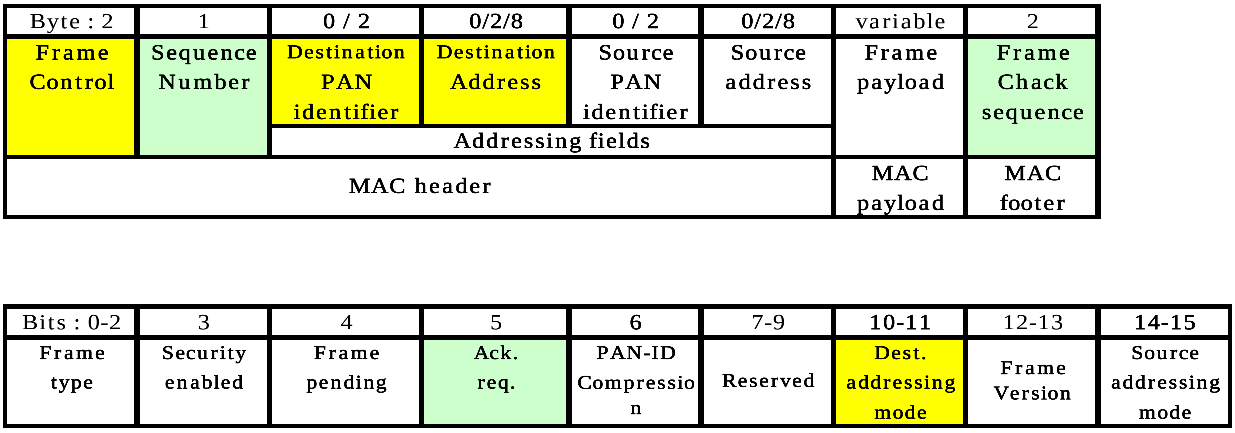
*Ack Reception (Terminate Ack packet waiting)
Condition: AUTO_RX_EN ([AUTO_ACK_SET:B0 0x55(6)])=0b1.

1) After competing transmission of data packet with Ack request, TX completion interrupt (INT[16]/[17] group3) will be generated, then transit to RX_ON state automatically for Ack packet to reception.

2) If MCU determined to terminate Ack packet waiting, set ACK_STOP ([AUTO_ACK_SET:B0 0x55(0)]) =0b1.
ML7396 family aborts Ack packet waiting and RF status will be back to TRX_OFF state automatically.

●Address filtering function:

ML7396 family has a function to receive RX packet which MAC header has specific code at yellow highlighted field in the MAC header (IEEE802.15.4) as below. By using [ADDFIL_CNTRL:B2 0x20] register, comparing field is selected from PANID, 64bit address, 16bit short address or I/G bit. Each specific code are defined by [PANID_L:B2 0x61] to [SHT_ADDR1_H:B2 0x6E] registers. Source address is out of comparing target.



<table>
<tr><td>Byte : 2</td><td>1</td><td>0 / 2</td><td>0/2/8</td><td>0 / 2</td><td>0/2/8</td><td>variable</td><td>2</td></tr>
<tr><td rowspan="2">Frame Control</td><td rowspan="2">Sequence Number</td><td>Destination PAN identifier</td><td>Destination Address</td><td>Source PAN identifier</td><td>Source address</td><td rowspan="2">Frame payload</td><td rowspan="2">Frame Chack sequence</td></tr>
<tr><td colspan="4">Addressing fields</td></tr>
<tr><td colspan="6">MAC header</td><td>MAC payload</td><td>MAC footer</td></tr>
</table>

Bits : 0-2	3	4	5	6	7-9	10-11	12-13	14-15
Frame type	Security enabled	Frame pending	Ack. req.	PAN-ID Compression	Reserved	Dest. addressing mode	Frame Version	Source addressing mode

Fig. MAC header and Frame Control Field

Destination Addressing Mode
- 00: Beacon or Ack Packet (Beacon packet is always received, Ack packet reception can be selectable)
- 01: Reserved (Does not receive)
- 10: 16 bits address
- 11: 64 bits address

Destination.PAN-ID
- 0xFFFF: Broadcasting, then always receive this packet regardless to address mode.
- 16 bits address mode: Receive packet if PAN_ID (setting vslue) is matched.
- 64 bits address mode: Ignoring this field.

Destination Address
- 16 bit address mode: Receive packet only if short address (setting value) is matched.
- 64 bit address mode: Receive packet only if 64 bits address is matched, or I/G bit is set to 0b1 (multicast).

References:

When Address Filtering function is enabled, packet analisis will be executed. Therefore when using RX_ACK CANCEL ([AUTO_ACK_SET:B0 0x55(7)]) function, Address Filtering function should be enabled, since packet anlisis is need uted to detect Ack packet. For details, please refer to [AUTO_ACK_SET:B0 0x55] register.

When address fields are mismatch with set value, following procedure is determined by the setting to ADDFIL_NG_SET ([PACKET_MODE_SET:B0 0x45(5)]) and packet discard completion interrupt (INT[03] group1) timing is defined by ADDFIL_IDLE_DET ([PACKET_MODE_SET:B0 0x45(0)]).

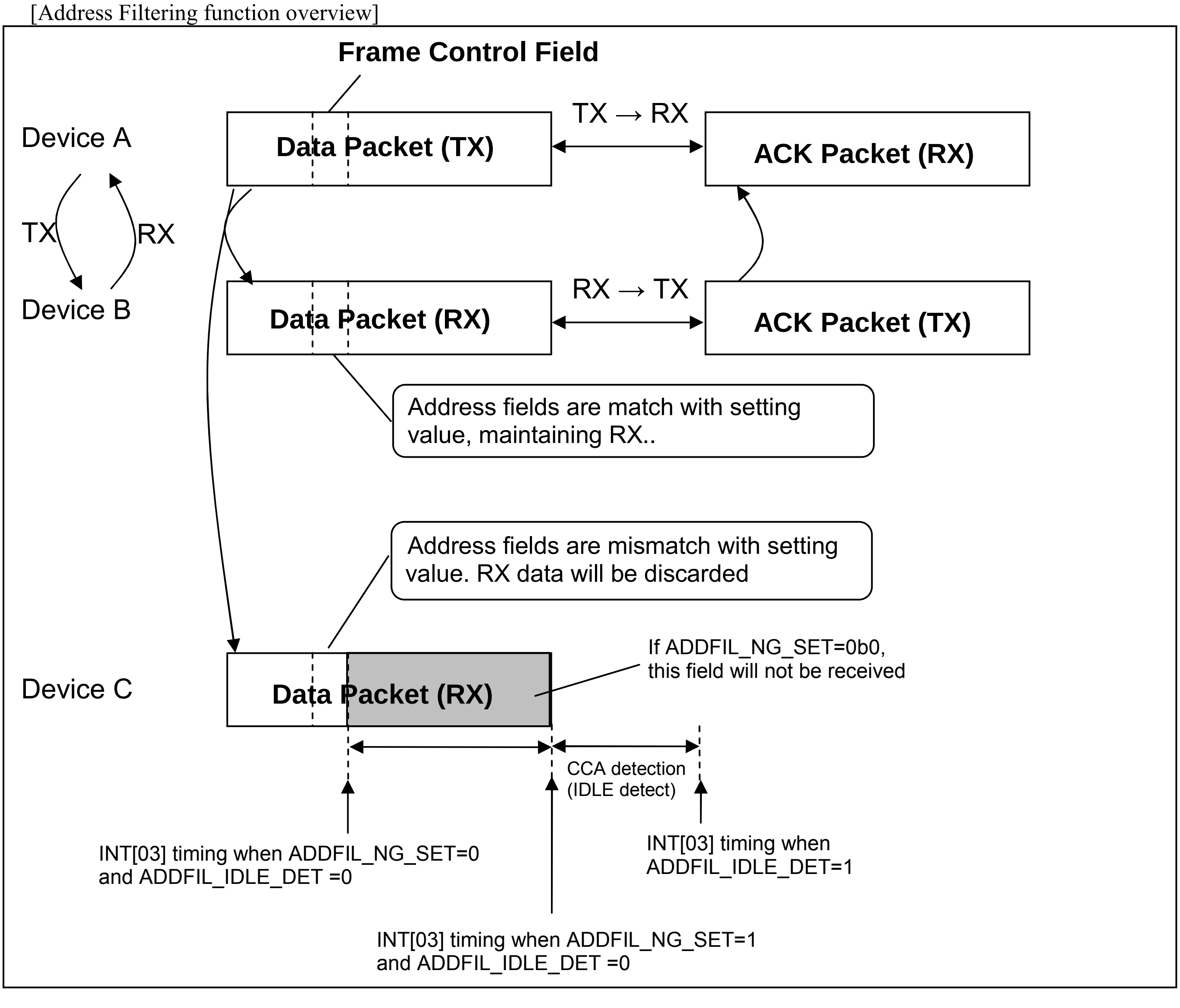
ADDFIL_NG_SET (bit5)
0b1: When address-mismatch is detected, discarding RX data after RX completetion.
0b0: When address-mismatch is detected, discarding RX data immediately.

ADDFIL_IDLE_DET (bit0)
0b1: After discarding RX data perform CCA and “IDLE” is detected, INT[03] will be generated.
0b0: After discarding RX data, INT[03] will be generated immediately.

When RX data is discarded, adding to INT[03] generation, discarded packet can be counted up to 1023 and result stored in [DISCARD_COUNT0:B2 0x6F] and [DISCARD_COUNT1:B2 0x70] registers.

[Note]
When using Address Filtering function while FEC function is enabled, if INT[03] is notified. PHY reset by [RST_SET:B0 0x01] should be required. If not issuing PHY reset, after that, ML7396 can not receive packet with address match also.

[Address Filtering function overview]

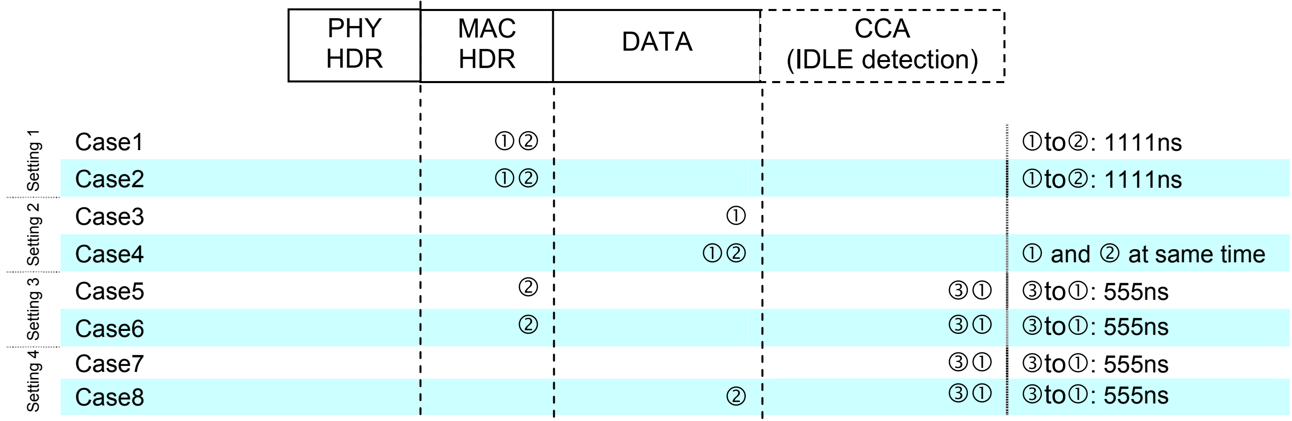

Frame Control Field
Device A
TX
RX
Device B
Device C
Data Packet (TX)
TX → RX
ACK Packet (RX)
Data Packet (RX)
RX → TX
ACK Packet (TX)
Address fields are match with setting value, maintaining RX..
Address fields are mismatch with setting value. RX data will be discarded
Data Packet (RX)
If ADDFIL_NG_SET=0b0, this field will not be received
CCA detection (IDLE detect)
INT[03] timing when ADDFIL_NG_SET=0 and ADDFIL_IDLE_DET =0
INT[03] timing when ADDFIL_IDLE_DET=1
INT[03] timing when ADDFIL_NG_SET=1 and ADDFIL_IDLE_DET =0

[Interrupts timing when using INT_TIM_CTRL]
By setting INT_TIM_CTRL ([PLL_MOD/DIO_SEL:B0 0x69(6)]), it is possible to select interrupt timing during Address filtering mode.

According to the ADDFIL_NG_SET or ADDFIL_IDLE_DET setting and CRC result in the RX packet, interrupt generation timings of ①Packet discard completion interrupt, ②CRC error interrupt, and ③CCA completion interrupt, will become as below figures.

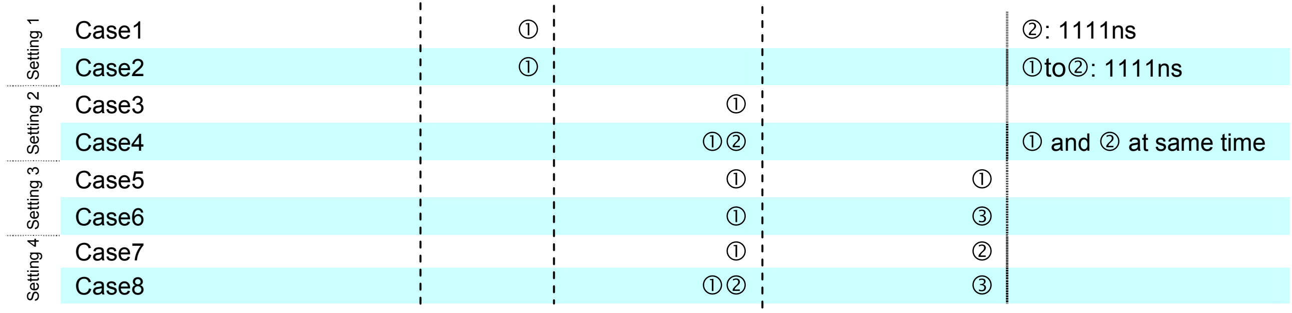
			Setting 1		Setting 2		Setting 3		Setting 4	
	Setting	setting register	Case1	Case2	Case3	Case4	Case5	Case6	Case7	Case8
Input	Discard packet after address mismatch	ADDFIL_NG_SET=0b0	O	O	-	-	O	O	-	-
	Discar packet after address mismatch and RX completion	ADDFIL_NG_SET=0b1	-	-	O	O	-	-	O	O
	Execute CCA after address mismatch	ADDFIL_IDLE_DET=0b 1	-	-	-	-	O	O	O	O
	CRC_OK	-	O	-	O	-	O	-	O	-
	CRC_NG	-	-	O	-	O	-	O	-	O
Interrupt result	Packet discard cpmpletion interrupt	INT[3] [INT_SOURCE_GRP1]	O	O	O	O	O	O	O	O
	CRC error interrupt	INT[21/20] [INT_SOURCE_GRP3]	O	O	-	O	O	O	-	O
	CCA completion interrupt	INT[8] [INT_SOURCE_GRP2]	-	-	-	-	O	O	O	O

(1) When INT_TIM_CTRL=0b0 (timing is comatible with ML7396)



		PHY HDR	MAC HDR	DATA	CCA (IDLE detection)	
Setting 1	Case1		①②			①to②: 1111ns
	Case2		①②			①to②: 1111ns
Setting 2	Case3			①		
	Case4			①②		① and ② at same time
Setting 3	Case5		②		③①	③to①: 555ns
	Case6		②		③①	③to①: 555ns
Setting 4	Case7				③①	③to①: 555ns
	Case8			②	③①	③to①: 555ns

(2) When INT_TIM_CTRL=0b1 (ML7396B timing)



		PHY HDR	MAC HDR	DATA	CCA (IDLE detection)	
Setting 1	Case1		①			②: 1111ns
	Case2		①			①to②: 1111ns
Setting 2	Case3			①		
	Case4			①②		① and ② at same time
Setting 3	Case5			①	①	
	Case6			①	③	
Setting 4	Case7			①	②	
	Case8			①②	③	

●Interrupt generation function

ML7396 family supports intterupt generation function. When interrupt occurs, SINTN pin (#10) will become “Low” to notify interrupt to the host MCU.

Interrupt elements are divided into 4groups, [INT_SOURCE_GRP1:B0 0x24] to [INT_SOURCE_GRP4:B0 0x27]. Each interrupt elements can be masked by using [INT_EN_GRP1:B0 0x2A] to [INT_EN_GRP4] registers.

Note: If one of unmask interrupt event occurs, SINTN maintains “Low”.

○Interrupt events table

Each interrupt events is described as belo table.

Group	Name	Function:
INT_SOURCE_GRP4	INT[25]	PLL unlock interrupt
	INT[24]	Auto_Ack ready interrupt
INT_SOURCE_GRP3	INT[23]	FIFO1 TX data request accept completion interrupt
	INT[22]	FIFO0 TX data request accept completion interrupt
	INT[21]	FIFO1 CRC error interrupt
	INT[20]	FIFO0 CRC error interrupt
	INT[19]	FIFO1 RX completion interrupt
	INT[18]	FIFO0 RX completion interrupt
	INT[17]	FIFO1 TX completion interrupt
	INT[16]	FIFO0 TX completion interrupt
INT_SOURCE_GRP2	INT[15]	TX FIFO access error interrupt
	INT[14]	RX FIFO access error interrupt
	INT[13]	TX Length error interrupt
	INT[12]	RX Length error interrupt
	INT[11]	SFD detection interrupt
	INT[10]	RF state transition completion interrupt
	INT[09]	Diversity search completion interrupt
	INT[08]	CCA completion interrupt
INT_SOURCE_GRP1	-	no function
	-	no function
	INT[05]	FIFO_Full interrupt
	INT[04]	FOFO_Empty interrupy
	INT[03]	Packet discard competion interrupt
	INT[02]	VCO calbration completion interrupt
	INT[01]	Reserved
	INT[00]	Clock stabilization completion interrupt

○Interrupt generation timing

In each interrupt generation, timing from reference point to interrupt interrupt generation (nitification) are described in the following table. Timeout procedure for interrupt notification waiting, are also described below.

[Note]
(1)The values are decribed in units of "symbol time" in the below table is the value at 100kbps. If using other data, please use 20, 5, and 2.5 for 50kbps, 200kbps, and 400kbps, respectively.

(2)Below table uses the following format of TX/RX data.

10 byte	2 byte	2 byte	24 byte	2 byte
Preamble	SFD	Length	User data	CRC

(3)Even if each interrupt notification is masked, in case of interrupt occurrence, interrupt elements are stored internnaly. Therefore, as soon as interrupt notification is unmasked, interrupt will generate.

Interrupt notification		Reference point	Time from reference point to interrupt generation or interrupt generation timing
INT[0]	CLK stabilization completion	RESETN release (upon power-on)	660μs
		SLEEP release (recovered from SLEEP)	660μs
INT[1]			
INT[2]	VCO calibration completion	VCO calibration start	230μs
INT[3]	Packet discard completion during Address Filtering function	SFD detection	(1)If ADDFIL_NG_SET([PACKET_MODE_SET:B0 0x45(5)]) =0b0, the right timing to address mismatch detection. (2)If ADDFIL_NG_SET([PACKET_MODE_SET:B0 0x45(5)]) =0b1, (When FEC is disabled) 28byte (Length to CRC) * 8bit * 10(symbol time) + process delay(5.55μs) =2245.55μs (When FEC is enabled) 28byte (Length to CRC) * 2 * 8bit *10(symbol time) + process delay(315.55μs) =4795.55μs
INT[4]	FIFO-Empty detection	(TX) TX_ON command (* 1)	Empty trigger level is set to 0x02 (When FEC is disabled) 37 byte (preamble to 23th data) * 8bit * 10 (symbol time) =2960μs (When FEC is enabled) {12byte (preamble to SFD) + 25byte(Length to 23th data) * 2} * 8bit* 10(symbol time) + RF wake-up & process delay (106μs) =5066μs
		(RX)	By FIFO read, remaining FIFO data is under trigger level
INT[5]	FIFO-Full detection	(TX)	By FIDO write, FIFO usage exceeds trigger level
		(RX) SFD detection	Full trigger level is set to 0x05 (When FEC is disabled) 8byte (Length + 6^{th} data) * 8bit * 10(symbol time) =640μs (Wwhen FEC is enabled) 8byte (Length + 6^{th} data) * 8bit * 2 * 10(symbol time) + process delay(305μs) =1585μs
(INT[6])	-		
(INT[7])	-		

(* 1) Befor issuing TX_ON, writing full-length TX data into a FIFO.

Interrupt notification		Reference point	Time from reference point to interrupt generation or interrupt generation timing
INT[8]	CCA completion	CCA execution start	(1)Normal mode {ED value calculation averaging time + IDLE_WAIT setting [IDLE_WAIT_L/H:B0 0x17/18] + 2 (filter stbilization)} * A/D conversion time (2) IDLE detection mode ○ IDLE detection case {ED value calculation averaging time + IDLE_WAIT setting [IDLE_WAIT_L/H:B0 0x17/18] + 2(filter stbilization)} * A/D conversion time ○ BUSY detection case (ED value calculation averaging tim+ 2(filter stbilization)) * A/D conversion Note: A/D conversion time can be changed by ADC_CLK_SET (ADC_CLK_SET:B0 0x08(4)). ADC conversion time= 17.7μs (1.8MHz), 16μs (2.0MHz) Note: When executing CCA during diversity, set the abort timer for CCA completion notification. When CCA is run during diversity, since there is a case CCA completion is not notified.
INT[9]	Diversity search completion	-	diversity search completion
INT[10]	RF state transition completion	TX_ON command	(IDLE) 122μs (RX) 89μs
		RX_ON command	(IDLE) 136μs (TX) 142μs
		TRX_OFF command	(TX) 410μs (RX) 11μs
		Force_TRX_OFF command	(TX) 410μs (RX) 10μs
INT[11]	SFD detection	-	SFD detection
INT[12]	RX length error	SFD detection	80μs
INT[13]	TX length error	-	Writing TX data to a FIFO
INT[14]	RX FIFO access error	-	(1).receiving 3rd packet with remaining RX dara in both FIFO0 and FIFO1 (2) overfolow occurs because FIFO read is too slow (3) underflow occurs because too many FIFO data is read
INT[15]	TX FIFO access error	-	(1) writing 3rd packet with remaining TX data in both FIFO0 and FIFO1 (2) FIFO overflow when writing (3) FIFO underflow (or no data) when transmitting
INT[16] INT[17]	FIFO0/FIFO1 TX completion	TX_ON command (* 1)	(When FEC is disabled) 40byte (preamble to CRC) * 8bit * 10(symbol time) + RF wake-up & process delay(154μs) =3354μs (When FEC is enabled) {12byte (preamble to SFD) + 28byte (Length to CRC) * 2} * 8bit * 10(symbol time) + RF wake-up & process delay(224μs) =5664μs

(* 1) Befor issuing TX_ON, writing full-length TX data into a FIFO.

Interrupt notification		Reference point	Time from reference point to interrupt generation or interrupt generation timing
INT[18] INT[19]	FIFO0/FIFO1 RX completion	SFD detection	(When FEC is disabled) 28byte (Length to CRC) * 8bit * 10(symbol time + process delay(5μs) =2245μs (When FEC is enabled) 28byte (Length to CRC) * 2 * 8bit * 10(symbol time) + process delay(315μs) =4795μs
INT[20] INT[21]	FIFO0/FIFO1CRC error detection	SFD detection	(With FEC disabled) 28byte (Length to CRC) *8bit * 10(symbol time) + process delay(5μs) =2245μs (With FEC enabled) 28byte (Length to CRC) * 2 * 8bit * 10(symbol time + process delay(315μs) =4795μs
INT[22] INT[23]	FIFO0/FIFO1 TX data request accept completion	-	After full-length data are written into a FIFO
INT[24]	AutoAck ready	RX completion	92us
INT[25]	PLL unlock detection	-	(TX) during TX after PA enable (RX) during RX after RX enable

○Clearing interrupt condition

The following table shows the condition of clearing each interrupt.

Interrupt notification		Requirements for clearing interrupt
INT[0]	CLK stabilization completion	After the interrupt generation
INT[1]	Reserved	
INT[2]	VCO calibration completion	After the interrupt generation
INT[3]	Packet discard completion during Address Filtering function	After the interrupt generation
INT[4]	FIFO-Empty detection	After the interrupt generation (must clear before the next FIFO-Empty trigger timing)
INT[5]	FIFO-Full detection	After the interrupt generation (must clear before the next FIFO-Full trigger timing)
INT[6]	-	
INT[7]	-	
INT[8]	CCA completion	After the interrupt generation (must clear before the next CCA execution) * clearing interrupt erases CCA result as well
INT[9]	Diversity search completion	After RX completion interrupt(INT[18/19]), must cleare with RX completion interrupt * during RECEIVE stare, clearing is prohibited.
INT[10]	RF state transition completion	After the interrupt generation
INT[11]	SFD detection	After the interrupt generation
INT[12]	RX length error	After the interrupt generation
INT[13]	TX length error	After the interrupt generation
INT[14]	RX FIFO access error	After the interrupt generation
INT[15]	TX FIFO access error	After the interrupt generation (must clear before the next packet transmission)
INT[16/17]	FIFO0/FIFO1 TX completion	After the interrupt generation (must clear before the next packet transmission)
INT[18/19]	FIFO0/FIFO1 RX completion	After the interrupt generation (must clear before the next packet reception)
INT[20/21]	FIFO0/FIFO1CRC error detection	After the interrupt generation * clearing interrupt erases CRC result (CRC_RSLT1/0).
INT[22/23]	FIFO0/FIFO1 TX data request accept completed	After TX completion interrupt (INT[16/17]) (must clear before the next packet transmission) * during TRANSMIT state, clearing is prohibited.
INT[24]	AutoAck ready	After the interrupt generation
INT[25]	PLL unlock detection	After the interrupt generation (must clear before the next packet transmission or reception)

●Temperature Measurement Function

ML7396 family has temeperature measurement function. This temperature information can be from A_MON pin (#24) as analog output or digital information using [TEMP_MON:B0 0x79] register. Analog or digital can be switched by [RSSI/TEMP_OUT:B1 0x03] register.

Notes:
1) Please do not set TEMP_OUT ([RSSI/TEMP_OUT:B1 0x03(4)]) and TEMP_ADC_OUT ([RSSI/TEMP_OUT:B1 0x03(5)]) at the same time. Correct value reading may not be guaranteed.
2) When TEMP_ADC_OUT is set, packet data is not able to receive normally.

[Analog output]
ML7396 family has current source circuits and its current flow through 75kΩ to A_MON pin (#24). From voltage information, temperature information can be obtained.

Current from currwnt source circuits are 10μA at 25˚C. Following formula can be used to calculate temperature from the current.

Itemp = (273+ Temp) / (273+25) * 10 (μA)

Therefore, if 75kΩ resister is connected, temprature can be calculated usng following formula.

Vamon = (273+ Temp) / (275+25) * 10E-6 * 75000

If temprature is -40˚C to +85˚C, Vamon will be 0.59V to 0.9V.
Therefore temperature can be calculated from voltage using following formula.

Temp = Vamon * 397.3 - 273

[Digital output]
Digital temperature information is using 6bits ADC to convert from the above analog information. Internally, 4samples information are added and indicates as 8bits information in [TEMP_MON:B0 0x79] register. Ignorimg low 2 bits, upper 6bits are used for average temperature information.
Temperature information is updated every 17.8μs. (if 2MHz is selected in [ADC_CLK_SET:B0 0x08] register, it is updated every 16 μs)

●Ramp control function

ML7396 has Ramp control function. This function will contribute reducing spurious emission when transmission is terminated. Ramp control will be executed when switching TX_ON to TRX_OFF state and TX_ON to RX_ON state.

The following are control bits retative with ramp control function.

TXOFF_RAMP_EN ([RAMP_CNTRL:B2 0x2C(4)]): Ramp control enable bit

TIM_TX_OFF1[7:0] ([TX_OFF_ADD1:B1 0x55(7-0)]): Ramp down timing adjustment when transitioning from TX_ON to TRX_OFF.

TIM_RX_ON2[2:0] ([RX_ON_ADJ2:B1 0x3F(6-4)]): RX_ON timing adjustment when transitioning from TX_ON to RX_ON

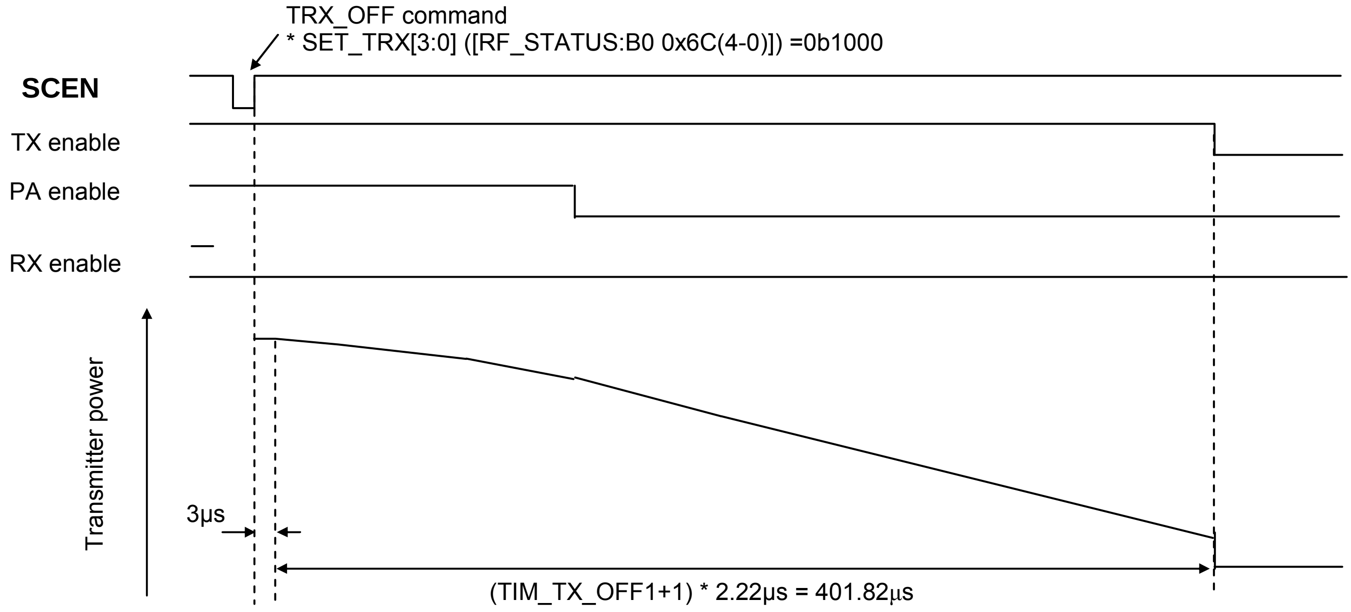
TIM_TX_OFF2[5:0] [2DIV_GAIN_CONTRL:B0 0x6E(7-2)]): Ramp down timing adjustment when transitioning from TX_ON to RX_ON.

[Operation Overview]

(1) Ramp down timing when transitioning from TX_ON to TRX_OFF

[Condition]

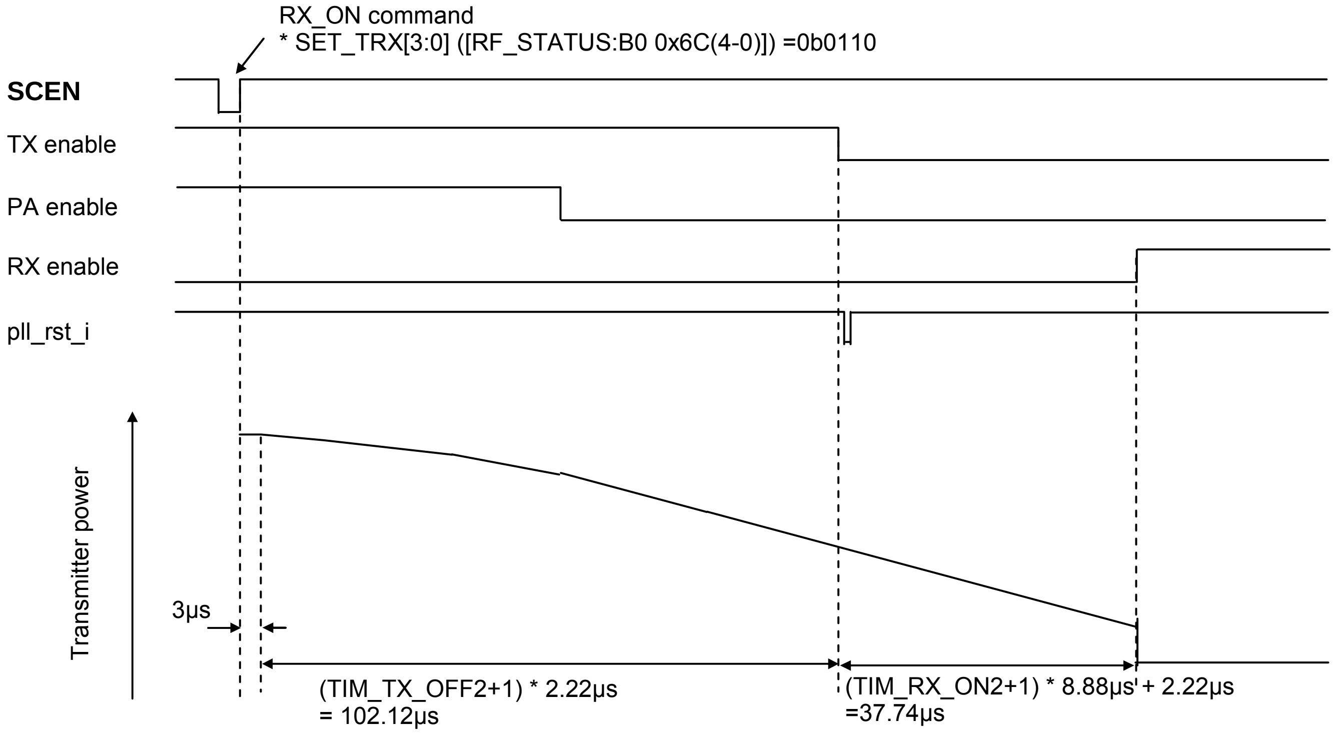
TXOFF_RAMP_EN ([RAMP_CNTRL:B2 0x2C(4)]) =0b1
TIM_TX_OFF1[7:0] ([TX_OFF_ADD1:B1 0x55(7-0)] =0xb4(400 µs), 0x42 (150µs)
TIM_RX_ON2[2:0] ([RX_ON_ADJ2:B1 0x3F(6-4)]) =0b011
TIM_TX_OFF2[5:0] ([2DIV_GAIN_CONTRL:B0 0x6E(7-2)]) =0b1011_01


TRX_OFF command
* SET_TRX[3:0] ([RF_STATUS:B0 0x6C(4-0)]) =0b1000
SCEN
TX enable
PA enable
RX enable
Transmitter power
3µs
(TIM_TX_OFF1+1) * 2.22µs = 401.82µs

(2) Ramp down timing when transitioning from TX_ON to RX_ON

[Condition]

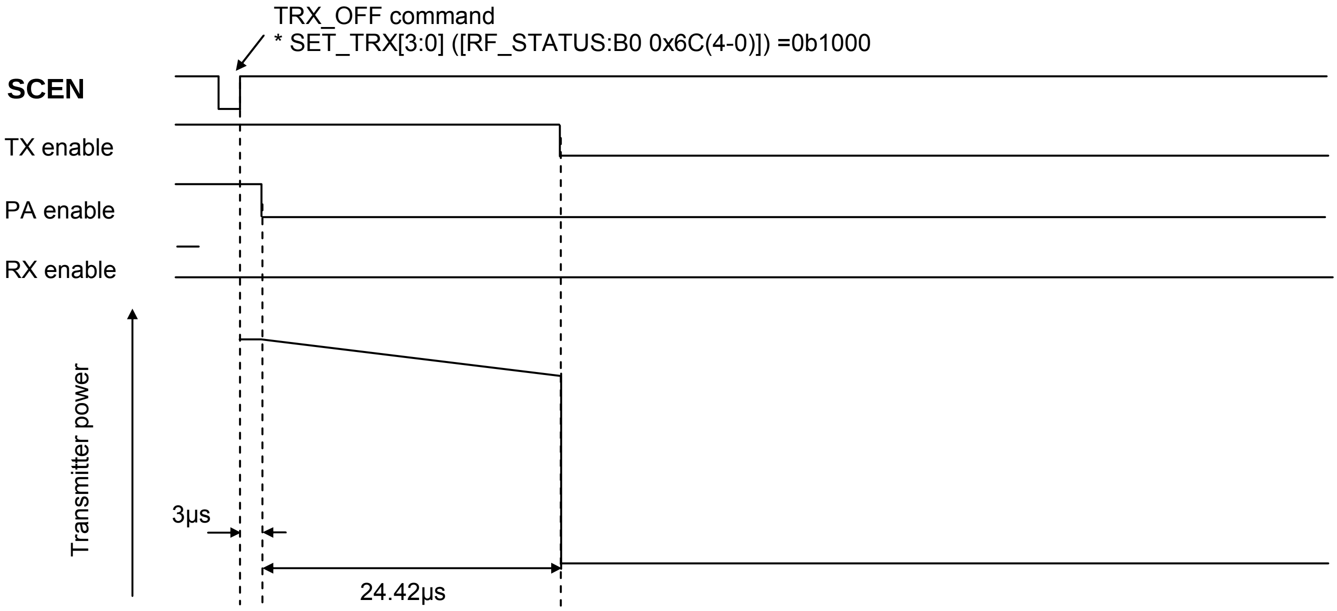
TXOFF_RAMP_EN ([RAMP_CNTRL:B2 0x2C(4)]) = 0b1
TIM_TX_OFF1[7:0] ([TX_OFF_ADD1:B1 0x55(7-0)]) =0xb4 (400 µs)
TIM_RX_ON2[2:0] ([RX_ON_ADJ2:B1 0x3F(6-5)]) =0b011
TIM_TX_OFF2 ([2DIV_GAIN_CONTRL:B0 0x6E(7-2)]) =0b1011_01


RX_ON command
* SET_TRX[3:0] ([RF_STATUS:B0 0x6C(4-0)]) =0b0110
SCEN
TX enable
PA enable
RX enable
pll_rst_i
Transmitter power
3µs
(TIM_TX_OFF2+1) * 2.22µs
= 102.12µs
(TIM_RX_ON2+1) * 8.88µs + 2.22µs
=37.74µs

(3) Ramp down timing when transitioning from TX_ON to TRX_OFF (ramp control disabled)

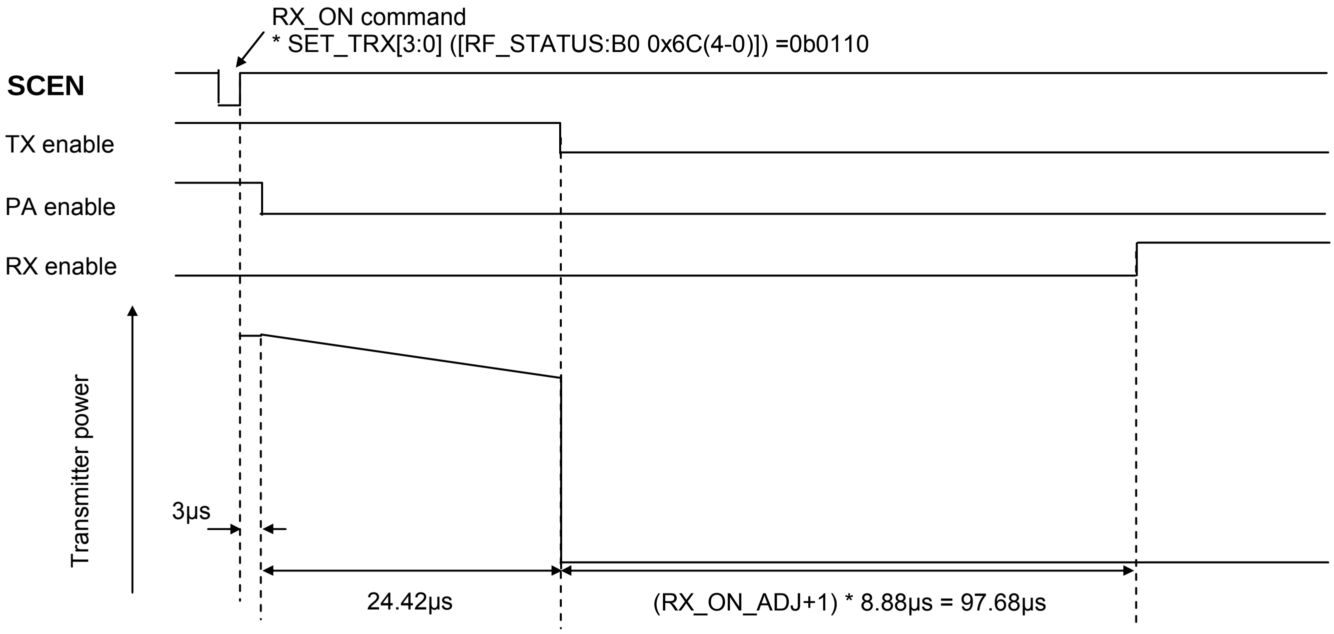
[Condition]

TXOFF_RAMP_EN ([RAMP_CNTRL:B2 0x2C(4)]) =0b0
TIM_TX_OFF1[7:0] ([TX_OFF_ADD1:B1 0x55(7-0)]) =0xb4 (400 µs)
TIM_RX_ON2[2:0] ([RX_ON_ADJ2:B1 0x3F(6-4)]) =0b011
TIM_TX_OFF2 ([2DIV_GAIN_CONTRL:B0 0x6E(7-2)]) =0b1011_01


TRX_OFF command
* SET_TRX[3:0] ([RF_STATUS:B0 0x6C(4-0)]) =0b1000
SCEN
TX enable
PA enable
RX enable
Transmitter power
3µs
24.42µs

(4) Ramp down timing when transitioning from TX_ON to RX_ON (ramp control disabled)

[Condition]
TXOFF_RAMP_EN ([RAMP_CNTRL:B2 0x2C(4)]) =0b0
TIM_TX_OFF1[7:0] ([TX_OFF_ADD1:B1 0x55(7-0)]) =0xb4 (400 µs)
TIM_RX_ON2[2:0] ([RX_ON_ADJ2:B1 0x3F(6-4)]) =0b011
TIM_TX_OFF2[5:0] ([2DIV_GAIN_CONTRL:B0 0x6E(7-2)]) =0b1011_01
RX_ON_ADJ[7:0] ([RX_ON_ADJ:B2 0x22(7-0)]) =0x0A


RX_ON command
* SET_TRX[3:0] ([RF_STATUS:B0 0x6C(4-0)]) =0b0110
SCEN
TX enable
PA enable
RX enable
Transmitter power
3µs
24.42µs
(RX_ON_ADJ+1) * 8.88µs = 97.68µs

■RF Configuration

●Programming Channel Frequency

Maximum 16 channels can be selected. (CH#0 to CH#15) Cahnnel allocation is defined by channel #0 frequency specified by [CH0_FL:B0 0x48], [CH0_FM:B0 0x49], [CH0_FH:B0 0x4A] and [CH0_NA:B0 0x4B] registers, and channel spacing specified by [CH_SPACE_L:B0 0x4C] and [CH_SPACE_H:B0 0x4D] registers.
16 channels can be enabled or disabled by [CH_EN_L:B0 0x2E] and [CH_EN_H:B0 0x2F] registers.
RF channel is set as channel number (#0 to #15) at [CH_SET:B0 0x6B] register

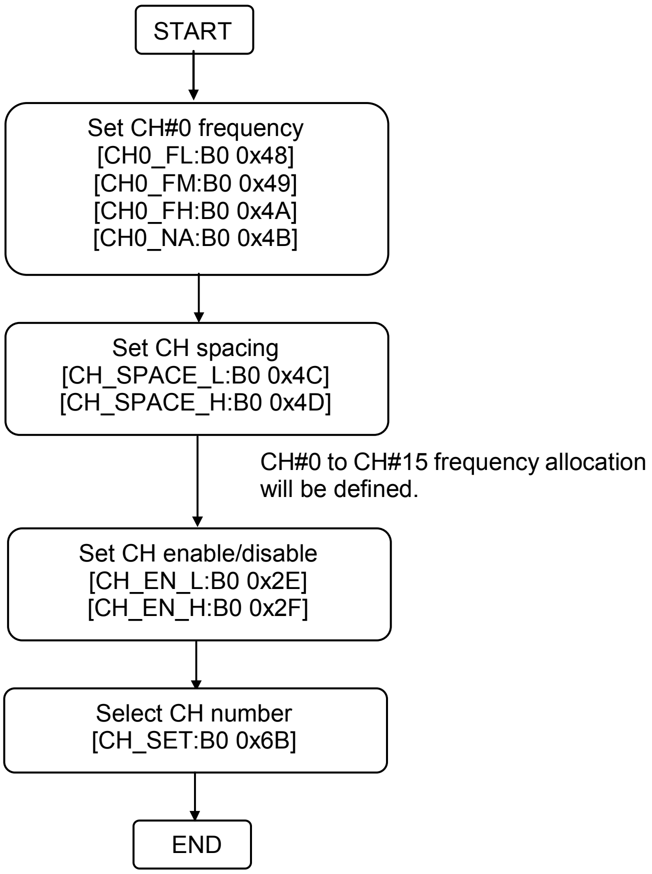
Notes:

1) Frequency range (from CH#0 to CH#15) can not include integer multiple of 36MHz. (ex: 900MHz, 936MHz)
2) The channel frequency must meet the following condition. If the following condition can not meet, please change the channel #0 frequency or disabling channels that can not meet the condition by [CH_EN_L:B0 0x2E] and [CH_EN_H:B0 0x2F] register.

$$36\text{MHz} * n + 2.2\text{MHz} \le \text{channel frequency} < 36\text{MHz} * (n+1) - 500\text{kHz} \quad * \ n=\text{integer}$$

3) If the above condition can not be met, expected channel frequency is not functional or PLL may not be locked.

[Channel frequency programming flow]


START
Set CH#0 frequency
[CH0_FL:B0 0x48]
[CH0_FM:B0 0x49]
[CH0_FH:B0 0x4A]
[CH0_NA:B0 0x4B]
Set CH spacing
[CH_SPACE_L:B0 0x4C]
[CH_SPACE_H:B0 0x4D]
CH#0 to CH#15 frequency allocation will be defined.
Set CH enable/disable
[CH_EN_L:B0 0x2E]
[CH_EN_H:B0 0x2F]
Select CH number
[CH_SET:B0 0x6B]
END

○Programming Channel#0 Frequency

Channel #0 frequency can be set by [CH0_FL:B0 0x48], [CH0_FM:B0 0x49], [CH_FH:B0 0x4A] and [CH_NA:B0 0x4B] registers.

Each setting parameters for channel #0 can be calculated using the following formula.

$N = f / f_{REF} / P$ (Integer part)
$A = f / f_{REF} - N * P$ (Integer part)
$F = \{f / f_{REF} - (N * P + A)\} * 2^{20}$ (Integer part) [note: useing 20bit circuit]

Here

f	: Channel #0 fequency
f_{REF}	: PLL reference frequency (input clock=36MHz)
P	: Dual modulus parameter (fixed to 4)
N	: N-counter parameter
A	: A-counter parameter
F	: F-counter parameter

And frequency error can be calculated using the following formula.

$ferr = f - [f_{REF} * \{(N * P + A) + F/2^{20}\}]$

[Example] When set channel #0 frequecy to 923.1MHz, the calculations are as follows. (f_{REF} = 36MHz)

N = 923.1MHz / 36MHz / 4 (Integer part) = 6
A = 923.1MHz / 36MMHz- 6 * 4 (Integer part) = 1
F = {923. 1MHz / 36MHz - (6 *4 + 1)} *2^{20} (Integer part) = 672836 (0xA4444)

Therefore
[CH0_FL:B0 0x48] = 0x44
[CH0_FM:B0 0x49] = 0x44
[CH0_FH:B0 0x4A] = 0x0A
[CH0_NA:B0 0x4B] = 0x61

Feuqency error will be ferr = 923. 1MHz - [36MHz * {(6 * 4 + 1) + 672836 / 2^{20}}] = +31.7Hz

○Programming Channel pace

Channel space can be set by [CH_SPACE_L:B0 0x4C] and [CH_SPACE_H:B0 0x4D] registers.
Channel space is frequency space between centre frequency of given channel and that of adjacent channel.

Channel space setting value can be calculated using the following formula.

$CH\_SP\_F = \{f_{SP} / f_{REF}\} * 2^{20}$ (Integr part) [note: using 20bit circuit]

Here

CH_SP_F	: Channel space setting
f_{SP}	: Channel space [MHz]
f_{REF}	: PLL reference frequency (input clock=36MHz)

[Example] When set channel space is 400kHz, the calculation are as follow. (f_{REF} = 36MHz)

CH_SP_F = {0.4MHz / 36MHz} * 2^{20} (Integer part) = 11650 (0x2D82)

Therefore
[CH_SPACE_L:B0 0x4C] = 0x82
[CH_SPACE_H:B0 0x4D] = 0x2D

●Programming IF Frequency

In order to support various data rate , RX filters have to be optimised. The RX filter can be selected according to the IF frequency. IF frequency can be set by using [IF_FREQ_H: B1 0x0A] and [IF_FREQ_L: B1 0x0B] registers. (default: 178.22kHz) According to the RATE[2:0] ([DATA_SET:B0 0x47(2-0)]) setting and NBO_SEL([DATA_SET:B0 0x47(7)]) setting, IF frequency will be multiplied automatically as following table.

NBO_SEL	Data rate				
	50kbps	100kbps	150kbps	200kbps	400kbps
0b0	x2	x4	x4	x6	x6
0b1	x2	x2	-	x4	-

IF frequency value should be set as the multiplied IF frequency corresponding to each data rate becomes the values described in the following table.

NBO_SEL	Data rate				
	50kbps	100kbps	150kbps	200kbps	400kbps
0b0	500kHz	720kHz	900kHz	1300kHz	2100kHz
0b1	500kHz	720kHz	-	1300kHz	-

[Notes]

1. NBO_SEL=0b1 can not be set for the data rate other than 50kbps, 100kbps and 200kbps.
2. For 10kbps, 20kbps, 40kbps setting, please refer to the "Initial register setting" file .

If AFC is used, IF frequency setting in [IF _FREQ_AFC_H: B0 0x30] and [IF_FREQ_AFC_L: B0 0x31] registers will be used. IF frequency setting for AFC operation is same as normal operation.

If CCA is used to detect channel carrier power, required RX filter bandwidth may be different. [IF _FREQ_CCA_H: B1 0x0C] and [IF_FREQ_CCA_L: B1 0x57] registers must be used for CCA purpose. During CCA operation IF frequency calculation becomes as below.

NBO_SEL	Data rate				
	50kbps	100kbps	150kbps	200kbps	400kbps
0b0	x2	x6	x8	x8	x8
0b1	x2	x2	-	x6	-

IF frequency value for CCA operation should be set as the multiplied IF frequency corresponding to each data rate becomes the values described in the following table.

NBO_SEL	Data rate				
	50kbps	100kbps	150kbps	200kbps	400kbps
0b0	500kHz	1500kHz	1450kHz	2000kHz	2100kHz
0b1	500kHz	720kHz	-	1500kHz	-

[Notes]

1. NBO_SEL=0b1 can not be set for the data rate other than 50kbps, 100kbps and 200kbps.
2. For 10kbps, 20kbps, 40kbps setting, please refer to the "Initial register setting" file..

IF frequency setting value can be calculated using the following formula.

$$IF\_FREQ = \{f_{IF} / f_{REF}\} * 2^{20} \text{ (Integr part) [note: using 20bit circuit]}$$

Here

IF_FREQ : IF frequency setting
f_{IF} : IF frequency [MHz]
f_{REF} : PLL reference frequency (input clock=36MHz)

[Example] When set IF frequency is 178.22kHz, the calculation are as follow. (f_{REF} = 36MHz)

IF_FREQ = {0.17822MHz / 36MHz} * 2^{20} (Integer part) = 5191 (0x1447)

Therefore

[IF_FREQ_H] = 0x14
[IF_FREQ_L] = 0x47

●Programming BPF band width

For normal operation (including AFC) and CCA operation, optimized BPF setting are necessary. To compensating LSI variations, [BPF_ADJ_OFFSET:B1 0x1E] register indicates individual cpmpensation value.

According to the below table, multiplying BPF_OFFSET[6:0] ([BPF_ADJ_OFFSET:B1 0x1E(6-0)]) by the coefficient value corresponding to each data rate. If BPF_OFFSET_POL ([BPF_ADJ_OFFSET:B1 0x1E(7)] = 0b1, incraseing, otherwise (=0b0) decrasing to the default value corresponding each data rate.

Compensated value is set into [BPF_ADJ_H/L:B1 0x0E/0F] and [BPF_AFC_ADJ_H/L:B0 0x32/33] registers for normal operation. For CCA operation, set to [BF_CCA_ADJ_H/L:B1 0x10/11] register.

Following tables show coefficient value and default value corresponfding to RATE[2:0] ([DATA_SET:B0 0x47(2-0)]) setting and NBO_SEL([DATA_SET:B0 0x47(7)]) setting

[When NBO_SEL=0b1]

Data rate [kbps]	RATE[2:0] [B0 0x47]	Normal operation		CCA Operation	
		Coefficient value	Default value	Coefficient value	Default value
50	0b000	1.44	0x034B	1.44	0x034B
100	0b01	1	0x024A	0.48	0x0119
150	0b010	0.8	0x01D4	0.497	0x0122
200	0b010	0.554	0x0144	0.36	0x00D2
400	0b011	0.343	0x00C8	0.343	0x00C8

[When NBO_SEL=0b0]

Data rate [kbps]	RATE[2:0] [B0 0x47]	Normal operation		CCA Operation	
		Coefficient value	Default value	Coefficient value	Default value
50	0b000	1.44	0x034B	1.44	0x034B
100	0b01	1	0x024A	1	0x024A
150	0b010	-	-	-	-
200	0b010	0.554	0x0144	0.48	0x0119
400	0b011	-	-	-	-

[Example]

Condition: Data rate is 100kbps, and [BPF_ADJ_OFFSET:B1 0x1E] =0x91

[BPF_ADJ_H/L:B1 0x0E/0F] = 0x24A + 1 * (0x11) = 0x025B
[BPF_AFC_ADJ_H/L:B0 0x32/33] = 0x24A + 1 * (0x11) = 0x025B
[BF_CCA_ADJ_H/L:B1 0x10/11] = 0x119 + 0.48 * (0x11) = 0x0121

Note: For 10kbps, 20kbps, 40kbps setting, please refer to the "Initial register setting" file.

●Programming GFSK modulation

By setting GFSK_EN ([DATA_SET;B0 0x47(4)]) =0b1, GFSK modulation can be selected.

○Programming GFSK frequency deviation

In GFSK modulation, frequency deviation can be set by [F_DEV_L:B0 0x4E] and [F_DEV_H:B0 0x4F] registers. Frequency deviation setting value can be calculated using the following formula.

$F\_DEV = \{f_{DEV} / f_{REF}\} * 2^{20}$ (Integer part) [note: using 20bit circuit]

Here

F_DEV : Frequency deviation setting
f_{DEV} : Frequency deviation [MHz]
f_{REF} : PLL reference frequency (input clock=36MHz)

[Example] When set frequency deviation is 50 kHz at 100kbps, the calculation are as follow. (f_{REF} = 36MHz)

$F\_DEV = \{0.05MHz / 36MHz\} * 2^{20}$ (Integer part) = 1456 (0x05B0)

Therefore

[F_DEV_L:B0 0x4E] = 0xB0
[CH_SPACE_H:B0 0x4D] = 0x05

Following table shows frequency deviation value with modulation index (m) =1 for each data rate.

Register	Data rate			
	50kbps	100kbps	150kbps	200kbps
[F_DEV_L:B0 0x4E]	0xD8	0xB0	0x44	0x60
[F_DEV_H:B0 0x4F]	0x02	0x05	0x04	0x0B

Note: For 10kbps, 20kbps, 40kbps setting, please refer to the "Initial register setting" file.

○Programming Gaussian Filter

Gaussian filter can be set by [GFIL00/FSK_FDV1:B0 0x59] to [GFIL11:B0 0x64] registers. BT value of Gaussian filter and setting value to related registers are shown in the below tables. All setting values are described as hexadecimal value.

Remarks: Setting values for BT=0.5 at 100kbps are set as initial values in registers related to Gaussian filter, since initial values of [DATA_SET:B0 0x47] register is GFSK enable and 100kbps setting.

Gaussian filter register setting (for 10kbps/20kbps/40kbps/50kbps/100kbps/150kbps/200kbps)

(HEX)

Register	Address:	bit	BT=1.0	BT=0.5	BT=0.4	BT=0.3	BT=0.25
GFIL00	0x59	[1:0]	0	0	0	0	1
		[3:2]	0	0	0	0	1
		[5:4]	0	0	0	1	1
		[7:6]	0	0	0	1	2
GFIL01	0x5a	[3:0]	0	0	0	1	3
		[7:4]	0	0	1	2	4
GFIL02	0x5b	[3:0]	0	0	1	3	5
		[7:4]	0	1	2	5	6
GFIL03	0x5c	[7:0]	00	01	03	06	07
GFIL04	0x5d	[7:0]	00	03	05	08	09
GFIL05	0x5e	[7:0]	00	05	08	0A	0A
GFIL06	0x5f	[7:0]	00	09	0C	0C	0C
GFIL07	0x60	[7:0]	03	0F	0F	0E	0D
GFIL08	0x61	[7:0]	0B	15	13	10	0E
GFIL09	0x62	[7:0]	1D	1A	17	13	0F
GFIL10	0x63	[7:0]	35	1F	1A	14	10
GFIL11	0x64	[7:0]	40	20	1A	14	12

Gaussian filter register setting (for Optional 400kbps)

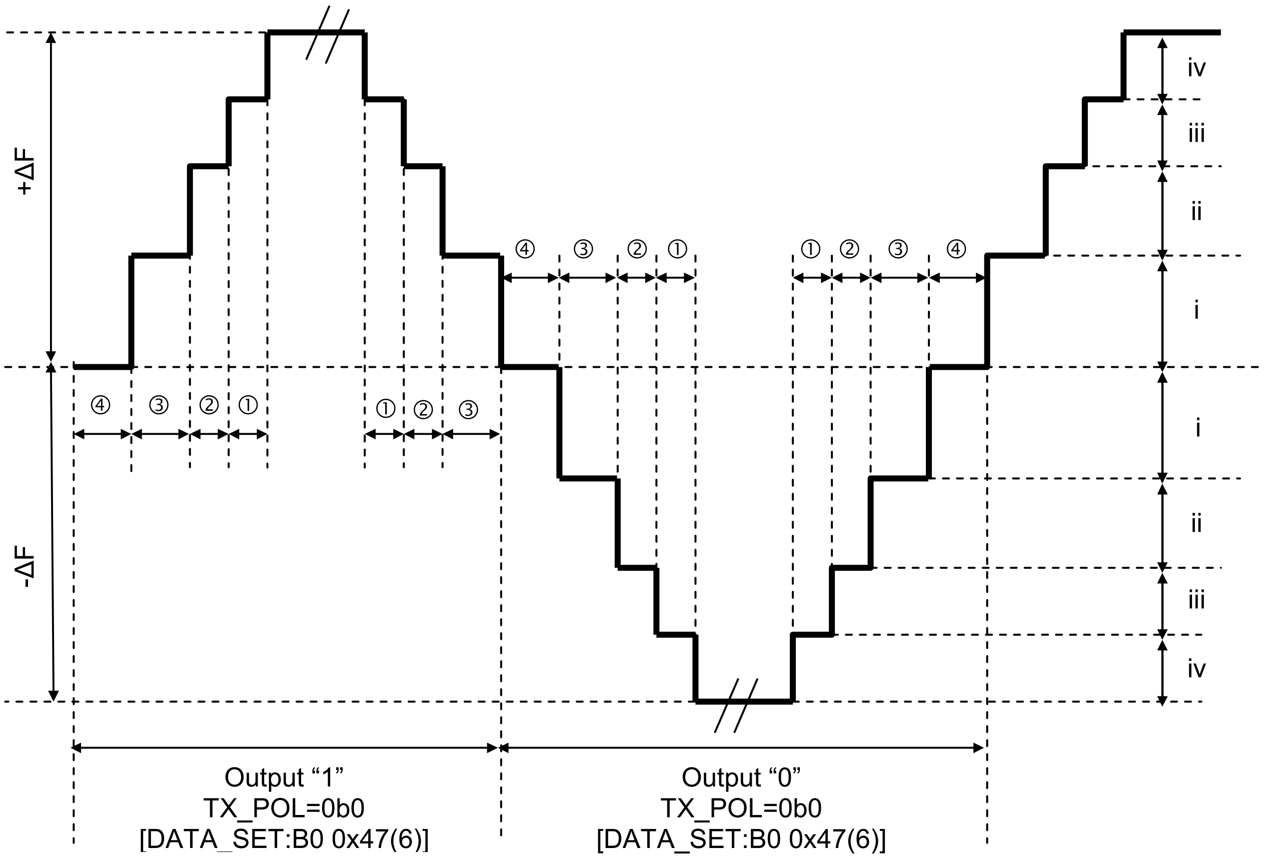
(HEX)

Register	Address:	bit	BT=1.0	BT=0.5	BT=0.4	BT=0.3	BT=0.25
GFIL00	0x59	[1:0]	0	0	0	0	0
		[3:2]	0	0	0	0	0
		[5:4]	0	0	0	0	0
		[7:6]	0	0	0	0	0
GFIL01	0x5A	[3:0]	0	0	0	0	0
		[7:4]	0	0	0	0	0
GFIL02	0x5B	[3:0]	0	0	0	0	0
		[7:4]	0	0	0	0	1
GFIL03	0x5C	[7:0]	00	00	00	00	01
GFIL04	0x5D	[7:0]	00	00	00	01	03
GFIL05	0x5E	[7:0]	00	00	01	03	05
GFIL06	0x5F	[7:0]	00	00	02	07	09
GFIL07	0x60	[7:0]	00	03	07	0C	0F
GFIL08	0x61	[7:0]	00	0B	10	14	15
GFIL09	0x62	[7:0]	05	1D	1F	1D	1A
GFIL10	0x63	[7:0]	3C	35	2D	24	1F
GFIL11	0x64	[7:0]	7E	40	34	28	20

●Programming FSK modulation

By setting GFSK_EN ([DATA_SET;B0 0x47(4)]) =0b0, FSK modulation can be selected.

In FSK modulation, fine frequency deviation can be set by [GFIL00/FSK_FDEV1:B0 0x59] to [GFIL03/FSK_FDEV4:B0 0x5C] registers. By setting [FSK_TIME1:B0 0x65] to [FSK_TIME4:B0 0x68] registers, FSK timing can be fine tuned.


+ΔF
-ΔF
④
③
②
①
iv
iii
ii
i
Output "1"
TX_POL=0b0
[DATA_SET:B0 0x47(6)]
Output "0"
TX_POL=0b0
[DATA_SET:B0 0x47(6)]

Symbol	Register	Address	Function	Symbol	Register	Address	Function
i	FSK_FDEV1	0x59	Freq dev 33.4x2(Hz)	①	FSK_TIME1	0x65	Modulation timing by 4MHz counter
ii	FSK_FDEV2	0x5a		②	FSK_TIME2	0x66	
iii	FSK_FDEV3	0x5b		③	FSK_TIME3	0x67	
iv	FSK_FDEV4	0x5c		④	FSK_TIME4	0x68	

[Note]

1. FSK modulation does not support optional 400kbps.

●Programming Data rate changing

50kbps, 100kbps, 200kbps and 400kbps data rate can be chnaged by RATE[2:0] ([DATA_SET:B0 0x47(2-0)]). When changing data rate, below registers may have to be changed.

Note:

1. Depending on data rate, the following chage may not be necessary. For details, please refer to each register setting value corresponding to each data rate in "Initial register setting" file.
2. Please change data rate setting in TRX_OFF state.

[Bank0]

[RATE_SET1:B0 0x04] register (Note: setting is necessary only when changing to 150kbps.)
[RATE_SET2:B0 0x05] register (Note: setting is necessary only when changing to 150kbps.)

[IF_FREQ_AFC_H:B0 0x30] register
[IF_FREQ_AFC_L:B0 0x31] register
[BPF_AFC_ADJ_H:B0 0x32] register
[BPF_AFC_ADJ_L:B0 0x33] register
[TX_PR_LEN:B0 0x42] register
[CH_SPACE_FL:B0 0x4C] register
[CH_SPACE_FH:B0 0x4D] register
[F_DEV_L:B0 0x4E] register
[F_DEV_H:B0 0x4F] register
[2DIV_SEARCH:B0 0x6F] register

[Bank1]

[PLL_CFP_ADJ:B1 0x09] register
[IF_FREQ_H:B1 0x0A] register
[IF_FREQ_L:B1 0x0B] register
[IF_FREQ_CCA_H:B1 0x0C] register
[IF_FREQ_CCA_L:B1 0x0D] register
[BPF_ADJ_H:B1 0x0E] register
[BPF_ADJ_L:B1 0x0F] register
[BPF_CCA_ADJ_H:B1 0x10] register
[BPF_CCA_ADJ_L:B1 0x11] register

[Bank2 registers]

[RATE_ADJ1:B2 0x2A] register (Note: setting is necessary only when changing to 150kbps.)
[RATE_ADJ2:B2 0x2B] register (Note: setting is necessary only when changing to 150kbps.)

●Programming narrow band option setting

By setting NBO_SEL ([DATA_SET:B0 0x47(7)]) = 0b1, narrow bandwidth mode can be selected. The narrow band mode is applying 200 kHz channel spacing instead of 400 kHz defined in IEEE802.15.4g standard. When selecting the narrow bandwidth mode, below registers should be changed to narrow RX bandpass filter bandwidth.

[Bank0]
 [IF_FREQ_AFC_H:B0 0x30] register
 [IF_FREQ_AFC_L:B0 0x31] register
 [BPF_AFC_ADJ_H:B0 0x32] register
 [BPF_AFC_ADJ_L:B0 0x33] register

[Bank1]
 [PLL_CFP_ADJ:B1 0x09] register
 [IF_FREQ_H:B1 0x0A] register
 [IF_FREQ_L:B1 0x0B] register
 [IF_FREQ_CCA_H:B1 0x0C] register
 [IF_FREQ_CCA_L:B1 0x0D] register
 [BPF_ADJ_H:B1 0x0E] register
 [BPF_ADJ_L:B1 0x0F] register
 [BPF_CCA_ADJ_H:B1 0x10] register
 [BPF_CCA_ADJ_L:B1 0x11] register

■RF adjustment

●PA adjustment

ML7306 family has output circuits for 1mW and 20mW (10mW as well). Output circuits can be selected by PA_SEL ([PA_CNTRL:B1 0x07(4)]).

Each output power can be adjusted with 16 resolutions by using [PA_ADJ1:B1 0x04] to [PA_ADJ3:B1 0x06] registers and [PA_REG_ADJ1:B1 0x33] to [PA_REG_ADJ3:B1 0x35] registers. In each register, 20mW circuit is adjusted by upper 4bits and 1mW circuit is adjusted by lower 4bits. 3 setting value can be stored for each output power circuit. Applying setting can be selected by PA_ADJ_SEL[1:0] ([PA_CNTRL:B1 0x07(1-0)]).

When switching output power between 10mW and 20mW, 10mW adjustment setting valueis stored into [PA_ADJ1:B0 0x04] and those for 20mW is stored into [PA_ADJ2:B1 0x05]. After that, output power can be switched by PA_ADJ_SEL[1:0] setting. Maximum 3 settings can be stored for each output circuit.

Note: Output impedance at PA_OUT pin (#27) differs between 1mW output circuit and 20mW output circuit.
Therefore, the most optimized matching circuit will also be different.

Following table shows setting validity corresponfding to PA_SEL and PA_ADJ_SEL[1:0] setting.

PA_SEL (B1 0x07)	PA_ADJ_SEL [1:0] (B1 0x07)	PA adjustment registers						PA regulator adjustment registers		
		PA_ADJ1		PA_ADJ2		PA_ADJ3		PA_REG_ADJ1	PA_REG_ADJ2	PA_REG_ADJ3
		[7:4]	[3:0]	[7:4]	[3:0]	[7:4]	[3:0]	[2:0]	[2:0]	[2:0]
0b0	0b01		valid					valid	▨	▨
0b0	0b10				valid			▨	valid	▨
0b0	0b11						valid	▨	▨	valid
0b1	0b01	valid						valid	▨	▨
0b1	0b10			valid				▨	valid	▨
0b1	0b11					valid		▨	▨	valid

●I/Q adjustment

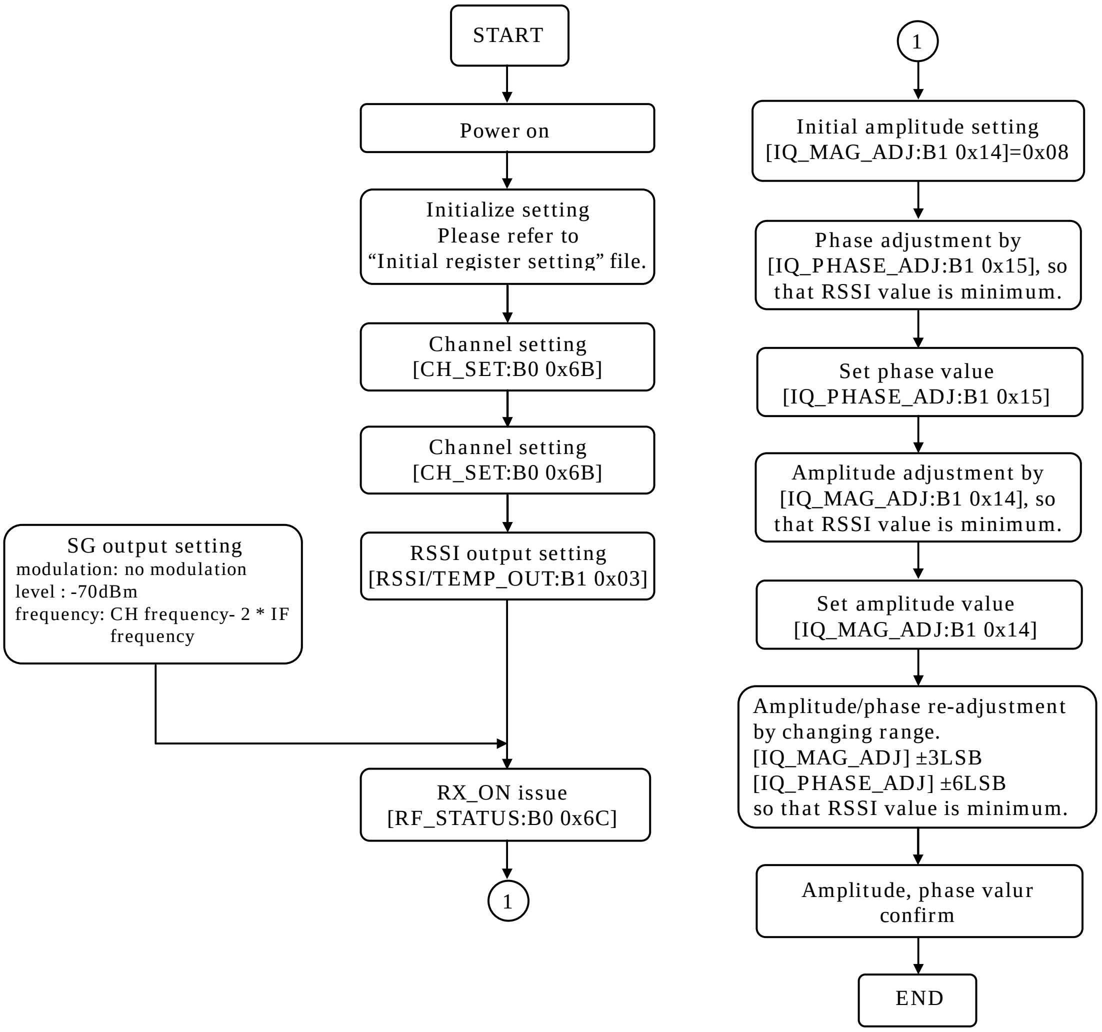
Image rejection ratio can be adjusted by tuning IQ signal balance. The adjustment procedure is as follows:

1. From SG, image frequency signal is input to ANT pin (#30).
   Input signal: no modulation.wave
   Input frequency: channel frequency - (2 * IF frequency)
   In case of 100kbps, IF frequency = 720kHz. please refer to the “Programing IF frequency”.
   Input level: -70dBm

2. By setting RSSI_OUT ([RSSI/TEMP_OUT:B1 0x03(0)]) =0b1, outputing RSSI from A_MON pin (#24).

3. Issuing RX_ON by [RF_STATUS:B0 0x6C] register, by adjusting [IQ_MAG_ADJ:B1 0x14] and [IQ_PHASE_ADJ: B1 0x15] registers, finding setting value so that RSSI value is minimum by measuring A_MON pin (#24).

[I\Q adjustment flow]


START
Power on
Initialize setting
Please refer to
“Initial register setting” file.
Channel setting
[CH_SET:B0 0x6B]
Channel setting
[CH_SET:B0 0x6B]
SG output setting
modulation: no modulation
level : -70dBm
frequency: CH frequency- 2 * IF frequency
RSSI output setting
[RSSI/TEMP_OUT:B1 0x03]
RX_ON issue
[RF_STATUS:B0 0x6C]
1
1
Initial amplitude setting
[IQ_MAG_ADJ:B1 0x14]=0x08
Phase adjustment by
[IQ_PHASE_ADJ:B1 0x15], so
that RSSI value is minimum.
Set phase value
[IQ_PHASE_ADJ:B1 0x15]
Amplitude adjustment by
[IQ_MAG_ADJ:B1 0x14], so
that RSSI value is minimum.
Set amplitude value
[IQ_MAG_ADJ:B1 0x14]
Amplitude/phase re-adjustment
by changing range.
[IQ_MAG_ADJ] ±3LSB
[IQ_PHASE_ADJ] ±6LSB
so that RSSI value is minimum.
Amplitude, phase valur
confirm
END

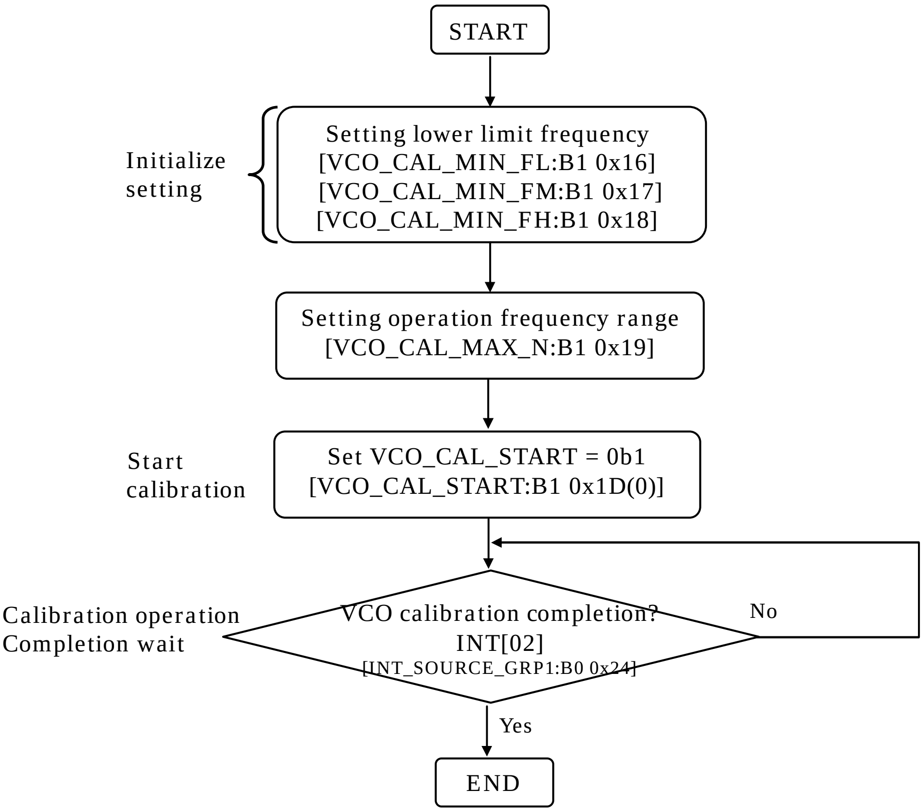
●VCO adjustment

In order to compensate VCO operation margin, optimized capacitance compensation value should be set in each operation frequency. This capacitance compensation value can be acquired by VCO calibration.

By performing VCO calibration when power-up or reset, acquired capacitance compensation values for upper limit and lower limit of operation frequency range (for both TX/RX), based on this value optimised capacitance value is applied during TX/RX operation. Lower limit frequency can be set by [VCO_CAL_MIN_FL:B1 0x16] to [VCO_CAL_MIN_FH:B1 0x18] registers. Upper frequency is defined by [VCO_CAL_MAX_N:B1 0x19] register as frequency range.

[VCO adjustment flow]

The following flow is the procedure for acquiring capacitance compensation value when power-up or reset.


START
Initialize setting
Setting lower limit frequency
[VCO_CAL_MIN_FL:B1 0x16]
[VCO_CAL_MIN_FM:B1 0x17]
[VCO_CAL_MIN_FH:B1 0x18]
Setting operation frequency range
[VCO_CAL_MAX_N:B1 0x19]
Start calibration
Set VCO_CAL_START = 0b1
[VCO_CAL_START:B1 0x1D(0)]
Calibration operation Completion wait
VCO calibration completion?
INT[02]
[INT_SOURCE_GRP1:B0 0x24]
No
Yes
END

Note: VCO calibration should be performed only during IDLE state.

VCO calibration is necessary every 0.9ms to 4.2ms.
After completion, capacitance compensation values are stored in the following registers.
Capacitance compensation value at lower limit frequency: [VCO_CAL_MIN:B1 0x1A]
Capacitance compensation value at upper limit frequency: [VCO_CAL_MAX:B1 0x1B]

In actual operation, based on the 2 compensation values, the most optimized capacitance value for the frequency is calculated and applied. The calculated value is stored in [VCO_CAL:B1 0x1C] register.

By evaluation stage, if below values are stored in the MCU memory and uses these values upon reset or power-up, calibration operation can be omitted.

Registers to be saved in the MCU memory.
[VCO_CAL_MIN_FL:B1 0x16]
[VCO_CAL_MIN_FM:B1 0x17]
[VCO_CAL_MIN_FH:B1 0x18]
[VCO_CAL_MAX_N:B1 0x19]
[VCO_CAL_MIN:B1 0x1A]
[VCO_CAL_MAX: B1 0x1B]

NOTE:

1. For lower limit frequency, please use frequency at least 2MHz lower than operation frequency
2. For upper limit frequency should be selected so that operation frequency is in the frequency range.
3. Frequency range should not include 36MHz multiplied frequency, i.e. 900MHz, 936MHz.
4. In case of like a channel change, if the setting frequency is outside of calibration frequency range, calibration process has to be performed again with proper frequency.

●VCO lower limit frequency setting

As described in the “Programing Channel #0 Frequency”, VCO lower limit frequency can be set by setting F-counter parameter into [VCO_CAL_MIN_FL:B1 0x16], [VCO_CAL_MIN_FM:B1 0x17] and [VCO_CAL_MIN_FH:B1 0x18] registers. N-counter and A-counter parametrs are applied the valu stored in [CH0_NA:B0 0x4B] register.

Lower limit frequency setting value can be calculated using the following formula.

$$LOW\_F = \{F_{LOW} - (4 * N + A) * f_{REF}\} / f_{REF} * 2^{20} \text{ (Integer part)} \qquad \text{[note: using 20bit circuit]}$$

Here

LOW_F	: Lower limit frequency F-counter setting
F_{LOW}	: Lower limit frequency [MHz]
f_{REF}	: PLL reference frequency (input clock=36MHz)
N	: N-counter parameter
A	: A-counter parameter

If operation low limit frequency is 923.1MHz, N= 6 and A=1. Setting value should be lower than 2MHz. Then in following example, lower limit frequency is set to 921.1MHz. (f_{REF} = 36MHz)

$$LOW\_F = \{921.1 - (4 * 6 + 1) * 36\text{MHz}\} / 36\text{MHz} * 2^{20} \text{ (Integer part)} = 614582 \text{ (0x960B6)}$$

Setting values for each register is as follows:
[VCO_CAL_MIN_FL:B1 0x16]= 0xB6
[VCO_CAL_MIN_FM:B1 0x17]= 0x60
[VCO_CAL_MIN_FL:B1 0x18]= 0x09

●VCO upper limit frequency setting

VCO upper limit frequency is calculated as following formula, based on low limit frequency values and VCO_CAL_MAX_N[4:0] ([VCO_CAL_MAX_N: B1 0x19(5-0)]).

VCO calibration upper limit frequency = VCO calibration lower limit frequency (B1 0x16-0x18) + ΔF(B1 0x51)

ΔF is defined in the table below.

VCO_CAL_MAX_N[4:0]	ΔF[MHz]
0b0_0000	1.125
0b0_0001	2.25
0b0_0011	4.5
0b0_0111	9
0b0_1111	18
0b1_1111	36
Other than aboev	Prohibited

●Energy Detection value (ED value) adjustment

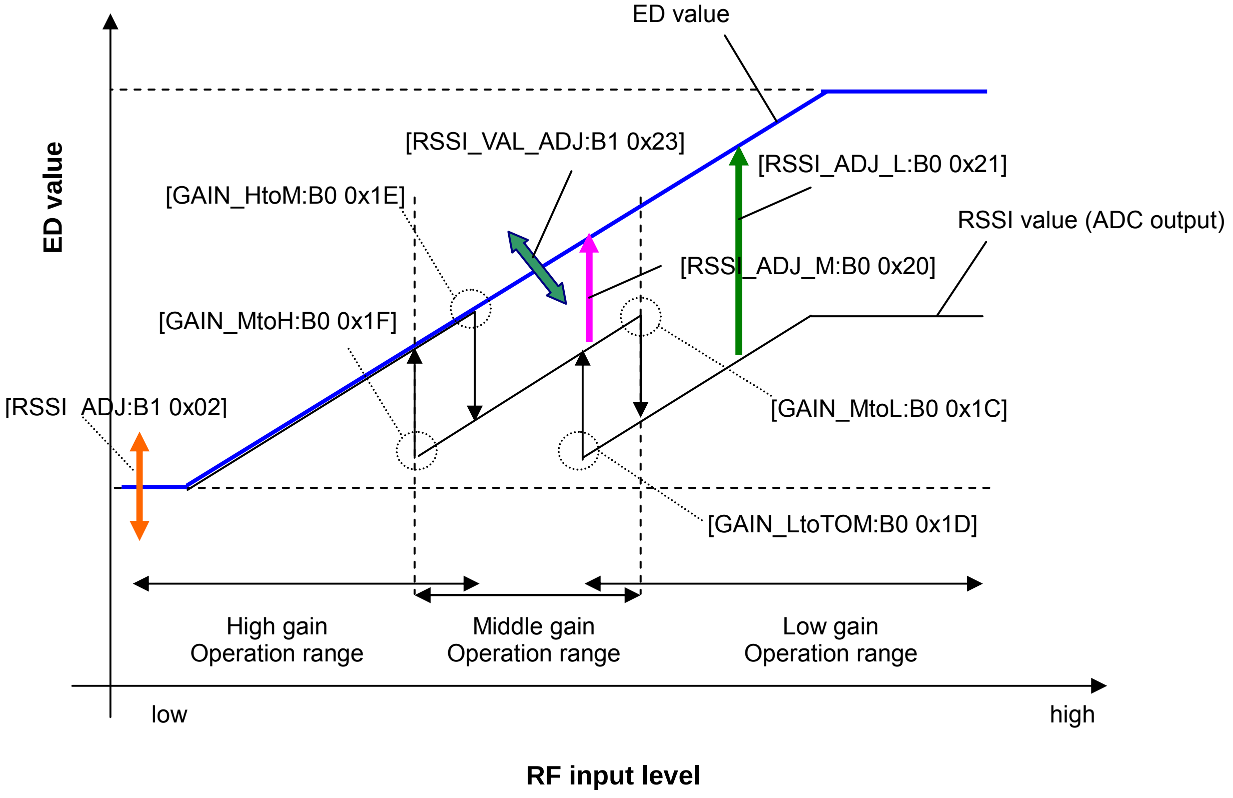
[ED value adjustment]

ED value is calculated by RSSI signal (analog signal) from RF part,. By performing the following adjustment, it is possible to correct the variation in LSIs.

The gain adjustment and related registers are described below.

In order to cover wider input range, gain should be changed at given point. Threshold for gain change points are set by [GAIN_MtoL:B1 0x1C] to [GAIN_MtoH:B0 0x1F]. [RSSI_ADJ_M:B1 0x20] and [RSSI_ADJ_L:B1 0x21] registers are used to addition values to maintain linearity when changing gain. RSSI slope can be set to [RSSI_VAL_ADJ:B1 0x23] register so that ED value can be between 0x00(min) and 0xFF(max). For thse register setting, please use the value specified in the “Initial register setting” file.

Adjusting the input level variation for the same input level can be set to [RSSI_ADJ:B1 0x02] register. It must compensate the slope before compensation defined by [RSSI_VAL_ADJ:B1 0x23] register. However, if positive value is set , ED value cannot be decreased down to 0x00 at low input signal level. If negative value is set, ED value cannot be increased up to 0xFF.



Operation in the High gain range:	RSSI value>GAIN_HtoM, and move to Middle gain.
Operation in the Middle gain range:	RSSI value>GAIN_MtoL, and move to Low gain. GAIN_MtoH≥RSSI value, and move to High gain.
Operation in the Low gain range:	GAIN_LtoM≥RSSIvalue, and move to Middle gain.

■Other Setting

●BER measurement setting

The following registers setting are necessary for RX side when measuring BER.

[PLL_MON/DIO_SEL:B0 0x69] = 0x01
[DEMOD_SET:B1 0x01] = 0x80
[DEMOD_SET2:B2 0x0A] = 0x10
[SYNC_MODE:B2 0x12] = 0x00

■Flow Charts

●Initialization

In initialization status, interrupt process, registers setting, VCO calibration are necessary.

(1) Interrupt process

Upon reset, all interrupt notification settings ([INT_EN_GRP1-4:B0 0x2A-0x2D]) are enabled.

After hard reset is released, INT[00] (group 1: Clock stabilization completion interrupt) will be detected. After INT[00] notification, please mask unused interruput elements by using [INT_EN_GRP1:B0 0x2A] to [INT_EN_GRP4] registers.

If interrupt elements are stored internnaly, interrupt will generate as soon as interrupt is unmasked, unless clearing the interrpt. When clearing interrupt, it is recommended to clear interrput after masking the interrupt.

(2) Registers setting

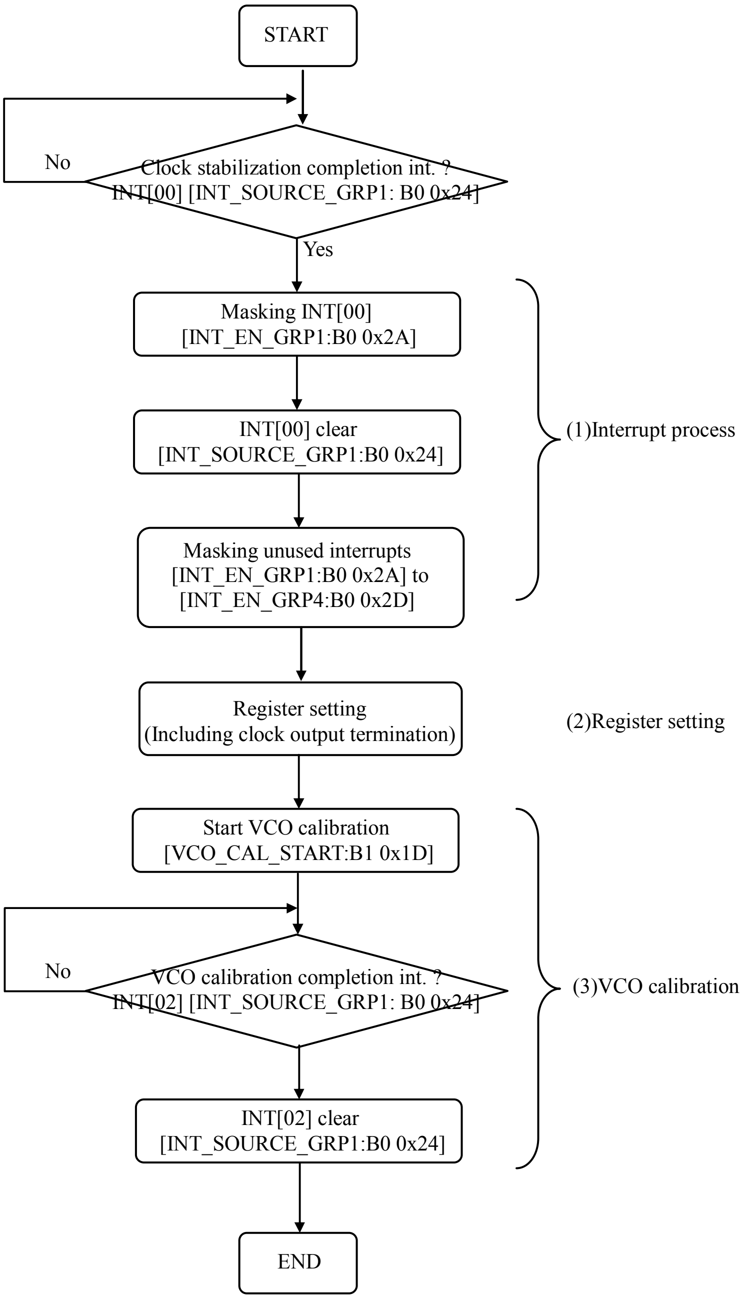
In reset value setting, clock is output from DMON pin (#17). If clock output is not used, please assign another monitoring function to DMON pin and terminate clock output.

After hard reset is released, all registers are accesible except for FIFO access registers and BANK1 registers before INT[00] notification.

(3) VCO calibration

Executing VCO calibration after setting upper and lower limit of the operation frequency range. Operating frequency should be in the calibration frequency range. In case of using frequency which is outside of calibration frequency range, calibration process has to be performed again with proper frequency.

During VCO calibration, please register access is prohibited.


START
No
Clock stabilization completion int. ?
INT[00] [INT_SOURCE_GRP1: B0 0x24]
Yes
Masking INT[00]
[INT_EN_GRP1:B0 0x2A]
INT[00] clear
[INT_SOURCE_GRP1:B0 0x24]
Masking unused interrupts
[INT_EN_GRP1:B0 0x2A] to
[INT_EN_GRP4:B0 0x2D]
(1)Interrupt process
Register setting
(Including clock output termination)
(2)Register setting
Start VCO calibration
[VCO_CAL_START:B1 0x1D]
No
VCO calibration completion int. ?
INT[02] [INT_SOURCE_GRP1: B0 0x24]
INT[02] clear
[INT_SOURCE_GRP1:B0 0x24]
(3)VCO calibration
END

●TX mode (DIO mode)

DIO (TX) mode can be selected by setting DIO_EN ([PLL_MON/DIO_SEL:B0 0x69(1)]) =0b1. In DIO (TX) mode, when issuing TX_ON command, data input to DIO pin (#15) will be transmitted to the air. TX Data following SFD field should be input from host MCU and TX data should be synchronized with DCLK from DCLK pin (#16). After TX completion, TRX_OFF commnand should be issued.

TX data request accept completion interrupt (INT[22] or INT[23] group3) notification should be required to start DIO (TX) transmission. Before issuing TX_ON command, writing dummy data to a FIFO to generate TX data request accept completion interrupt. More than 4byte dummy data (excluding Lngth field) is required.

[Example: Setting minimum dummy packet]

Set CRC_DONE ([FEC/CRC_SEC:B0 0x46(0)]) =0b0, and write 0x00-01-02 (3byte) tp [WR_TX_FIFO:B0 0x7E] register.

Note: The first TX data input during DIO (TX) mode.

Initial status of DCLK pin (#16) is “L”. Therefore there is no falling edge for the 1st TX data, the 1st TX data should be pre-set to DIO pin (#15) before writing dummy packet.

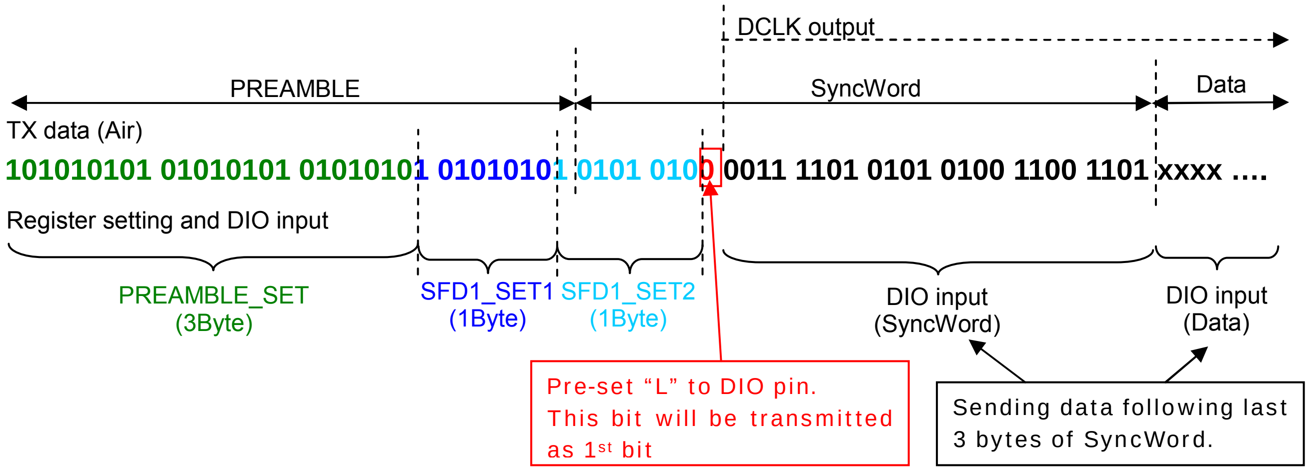
For more details, please refer to the explanation in following page.

TX data corresponding to each register setting and DIO input is as below:

[Example] Transmitting prEN 13757-4rev Mode C format A packet (ML7396E)

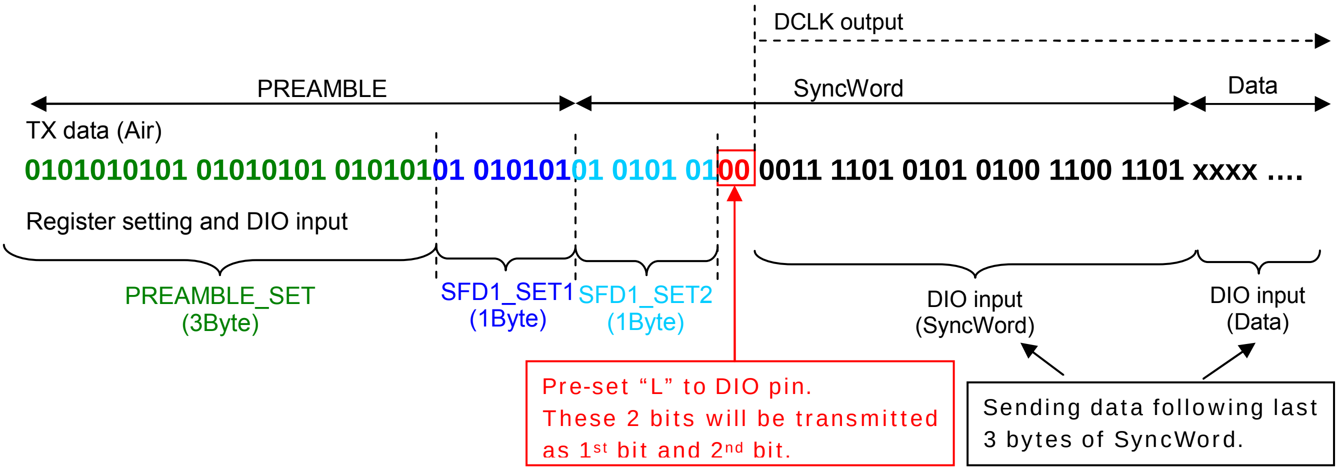
Case 1: Input TX data at rising edge of DCLK

[Conditions]
[PREAMBLE_SET:B0 0x39] =0x55
[SFD1_SET1:B0 0x3A] =0x55
[SFD1_SET2:B0 0x3B] =0x55
[TX_PB_LEN:B0 0x42] =0x03
[RX_PR_LEN/SFD_LEN:B0 0x43] =0x02

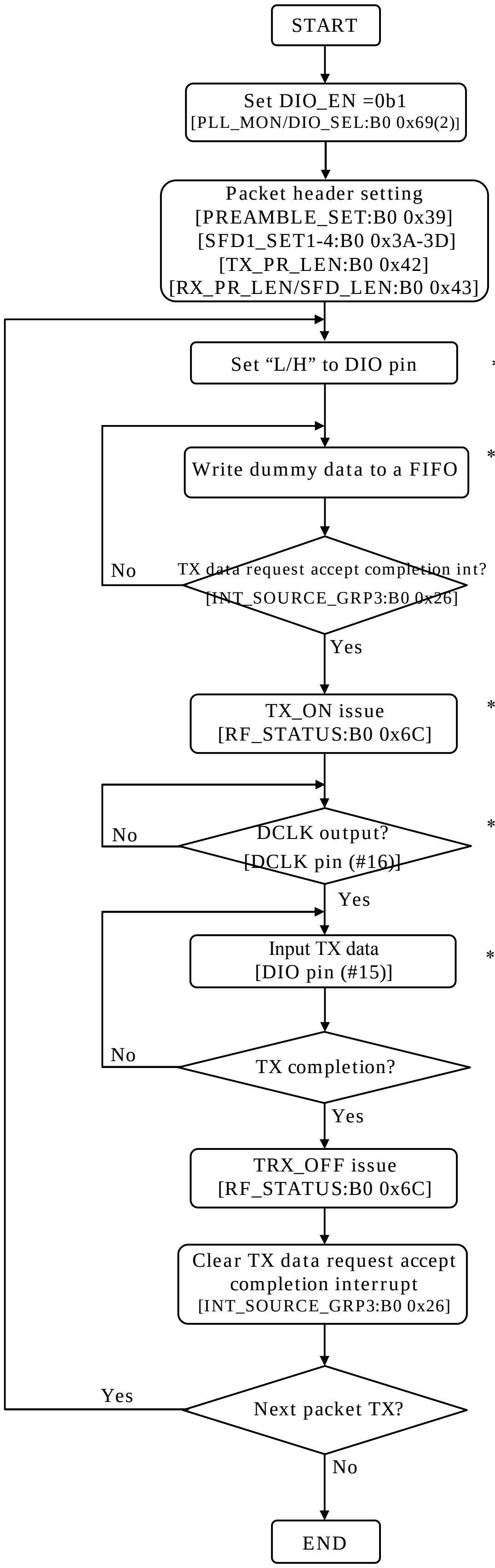

DCLK output
PREAMBLE
SyncWord
Data
TX data (Air)
101010101 01010101 01010101 01010101 0101 0100 0011 1101 0101 0100 1100 1101 xxxx ….
Register setting and DIO input
PREAMBLE_SET
(3Byte)
SFD1_SET1
(1Byte)
SFD1_SET2
(1Byte)
DIO input
(SyncWord)
DIO input
(Data)
Pre-set "L" to DIO pin.
This bit will be transmitted as 1st bit
Sending data following last 3 bytes of SyncWord.

Case 2: Input TX data at falling edge of DCLK

[Conditions]
[PREAMBLE_SET:B0 0x39]=0xAA
[SFD1_SET1:B0 0x3A] =0xAA
[SFD1_SET2:B0 0x3B] =0xAA
[TX_PB_LEN:B0 0x42] =0x03
[RX_PR_LEN/SFD_LEN:B0 0x42] =0x02


DCLK output
PREAMBLE
SyncWord
Data
TX data (Air)
0101010101 01010101 01010101 01010101 0101 0100 0011 1101 0101 0100 1100 1101 xxxx ….
Register setting and DIO input
PREAMBLE_SET
(3Byte)
SFD1_SET1
(1Byte)
SFD1_SET2
(1Byte)
DIO input
(SyncWord)
DIO input
(Data)
Pre-set "L" to DIO pin.
These 2 bits will be transmitted as 1st bit and 2nd bit.
Sending data following last 3 bytes of SyncWord.

[Flowchart]


START
Set DIO_EN =0b1
[PLL_MON/DIO_SEL:B0 0x69(2)]
Packet header setting
[PREAMBLE_SET:B0 0x39]
[SFD1_SET1-4:B0 0x3A-3D]
[TX_PR_LEN:B0 0x42]
[RX_PR_LEN/SFD_LEN:B0 0x43]
Set "L/H" to DIO pin
Write dummy data to a FIFO
TX data request accept completion int?
[INT_SOURCE_GRP3:B0 0x26]
No
Yes
TX_ON issue
[RF_STATUS:B0 0x6C]
DCLK output?
[DCLK pin (#16)]
No
Yes
Input TX data
[DIO pin (#15)]
TX completion?
No
Yes
TRX_OFF issue
[RF_STATUS:B0 0x6C]
Clear TX data request accept
completion interrupt
[INT_SOURCE_GRP3:B0 0x26]
Next packet TX?
Yes
No
END

* RX_FIFO_MON ([PLL_MON/DIO_SEL:B0 0x69(0)]) setting does not affect on DIO (TX) mode operation.

* Set 1st biy of TX data to the DIO pin.

* Set CRC_DONE ([FEX/CRC_SET:B0 0x46(0)])=0b0 (disable) and write 0x00-01-02 to [WR_TX_FIFO:B0 0x7E] register.

* If issuing TX_ON before writing dummy data, same result can be achieved

* Timing up to DCLK output varies depending on preamble length, SFD length and data rate

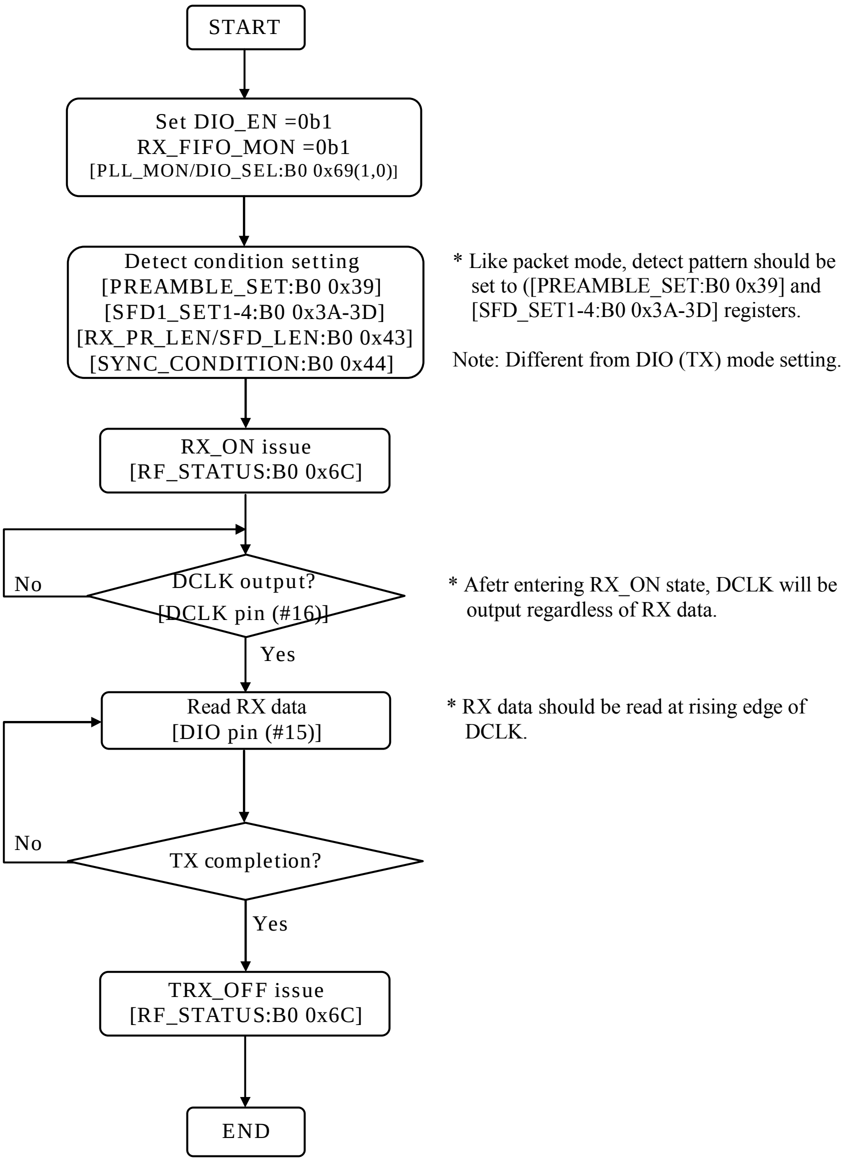
* TX data should be input at falling edge of DCLK.

●RX mode (DIO mode)

DIO (RX) mode can be selected by setting DIO_EN ([PLL_MON/DIO_SEL:B0 0x69(1)]) =0b1 and RX_FIFO_MON ([PLL_MON/DIO_SEL:B0 0x69(1)]) =0b1. In DIO (RX) mode, when issuing RX_ON command, preamble and SFD detection will be started. After preamble and SFD are detected, RX data is output through DIO pin (#15). RX Data following SFD field are output and RX data should be read at rising edge of DCLK from DCLK pin (#16). After RX completion, TRX_OFF commnand should be issued.

Like packet mode, preamble and SFD detection are done according to the settings of [PREAMBLE_SET:B0 0x39], [SFD1_SET1:B0 0x3A] to [SFD1_SET4:B0 0x3D], [RX_PR_LEN/SFD_LEN:B0 0x43] and [SYNC_CONDITION:B0 0x44] registers.After SFD is deteceted, SFD detection interrupt (INT[11] group2) will generate.

The first RX data is output at the first rising edge of DCLK after SFD detection interrupt notification.(Timing from SFD detection interrupt to the first DCLK rising edge is 9μs at 100kbps setting.)

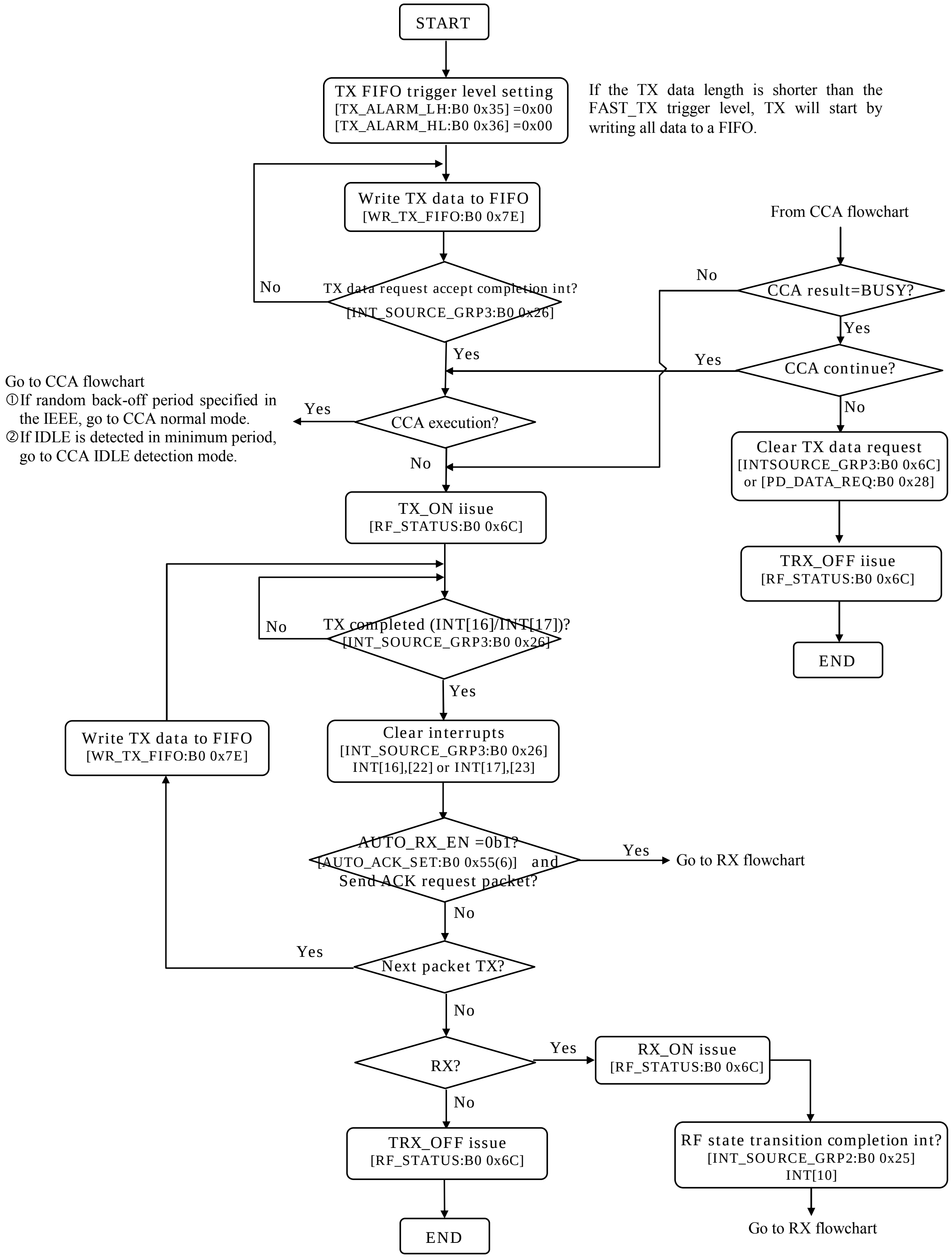

START
Set DIO_EN =0b1
RX_FIFO_MON =0b1
[PLL_MON/DIO_SEL:B0 0x69(1,0)]
Detect condition setting
[PREAMBLE_SET:B0 0x39]
[SFD1_SET1-4:B0 0x3A-3D]
[RX_PR_LEN/SFD_LEN:B0 0x43]
[SYNC_CONDITION:B0 0x44]
* Like packet mode, detect pattern should be set to ([PREAMBLE_SET:B0 0x39] and [SFD_SET1-4:B0 0x3A-3D] registers.
Note: Different from DIO (TX) mode setting.
RX_ON issue
[RF_STATUS:B0 0x6C]
No
DCLK output?
[DCLK pin (#16)]
Yes
* Afetr entering RX_ON state, DCLK will be output regardless of RX data.
Read RX data
[DIO pin (#15)]
* RX data should be read at rising edge of DCLK.
No
TX completion?
Yes
TRX_OFF issue
[RF_STATUS:B0 0x6C]
END

●TX mode (Packet mode, packet length ≤ 256byte)

Packet mode can be selected by setting DIO_EN ([PLL_MON/DIO_SEL:B0 0x69(1)]) =0b0. In Packet mode, each TX data is written into a FIFO by [WR_TX_FIFO:B0 0x7E] register. After writing full TX data of a packet, issuing TX_ON command. Following PB (preamble), SFD data, TX data is transmitted to the air. When CRC is enabled, the CRC calcuration will be done automatically and CRC result is set to FCS field and transmitted to the air.

After TX completion interrupt (INT[16]/[17] group3) occurs, the interrupt must be cleared. If the next TX packet is sent, the next TX packet data is written to a FIFO. If RX is expected after TX, RX_ON should be issued by [RF_STATUS:B0 0x6E] register. TX can be terminated by issuing TRX_OFF by [RF_STATUS:B0 0x6E] register.

At every packet writing, FIFO0 and FIFO1 are switched automatically. (FIFO0 → FIFO1 → FIFO0)


START
TX FIFO trigger level setting
[TX_ALARM_LH:B0 0x35] =0x00
[TX_ALARM_HL:B0 0x36] =0x00
Write TX data to FIFO
[WR_TX_FIFO:B0 0x7E]
TX data request accept completion int?
[INT_SOURCE_GRP3:B0 0x26]
No
Yes
From CCA flowchart
CCA result=BUSY?
No
Yes
CCA continue?
Yes
No
Clear TX data request
[INTSOURCE_GRP3:B0 0x6C]
or [PD_DATA_REQ:B0 0x28]
TRX_OFF iisue
[RF_STATUS:B0 0x6C]
END
CCA execution?
Yes
No
TX_ON iisue
[RF_STATUS:B0 0x6C]
TX completed (INT[16]/INT[17])?
[INT_SOURCE_GRP3:B0 0x26]
No
Yes
Write TX data to FIFO
[WR_TX_FIFO:B0 0x7E]
Clear interrupts
[INT_SOURCE_GRP3:B0 0x26]
INT[16],[22] or INT[17],[23]
AUTO_RX_EN =0b1?
[AUTO_ACK_SET:B0 0x55(6)] and
Send ACK request packet?
Yes
Go to RX flowchart
No
Next packet TX?
Yes
No
RX?
Yes
RX_ON issue
[RF_STATUS:B0 0x6C]
No
TRX_OFF issue
[RF_STATUS:B0 0x6C]
END
RF state transition completion int?
[INT_SOURCE_GRP2:B0 0x25]
INT[10]
Go to RX flowchart

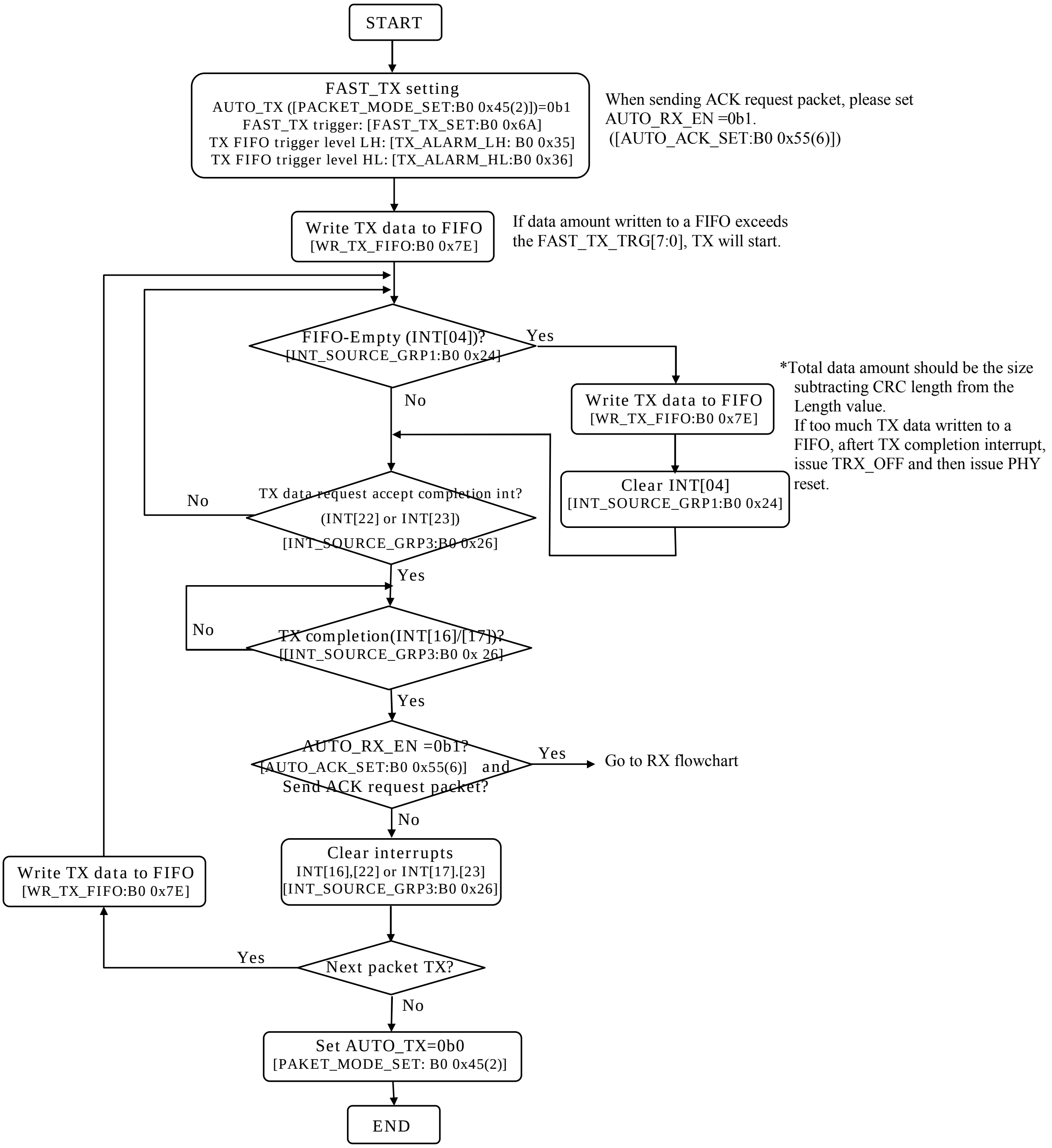
If the TX data length is shorter than the FAST_TX trigger level, TX will start by writing all data to a FIFO.

Go to CCA flowchart
①If random back-off period specified in the IEEE, go to CCA normal mode.
②If IDLE is detected in minimum period, go to CCA IDLE detection mode.

●TX mode (Packet mode, packet length ≥ 257byte)

The host MCU should write TX data to a FIFO while checking FIFO-Full interrupt (INT[05] group1) and FIFO-Empty interrupt (INT[04] group1) in order to avoid FIFO-Overrun or FIFO-Underrun. Other operation are same as packet mode (less than 256byte).

Enabling FAST_TX mode by setting AUTO_TX ([PACKET_MODE_SET:B0 0x45(2)] =0b1 and FAST_TX_TRG[7:0] ([FAST_TX_SET:B0 0x6A(7-0)], TX will start when data amount written to a FIFO exceeds the setting value of FAST_TX_TRG[7:0].


START
FAST_TX setting
AUTO_TX ([PACKET_MODE_SET:B0 0x45(2)])=0b1
FAST_TX trigger: [FAST_TX_SET:B0 0x6A]
TX FIFO trigger level LH: [TX_ALARM_LH: B0 0x35]
TX FIFO trigger level HL: [TX_ALARM_HL:B0 0x36]
Write TX data to FIFO
[WR_TX_FIFO:B0 0x7E]
FIFO-Empty (INT[04])?
[INT_SOURCE_GRP1:B0 0x24]
Yes
No
Write TX data to FIFO
[WR_TX_FIFO:B0 0x7E]
Clear INT[04]
[INT_SOURCE_GRP1:B0 0x24]
No
TX data request accept completion int?
(INT[22] or INT[23])
[INT_SOURCE_GRP3:B0 0x26]
Yes
No
TX completion(INT[16]/[17])?
[[INT_SOURCE_GRP3:B0 0x 26]
Yes
AUTO_RX_EN =0b1?
[AUTO_ACK_SET:B0 0x55(6)] and
Send ACK request packet?
Yes
Go to RX flowchart
No
Clear interrupts
INT[16],[22] or INT[17].[23]
[INT_SOURCE_GRP3:B0 0x26]
Write TX data to FIFO
[WR_TX_FIFO:B0 0x7E]
Yes
Next packet TX?
No
Set AUTO_TX=0b0
[PAKET_MODE_SET: B0 0x45(2)]
END

When sending ACK request packet, please set AUTO_RX_EN =0b1.
([AUTO_ACK_SET:B0 0x55(6)])

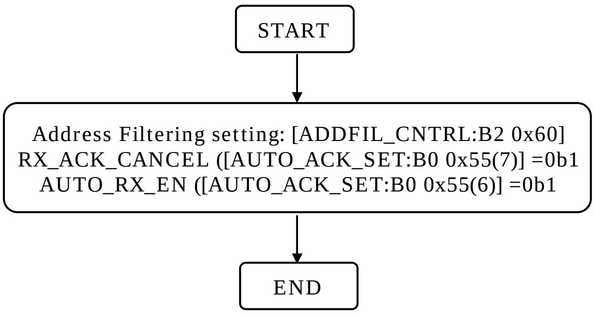
If data amount written to a FIFO exceeds the FAST_TX_TRG[7:0], TX will start.

*Total data amount should be the size subtracting CRC length from the Length value.
If too much TX data written to a FIFO, aftert TX completion interrupt, issue TRX_OFF and then issue PHY reset.

●TX mode (Ack receiving with address filter)

Even when Address Filtering function is enabled, Ack packet (or beacon packet) will be received. However dscarding Ack packet can be set by RX_ACK_CANCEL ([AUTO_ACK_SET:B0 0x55(7)]) =0b1.

And when AUTO_RX_EN ([AUTO_ACK_SET:B0 0x55(6)])=0b1, the Ack packet just after transmitting ACK request packet can be received without discarding.


START
Address Filtering setting: [ADDFIL_CNTRL:B2 0x60]
RX_ACK_CANCEL ([AUTO_ACK_SET:B0 0x55(7)] =0b1
AUTO_RX_EN ([AUTO_ACK_SET:B0 0x55(6)] =0b1
END

Note: Ack packet is detected by frame type only. Therefore even if the first Ack packet destination is different address, this Ack packet will be received. The following process is as below;

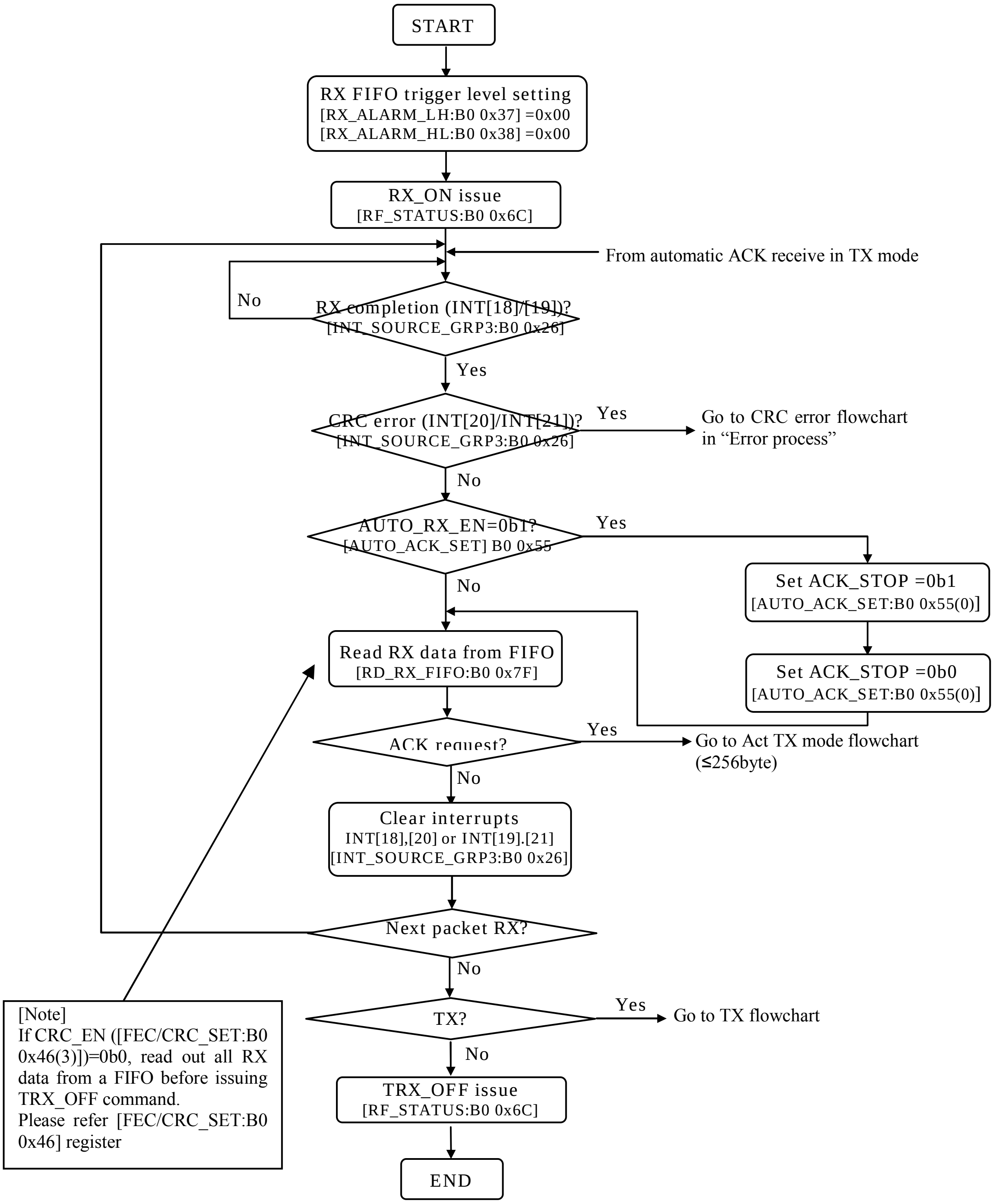
① Address match
Following 2nd packet will be discarded.

② Address mismatch
By setting RX_ACK_CANCEL=0b0, maintain RX until receiving Ack packet with right address.

●RX mode (Packet mode, packet length ≤ 256 bytes)

Packet mode can be selected setting DIO_EN ([PLL_MON/DIO_SEL:B0 0x69(1)]) =0b0. In DIO mode, when issuing RX_ON command, preamble and SFD detection will be started. After preamble and SFD are detected, RX data will be stored into a FIFO. After RX completion interrupt (INT[18]/[19] group3) occurs, the host MCU will read RX data from [RD_RX_FIFO:B0 0x7F] register. If CRC error interrupt (INT[20]/[21]) is generated, FIFO data has to be cleared by setting (FIFO_CLR1/0 ([INT_SOURCE_GRP1:B0 0x26(7/6)]) =0b0. After clearing RX retaive interrpts, if receiving the next packet, maintain RX_ON status and waiting for next RX completion interrupt. If TX is expected after RX, TX_ON should be issued by [RF_STATUS:B0 0x6E] register. If terminating RX, issuing TRX_OFF by [RF_STATUS:B0 0x6E] register.

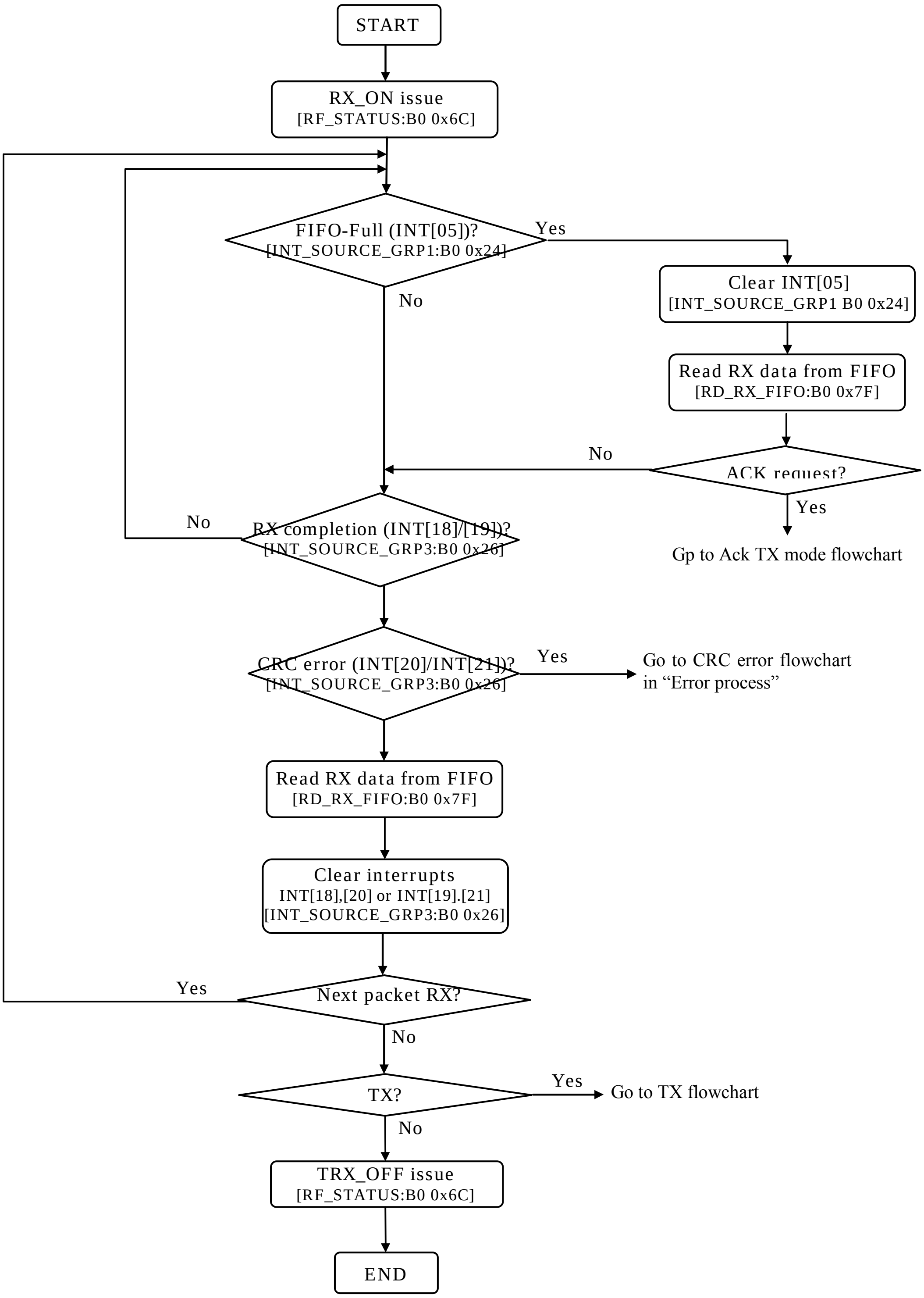
If FIFO-Full trigger and FIFO-Empty trigger are not used, please set 0x00 to both [RX_ALARM_LH:B0 0x37]) and [RX_ALARM_HL:B0 0x38)] registers.


START
RX FIFO trigger level setting
[RX_ALARM_LH:B0 0x37] =0x00
[RX_ALARM_HL:B0 0x38] =0x00
RX_ON issue
[RF_STATUS:B0 0x6C]
From automatic ACK receive in TX mode
No
RX completion (INT[18]/[19])?
[INT_SOURCE_GRP3:B0 0x26]
Yes
CRC error (INT[20]/INT[21])?
[INT_SOURCE_GRP3:B0 0x26]
Yes
Go to CRC error flowchart
in “Error process”
No
AUTO_RX_EN=0b1?
[AUTO_ACK_SET] B0 0x55
Yes
Set ACK_STOP =0b1
[AUTO_ACK_SET:B0 0x55(0)]
Set ACK_STOP =0b0
[AUTO_ACK_SET:B0 0x55(0)]
No
Read RX data from FIFO
[RD_RX_FIFO:B0 0x7F]
ACK request?
Yes
Go to Act TX mode flowchart
(≤256byte)
No
Clear interrupts
INT[18],[20] or INT[19].[21]
[INT_SOURCE_GRP3:B0 0x26]
Next packet RX?
No
TX?
Yes
Go to TX flowchart
No
TRX_OFF issue
[RF_STATUS:B0 0x6C]
END

[Note]
If CRC_EN ([FEC/CRC_SET:B0 0x46(3)])=0b0, read out all RX data from a FIFO before issuing TRX_OFF command.
Please refer [FEC/CRC_SET:B0 0x46] register

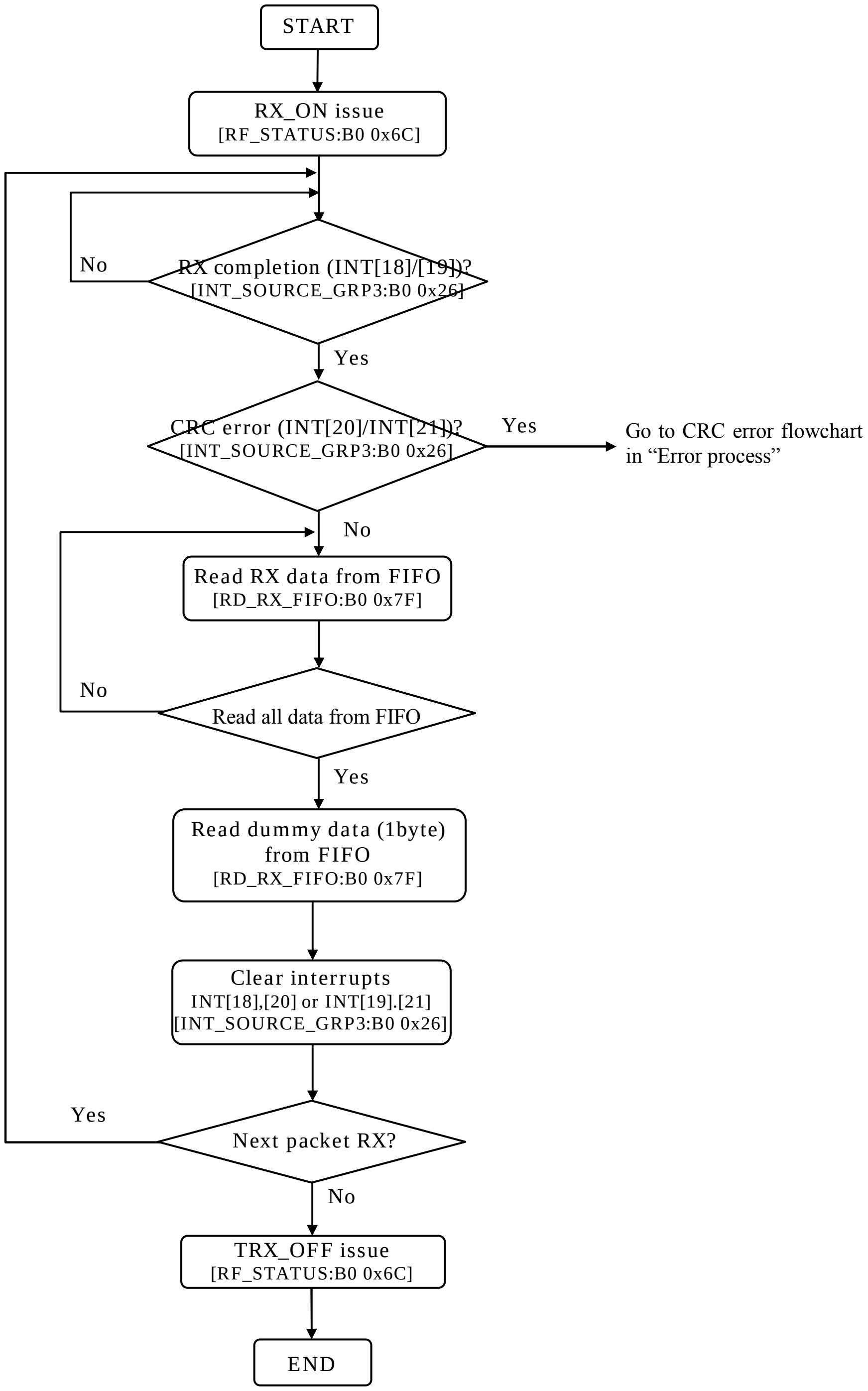
●RX mode (Packet mode, packet length ≥ 257 bytes)

The host MCU should read RX data from a FIFO while checking FIFO-Full interrupt (INT[05] group1) and FIFO-Empty interrupt (INT[04] group1) in order to avoid FIFO-Overrun or FIFO-Underrun. Other operation are same as packet mode (less than 256byte).


START
RX_ON issue
[RF_STATUS:B0 0x6C]
FIFO-Full (INT[05])?
[INT_SOURCE_GRP1:B0 0x24]
Yes
No
Clear INT[05]
[INT_SOURCE_GRP1 B0 0x24]
Read RX data from FIFO
[RD_RX_FIFO:B0 0x7F]
No
ACK request?
Yes
Gp to Ack TX mode flowchart
No
RX completion (INT[18]/[19])?
[INT_SOURCE_GRP3:B0 0x26]
CRC error (INT[20]/INT[21])?
[INT_SOURCE_GRP3:B0 0x26]
Yes
Go to CRC error flowchart
in "Error process"
Read RX data from FIFO
[RD_RX_FIFO:B0 0x7F]
Clear interrupts
INT[18],[20] or INT[19].[21]
[INT_SOURCE_GRP3:B0 0x26]
Yes
Next packet RX?
No
TX?
Yes
Go to TX flowchart
No
TRX_OFF issue
[RF_STATUS:B0 0x6C]
END

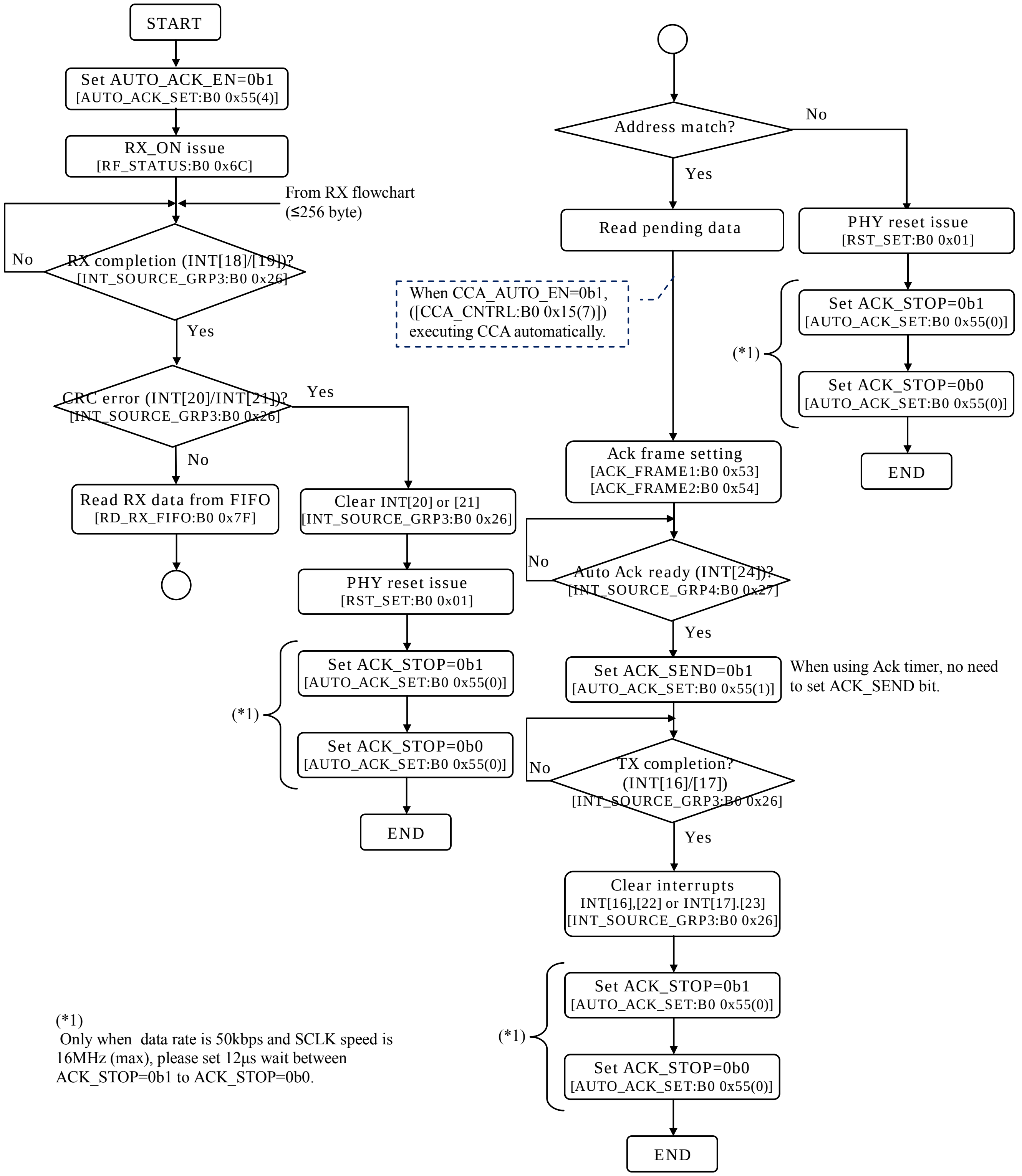
●RX mode (IEEE802.15.4d mode)

When using IEEE80.15.4d mode by IEEE_MODE ([PACKET_MODE_SET:B0 0x45(1)]) =0b0, Basic flowchart is same as IEEE 802.15.4g. However reading 1byte dummy data should be required after reading amount of data given by Length field.


START
RX_ON issue
[RF_STATUS:B0 0x6C]
No
RX completion (INT[18]/[19])?
[INT_SOURCE_GRP3:B0 0x26]
Yes
CRC error (INT[20]/INT[21])?
[INT_SOURCE_GRP3:B0 0x26]
Yes
Go to CRC error flowchart
in "Error process"
No
Read RX data from FIFO
[RD_RX_FIFO:B0 0x7F]
No
Read all data from FIFO
Yes
Read dummy data (1byte)
from FIFO
[RD_RX_FIFO:B0 0x7F]
Clear interrupts
INT[18],[20] or INT[19].[21]
[INT_SOURCE_GRP3:B0 0x26]
Yes
Next packet RX?
No
TRX_OFF issue
[RF_STATUS:B0 0x6C]
END

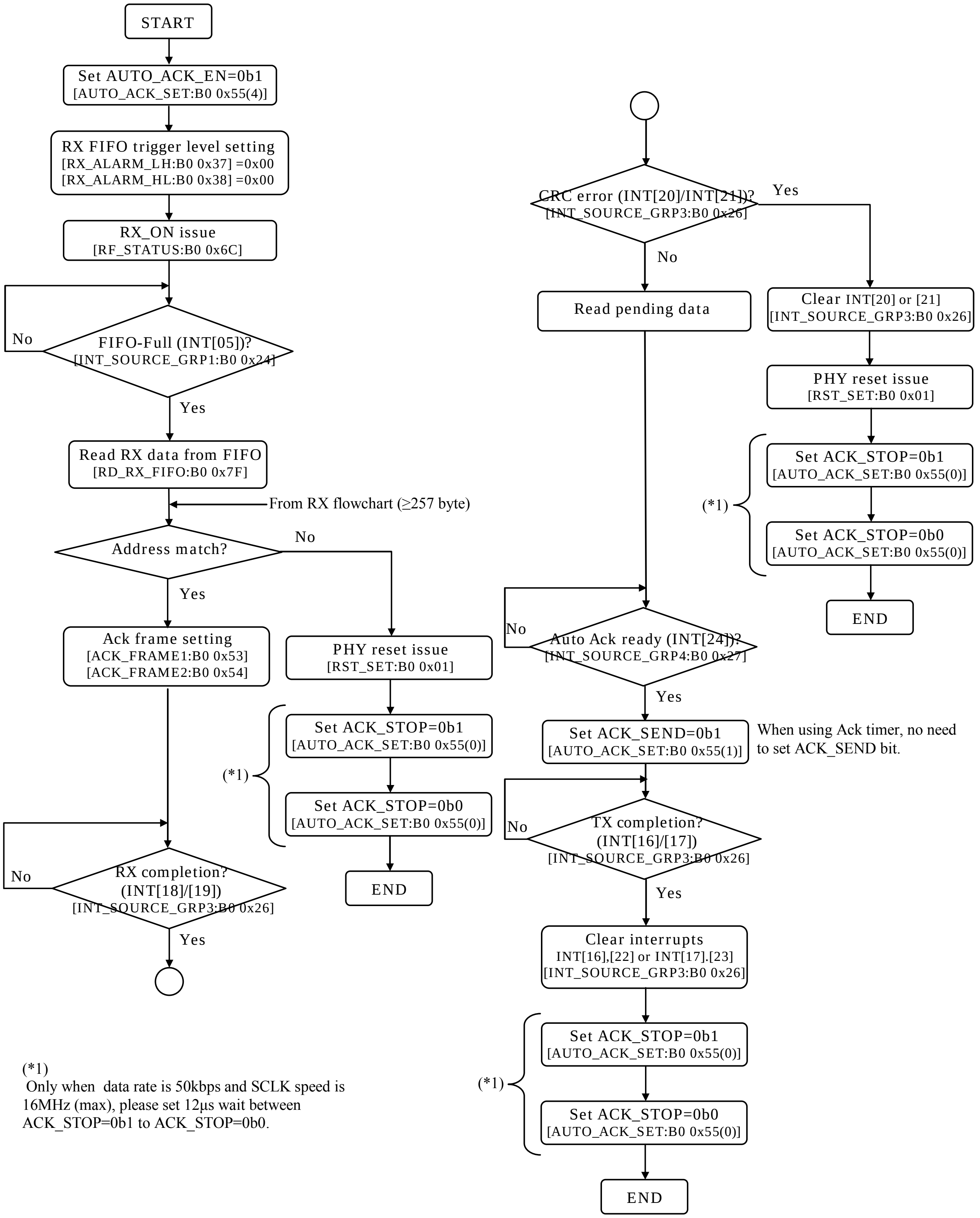
●ACK TX mode (AUTO_ACK, packet length ≤ 256 bytes)

When AUTO_ACK function is enabled by AUTO_ACK_EN ([AUTO_ACK_SET:B0 0x55(4)]) =0b1, if receiving TX packet with ACK request, preparing TX Ack packet (TX_ON) or transmitting Ack packet automatically (when using Ack timer).


START
Set AUTO_ACK_EN=0b1
[AUTO_ACK_SET:B0 0x55(4)]
RX_ON issue
[RF_STATUS:B0 0x6C]
From RX flowchart
(≤256 byte)
No
RX completion (INT[18]/[19])?
[INT_SOURCE_GRP3:B0 0x26]
Yes
CRC error (INT[20]/INT[21])?
[INT_SOURCE_GRP3:B0 0x26]
Yes
No
Read RX data from FIFO
[RD_RX_FIFO:B0 0x7F]
Clear INT[20] or [21]
[INT_SOURCE_GRP3:B0 0x26]
PHY reset issue
[RST_SET:B0 0x01]
(*1)
Set ACK_STOP=0b1
[AUTO_ACK_SET:B0 0x55(0)]
Set ACK_STOP=0b0
[AUTO_ACK_SET:B0 0x55(0)]
END
Address match?
No
Yes
Read pending data
PHY reset issue
[RST_SET:B0 0x01]
When CCA_AUTO_EN=0b1,
([CCA_CNTRL:B0 0x15(7)])
executing CCA automatically.
(*1)
Set ACK_STOP=0b1
[AUTO_ACK_SET:B0 0x55(0)]
Set ACK_STOP=0b0
[AUTO_ACK_SET:B0 0x55(0)]
END
Ack frame setting
[ACK_FRAME1:B0 0x53]
[ACK_FRAME2:B0 0x54]
No
Auto Ack ready (INT[24])?
[INT_SOURCE_GRP4:B0 0x27]
Yes
Set ACK_SEND=0b1
[AUTO_ACK_SET:B0 0x55(1)]
When using Ack timer, no need
to set ACK_SEND bit.
No
TX completion?
(INT[16]/[17])
[INT_SOURCE_GRP3:B0 0x26]
Yes
Clear interrupts
INT[16],[22] or INT[17].[23]
[INT_SOURCE_GRP3:B0 0x26]
(*1)
Set ACK_STOP=0b1
[AUTO_ACK_SET:B0 0x55(0)]
Set ACK_STOP=0b0
[AUTO_ACK_SET:B0 0x55(0)]
END

(*1)
Only when data rate is 50kbps and SCLK speed is 16MHz (max), please set 12µs wait between ACK_STOP=0b1 to ACK_STOP=0b0.

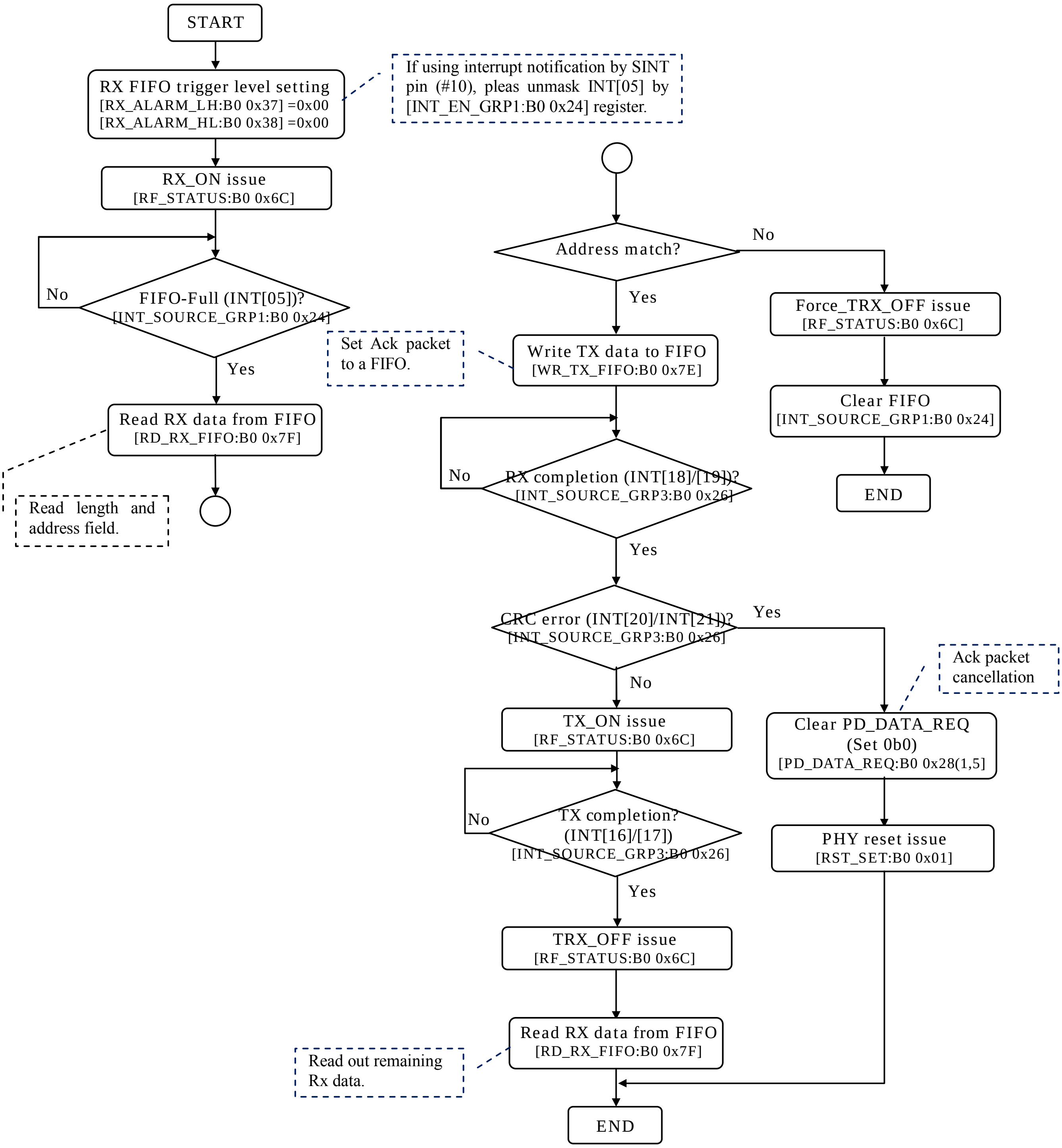
●ACK TX mode (AUTO_ACK, packet length ≥ 257 bytes)


START
Set AUTO_ACK_EN=0b1
[AUTO_ACK_SET:B0 0x55(4)]
RX FIFO trigger level setting
[RX_ALARM_LH:B0 0x37] =0x00
[RX_ALARM_HL:B0 0x38] =0x00
RX_ON issue
[RF_STATUS:B0 0x6C]
FIFO-Full (INT[05])?
[INT_SOURCE_GRP1:B0 0x24]
No
Yes
Read RX data from FIFO
[RD_RX_FIFO:B0 0x7F]
From RX flowchart (≥257 byte)
Address match?
No
Yes
Ack frame setting
[ACK_FRAME1:B0 0x53]
[ACK_FRAME2:B0 0x54]
PHY reset issue
[RST_SET:B0 0x01]
(*1)
Set ACK_STOP=0b1
[AUTO_ACK_SET:B0 0x55(0)]
Set ACK_STOP=0b0
[AUTO_ACK_SET:B0 0x55(0)]
END
RX completion?
(INT[18]/[19])
[INT_SOURCE_GRP3:B0 0x26]
No
Yes
CRC error (INT[20]/INT[21])?
[INT_SOURCE_GRP3:B0 0x26]
Yes
No
Read pending data
Clear INT[20] or [21]
[INT_SOURCE_GRP3:B0 0x26]
PHY reset issue
[RST_SET:B0 0x01]
(*1)
Set ACK_STOP=0b1
[AUTO_ACK_SET:B0 0x55(0)]
Set ACK_STOP=0b0
[AUTO_ACK_SET:B0 0x55(0)]
END
Auto Ack ready (INT[24])?
[INT_SOURCE_GRP4:B0 0x27]
No
Yes
Set ACK_SEND=0b1
[AUTO_ACK_SET:B0 0x55(1)]
When using Ack timer, no need to set ACK_SEND bit.
TX completion?
(INT[16]/[17])
[INT_SOURCE_GRP3:B0 0x26]
No
Yes
Clear interrupts
INT[16],[22] or INT[17].[23]
[INT_SOURCE_GRP3:B0 0x26]
(*1)
Set ACK_STOP=0b1
[AUTO_ACK_SET:B0 0x55(0)]
Set ACK_STOP=0b0
[AUTO_ACK_SET:B0 0x55(0)]
END

(*1)
Only when data rate is 50kbps and SCLK speed is 16MHz (max), please set 12μs wait between ACK_STOP=0b1 to ACK_STOP=0b0.

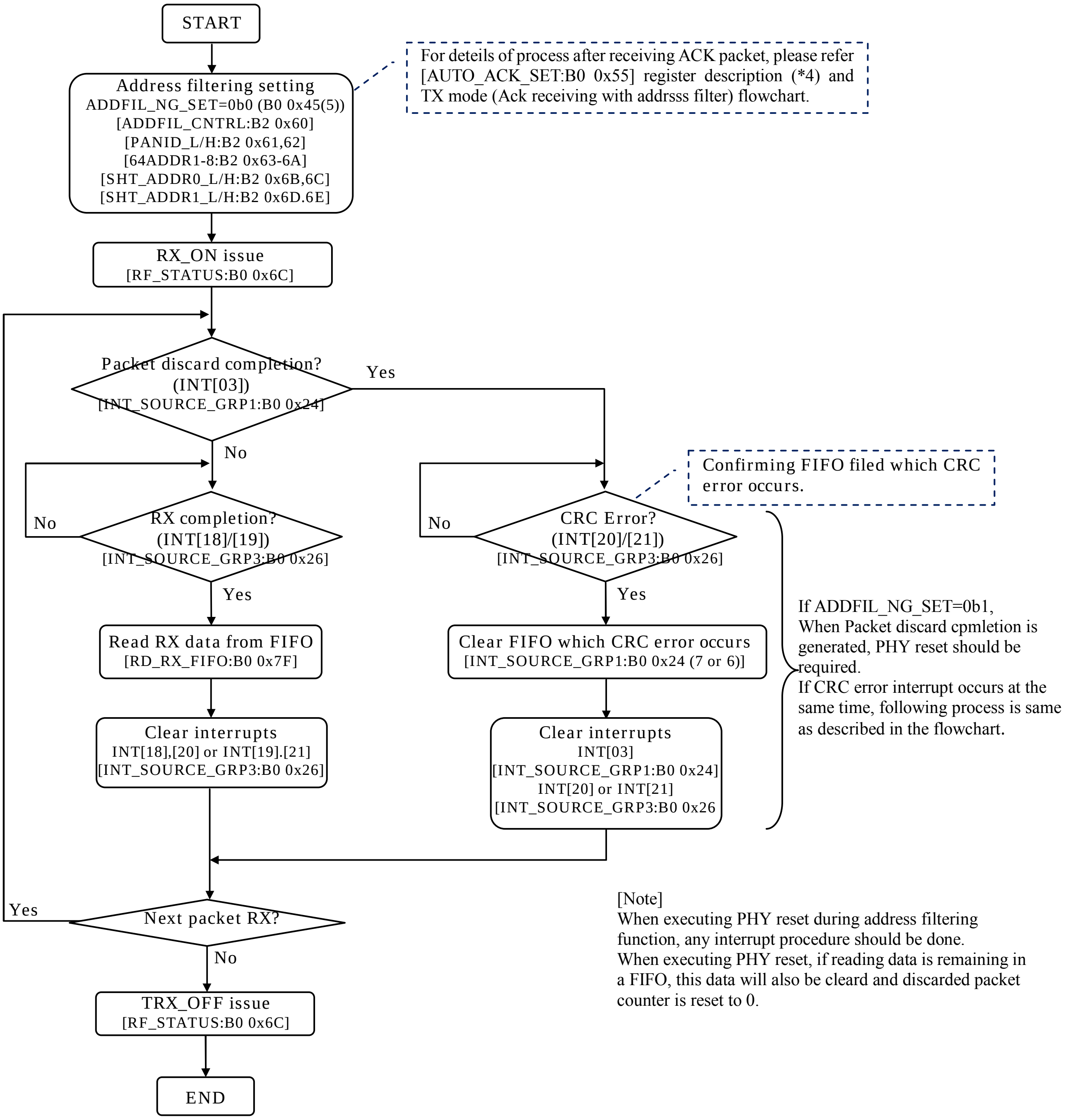
●ACK TX mode (without AUTO_ACK)

Below flowchart shows the Ack packet transmission without AUTO_AUK function. By using FIFO-Full interrupt (INT[05] gtoup1), the host MCU write Ack packet to a FIFO during RX. After RX completion, transmitting Ack paket.


START
RX FIFO trigger level setting
[RX_ALARM_LH:B0 0x37] =0x00
[RX_ALARM_HL:B0 0x38] =0x00
If using interrupt notification by SINT pin (#10), pleas unmask INT[05] by [INT_EN_GRP1:B0 0x24] register.
RX_ON issue
[RF_STATUS:B0 0x6C]
No
FIFO-Full (INT[05])?
[INT_SOURCE_GRP1:B0 0x24]
Yes
Read RX data from FIFO
[RD_RX_FIFO:B0 0x7F]
Read length and address field.
Address match?
No
Yes
Force_TRX_OFF issue
[RF_STATUS:B0 0x6C]
Set Ack packet to a FIFO.
Write TX data to FIFO
[WR_TX_FIFO:B0 0x7E]
Clear FIFO
[INT_SOURCE_GRP1:B0 0x24]
No
RX completion (INT[18]/[19])?
[INT_SOURCE_GRP3:B0 0x26]
END
Yes
CRC error (INT[20]/INT[21])?
[INT_SOURCE_GRP3:B0 0x26]
Yes
Ack packet cancellation
No
TX_ON issue
[RF_STATUS:B0 0x6C]
Clear PD_DATA_REQ
(Set 0b0)
[PD_DATA_REQ:B0 0x28(1,5]
No
TX completion?
(INT[16]/[17])
[INT_SOURCE_GRP3:B0 0x26]
PHY reset issue
[RST_SET:B0 0x01]
Yes
TRX_OFF issue
[RF_STATUS:B0 0x6C]
Read RX data from FIFO
[RD_RX_FIFO:B0 0x7F]
Read out remaining Rx data.
END

●Address Filter

When Address filtering function is enabled, if receiving packet which address field are mismatch, Packet discard completion interrupt (INT[03] group1) will be generated. At this time, if ADDFIL_NG_SET ([PACKET_MODE_SET:B0 0x45(5)]) =0b0, aborting packet data immediately after address mismatch detection and CRC error interrupt (INT[20]/[21] group3) is also generated at the same time. (The details of interrupt notifiaction, please refer to the [Interrupts timing when using INT_TIM_CTRL] in “Address filtering function”.) After notifying Packet discard completion interrupt and CRC error interrupt, it is need to clear FIFO by [INT_SOURCE_GRP1:B0 0x24] register or reading out data specified by Lngth field from the FIFO, in order to store next packet to right FIFO. After that, clearing Packet discard completion interrupt and CRC error interrupt, and then waiting next packet.

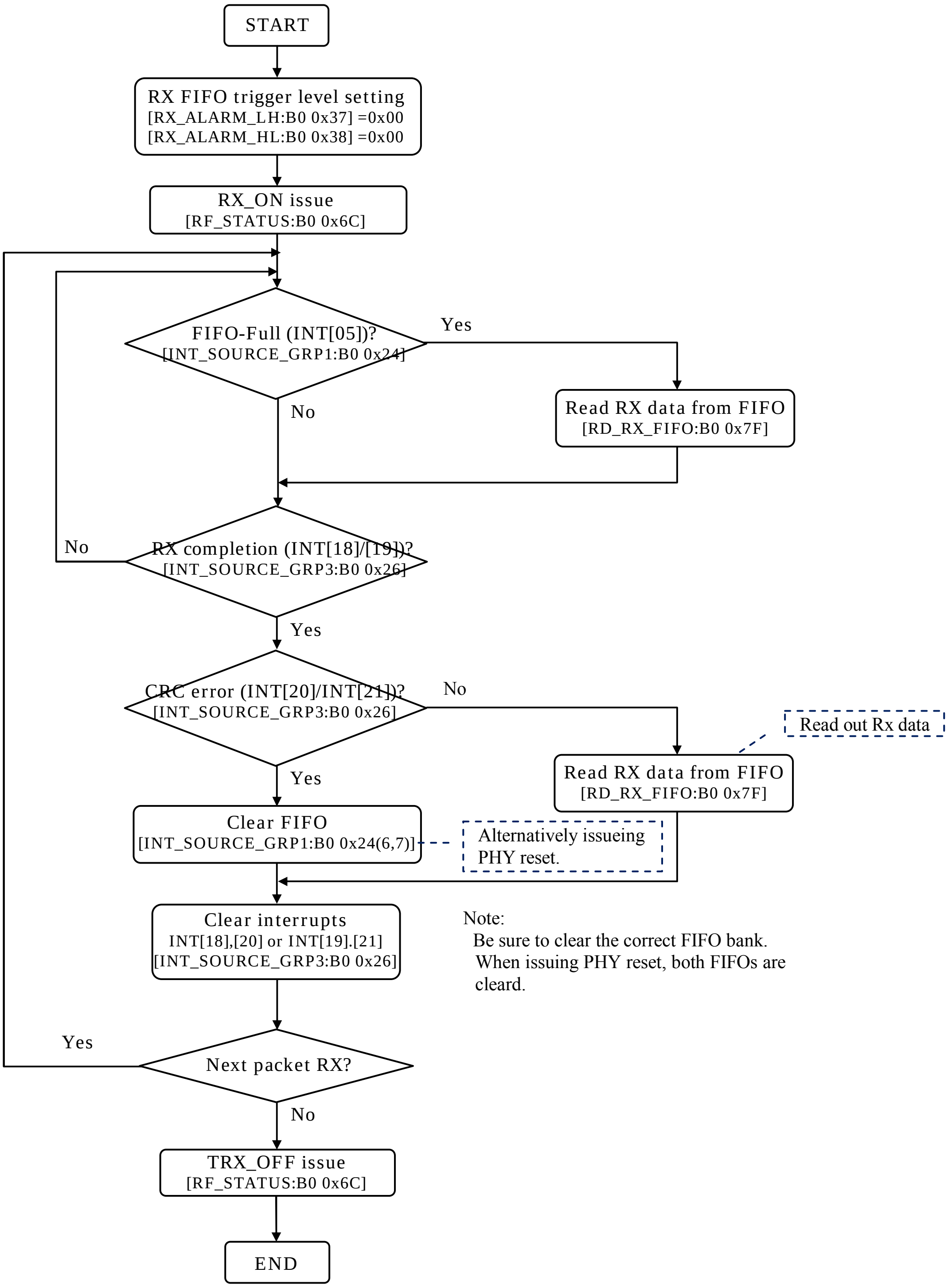

START
Address filtering setting
ADDFIL_NG_SET=0b0 (B0 0x45(5))
[ADDFIL_CNTRL:B2 0x60]
[PANID_L/H:B2 0x61,62]
[64ADDR1-8:B2 0x63-6A]
[SHT_ADDR0_L/H:B2 0x6B,6C]
[SHT_ADDR1_L/H:B2 0x6D.6E]
For deteils of process after receiving ACK packet, please refer [AUTO_ACK_SET:B0 0x55] register description (*4) and TX mode (Ack receiving with addrsss filter) flowchart.
RX_ON issue
[RF_STATUS:B0 0x6C]
Packet discard completion?
(INT[03])
[INT_SOURCE_GRP1:B0 0x24]
Yes
No
Confirming FIFO filed which CRC error occurs.
No
RX completion?
(INT[18]/[19])
[INT_SOURCE_GRP3:B0 0x26]
Yes
No
CRC Error?
(INT[20]/[21])
[INT_SOURCE_GRP3:B0 0x26]
Yes
Read RX data from FIFO
[RD_RX_FIFO:B0 0x7F]
Clear FIFO which CRC error occurs
[INT_SOURCE_GRP1:B0 0x24 (7 or 6)]
If ADDFIL_NG_SET=0b1,
When Packet discard cpmletion is generated, PHY reset should be required.
If CRC error interrupt occurs at the same time, following process is same as described in the flowchart.
Clear interrupts
INT[18],[20] or INT[19].[21]
[INT_SOURCE_GRP3:B0 0x26]
Clear interrupts
INT[03]
[INT_SOURCE_GRP1:B0 0x24]
INT[20] or INT[21]
[INT_SOURCE_GRP3:B0 0x26
Yes
Next packet RX?
No
TRX_OFF issue
[RF_STATUS:B0 0x6C]
END

[Note]
When executing PHY reset during address filtering function, any interrupt procedure should be done.
When executing PHY reset, if reading data is remaining in a FIFO, this data will also be cleard and discarded packet counter is reset to 0.

●FIFO Clear (Rx)

When RX completion interrupt (INT[18]/[19] group3) and CRC error interrupt (INT[20]/[21] group 3) is notified in the same time, clearing FIFO by set 0b0 to FIFO_CLR0/1 ([INT_SOURCE_GRP1:B0 0x24(6/7)]) if no need to read remaining RX data. And then clearing RX completion interript and CRC error interrupt.

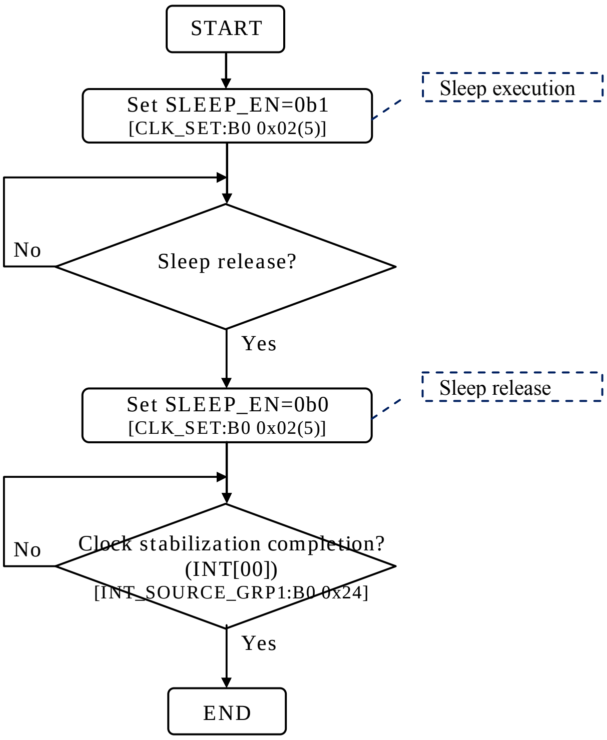
If receiving next packet, keeping RX_ON state. If terminating RX_ON state, please issueing TRX_OFF command by [RF_STATUS:B0 0x6C] register. Be sure to clear the correct FIFO bank only. Alternatively, FIFO can be cleared by issueing PHY reset by using [RST_SET:B0 0x01] register.


START
RX FIFO trigger level setting
[RX_ALARM_LH:B0 0x37] =0x00
[RX_ALARM_HL:B0 0x38] =0x00
RX_ON issue
[RF_STATUS:B0 0x6C]
FIFO-Full (INT[05])?
[INT_SOURCE_GRP1:B0 0x24]
Yes
No
Read RX data from FIFO
[RD_RX_FIFO:B0 0x7F]
No
RX completion (INT[18]/[19])?
[INT_SOURCE_GRP3:B0 0x26]
Yes
CRC error (INT[20]/INT[21])?
[INT_SOURCE_GRP3:B0 0x26]
No
Read out Rx data
Read RX data from FIFO
[RD_RX_FIFO:B0 0x7F]
Yes
Clear FIFO
[INT_SOURCE_GRP1:B0 0x24(6,7)]
Alternatively issueing PHY reset.
Clear interrupts
INT[18],[20] or INT[19].[21]
[INT_SOURCE_GRP3:B0 0x26]
Yes
Next packet RX?
No
TRX_OFF issue
[RF_STATUS:B0 0x6C]
END

Note:
Be sure to clear the correct FIFO bank.
When issuing PHY reset, both FIFOs are cleard.

●SLEEP

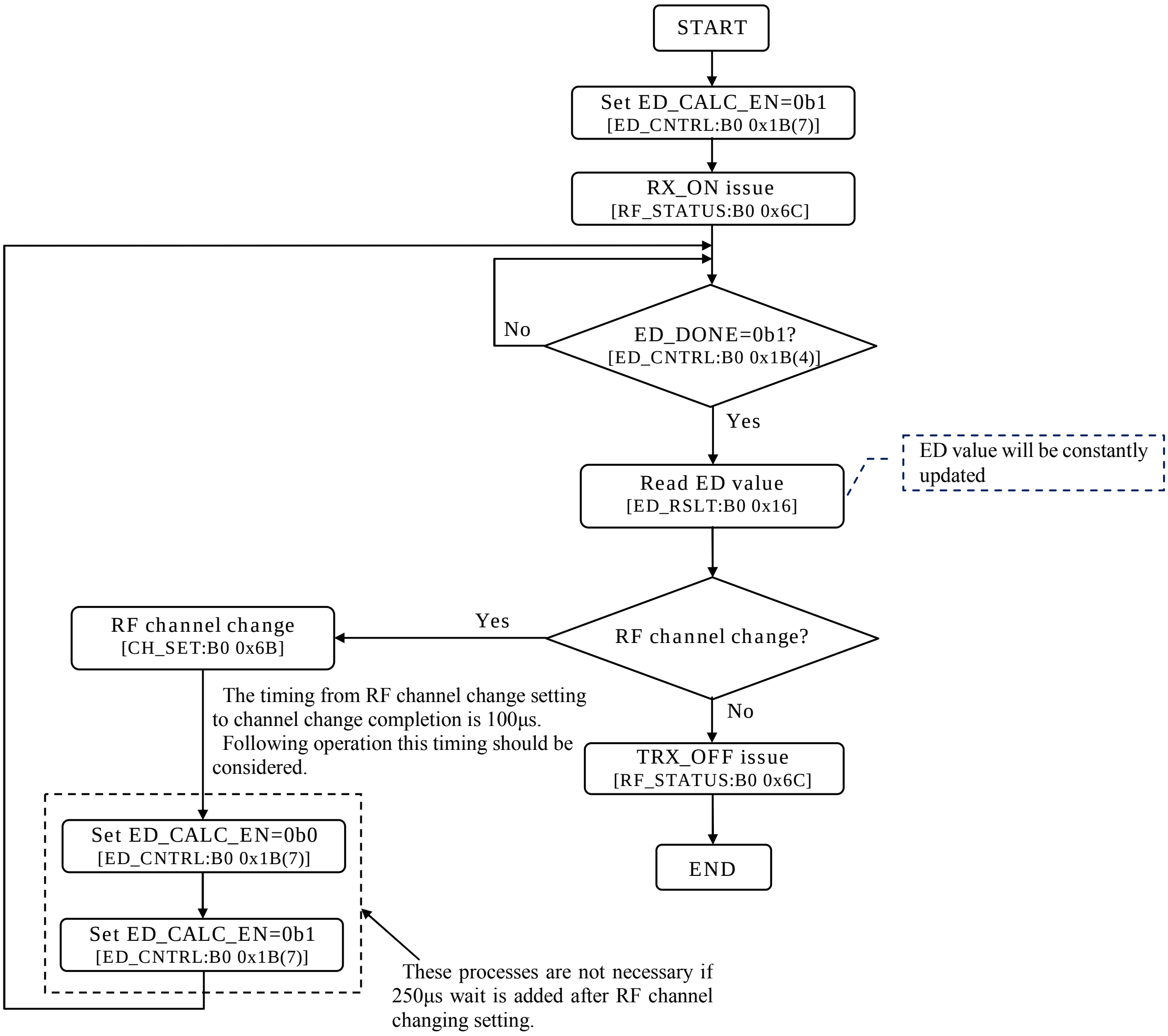
Set 0b1 to SLEEP_EN ([CLK_SET:B0 0x02(5)]) in order to enter into SLEEP state. SLEEP state can be released by setting SLEEP_EN=0b0.


START
Set SLEEP_EN=0b1
[CLK_SET:B0 0x02(5)]
Sleep execution
No
Sleep release?
Yes
Set SLEEP_EN=0b0
[CLK_SET:B0 0x02(5)]
Sleep release
No
Clock stabilization completion?
(INT[00])
[INT_SOURCE_GRP1:B0 0x24]
Yes
END

●ED Scan

ED value will be automatically acquired by issuing RX_ON by [RF_STATUS:B0 0x6C] register after setting ED_CALC_EN [ED_CNTRL:B0 0x1B(7)]) =0b1. ED values is constantly updated when ED_CALC_EN=0b1 during RX_ON state.

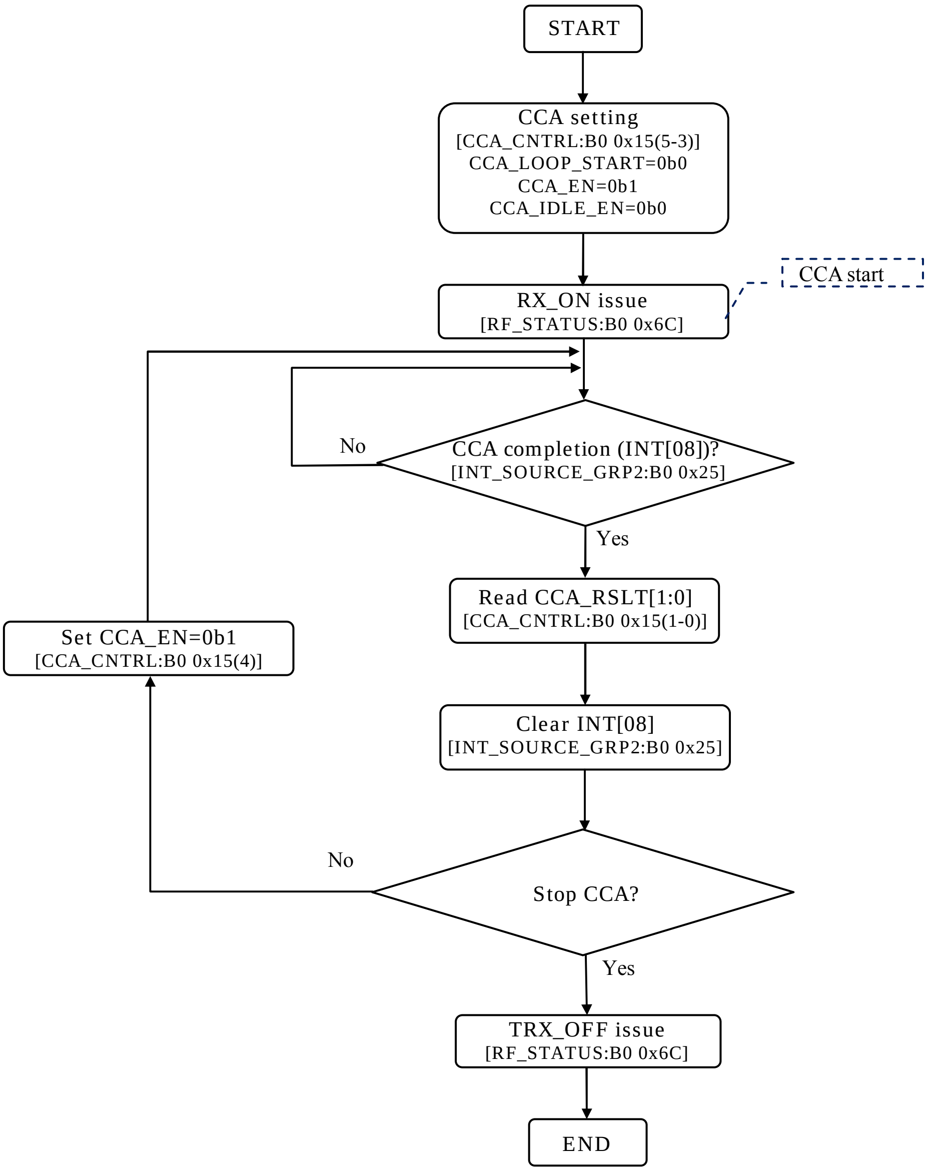
When changing RF channel, once set ED_CALC_EN=0b0 and set 0b1 again after RF channel change completion. Except for RF channel change, please do not set 0b0 to ED_CALC_EN bit.


START
Set ED_CALC_EN=0b1
[ED_CNTRL:B0 0x1B(7)]
RX_ON issue
[RF_STATUS:B0 0x6C]
No
ED_DONE=0b1?
[ED_CNTRL:B0 0x1B(4)]
Yes
ED value will be constantly updated
Read ED value
[ED_RSLT:B0 0x16]
RF channel change
[CH_SET:B0 0x6B]
Yes
RF channel change?
No
The timing from RF channel change setting to channel change completion is 100µs.
Following operation this timing should be considered.
TRX_OFF issue
[RF_STATUS:B0 0x6C]
Set ED_CALC_EN=0b0
[ED_CNTRL:B0 0x1B(7)]
END
Set ED_CALC_EN=0b1
[ED_CNTRL:B0 0x1B(7)]
These processes are not necessary if 250µs wait is added after RF channel changing setting.

- CCA operation

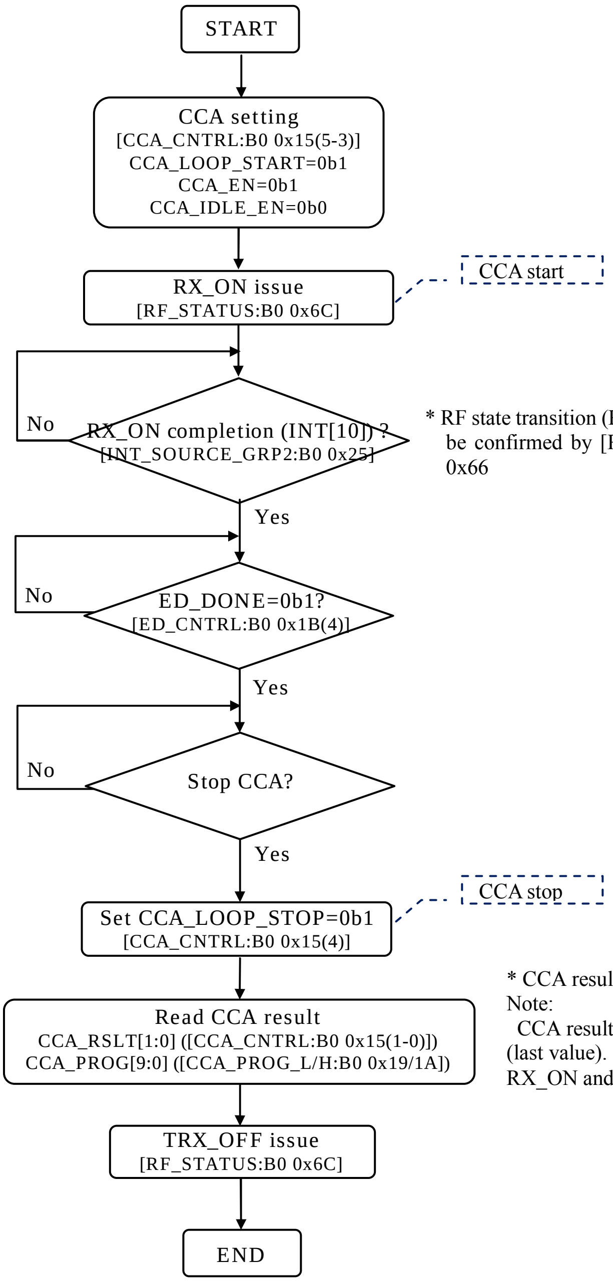
  - Normal mode

CCA normal mode will be executed by issueing RX_ON by [RF_STATUS:B0 0x6C] register after setting CCA_EN ([CCA_CNTRL:B0 0x15(4)])=0b1, CCA_IDLE_EN ([CCA_CNTRL:B0 0x15(3)])=0b0 and CCA_LOOP_START ([CCA_CNTRL:B0 0x15(5)])=0b0. Compariing acquired ED average value with CCA threshold value in [CCA_LEVEL:B0 0x13] register and notice the result. After CCA execution, CCA_EN is turned disabled, and RF maintains RX_ON state.
Even if set CCA_EN=0b1 during RX_ON state, CCA can be performed by. However, in this case, 16µs - 32µs (2 cycle of A/D conversion) WAIT is automatically added as the filter stabilization period before CCA execution. (If CCA_EN=0b1 is set before issuing RX_ON, WAIT is not added because filter stabilization period is included in RF transition period.)
If bit synchronization is detected during CCA, keep receiving with wider BPF bandwidth for CCA operation. If CCA is executed after bit synchronization detection, CCA is executed with normal BPF bandwidth.
CCA execution is also possible during diversity search. In this case, after CCA completion diversity search will be resumed automatically.


START
CCA setting
[CCA_CNTRL:B0 0x15(5-3)]
CCA_LOOP_START=0b0
CCA_EN=0b1
CCA_IDLE_EN=0b0
CCA start
RX_ON issue
[RF_STATUS:B0 0x6C]
No
CCA completion (INT[08])?
[INT_SOURCE_GRP2:B0 0x25]
Yes
Read CCA_RSLT[1:0]
[CCA_CNTRL:B0 0x15(1-0)]
Set CCA_EN=0b1
[CCA_CNTRL:B0 0x15(4)]
Clear INT[08]
[INT_SOURCE_GRP2:B0 0x25]
No
Stop CCA?
Yes
TRX_OFF issue
[RF_STATUS:B0 0x6C]
END

- Continuous mode

CCA continuous mode will be executed by issueing RX_ON by [RF_STATUS:B0 0x6C] register after setting CCA_EN ([CCA_CNTRL:B0 0x15(4)])=0b1, CCA_IDLE_EN ([CCA_CNTRL:B0 0x15(3)])=0b0 and CCA_LOOP_START ([CCA_CNTRL:B0 0x15(5)])=0b1. In this mode, CCA continues until CCA_LOOP_STOP ([CCA_CNTRL:B0 0x15(6)]) =0b1 is set. In this mode, CCA_DONE ([CCA_CNTRL: B0 0x15(2)]) will not be 0b1 and CCA completion interrupt (INT[08] group2) is not generated. During CCA execution, CCA_RSLT[1:0] ([CCA_CNTRL:B0 0x15(1-0)]) and CCA_PROG[9:0] ([CCA_PROG_L/H:B0 0x19(7-0)/1A(1-0)]) are constantly updated. The value will be kept by setting CCA_LOOP_STOP=0b1.

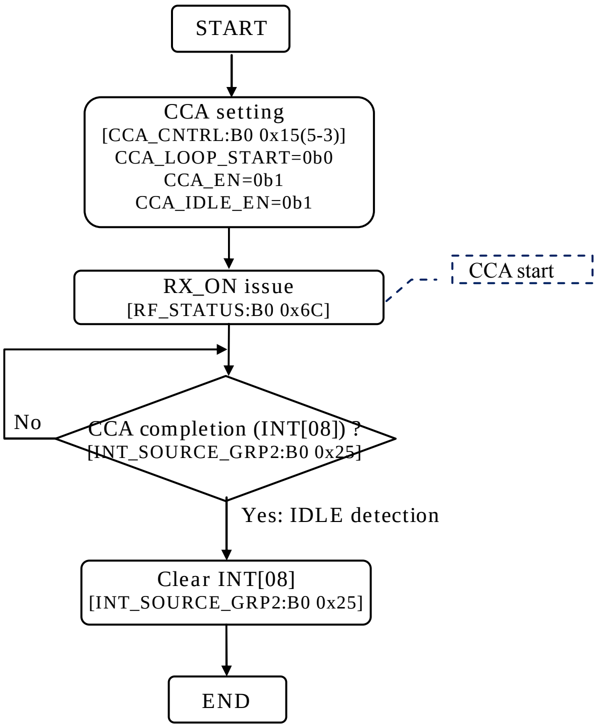

START
CCA setting
[CCA_CNTRL:B0 0x15(5-3)]
CCA_LOOP_START=0b1
CCA_EN=0b1
CCA_IDLE_EN=0b0
RX_ON issue
[RF_STATUS:B0 0x6C]
CCA start
No
RX_ON completion (INT[10]) ?
[INT_SOURCE_GRP2:B0 0x25]
Yes
No
ED_DONE=0b1?
[ED_CNTRL:B0 0x1B(4)]
Yes
No
Stop CCA?
Yes
Set CCA_LOOP_STOP=0b1
[CCA_CNTRL:B0 0x15(4)]
CCA stop
Read CCA result
CCA_RSLT[1:0] ([CCA_CNTRL:B0 0x15(1-0)])
CCA_PROG[9:0] ([CCA_PROG_L/H:B0 0x19/1A])
TRX_OFF issue
[RF_STATUS:B0 0x6C]
END

* RF state transition (RX_ON) completion can be confirmed by [RF_STATU:B0 0x0B] = 0x66

* CCA result can be read during CCA.
Note:
CCA results before RX_ON are invalid. (last value). Please read the valu after RX_ON and ED_DONE=0b1.

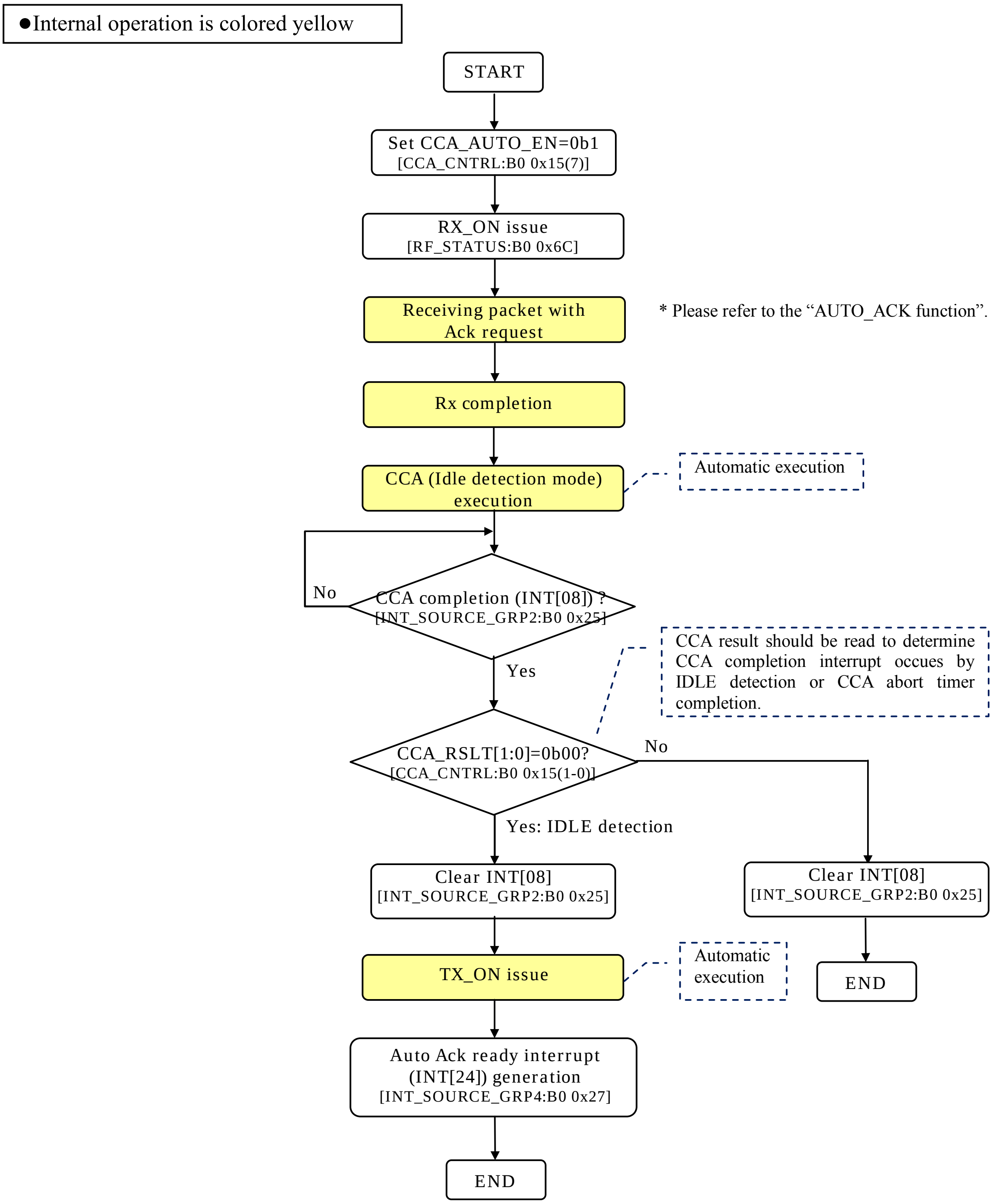
●IDLE detection mode

CCA is continuously executed until IDLE is detected. CCA (IDLE detection mode) will be executing by setting RX_ON by [RF_STATUS:B0 0x6C] register after setting CCA_EN ([CCA_CNTRL:B0 0x15(4)])=0b1, CCA_IDLE_EN ([CCA_CNTRL:B0 0x15(3)])=0b1 and CCA_LOOP_START ([CCA_CNTRL:B0 0x15(5)])=0b0..

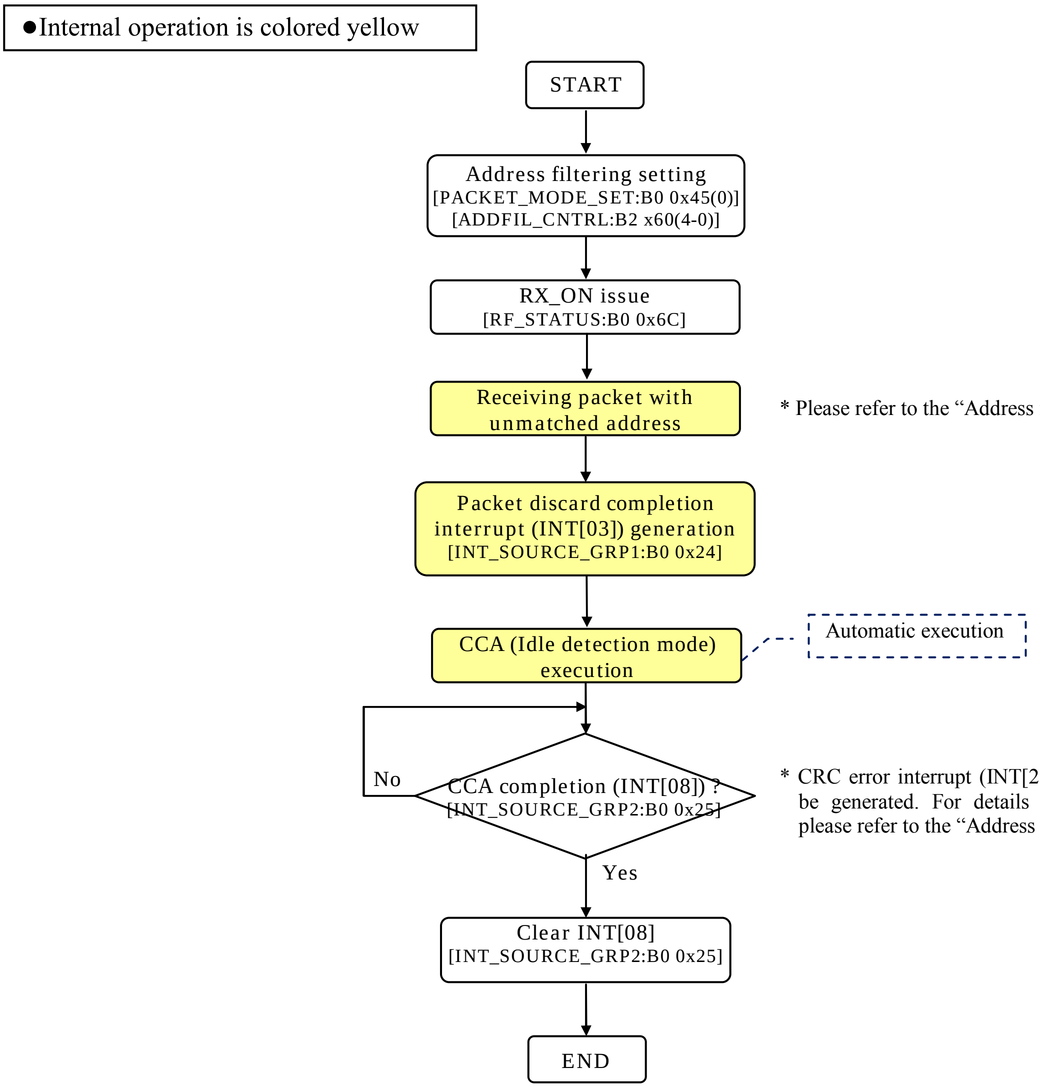

START
CCA setting
[CCA_CNTRL:B0 0x15(5-3)]
CCA_LOOP_START=0b0
CCA_EN=0b1
CCA_IDLE_EN=0b1
RX_ON issue
[RF_STATUS:B0 0x6C]
CCA start
No
CCA completion (INT[08]) ?
[INT_SOURCE_GRP2:B0 0x25]
Yes: IDLE detection
Clear INT[08]
[INT_SOURCE_GRP2:B0 0x25]
END

In the below condition, CCA (IDLE detection mode) will be executed automatically.

1. When set 0b1 to ting CCA_AUTO_EN ([CCA_CNTRL:B0 0x15(7)]), CCA (IDLE detection mode) will be executed after receiving Ack request packet.


●Internal operation is colored yellow
START
Set CCA_AUTO_EN=0b1
[CCA_CNTRL:B0 0x15(7)]
RX_ON issue
[RF_STATUS:B0 0x6C]
Receiving packet with Ack request
* Please refer to the "AUTO_ACK function".
Rx completion
CCA (Idle detection mode) execution
Automatic execution
No
CCA completion (INT[08]) ?
[INT_SOURCE_GRP2:B0 0x25]
Yes
CCA result should be read to determine CCA completion interrupt occues by IDLE detection or CCA abort timer completion.
CCA_RSLT[1:0]=0b00?
[CCA_CNTRL:B0 0x15(1-0)]
No
Yes: IDLE detection
Clear INT[08]
[INT_SOURCE_GRP2:B0 0x25]
Clear INT[08]
[INT_SOURCE_GRP2:B0 0x25]
TX_ON issue
Automatic execution
END
Auto Ack ready interrupt (INT[24]) generation
[INT_SOURCE_GRP4:B0 0x27]
END

2. When Address Filtering function is enabled by set 0b1 to one of bit4-0 in [ADDFIL_CNTRL:B2 0x60] register, and if ADDFIL_IDLE_DET ([PACKET_MODE_SET:B0 0x45(0)]) =0b1, CCA (IDLE detection mode) will be executed after discardingRx data.


●Internal operation is colored yellow
START
Address filtering setting
[PACKET_MODE_SET:B0 0x45(0)]
[ADDFIL_CNTRL:B2 x60(4-0)]
RX_ON issue
[RF_STATUS:B0 0x6C]
Receiving packet with unmatched address
Packet discard completion interrupt (INT[03]) generation
[INT_SOURCE_GRP1:B0 0x24]
CCA (Idle detection mode) execution
Automatic execution
CCA completion (INT[08]) ?
[INT_SOURCE_GRP2:B0 0x25]
No
Yes
Clear INT[08]
[INT_SOURCE_GRP2:B0 0x25]
END

* Please refer to the “Address filtering function”

* CRC error interrupt (INT[20]/[21] group3) may be generated. For details of interrupt timing, please refer to the “Address filtering function”.

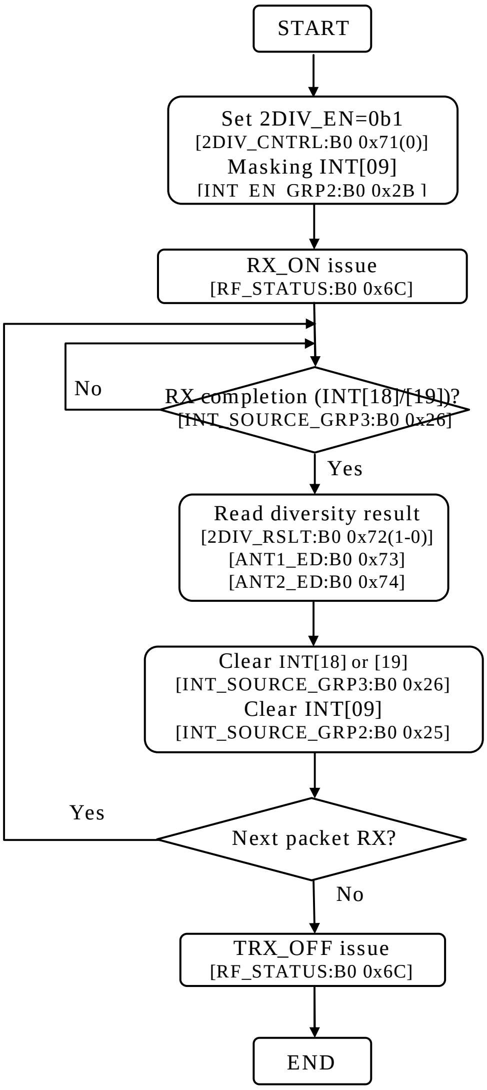
●2 diversity operation

After setting 2DIV_EN ([2DIV_CNTRL: B0 0x71(0)])=0b1, issuing RX_ON by [RF_STATUS:B0 0x6C] register. Antennas are switched to acquire each ED value, the antenna with higher ED value will be automatically selected.

ML7396 supports recovering function from incorrect diversity completion caused by errornous detection due to thermal noize, After dicersity search completion, if preamble can not be detected until antenna search timer expiration, ML7396 judges the previous diversity search completion is incorrect and resume diversity operation automatically.

When resume diversity operation for next packet receiving, please clear RX completion interrupt (INT[18]/[19] group3) and Diversity search completion interrupt (INT[09] group2). For details, please refer to “Diversity function”.

ED values ([ANT1_ED:B0 0x73], [ANT2_ED:B0 0x74] registers) from diversityantennas and the diversity result ([2DIV_RSLT:B0 0x72(1-0)]) will be cleard when clearing Diversity search completion interrpy, clearing RX completion or Diversity resume by errornous detection. ED values and diversity result should be read before clearing RX completion interrupt.


START
Set 2DIV_EN=0b1
[2DIV_CNTRL:B0 0x71(0)]
Masking INT[09]
[INT_EN_GRP2:B0 0x2B]
RX_ON issue
[RF_STATUS:B0 0x6C]
No
RX completion (INT[18]/[19])?
[INT_SOURCE_GRP3:B0 0x26]
Yes
Read diversity result
[2DIV_RSLT:B0 0x72(1-0)]
[ANT1_ED:B0 0x73]
[ANT2_ED:B0 0x74]
Clear INT[18] or [19]
[INT_SOURCE_GRP3:B0 0x26]
Clear INT[09]
[INT_SOURCE_GRP2:B0 0x25]
Yes
Next packet RX?
No
TRX_OFF issue
[RF_STATUS:B0 0x6C]
END

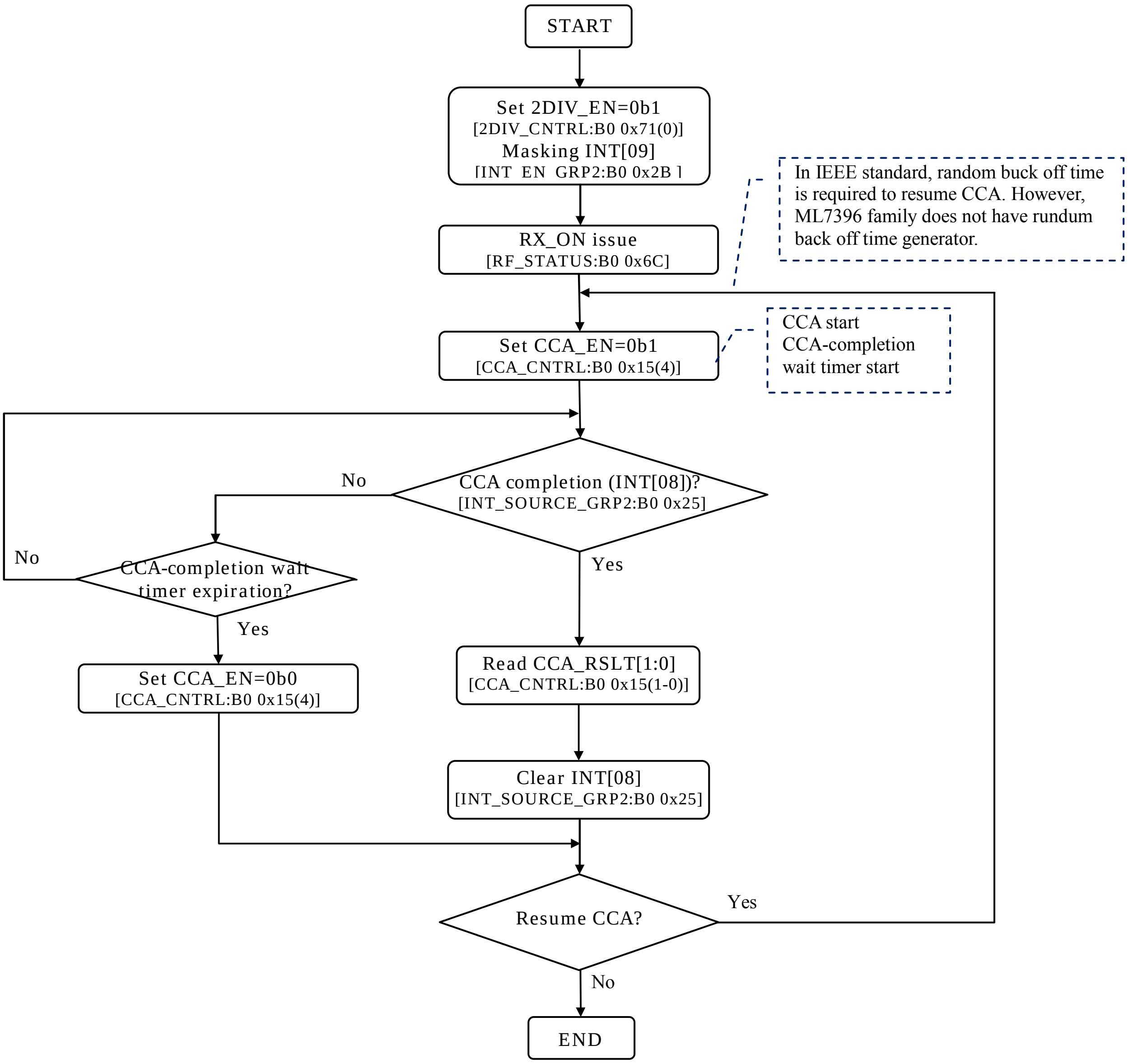
* If set 2DIV_EN=0b1 after issuing RX_ON, diversity will be executed after search timer completion defined by [2DIV_SEARCH:B0 0x6F] register.
If SFD is detected while seatch timer counting, diversity will not be executed and keep receiving.

* Diversity search completion interrupt (INT[09] group2) should be cleard at same timing of RX completion interrupt clearance.

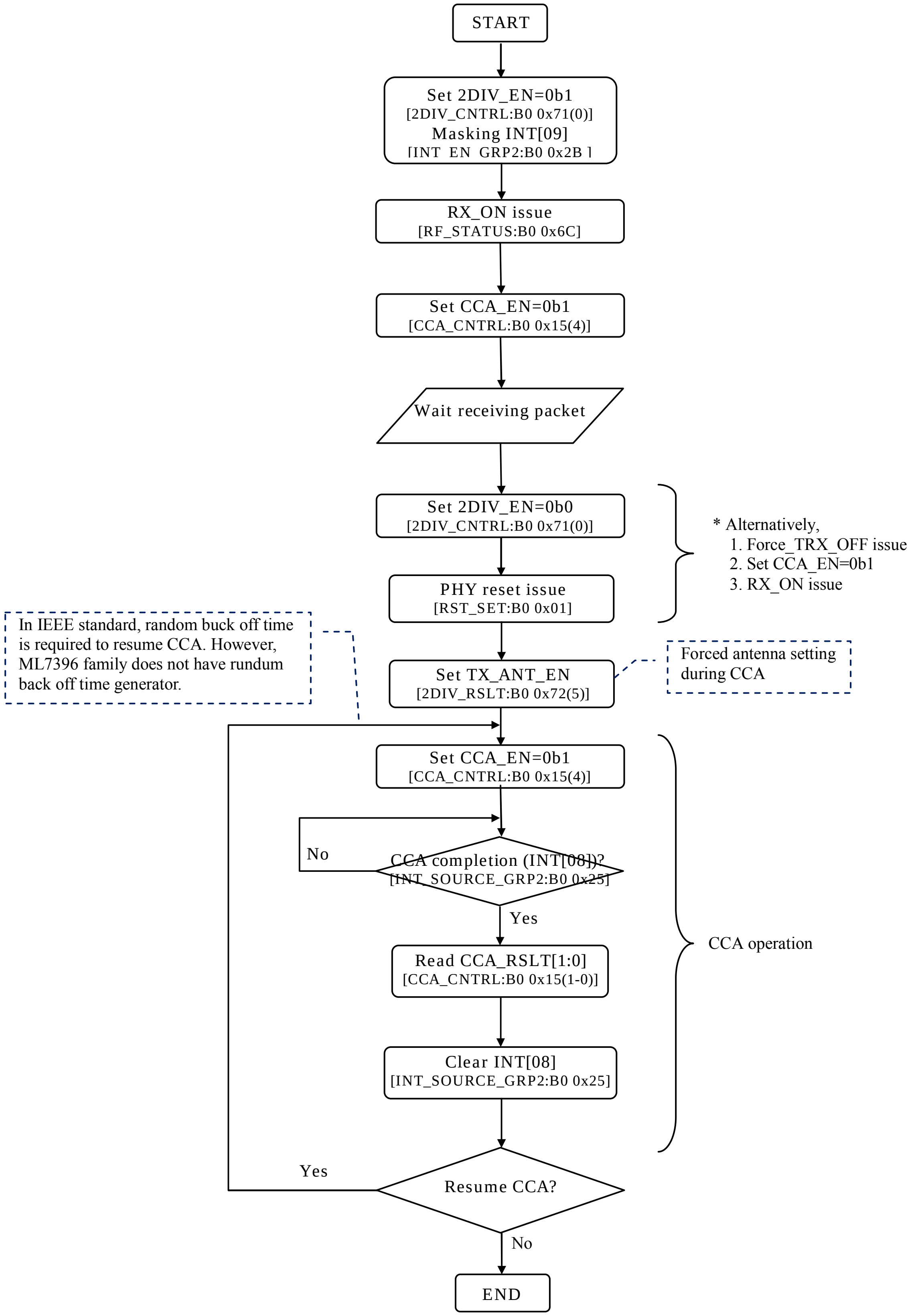
- CCA operation during diversity

If CCA is executed during diversity operation, there is a case CCA_DONE ([CCA_CNTRL:B0 0x15(2)]) is not notified and keep CCA operation. When executing CCA during diversity, set CCA-competion wait timer (case1), or once disabling diversity before CCA execution (case 2).

Case 1: Set CCA completion wait timer


START
Set 2DIV_EN=0b1
[2DIV_CNTRL:B0 0x71(0)]
Masking INT[09]
[INT_EN_GRP2:B0 0x2B]
RX_ON issue
[RF_STATUS:B0 0x6C]
In IEEE standard, random buck off time is required to resume CCA. However, ML7396 family does not have rundum back off time generator.
Set CCA_EN=0b1
[CCA_CNTRL:B0 0x15(4)]
CCA start
CCA-completion wait timer start
CCA completion (INT[08])?
[INT_SOURCE_GRP2:B0 0x25]
No
Yes
CCA-completion wait timer expiration?
No
Yes
Set CCA_EN=0b0
[CCA_CNTRL:B0 0x15(4)]
Read CCA_RSLT[1:0]
[CCA_CNTRL:B0 0x15(1-0)]
Clear INT[08]
[INT_SOURCE_GRP2:B0 0x25]
Resume CCA?
Yes
No
END

Case 2: Disbleing diversity before CCA execution


START
Set 2DIV_EN=0b1
[2DIV_CNTRL:B0 0x71(0)]
Masking INT[09]
[INT_EN_GRP2:B0 0x2B]
RX_ON issue
[RF_STATUS:B0 0x6C]
Set CCA_EN=0b1
[CCA_CNTRL:B0 0x15(4)]
Wait receiving packet
Set 2DIV_EN=0b0
[2DIV_CNTRL:B0 0x71(0)]
PHY reset issue
[RST_SET:B0 0x01]
* Alternatively,
1. Force_TRX_OFF issue
2. Set CCA_EN=0b1
3. RX_ON issue
In IEEE standard, random buck off time is required to resume CCA. However, ML7396 family does not have rundum back off time generator.
Set TX_ANT_EN
[2DIV_RSLT:B0 0x72(5)]
Forced antenna setting during CCA
Set CCA_EN=0b1
[CCA_CNTRL:B0 0x15(4)]
No
CCA completion (INT[08])?
[INT_SOURCE_GRP2:B0 0x25]
Yes
Read CCA_RSLT[1:0]
[CCA_CNTRL:B0 0x15(1-0)]
CCA operation
Clear INT[08]
[INT_SOURCE_GRP2:B0 0x25]
Yes
Resume CCA?
No
END

●Error process

●CRC Error

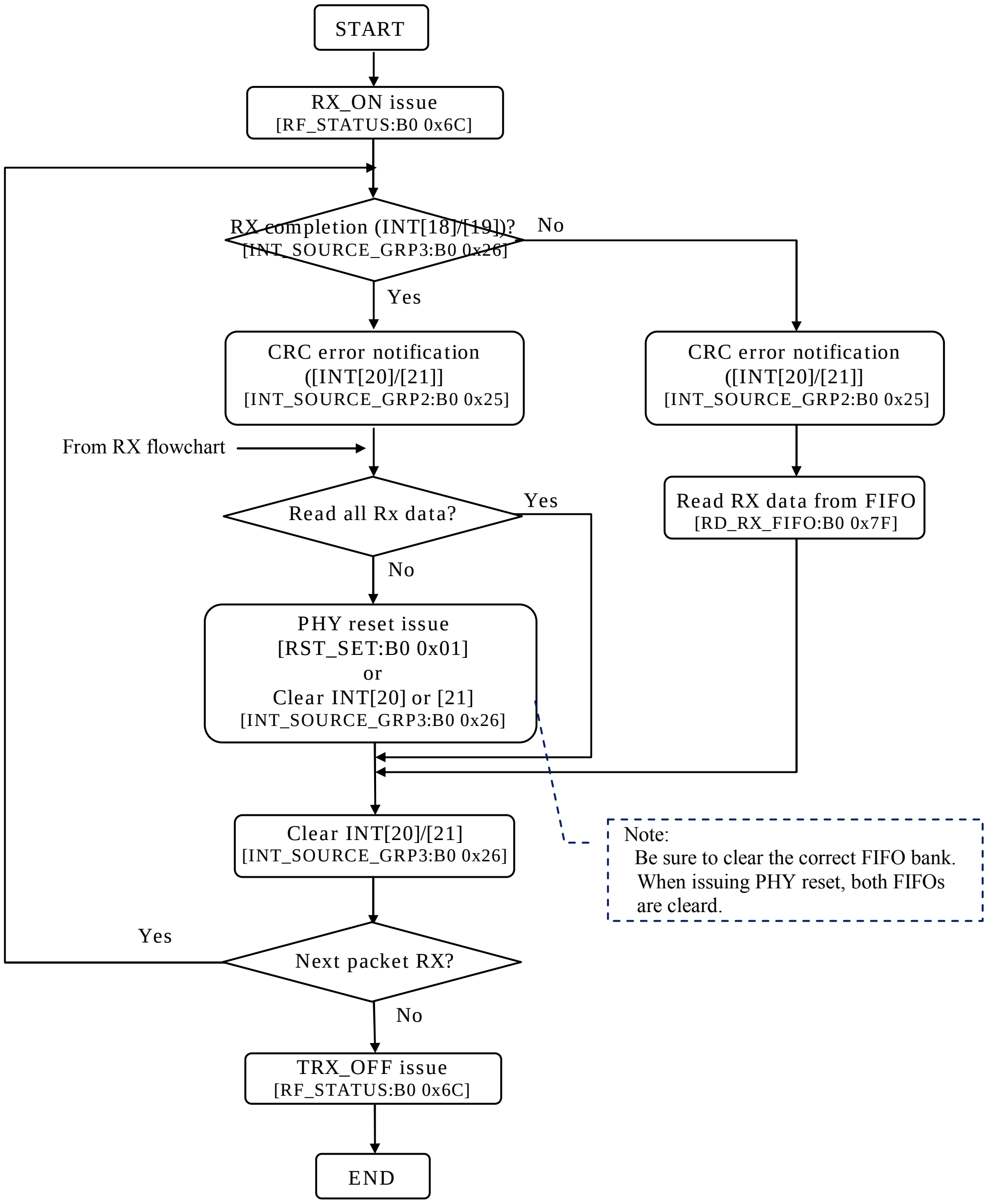
Case 1: CRC error occurs due to bit error

If CRC error occurs due to bit error, no need to read out Rx data from FIFO. By issuing PHY reset by [RST_SET:B0 0x01] register or FIFO clear by [INT_SOURCE_GRP1:B0 0x24] register, receiving status can be maintained.

For details of FIFO clear, please refer to "FIFO clear" in "Flow Charts".

Case 2: Out-of-sync detection after SFD detection (During Length, Data, CRC field receiving)

If out-of-syn is detected after SFD detection, CRC error interrupt (INT[20]/[21] group3) will be notified. However RX completion interrput (INT[18]/[19] group3) will not be generated. If this case occurs, read Rx data that amount is specified Length field from FIFO and then clearing CRC error interrpt.


START
RX_ON issue
[RF_STATUS:B0 0x6C]
RX completion (INT[18]/[19])?
[INT_SOURCE_GRP3:B0 0x26]
No
Yes
CRC error notification
([INT[20]/[21]]
[INT_SOURCE_GRP2:B0 0x25]
CRC error notification
([INT[20]/[21]]
[INT_SOURCE_GRP2:B0 0x25]
From RX flowchart
Read all Rx data?
Yes
No
Read RX data from FIFO
[RD_RX_FIFO:B0 0x7F]
PHY reset issue
[RST_SET:B0 0x01]
or
Clear INT[20] or [21]
[INT_SOURCE_GRP3:B0 0x26]
Clear INT[20]/[21]
[INT_SOURCE_GRP3:B0 0x26]
Note:
Be sure to clear the correct FIFO bank.
When issuing PHY reset, both FIFOs are cleard.
Yes
Next packet RX?
No
TRX_OFF issue
[RF_STATUS:B0 0x6C]
END

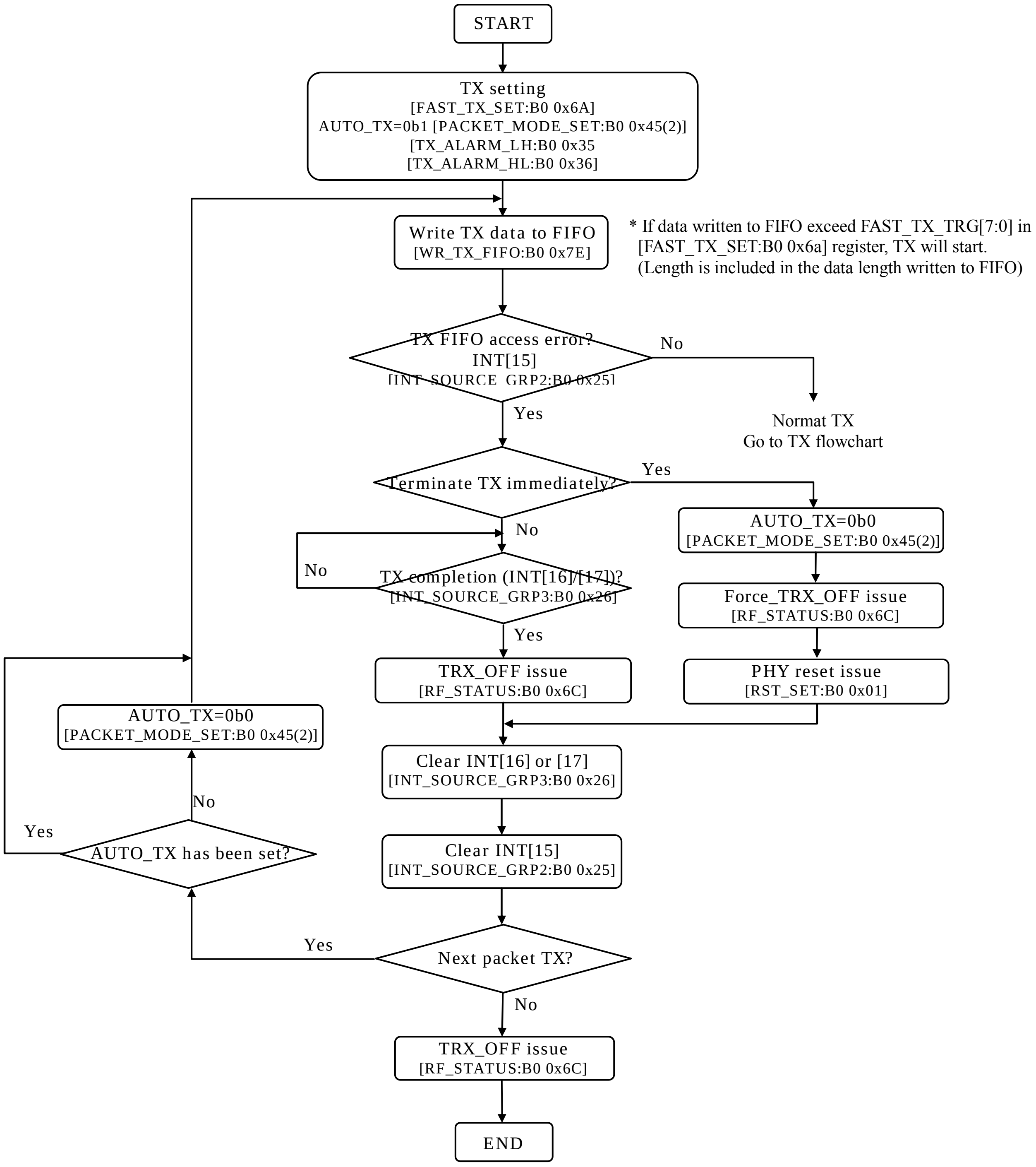
●TX FIFO Access Error

If one of the following conditions is met, TX FIFO access error interrupt (INT[15] group2) will be generated.

- The 3rd packet data is written to a FIFO when the transmitting data remain in both FIFO0 and FIFO1.
- Data write overflow occurs to a FIFO.
- No TX data in the TX_FIFO during TX data transimission.

When TX FIFO acccess error interrupt occurs, issuing TRX_OFF after TX completion interrupt(INT[16]/[17] group3) is recognized, or issueing Force_TRX_OFF by [RF_STATUS:B0 0x0A] register without waiting for TX completion interrupt. After that, clearing TX completion interrupt and TX FIFO access error interrrput..

If TX FIFO access error occurs, subquent TX data will be inverted. CRC error should be detected at rexeiver side even if TRX_OFF is issued when TX completion interrupt detected.


START
TX setting
[FAST_TX_SET:B0 0x6A]
AUTO_TX=0b1 [PACKET_MODE_SET:B0 0x45(2)]
[TX_ALARM_LH:B0 0x35
[TX_ALARM_HL:B0 0x36]
Write TX data to FIFO
[WR_TX_FIFO:B0 0x7E]
TX FIFO access error?
INT[15]
[INT_SOURCE_GRP2:B0 0x25]
No
Normat TX
Go to TX flowchart
Yes
Terminate TX immediately?
Yes
AUTO_TX=0b0
[PACKET_MODE_SET:B0 0x45(2)]
Force_TRX_OFF issue
[RF_STATUS:B0 0x6C]
PHY reset issue
[RST_SET:B0 0x01]
No
No
TX completion (INT[16]/[17])?
[INT_SOURCE_GRP3:B0 0x26]
Yes
TRX_OFF issue
[RF_STATUS:B0 0x6C]
AUTO_TX=0b0
[PACKET_MODE_SET:B0 0x45(2)]
No
Yes
AUTO_TX has been set?
Clear INT[16] or [17]
[INT_SOURCE_GRP3:B0 0x26]
Clear INT[15]
[INT_SOURCE_GRP2:B0 0x25]
Yes
Next packet TX?
No
TRX_OFF issue
[RF_STATUS:B0 0x6C]
END

* If data written to FIFO exceed FAST_TX_TRG[7:0] in [FAST_TX_SET:B0 0x6a] register, TX will start. (Length is included in the data length written to FIFO)

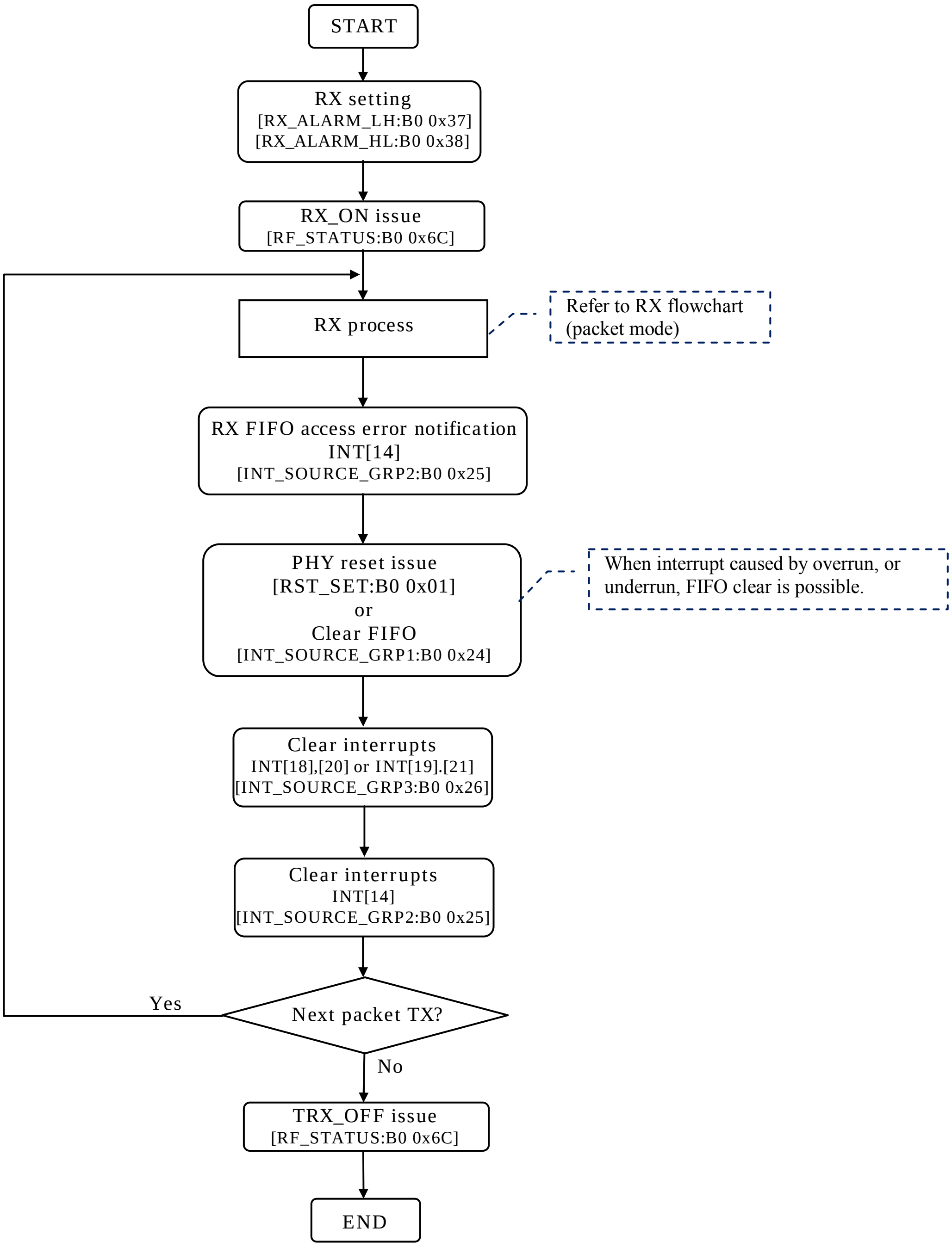
●RX FIFO Access Error

If one of the following conditions is met, RX FIFO access error interrupt (INT[14] group2) will be generated.

- ● Receiving the 3rd packet when the receiving data remain in both FIFO0 and FIFO1.
- ● RX data overflow occurs to RX_FIFO (Overrun)
- ● Read RX_FIFO during no data in the RX_FIFO (Underrun)

When RX FIFO access error interrupt occurs, after RX completion interrupt (INT[18]/[19] group3) is recognized, issuing PHY reset by [RST_SET:B0 0x01] register or FIFO clear by [INT_SOURCE_GRP1:B0 0x24] register. After that, clearing RX completion interrupt and RX FIFO access error interrupt.

After receiving 2 packets, by setting CLK1_EN ([CLK_SET:B0 0x02(1)] = 0b0, RX FIFO access error can be avoid.


START
RX setting
[RX_ALARM_LH:B0 0x37]
[RX_ALARM_HL:B0 0x38]
RX_ON issue
[RF_STATUS:B0 0x6C]
RX process
Refer to RX flowchart (packet mode)
RX FIFO access error notification
INT[14]
[INT_SOURCE_GRP2:B0 0x25]
PHY reset issue
[RST_SET:B0 0x01]
or
Clear FIFO
[INT_SOURCE_GRP1:B0 0x24]
When interrupt caused by overrun, or underrun, FIFO clear is possible.
Clear interrupts
INT[18],[20] or INT[19].[21]
[INT_SOURCE_GRP3:B0 0x26]
Clear interrupts
INT[14]
[INT_SOURCE_GRP2:B0 0x25]
Yes
Next packet TX?
No
TRX_OFF issue
[RF_STATUS:B0 0x6C]
END

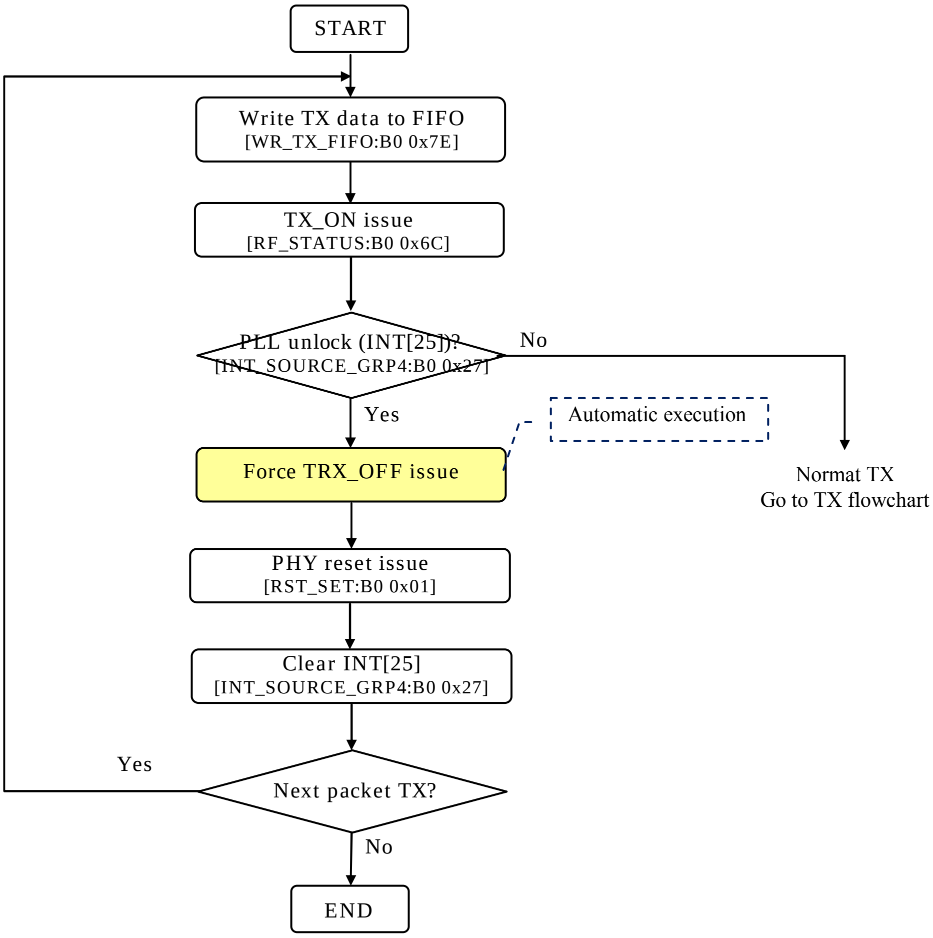
●PLL Unlock Detection

○ TX

During TX, if PLL unlock is detected, PLL unlock interrupt (INT[25] group4) will be generated. When PLL unlock interrupt occurs, Force_TRX_OFF is automaticcally issued and move to IDLE state.

Before next TX operation, issuing PHY reset by [RST_SET:B0 0x01] register and clearing PLL unlock interrupt should be required.

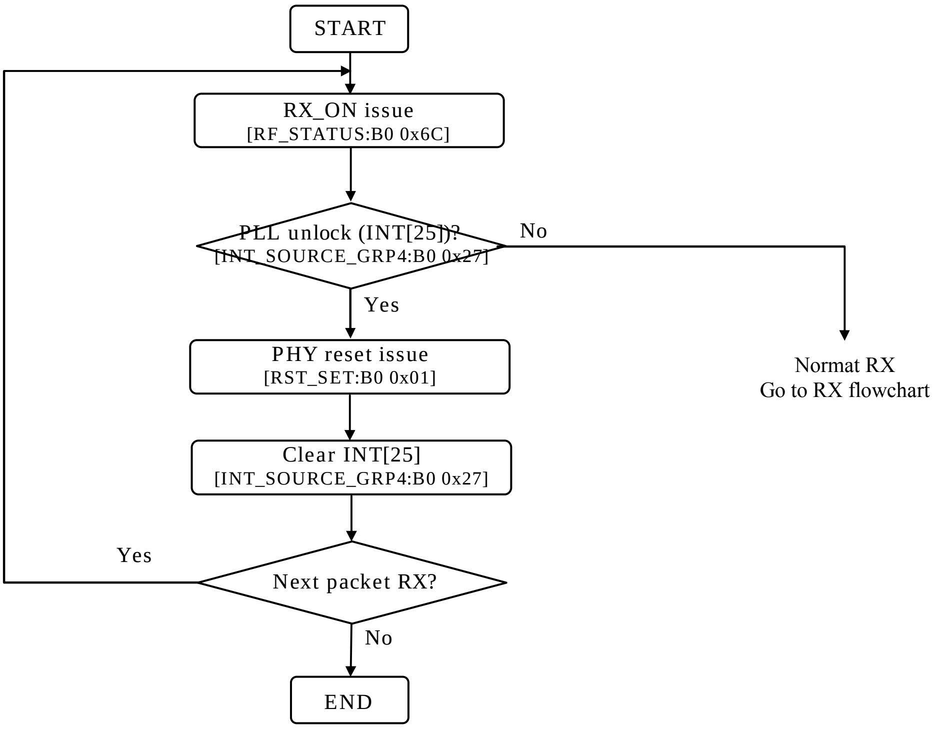
●Internal operation is colored yellow


START
Write TX data to FIFO
[WR_TX_FIFO:B0 0x7E]
TX_ON issue
[RF_STATUS:B0 0x6C]
PLL unlock (INT[25])?
[INT_SOURCE_GRP4:B0 0x27]
No
Yes
Automatic execution
Force TRX_OFF issue
Normat TX
Go to TX flowchart
PHY reset issue
[RST_SET:B0 0x01]
Clear INT[25]
[INT_SOURCE_GRP4:B0 0x27]
Yes
Next packet TX?
No
END

○ RX

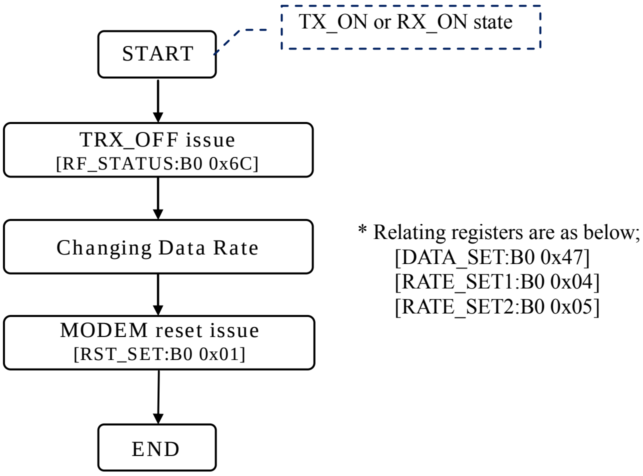
During RX, if PLL unlock is detected, PLL unlock interrupt (INT[25] group4) will be generated. During RX, even if PLL unlock is detected, RX_ON state is maintained (do not move to IDLE state).

Before next RX operation, issuing PHY reset by [RST_SET:B0 0x01] register and clearing PLL unlock interrupt should be required.


START
RX_ON issue
[RF_STATUS:B0 0x6C]
PLL unlock (INT[25])?
[INT_SOURCE_GRP4:B0 0x27]
No
Yes
Normat RX
Go to RX flowchart
PHY reset issue
[RST_SET:B0 0x01]
Clear INT[25]
[INT_SOURCE_GRP4:B0 0x27]
Yes
Next packet RX?
No
END

●Data Rate Change sequence

When changing data rate during operation, data rate should be set in TRX_OFF state. Issuing MODEM reset by [RST_SET: B0 0x01] register is required after data rate change. If not issuing MODEM reset, ML7396 can not transmit or receive correctlly.

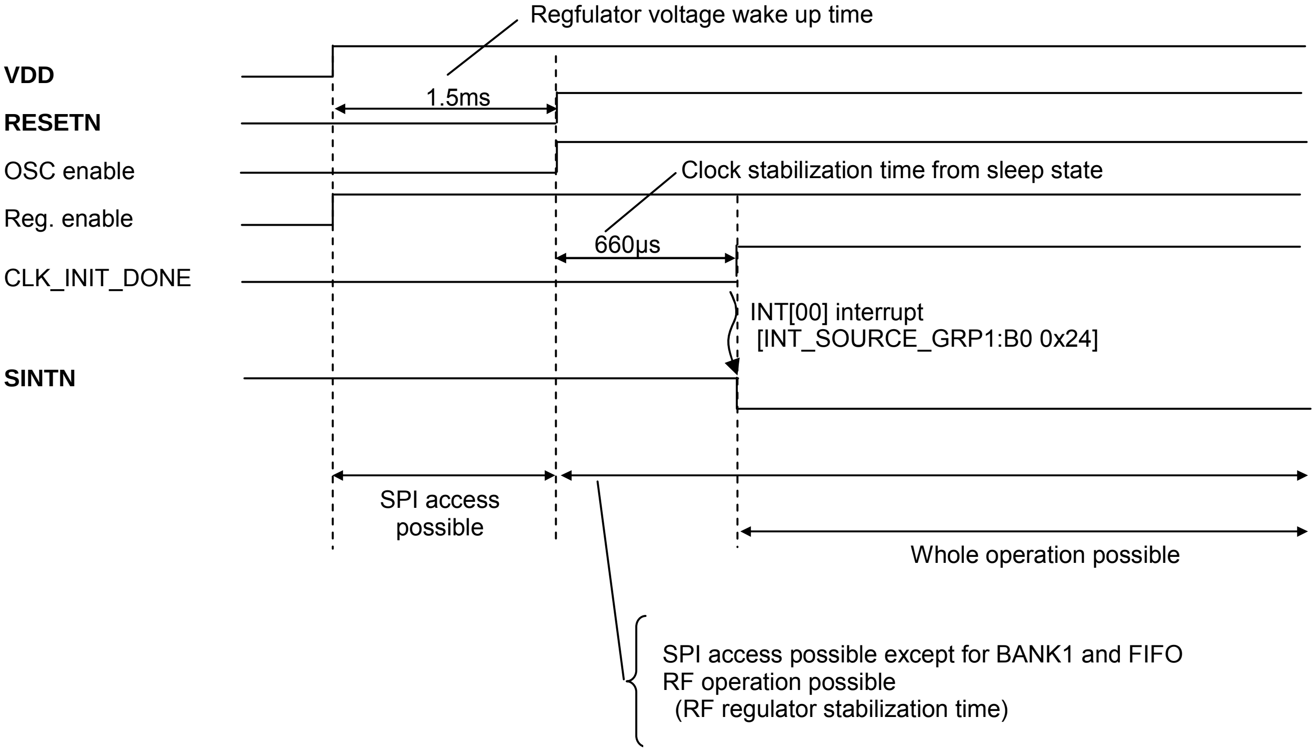

TX_ON or RX_ON state
START
TRX_OFF issue
[RF_STATUS:B0 0x6C]
Changing Data Rate
MODEM reset issue
[RST_SET:B0 0x01]
END
* Relating registers are as below;
[DATA_SET:B0 0x47]
[RATE_SET1:B0 0x04]
[RATE_SET2:B0 0x05]

■Timing Chart

The followings are operation timing of major functions.

[Note]
Bold characters indicate pins relative signals. Non bold characters indicate internal signal.

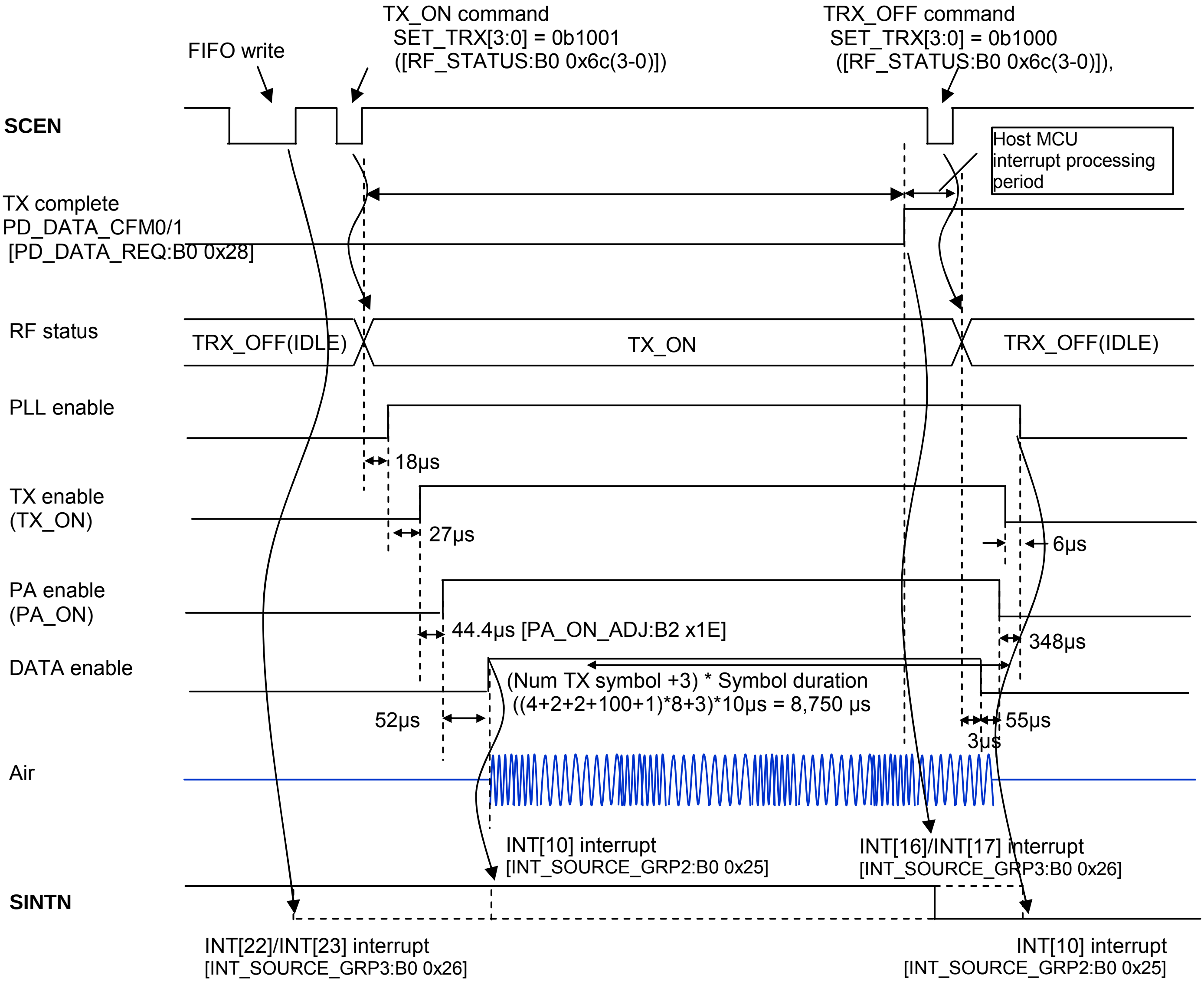
●Start up


Regfulator voltage wake up time
VDD
1.5ms
RESETN
OSC enable
Clock stabilization time from sleep state
Reg. enable
660μs
CLK_INIT_DONE
INT[00] interrupt
[INT_SOURCE_GRP1:B0 0x24]
SINTN
SPI access possible
Whole operation possible
SPI access possible except for BANK1 and FIFO
RF operation possible
(RF regulator stabilization time)

- TX

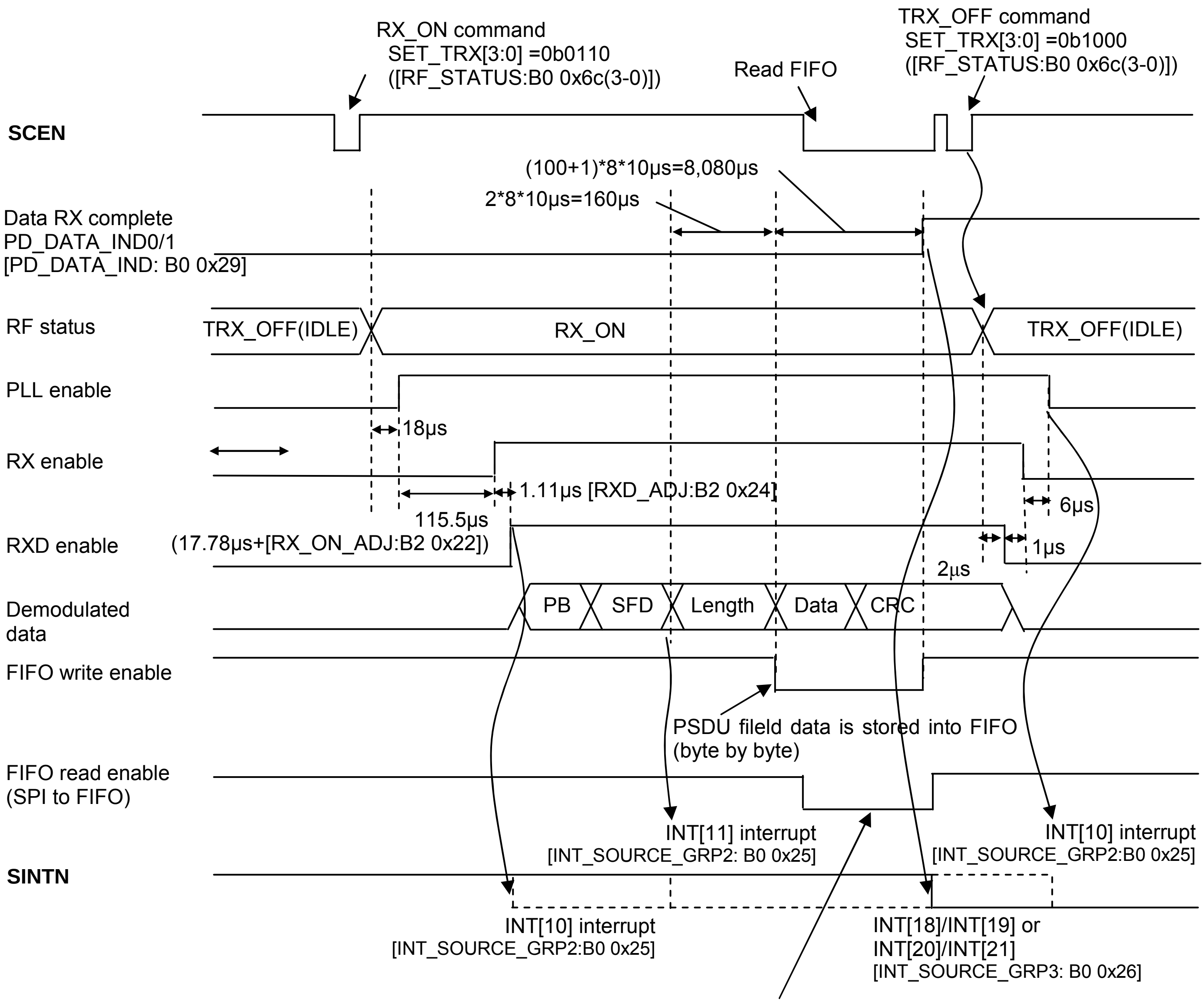
Conditions
•Symbol rate: 100 kbps
•Preamble length: 4 byte
•SFD length: 2 byte
•Length: 2 byte
•CRC: 8 bit (1 byte)
•Data length: 100 byte
•Ramp control: On

* Lamp control timing can be adjusted by the [2DIV_GAIN_CNTRL:B0 0x6E], [RX_ON_ADJ2:B1 0x3F] and [TX_OFF_ADJ1:B1 0x55] registers. For more details, please refer to the “Ramp control function”.


FIFO write
TX_ON command
SET_TRX[3:0] = 0b1001
([RF_STATUS:B0 0x6c(3-0)])
TRX_OFF command
SET_TRX[3:0] = 0b1000
([RF_STATUS:B0 0x6c(3-0)]),
SCEN
Host MCU
interrupt processing
period
TX complete
PD_DATA_CFM0/1
[PD_DATA_REQ:B0 0x28]
RF status
TRX_OFF(IDLE)
TX_ON
TRX_OFF(IDLE)
PLL enable
18μs
TX enable
(TX_ON)
27μs
6μs
PA enable
(PA_ON)
44.4μs [PA_ON_ADJ:B2 x1E]
348μs
DATA enable
(Num TX symbol +3) * Symbol duration
((4+2+2+100+1)*8+3)*10μs = 8,750 μs
52μs
55μs
3μs
Air
INT[10] interrupt
[INT_SOURCE_GRP2:B0 0x25]
INT[16]/INT[17] interrupt
[INT_SOURCE_GRP3:B0 0x26]
SINTN
INT[22]/INT[23] interrupt
[INT_SOURCE_GRP3:B0 0x26]
INT[10] interrupt
[INT_SOURCE_GRP2:B0 0x25]

●RX (without CCA)

Conditions
- •Symbol rate: 100 kbps
- •Preamble length: 4 byte
- •SFD length: 2 byte
- •Length: 2 byte
- •CRC: 8 bit (1 byte)
- •Data length: 100 byte
- •Ramp control: On

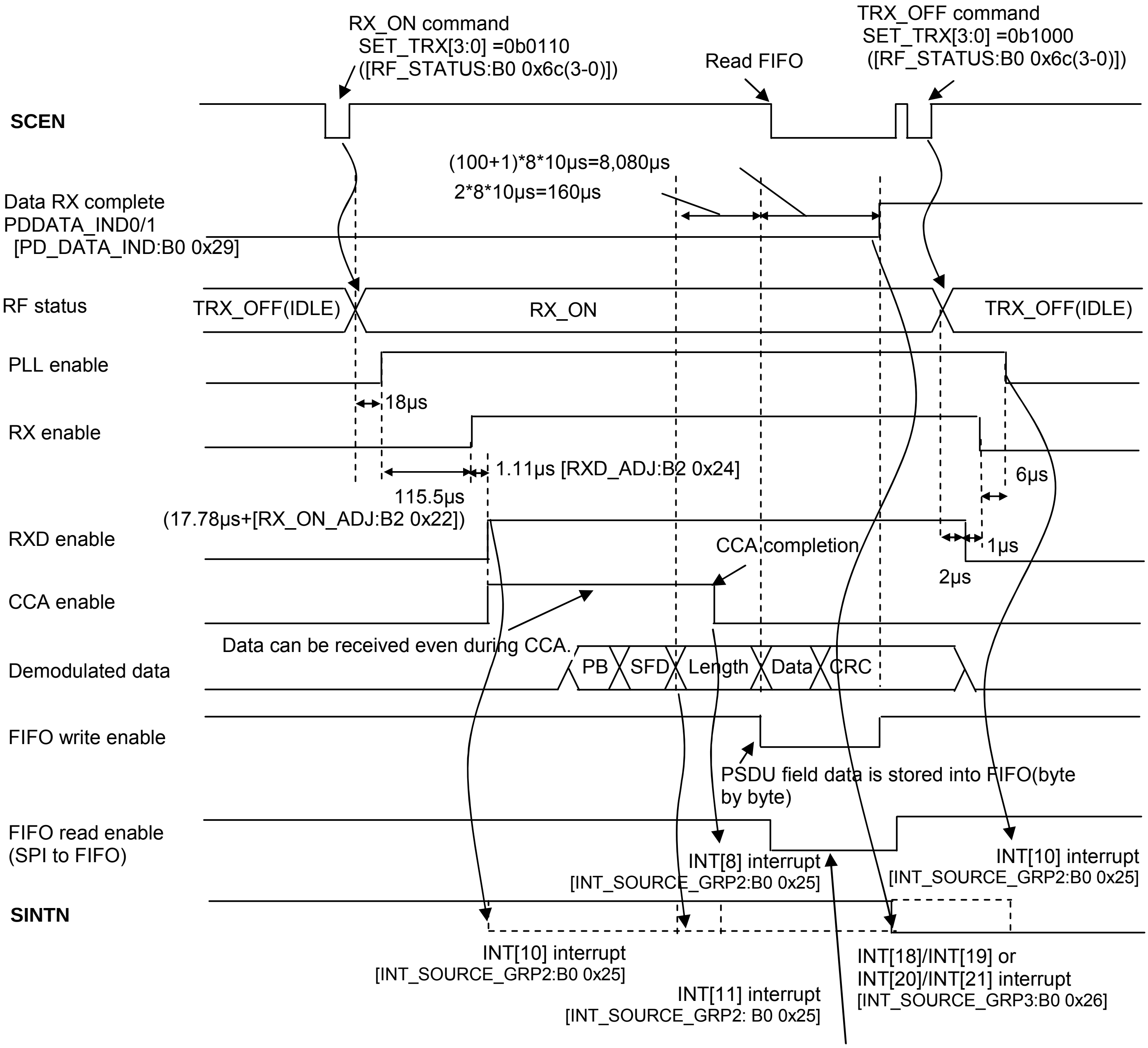

RX_ON command
SET_TRX[3:0] =0b0110
([RF_STATUS:B0 0x6c(3-0)])
Read FIFO
TRX_OFF command
SET_TRX[3:0] =0b1000
([RF_STATUS:B0 0x6c(3-0)])
SCEN
(100+1)*8*10µs=8,080µs
2*8*10µs=160µs
Data RX complete
PD_DATA_IND0/1
[PD_DATA_IND: B0 0x29]
RF status
TRX_OFF(IDLE)
RX_ON
TRX_OFF(IDLE)
PLL enable
18µs
RX enable
1.11µs [RXD_ADJ:B2 0x24]
6µs
115.5µs
(17.78µs+[RX_ON_ADJ:B2 0x22])
RXD enable
1µs
2µs
Demodulated data
PB
SFD
Length
Data
CRC
FIFO write enable
PSDU fileld data is stored into FIFO
(byte by byte)
FIFO read enable
(SPI to FIFO)
INT[11] interrupt
[INT_SOURCE_GRP2: B0 0x25]
INT[10] interrupt
[INT_SOURCE_GRP2:B0 0x25]
SINTN
INT[10] interrupt
[INT_SOURCE_GRP2:B0 0x25]
INT[18]/INT[19] or
INT[20]/INT[21]
[INT_SOURCE_GRP3: B0 0x26]

RX data can be read from a FIFO.
The last data can be read after PDDATA_IND0/1=0b1.
The shortest read out time will be approx 8,240µs+ 16 SCLK cycles from SFD detection (INT[11] , group2).

●RX (with CCA)

Conditions

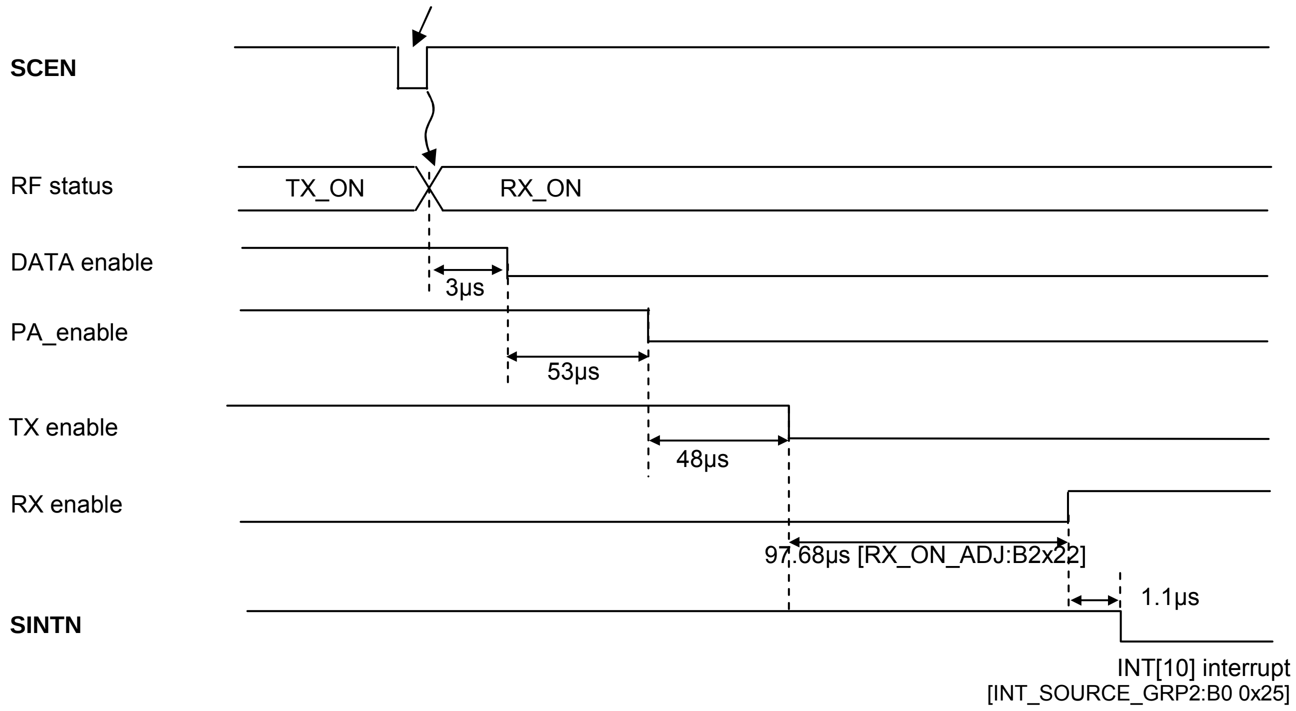
•Symbol rate:	100 kbps
•Preamble length:	4 byte
•SFD length:	2 byte
•Length:	2 byte
•CRC:	8 bit (1 byte)
•Data length:	100 byte
•Ramp control:	On


RX_ON command
SET_TRX[3:0] =0b0110
([RF_STATUS:B0 0x6c(3-0)])
Read FIFO
TRX_OFF command
SET_TRX[3:0] =0b1000
([RF_STATUS:B0 0x6c(3-0)])
SCEN
(100+1)*8*10µs=8,080µs
2*8*10µs=160µs
Data RX complete
PDDATA_IND0/1
[PD_DATA_IND:B0 0x29]
RF status
TRX_OFF(IDLE)
RX_ON
TRX_OFF(IDLE)
PLL enable
18µs
RX enable
1.11µs [RXD_ADJ:B2 0x24]
115.5µs
(17.78µs+[RX_ON_ADJ:B2 0x22])
6µs
RXD enable
CCA completion
1µs
2µs
CCA enable
Data can be received even during CCA.
Demodulated data
PB
SFD
Length
Data
CRC
FIFO write enable
PSDU field data is stored into FIFO(byte by byte)
FIFO read enable
(SPI to FIFO)
INT[8] interrupt
[INT_SOURCE_GRP2:B0 0x25]
INT[10] interrupt
[INT_SOURCE_GRP2:B0 0x25]
SINTN
INT[10] interrupt
[INT_SOURCE_GRP2:B0 0x25]
INT[11] interrupt
[INT_SOURCE_GRP2: B0 0x25]
INT[18]/INT[19] or
INT[20]/INT[21] interrupt
[INT_SOURCE_GRP3:B0 0x26]

RX DATA can be read from a FIFO.
The last data can be read after PD_DATA_IND0/1=0b1.
The shortest read out time will be approx 8,240µs+ 16 SCLK cycles from SFD detection (INT[11], group2).

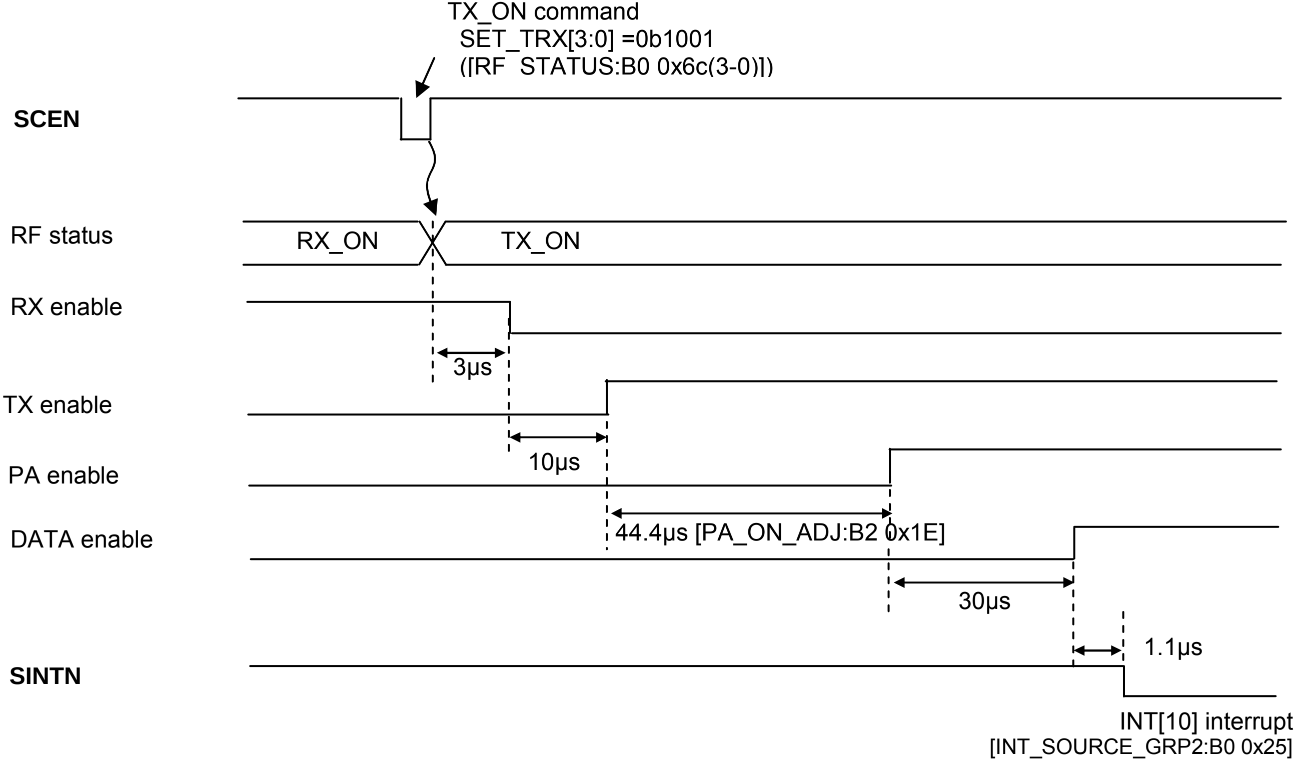
●Transition from TX to RX

Condition:
•Ramp control: On


SCEN
RF status
TX_ON
RX_ON
DATA enable
3µs
PA_enable
53µs
TX enable
48µs
RX enable
97.68µs [RX_ON_ADJ:B2x22]
1.1µs
SINTN
INT[10] interrupt
[INT_SOURCE_GRP2:B0 0x25]

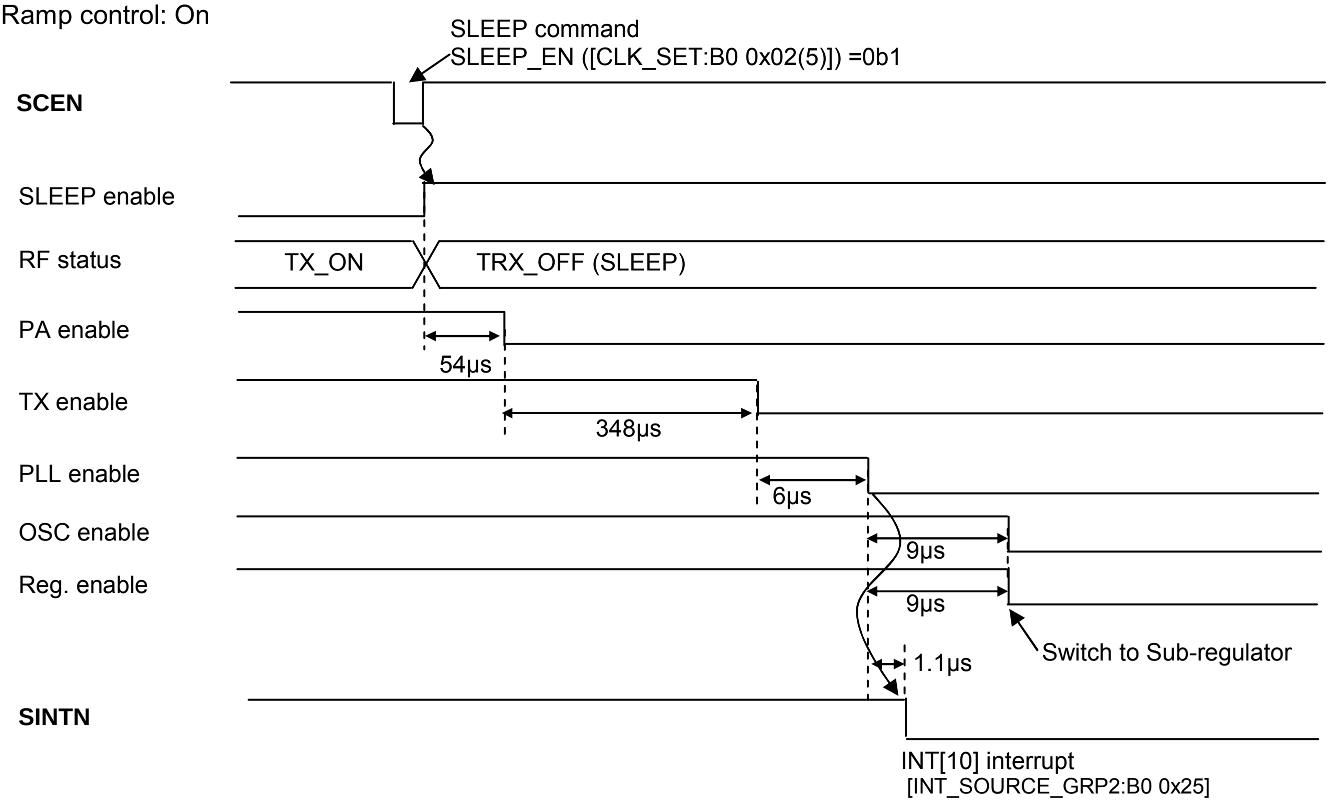
●Transition from RX to TX mode

Condition:
•Ramp control: On


TX_ON command
SET_TRX[3:0] =0b1001
([RF STATUS:B0 0x6c(3-0)])
SCEN
RF status
RX_ON
TX_ON
RX enable
3µs
TX enable
10µs
PA enable
44.4µs [PA_ON_ADJ:B2 0x1E]
DATA enable
30µs
1.1µs
SINTN
INT[10] interrupt
[INT_SOURCE_GRP2:B0 0x25]

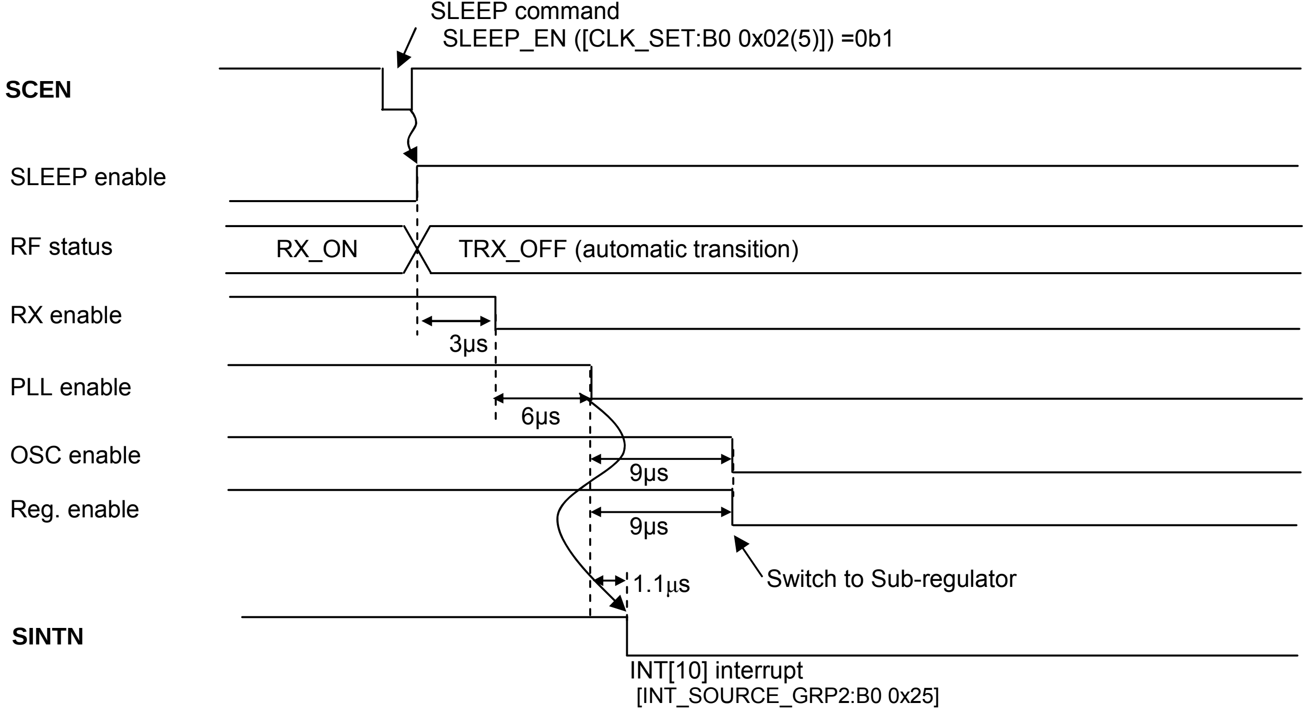
●Transition from TX to SLEEP

Condition:
•Ramp control: On

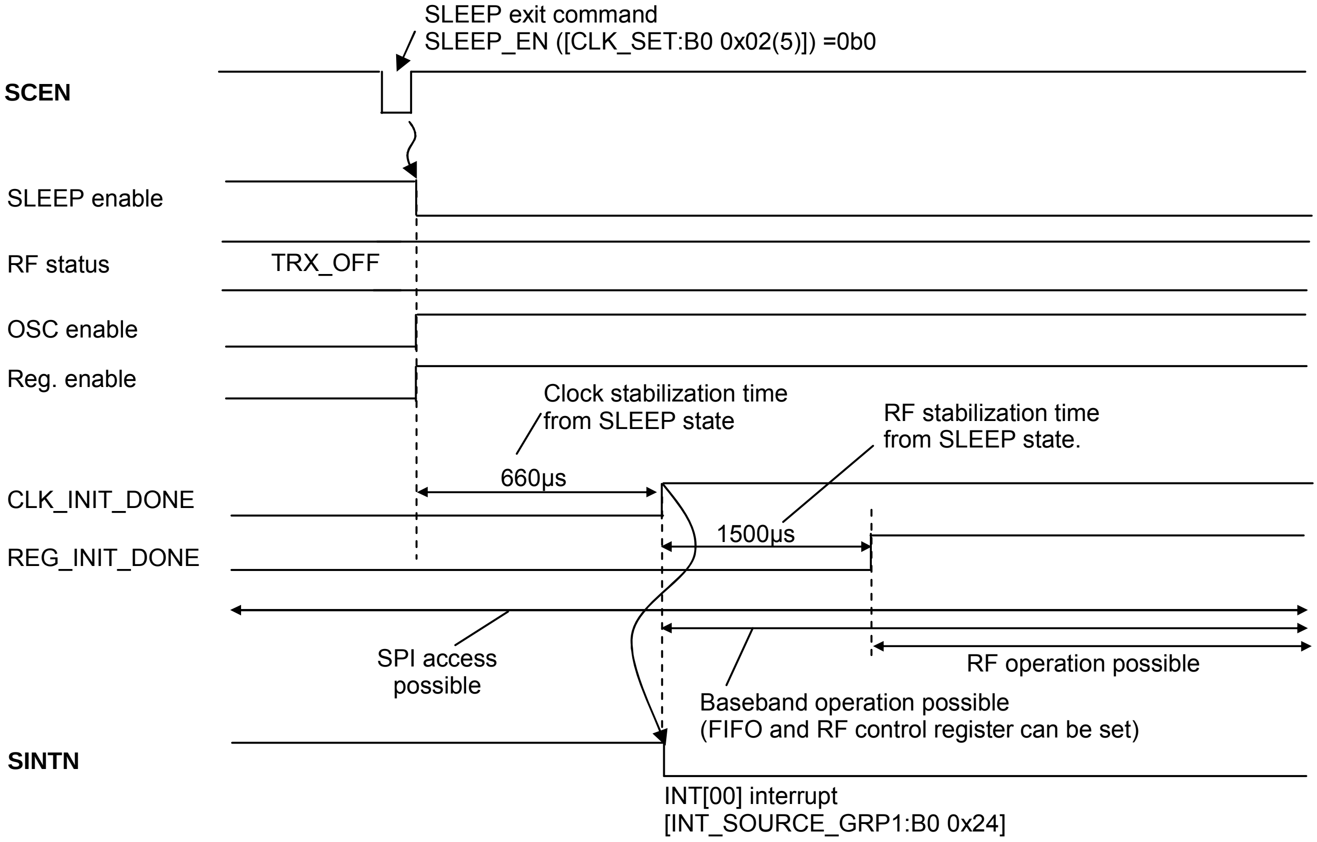

SLEEP command
SLEEP_EN ([CLK_SET:B0 0x02(5)]) =0b1
SCEN
SLEEP enable
RF status
TX_ON
TRX_OFF (SLEEP)
PA enable
54µs
TX enable
348µs
PLL enable
6µs
OSC enable
9µs
Reg. enable
9µs
1.1µs
Switch to Sub-regulator
SINTN
INT[10] interrupt
[INT_SOURCE_GRP2:B0 0x25]

●Transition from RX to SLEEP

Condition:
•Ramp control: On

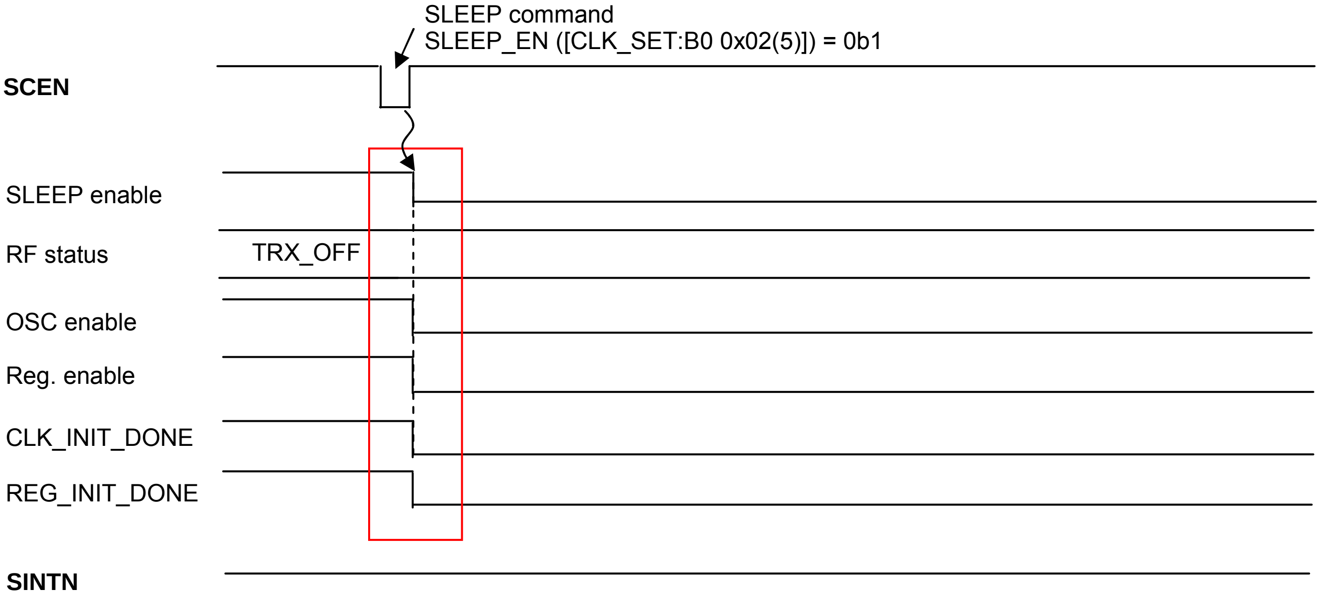

SLEEP command
SLEEP_EN ([CLK_SET:B0 0x02(5)]) =0b1
SCEN
SLEEP enable
RF status
RX_ON
TRX_OFF (automatic transition)
RX enable
3µs
PLL enable
6µs
OSC enable
9µs
Reg. enable
9µs
1.1µs
Switch to Sub-regulator
SINTN
INT[10] interrupt
[INT_SOURCE_GRP2:B0 0x25]

- Transition from SLEEP to IDLE


SLEEP exit command
SLEEP_EN ([CLK_SET:B0 0x02(5)]) =0b0
SCEN
SLEEP enable
RF status
TRX_OFF
OSC enable
Reg. enable
Clock stabilization time from SLEEP state
RF stabilization time from SLEEP state.
660μs
CLK_INIT_DONE
1500μs
REG_INIT_DONE
SPI access possible
RF operation possible
Baseband operation possible
(FIFO and RF control register can be set)
SINTN
INT[00] interrupt
[INT_SOURCE_GRP1:B0 0x24]

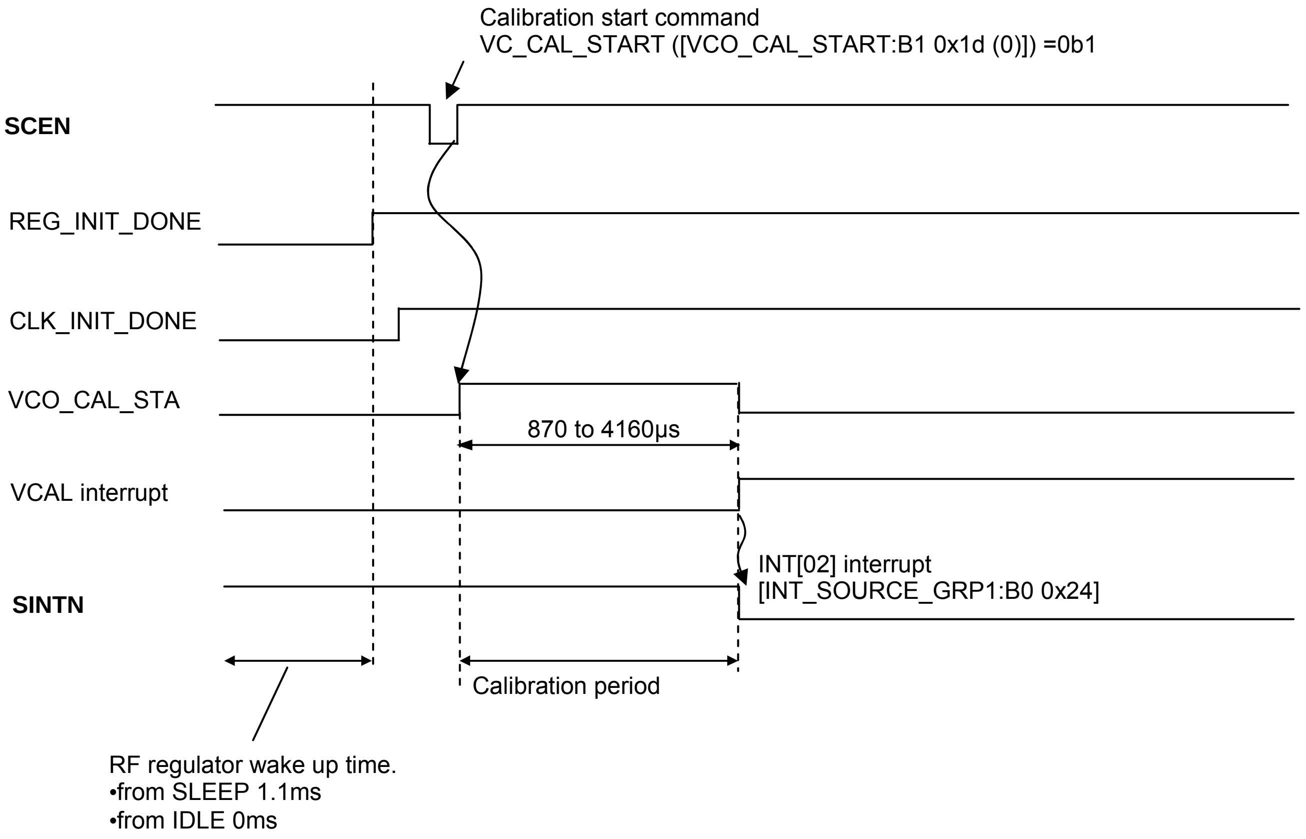
Note: When using TCXO, enabling TCXO (clock) before issuing SLEEP exit command. If enabling TCXO after issuing SLEEP exit command, the start time will delay for a certain time.

- Transition from IDLE to SLEEP


SLEEP command
SLEEP_EN ([CLK_SET:B0 0x02(5)]) = 0b1
SCEN
SLEEP enable
RF status
TRX_OFF
OSC enable
Reg. enable
CLK_INIT_DONE
REG_INIT_DONE
SINTN

Note: If disabling TCXO during SLEEP, wait more than 4μs after issuing SLEEP command, then disabling TCXO (clock).

●VCO Calibration


Calibration start command
VC_CAL_START ([VCO_CAL_START:B1 0x1d (0)]) =0b1
SCEN
REG_INIT_DONE
CLK_INIT_DONE
VCO_CAL_STA
870 to 4160μs
VCAL interrupt
INT[02] interrupt
[INT_SOURCE_GRP1:B0 0x24]
SINTN
Calibration period
RF regulator wake up time.
•from SLEEP 1.1ms
•from IDLE 0ms

■About FCC Support

ML7396A (915MHz band) complies with FCC PART 15. When the outputpowe is -1dBm or less, PART 15.249 is applied, and when the output power is +30dBm or less, PART 15.247 is applied. Spurious emissions should comply with PART 15.209.
PART 15.247 requires the frequency hopping or the wideband digital modulation. For details of the frequency hopping, please refer to the "About frequency hopping" below. For details of the wideband digital modulation, please refer to the " Initial register setting " file.

●About frequency hopping (FHSS: Frequency Hopping Spread Spectrum)

According to the FCC (United States radio act) Part 15.247, the FHSS system which 20dB bandwidth is less than 250 kHz, should have 50 or more hopping channels. If 20dB bandwidth is 250 kHz or more, 25 or more hopping channels should be supported. And the channel occupation time should be limited to 400ms at a maximum.
The following examples show how to control and set registers in order to comply with above regulations.
For details of register settings, please refer to the "Initial registers setting" file.

・Frequency switch flow during TX
(0) TX completion (TX_ON)
(1) Transition to TRX_OFF or RX_ON state by SET_TRX[3:0] ([RF_STATUS:B0 0x6C(3-0)]).
(2) Switching frequency by [CH0_FL:B0 0x48], [CH0_FM:B0 0x49] and [CH0_FH:B0 0x4A] registers.
(3) Issuing TX_ON command by SET_TRX[3:0].
Repeat (0) to (3).

• Frequency switch flow during RX
(0) RX completion (RX_ON)
(1) Masking PLL unlock interrupt by INT_EN[25] ([INT_EN_GRP4:B0 0x2D(1)]) =0b0.
(2) Switching frequency by [CH0_FL:B0 0x48], [CH0_FM:B0 0x49] and [CH0_FH:B0 0x4A] registers.
(3) Wait 100µs. (PLL lock period)
(4) Clear the PLL unlock interrupt (INT[25] group4), and enable the interrupt by INT_EN[25] =0b1
(5) Receive data
Repeat (0) to (5).
* PLL unlock interrupt may be detected during frequency switch.
It is recommended to masking the PLL unlock interrupt for 100µs during frequency switch as shown in (1) to (4).

The following examples show how to control the frequency hopping system.

•Control example 1. TX equipment transmits a long term preamble, and the RX equipment scans channels to detect a preamble

TX equipment hops the frequency according to the hopping pattern. And the channel occupation time should be less than 400ms to comply with the regulation.
RX equipment does not know the using channel transmitting preamble, and so scans all channels for detecting preamble. The preamble transmitting period should be longer than the channel scan period on the RX equipment. For details of the channel scan flow, please refer to the flow chart shown later.
The one channel scan time can be calculated as "preamble search period (36bits / data rate) + PLL lock period (100µs)".
The following table shows the channel scan period for each data rate. Please set an appropriate preamble length according to the following table. The preamble length can be set by [TX_PR_LEN:B0 0x42] register. (max. 255 bytes)

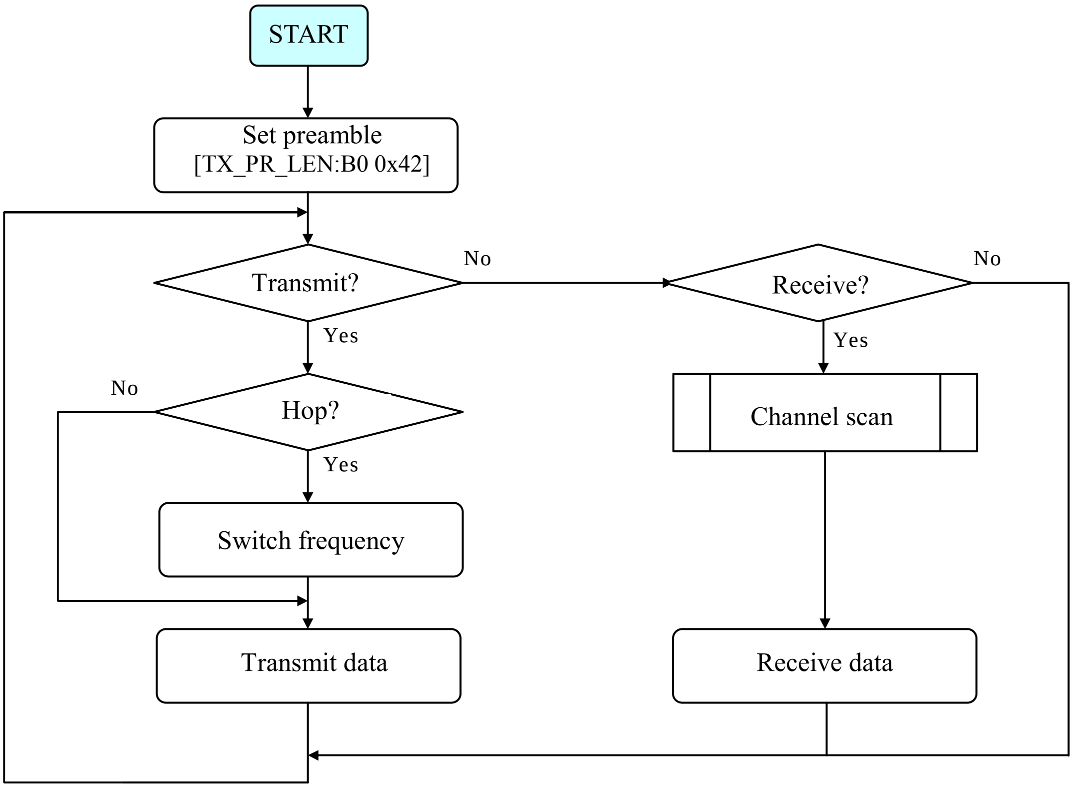
Table. Channel scan period for each data rate

data rate [kbps]	255 byte PB transmitting period [ms]	Required period for one channel scan [ms]	Required period for all channels scan [ms] 25ch	 50ch	Availability 25ch	 50ch
10	204.0	3.70	92.5	185.0	○	○
20	102.0	1.90	47.5	95.0	○	○
40	51.0	1.00	25.0	50.0	○	○
50	40.8	0.82	20.5	41.0	○	×
100	20.4	0.46	11.5	23.0	○	×
150	13.6	0.34	8.5	17.0	○	×
200	10.2	0.28	7.0	14.0	○	×
400	5.1	0.19	4.8	9.5	○	×

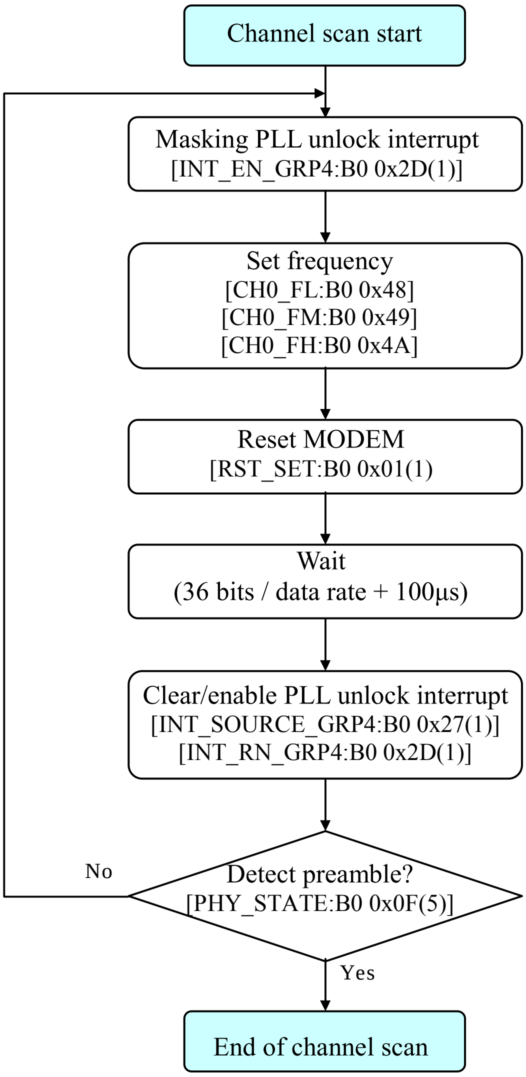
* This table does not take into account the register access time.

* This control method cannot be applied under the "×" condition, since the all channel scanning period exceeds the preamble transmission period.

Control example 1 flowchart.


START
Set preamble
[TX_PR_LEN:B0 0x42]
Transmit?
No
Yes
Receive?
No
Yes
No
Hop?
Yes
Channel scan
Switch frequency
Transmit data
Receive data

Details of channel scan flow.


Channel scan start
Masking PLL unlock interrupt
[INT_EN_GRP4:B0 0x2D(1)]
Set frequency
[CH0_FL:B0 0x48]
[CH0_FM:B0 0x49]
[CH0_FH:B0 0x4A]
Reset MODEM
[RST_SET:B0 0x01(1)
Wait
(36 bits / data rate + 100µs)
Clear/enable PLL unlock interrupt
[INT_SOURCE_GRP4:B0 0x27(1)]
[INT_RN_GRP4:B0 0x2D(1)]
No
Detect preamble?
[PHY_STATE:B0 0x0F(5)]
Yes
End of channel scan

- Control example 2. Use beacon for synchronization and common hopping pattern

In this example, both master and slave nodes use the same synchronized hopping pattern.

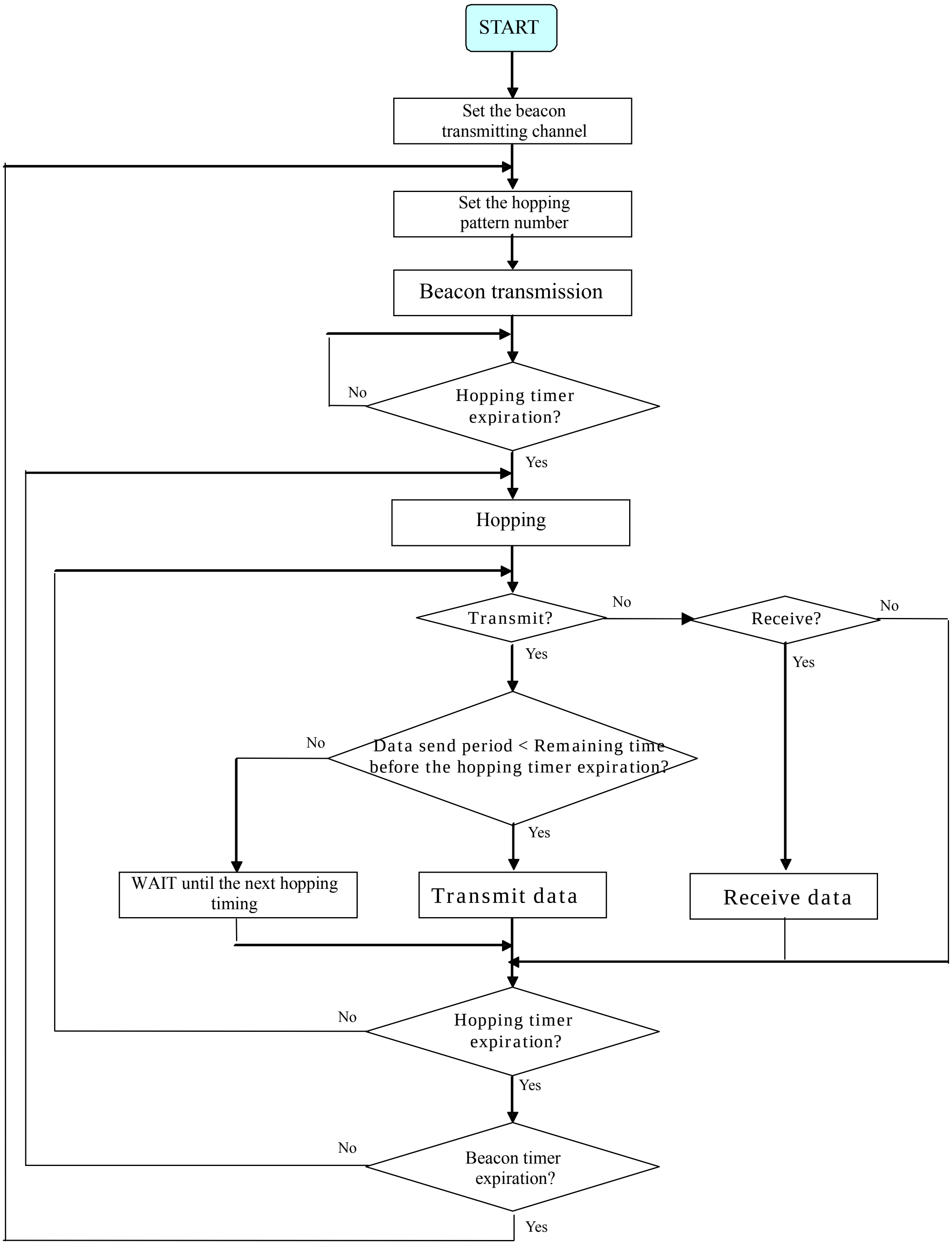
The master node periodically transmits a beacon on pre-defined channel. The slave node receives the beacon for synchronizing the hopping pattern.

The slave node waits for a beacon at the pre-defined channel. Once completing synchronization, both nodes hop frequencies according to the common hopping pattern. The hopping interval should be "the beacon interval divided by the number of hopping channels" and required less than 400ms. When transmitting, the transmitting period should be calculated from the data length, making sure to avoid spanning hopping intervals.

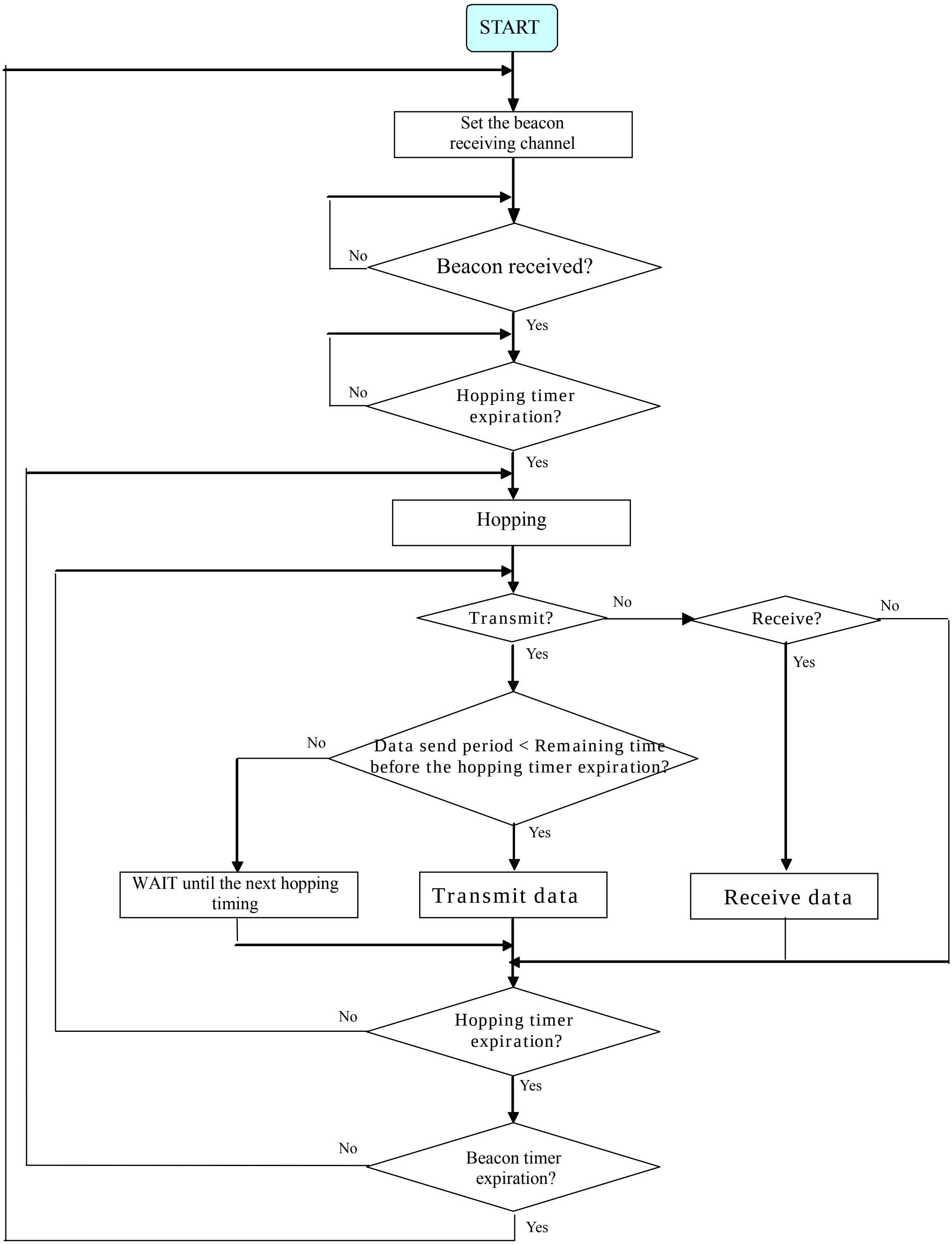
When using multiple hopping patterns, adding sequential numbers (pattern number) on each hopping pattern. And the master node attaches the using pattern number into a beacon.

This hopping method is available regardless of the data rate, the diversity search setting, and the number of hopping channels.

[Master node flowchart]


START
Set the beacon transmitting channel
Set the hopping pattern number
Beacon transmission
No
Hopping timer expiration?
Yes
Hopping
Transmit?
No
Receive?
No
Yes
Yes
No
Data send period < Remaining time before the hopping timer expiration?
Yes
WAIT until the next hopping timing
Transmit data
Receive data
No
Hopping timer expiration?
Yes
No
Beacon timer expiration?
Yes

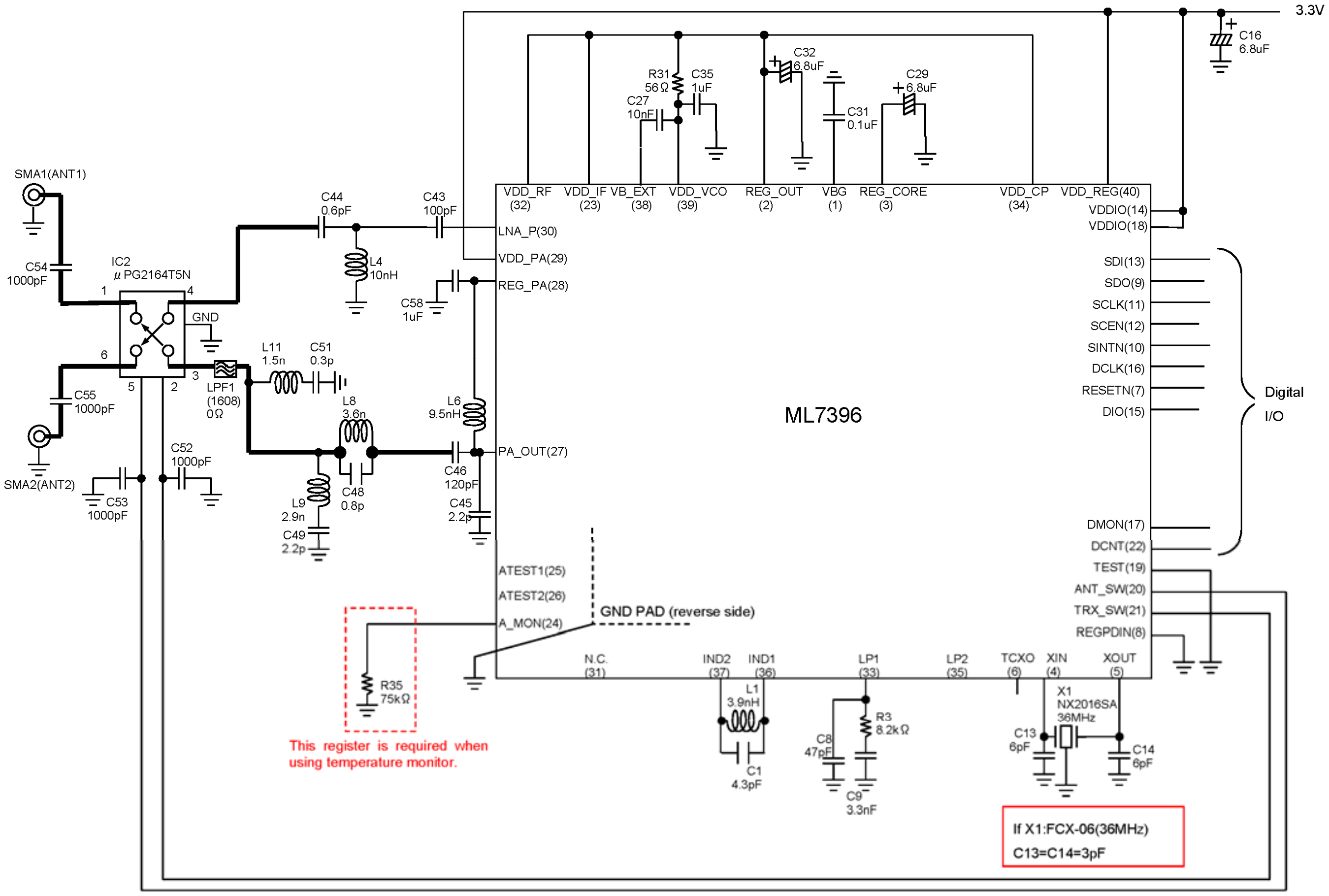
[Slave node flowchart]


START
Set the beacon receiving channel
Beacon received?
No
Yes
Hopping timer expiration?
No
Yes
Hopping
Transmit?
No
Yes
Receive?
No
Yes
Data send period < Remaining time before the hopping timer expiration?
No
Yes
WAIT until the next hopping timing
Transmit data
Receive data
Hopping timer expiration?
No
Yes
Beacon timer expiration?
No
Yes

■Application Circuit Example

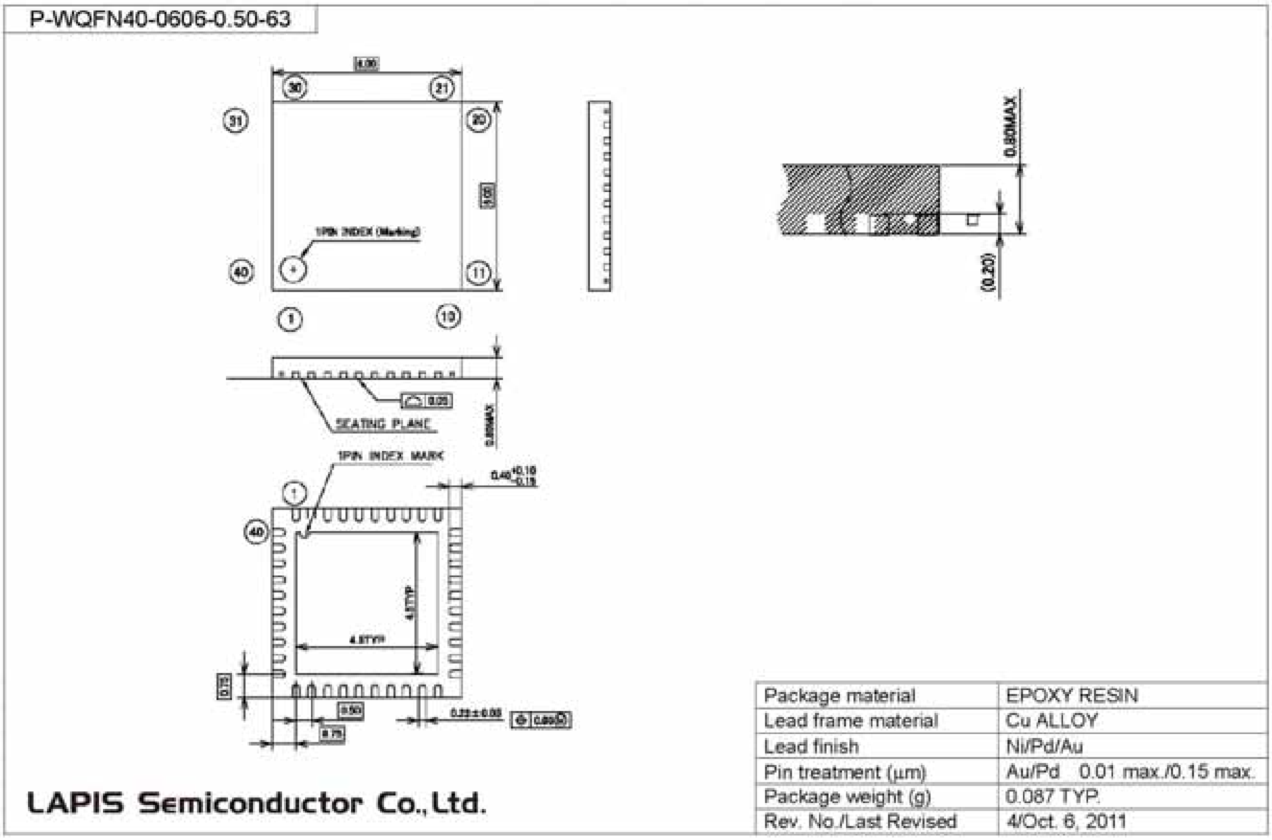
Here is a circuit example for 915MHz/920MHz, 13dBm, and up to 200kbps.
10µF decoupling capacitor should be placed to common 3.3V power pins .
MURATA LQW15series inductors are recommended.

For more details about designing information, please refer to the “ML7396 Family LSIs Hardware Design Manual”.


3.3V
C16 6.8uF
R31 56Ω
C35 1uF
C27 10nF
C32 6.8uF
C31 0.1uF
C29 6.8uF
SMA1(ANT1)
C44 0.6pF
C43 100pF
C54 1000pF
IC2 µPG2164T5N
GND
L4 10nH
C58 1uF
L11 1.5n
C51 0.3p
LPF1 (1608) 0Ω
C55 1000pF
L8 3.6n
L6 9.5nH
SMA2(ANT2)
C53 1000pF
C52 1000pF
L9 2.9n
C48 0.8p
C46 120pF
C45 2.2p
C49 2.2p
VDD_RF (32)
VDD_IF (23)
VB_EXT (38)
VDD_VCO (39)
REG_OUT (2)
VBG (1)
REG_CORE (3)
VDD_CP (34)
VDD_REG(40)
VDDIO(14)
VDDIO(18)
LNA_P(30)
VDD_PA(29)
REG_PA(28)
PA_OUT(27)
ATEST1(25)
ATEST2(26)
A_MON(24)
GND PAD (reverse side)
ML7396
SDI(13)
SDO(9)
SCLK(11)
SCEN(12)
SINTN(10)
DCLK(16)
RESETN(7)
DIO(15)
Digital I/O
DMON(17)
DCNT(22)
TEST(19)
ANT_SW(20)
TRX_SW(21)
REGPDIN(8)
N.C. (31)
IND2 (37)
IND1 (36)
LP1 (33)
LP2 (35)
TCXO (6)
XIN (4)
XOUT (5)
L1 3.9nH
C1 4.3pF
C8 47pF
R3 8.2kΩ
C9 3.3nF
X1 NX2016SA 36MHz
C13 6pF
C14 6pF
R35 75kΩ
This register is required when using temperature monitor.
If X1:FCX-06(36MHz) C13=C14=3pF

	915MHz	920MHz
L1	4.3nH	3.9nH
C1	3.9pF	4.3pF
LPF1	DEA160915LT-5038A (TDK)	0Ω

■Package Dimensions


P-WQFN40-0606-0.50-63
6.00
30
21
31
20
6.00
1PIN INDEX (Marking)
40
11
1
10
0.05
SEATING PLANE
0.80MAX
1PIN INDEX MARK
0.40+0.10/-0.15
4.5TYP
4.5TYP
0.75
0.50
0.75
0.22±0.05
0.05
0.80MAX
(0.20)
LAPIS Semiconductor Co.,Ltd.

Package material	EPOXY RESIN
Lead frame material	Cu ALLOY
Lead finish	Ni/Pd/Au
Pin treatment (μm)	Au/Pd 0.01 max./0.15 max.
Package weight (g)	0.087 TYP.
Rev. No./Last Revised	4/Oct. 6, 2011

Remarks for surface mount type package

Surface mount type package is very sensitive affected by heating from reflow process, humidity during storaging Therefore, in case of reflow mounting process, please contact sales representative about product name, package name, number of pin, package code and required reflow process condition (reflow method, temperature, number of reflow process), storage condition.

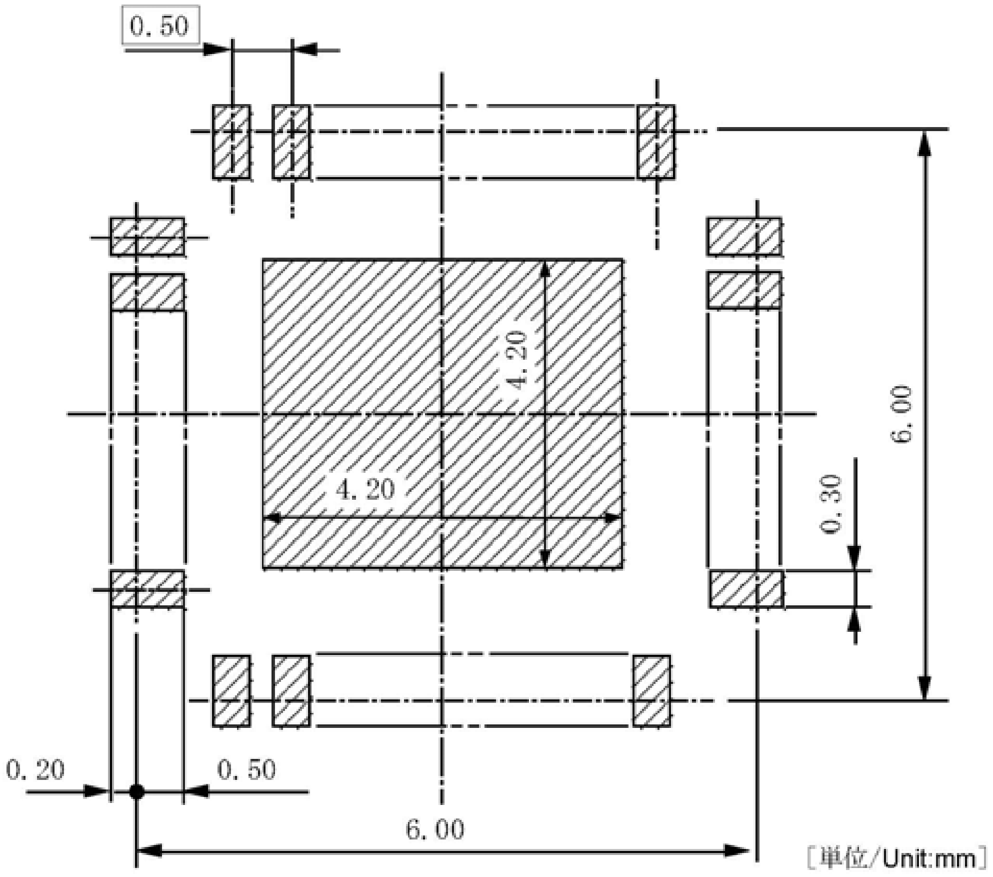
■Footprint Pattern (Recommendation)

P-WQFN40-0606-0.50-63

参考図
for reference

半田付け部端子存在範囲図

Mounting area for package lead soldering to PC boards



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When laying out PC boards, it is important to design the foot pattern so as to give consideration to ease of mounting, bonding, positioning of parts,reliability, wiring,and elimination of solder bridges.

The optimum design for the foot pattern varies with the materials of the substrate,the sort and thickness of used soldering paste,and the way of soldering. Therefore when laying out the foot pattern on the PC boards, refer to this figure which mean the mounting area that the package leads are allowable for soldering to PC boards.

■Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7396A B E-01	2013.02.27	–	–	Initial release (Draft version)
FEDL7396A_B_E-02 to -06	–	–	–	These versions are not released.
FEDL7396A B E-07	2015.01.15	–	–	Official release (Base on FJDL7396A B E-07)

■NOTES

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