Triple Differential Receiver with 300 Meter Adjustable Line Equalization

Data Sheet

AD8122

FEATURES

- Compensates cables up to 300 meters for wideband video
  - 60 MHz equalized BW at 300 meters of UTP cable
  - 120 MHz equalized BW at 150 meters of UTP cable
- Fast time domain performance
  - 70 ns settling time to 1% at 300 meters of UTP cable
  - 7 ns rise/fall times with 2 V step at 300 meters of UTP cable
- 3 frequency response gain adjustment pins
  - High frequency peaking adjustment (V_{PEAK})
  - Output low-pass filter cutoff adjustment (V_{FILTER})
  - Broadband flat gain adjustment (V_{GAIN})
- Selectable for UTP or coaxial compensation
- DC output offset adjustment pin (V_{OFFSET})
- Low output offset voltage: ±4 mV at G = 1
- Compensates both RGB and YPbPr
- 2 on-chip comparators with hysteresis can be used for common-mode sync pulse extraction
- Available in 40-lead, 6 mm × 6 mm LFCSP

APPLICATIONS

- Keyboard-video-mouse (KVM)
- Digital signage
- RGB video over UTP cables
- Professional video projection and distribution
- HD video
- Security video

FUNCTIONAL BLOCK DIAGRAM

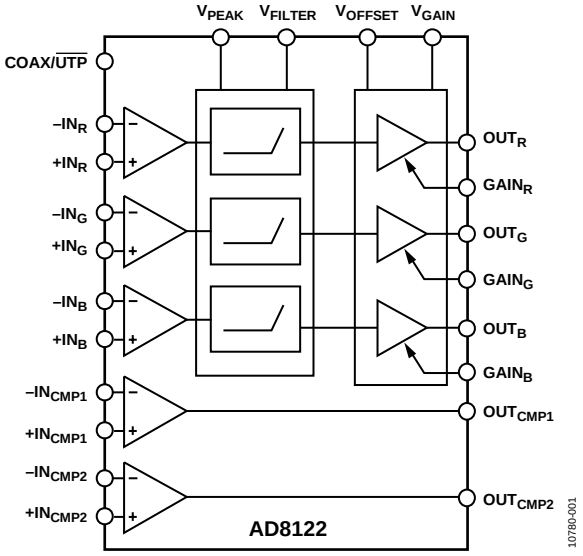


Figure 1.

GENERAL DESCRIPTION

The AD8122 is a high speed, triple differential receiver and equalizer that compensates for the transmission losses of UTP cables up to 300 meters in length and coaxial cables up to 200 meters in length. Various gain stages are summed to best approximate the inverse frequency response of the cable. Each channel features a high impedance differential input with high rejection of common-mode (CM) signals that is ideal for interfacing directly with the cable.

The AD8122 has two control inputs for optimal cable compensation, one LPF control input, an input to select UTP or coaxial cable, and an input to adjust the dc output offset. The cable compensation inputs are used to compensate for different cable lengths: the V_{PEAK} input controls the amount of high frequency peaking, and the V_{GAIN} input adjusts the broadband flat gain to compensate for the flat cable loss. The V_{FILTER} input controls the cutoff frequency of output low-pass filters on each channel.

The selection of UTP or coaxial cable compensation responses is determined by the binary COAX/$\overline{\text{UTP}}$ input, which can be left floating in UTP applications. The V_{OFFSET} input allows the dc voltage at the output to be adjusted, which can be useful in dc-coupled systems.

For added flexibility, the gain of each channel can be set to 1 or 2 using the associated gain control pin.

The AD8122 is available in a 6 mm × 6 mm, 40-lead LFCSP and is rated to operate over the extended temperature range of −40°C to +85°C.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

IMPORTANT LINKS for the AD8122*

Last content update 06/26/2013 07:12 pm

PARAMETRIC SELECTION TABLES

Find Similar Products By Operating Parameters

DOCUMENTATION

AD8122: 300m Cable Equalizer & Complete System Solution CFTL

Analog Devices Introduces Industry's Fastest and Most Power Efficient 300 meter UTP Cable Equalizer for Analog Video Distribution

PRODUCT RECOMMENDATIONS & REFERENCE DESIGNS

CN-0275: Complete Broadband Video-over-UTP Driver and Receiver Solution for RGB, YPbPr, and More

EVALUATION KITS & SYMBOLS & FOOTPRINTS

View the Evaluation Boards and Kits page for documentation and purchasing

Symbols and Footprints

DESIGN COLLABORATION COMMUNITY

Collaborate Online with the ADI support team and other designers about select ADI products.

Follow us on Twitter: www.twitter.com/ADI_News
Like us on Facebook: www.facebook.com/AnalogDevicesInc

DESIGN SUPPORT

Submit your support request here:
Linear and Data Converters
Embedded Processing and DSP

Telephone our Customer Interaction Centers toll free:

Americas:	1-800-262-5643
Europe:	00800-266-822-82
China:	4006-100-006
India:	1800-419-0108
Russia:	8-800-555-45-90

Quality and Reliability
Lead(Pb)-Free Data

SAMPLE & BUY

AD8122

- View Price & Packaging
- Request Evaluation Board
- Request Samples Check Inventory & Purchase

Find Local Distributors

TABLE OF CONTENTS

REVISION HISTORY

7/12—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = ±5 V, Category 5e UTP cable, input V_{CM} = 0 V, V_{OFFSET} = 0 V, V_{PEAK}, V_{GAIN}, and V_{FILTER} are set to the recommended settings shown in Figure 24, unless otherwise noted. For G = 2, R_L = 150 Ω and V_{OUT} = 2 V p-p; for G = 1, R_L = 1 kΩ and V_{OUT} = 1 V p-p.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC AND NOISE PERFORMANCE					
−3 dB Large Signal Bandwidth	AD8122 only, G = 1/G = 2		270/165		MHz
	150 meters of cable, G = 1/G = 2		120/110		MHz
	300 meters of cable, G = 1, G = 2		60		MHz
Slew Rate	V_{OUT} = 2 V p-p, AD8122 only, G = 1, G = 2		1000		V/µs
10% to 90% Rise/Fall Times	V_{OUT} = 2 V step, 150 meters of cable, G = 2		6		ns
	V_{OUT} = 2 V step, 300 meters of cable, G = 2		7		ns
	V_{OUT} = 1 V step, 150 meters of cable, G = 1		6		ns
	V_{OUT} = 1 V step, 300 meters of cable, G = 1		7		ns
Settling Time to 1%	V_{OUT} = 2 V step, 150 meters of cable, G = 2		70		ns
	V_{OUT} = 2 V step, 300 meters of cable, G = 2		70		ns
	V_{OUT} = 1 V step, 150 meters of cable, G = 1		85		ns
	V_{OUT} = 1 V step, 300 meters of cable, G = 1		70		ns
Integrated Output Voltage Noise	150 meters of cable, integrated to 160 MHz, G = 1/G = 2		3.7/6.2		mV rms
	300 meters of cable, integrated to 160 MHz, G = 1/G = 2		17/27		mV rms
INPUT PERFORMANCE					
Input Voltage Range	Common mode, $-IN_x = +IN_x$		±4.0		V
Maximum Differential Voltage Swing	$\lvert(+IN_x) - (-IN_x)\rvert$		3		V
Voltage Gain Error	$\Delta V_{OUT}/\Delta V_{IN}$, V_{GAIN} set for 0 meters of cable, G = 1		1.5		%
	$\Delta V_{OUT}/\Delta V_{IN}$, V_{GAIN} set for 0 meters of cable, G = 2		0.50		%
Channel-to-Channel Gain Matching	G = 1, G = 2		0.15		%
Common-Mode Rejection (CMR)	$\Delta V_{OUT}/\Delta V_{IN, CM}$				
	DC, $V_{PEAK} = V_{GAIN}$ = 0 V, G = 1/G = 2		−92/−87		dB
	DC, 300 meters of cable, G = 1/G = 2		−89/−85		dB
	1 MHz, 300 meters of cable, G = 1/G = 2		−63/−57		dB
	50 MHz, 300 meters of cable, G = 1/G = 2		5/10		dB
	100 MHz, 300 meters of cable, G = 1/G = 2		10/14		dB
Input Resistance	Common mode		4.4		MΩ
	Differential		3.7		MΩ
Input Capacitance	Common mode		1.0		pF
	Differential		0.5		pF
Input Bias Current			1.1		µA
ADJUSTMENT PINS					
V_{PEAK} Input Voltage Range	Relative to ground		0 to 2		V
V_{GAIN} Input Voltage Range	Relative to ground		0 to 2		V
V_{OFFSET} Input Current			1.1		µA
V_{GAIN} Input Current			−0.5		µA
V_{PEAK} Input Current			±0.6		µA
V_{FILTER} Input Current			0.5		µA
V_{OFFSET} to OUT_x Gain	$OUT_x = OUT_R$, OUT_G, OUT_B, range limited by output swing, V_{GAIN} = 0 V, G = 1		1		V/V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	G = 1, G = 2		−3.9 to +3.9		V
Output Offset Voltage	RTO, $V_{PEAK} = V_{GAIN} = V_{FILTER} = V_{OFFSET}$ = 0 V, G = 1/G = 2		±4/±8		mV
	RTO, 300 meters of cable, G = 1/G = 2		±10/±30		mV
Output Offset Voltage Drift	RTO, G = 1/G = 2		2.6/3.2		µV/°C

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMPARATORS					
Output Voltage Level Low, V_{OL}			0.3		V
Output Voltage Level High, V_{OH}			3.3		V
Hysteresis, V_{HYST}			70		mV
Propagation Delay					
Low to High, $t_{PD, LH}$			14		ns
High to Low, $t_{PD, HL}$			10		ns
Rise Time, t_{RISE}			8		ns
Fall Time, t_{FALL}			7		ns
Output Resistance, V_{OL}			18		Ω
Output Resistance, V_{OH}			1		Ω
DIGITAL CONTROLS					
COAX/$\overline{\text{UTP}}$ Pin					
Input Voltage Level Low, V_{IL}				1.5	V
Input Voltage Level High, V_{IH}		3.5			V
Input Current, Low			±0.7		µA
Input Current, High			24		µA
$\overline{\text{PD}}$ Pin					
Input Voltage Level Low, V_{IL}				2.9	V
Input Voltage Level High, V_{IH}		3.2			V
Input Current, Low			1		µA
Input Current, High			1		µA
POWER SUPPLY					
Operating Voltage Range		±4.5		±5.5	V
Positive Quiescent Supply Current			120		mA
Negative Quiescent Supply Current			66		mA
Supply Current Drift, I_{CC}			210		µA/°C
Supply Current Drift, I_{EE}			−120		µA/°C
Positive Power Supply Rejection	$\Delta V_{OUT}/\Delta V_{SUPPLY}$				
	DC, RTO, 0 meters of cable, G = 1/G = 2		−72/−66		dB
	DC, RTO, 300 meters of cable, G = 1/G = 2		−68/−62		dB
	100 MHz, RTO, 300 meters of cable, G = 1/G = 2		5/8		dB
Negative Power Supply Rejection	$\Delta V_{OUT}/\Delta V_{SUPPLY}$				
	DC, RTO, 0 meters of cable, G = 1/G = 2		−88/−80		dB
	DC, RTO, 300 meters of cable, G = 1/G = 2		−80/−74		dB
	100 MHz, RTO, 300 meters of cable, G = 1/G = 2		18/14		dB
Positive Supply Current, Powered Down	$V_{PEAK} = V_{GAIN} = V_{FILTER} = 0$ V		3.4		mA
Negative Supply Current, Powered Down	$V_{PEAK} = V_{GAIN} = V_{FILTER} = 0$ V		0.4		mA
OPERATING TEMPERATURE RANGE		−40		+85	°C

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	11 V
Power Dissipation	See Figure 2
Input Voltage (Any Input)	V_{S-} − 0.3 V to V_{S+} + 0.3 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, the device soldered in a circuit board in still air. This value was measured using a JEDEC standard 4-layer printed circuit board (PCB).

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP	39	1.3	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8122 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8122. Exceeding a junction temperature of 175°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_{S+} and V_{S-}) times the quiescent current (I_S). The power dissipation due to each load current is calculated by multiplying the load current by the voltage difference between the associated power supply and the output voltage. The total power dissipation due to load currents is then obtained by taking the sum of the individual power dissipations. RMS output voltages must be used when dealing with ac signals.

Airflow reduces θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}. The exposed pad on the underside of the package must be soldered to a pad on the PCB surface that is thermally connected to a solid plane (usually the ground plane) to achieve the specified θ_{JA}.

Figure 2 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 40-lead LFCSP (θ_{JA} = 39°C/W) on a JEDEC standard 4-layer board with the exposed pad soldered to a pad that is thermally connected to a PCB plane. θ_{JA} values are approximations.

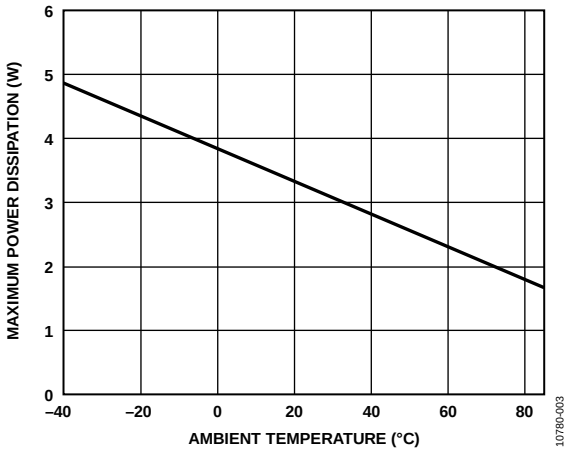


Figure 2. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

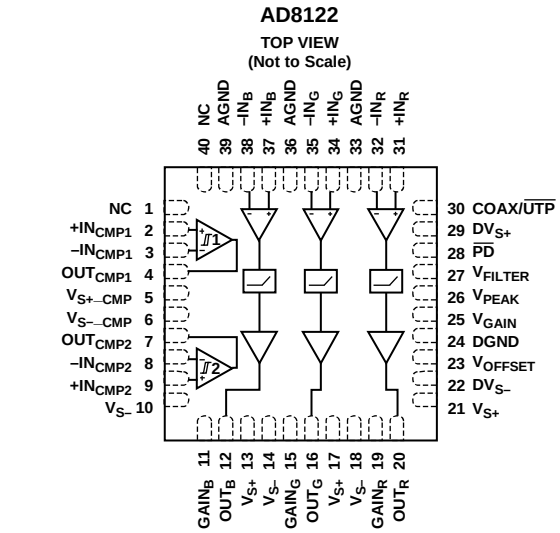


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 40	NC	No Internal Connection.
2	$+IN_{CMP1}$	Positive Input, Comparator 1.
3	$-IN_{CMP1}$	Negative Input, Comparator 1.
4	OUT_{CMP1}	Output, Comparator 1.
5	V_{S+_CMP}	Positive Power Supply, Comparator. Connect to +5 V.
6	V_{S-_CMP}	Negative Power Supply, Comparator. Connect to −5 V.
7	OUT_{CMP2}	Output, Comparator 2.
8	$-IN_{CMP2}$	Negative Input, Comparator 2.
9	$+IN_{CMP2}$	Positive Input, Comparator 2.
10, 14, 18	V_{S-}	Negative Power Supply, Equalizer Sections. Connect to −5 V.
11	$GAIN_B$	Blue Channel Gain. Connect to OUT_B for G = 1; connect to AGND for G = 2.
12	OUT_B	Output, Blue Channel.
13, 17, 21	V_{S+}	Positive Power Supply, Equalizer Sections. Connect to +5 V.
15	$GAIN_G$	Green Channel Gain. Connect to OUT_G for G = 1; connect to AGND for G = 2.
16	OUT_G	Output, Green Channel.
19	$GAIN_R$	Red Channel Gain. Connect to OUT_R for G = 1; connect to AGND for G = 2.
20	OUT_R	Output, Red Channel.
22	DV_{S-}	Negative Power Supply, Digital Control. Connect to −5 V.
23	V_{OFFSET}	Output Offset Control Voltage.
24	DGND	Digital Ground Reference.
25	V_{GAIN}	Broadband Flat Gain Control Voltage.
26	V_{PEAK}	Equalizer High Frequency Boost Control Voltage.
27	V_{FILTER}	Low-Pass Filter Cutoff Frequency Adjustment Control Voltage.
28	$\overline{PD}$	Power-Down.
29	DV_{S+}	Positive Power Supply, Digital Control. Connect to +5 V.
30	$COAX/\overline{UTP}$	Cable Compensation Control Input. Connect this pin to Logic 1 for coaxial cable; connect this pin to Logic 0 for UTP cable. This input can be left floating in UTP applications.

Pin No.	Mnemonic	Description
31	$+IN_R$	Positive Input, Red Channel.
32	$-IN_R$	Negative Input, Red Channel.
33, 36, 39	AGND	Analog Ground Reference.
34	$+IN_G$	Positive Input, Green Channel.
35	$-IN_G$	Negative Input, Green Channel.
37	$+IN_B$	Positive Input, Blue Channel.
38	$-IN_B$	Negative Input, Blue Channel.
	EP	Exposed Pad. To achieve the specified thermal resistance, the exposed pad on the underside of the package must be soldered to a pad on the PCB surface that is thermally connected to a solid plane with voltage between V_S+ and V_S-.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±5 V, Category 5e UTP cable, input V_{CM} = 0 V, V_{OFFSET} = 0 V, V_{PEAK}, V_{GAIN}, and V_{FILTER} are set to the recommended settings shown in Figure 24, unless otherwise noted. For G = 2, R_L = 150 Ω and V_{OUT} = 2 V p-p; for G = 1, R_L = 1 kΩ and V_{OUT} = 1 V p-p.

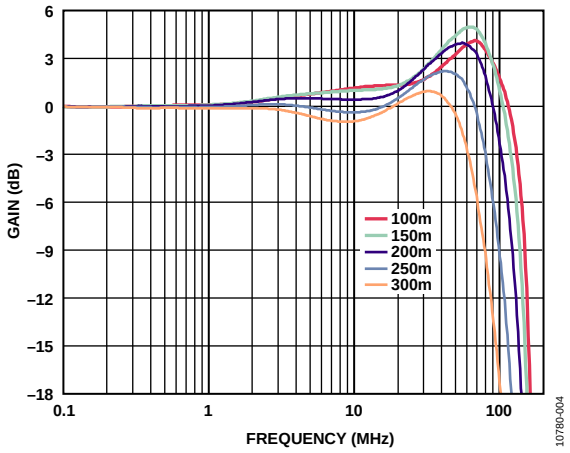


Figure 4. Equalized Frequency Response for Various UTP Cable Lengths, G = 1

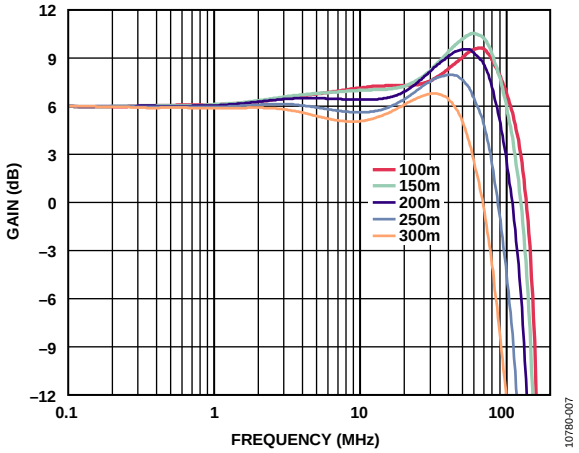


Figure 7. Equalized Frequency Response for Various UTP Cable Lengths, G = 2

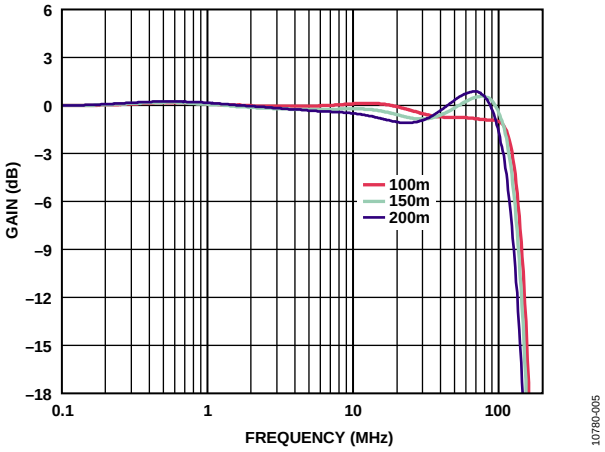


Figure 5. Equalized Frequency Response for Various Coaxial Cable Lengths, G = 1

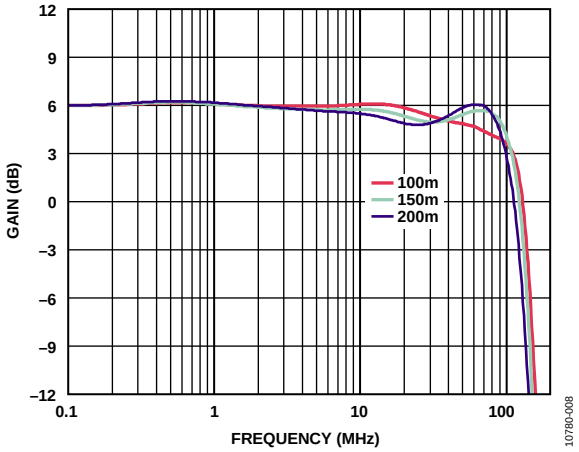


Figure 8. Equalized Frequency Response for Various Coaxial Cable Lengths, G = 2

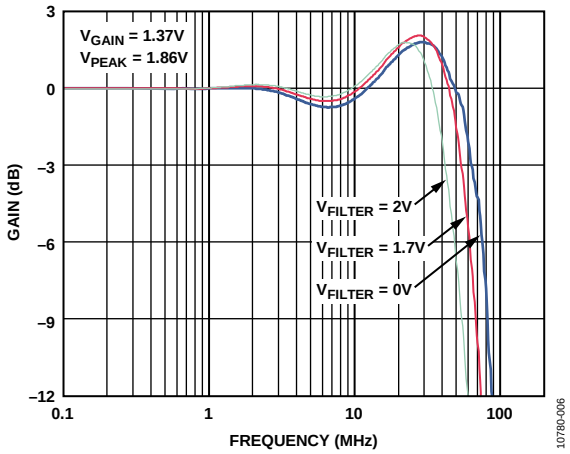


Figure 6. Equalized Frequency Response for Various V_{FILTER} Levels, 300 m Cable Length, G = 1

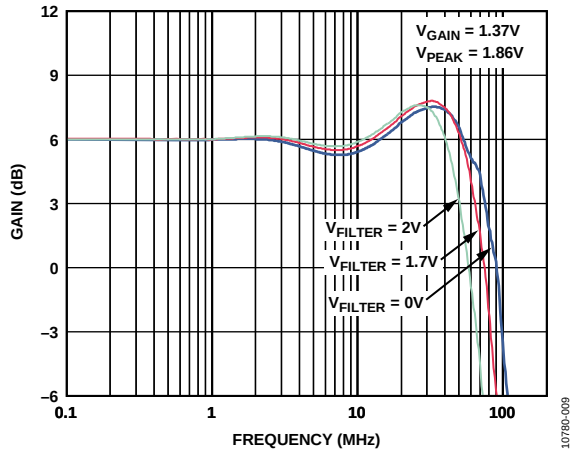


Figure 9. Equalized Frequency Response for Various V_{FILTER} Levels, 300 m Cable Length, G = 2

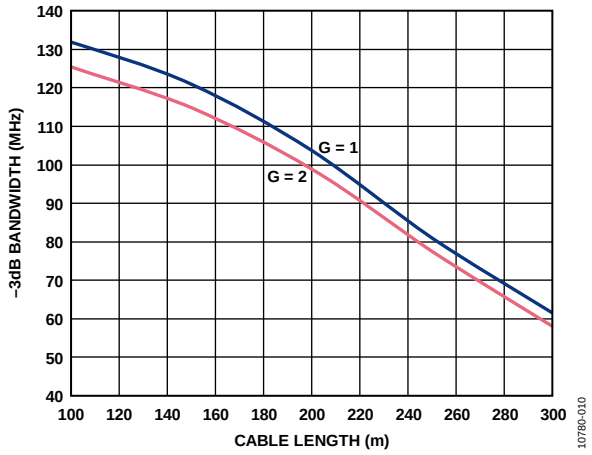


Figure 10. Equalized –3 dB Bandwidth vs. Cable Length

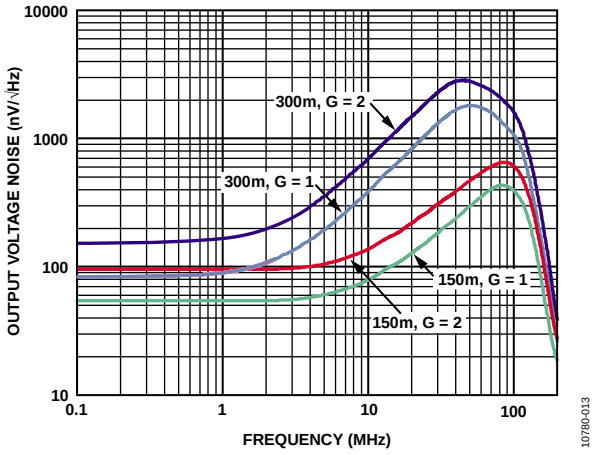


Figure 13. Voltage Noise Density vs. Frequency for 300 m and 150 m Cable Lengths, RTO

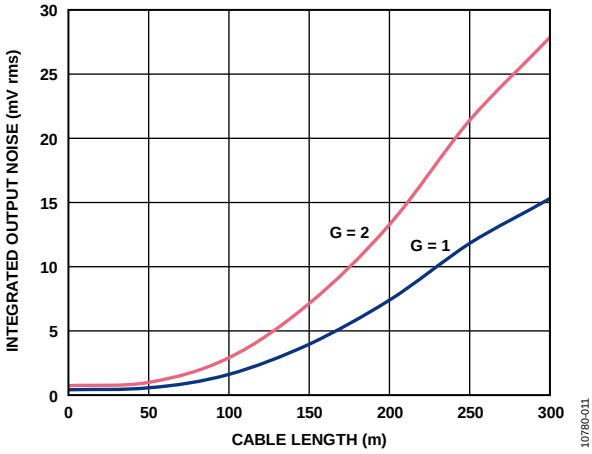


Figure 11. Integrated Output Noise (1 MHz to 160 MHz) vs. Cable Length

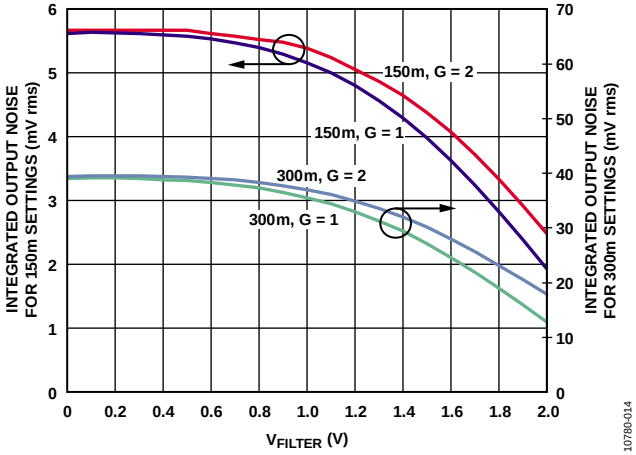


Figure 14. Integrated Output Noise (1 MHz to 160 MHz) vs. V_{FILTER} for 300 m and 150 m Cable Lengths

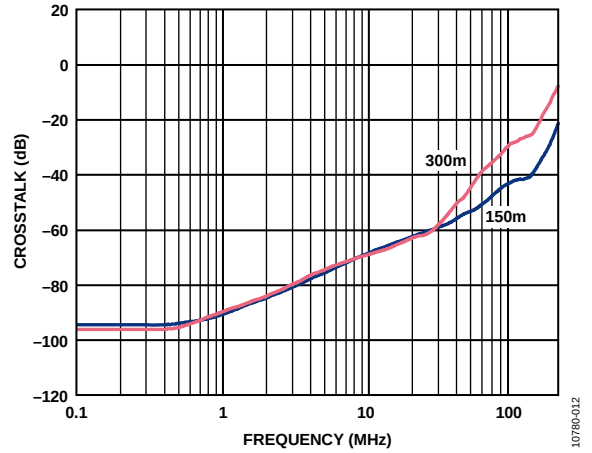


Figure 12. Crosstalk vs. Frequency for 300 m and 150 m Cable Lengths, G = 1

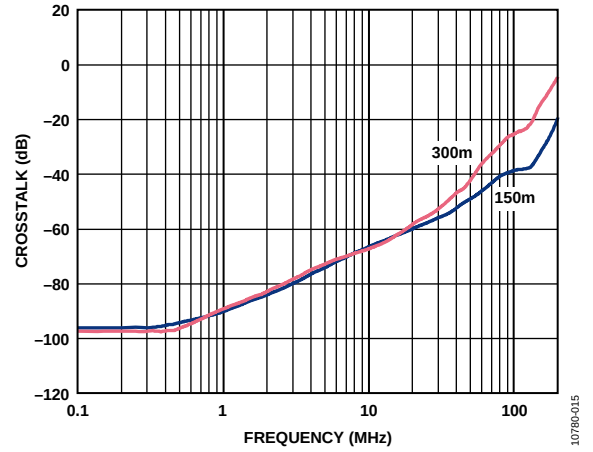


Figure 15. Crosstalk vs. Frequency for 300 m and 150 m Cable Lengths, G = 2

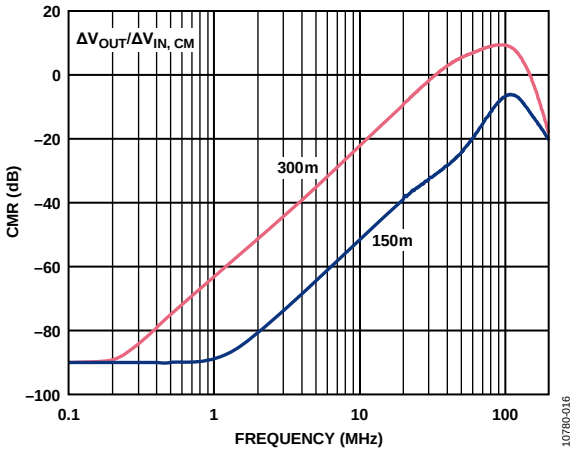


Figure 16. Input Common-Mode Rejection vs. Frequency for 300 m and 150 m Cable Lengths, G = 1

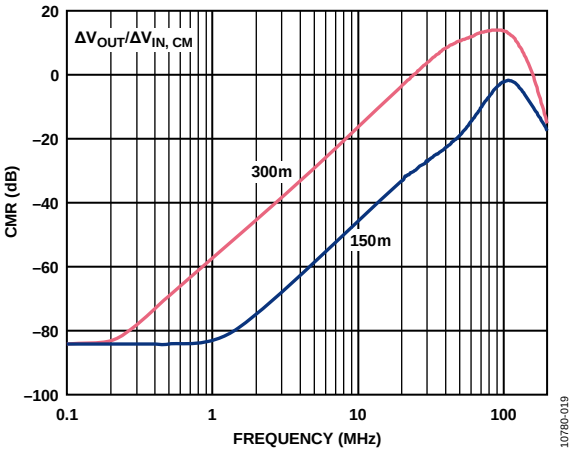


Figure 19. Input Common-Mode Rejection vs. Frequency for 300 m and 150 m Cable Lengths, G = 2

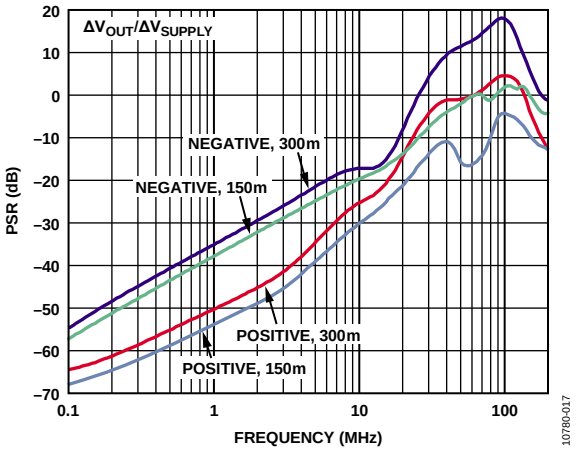


Figure 17. Power Supply Rejection vs. Frequency for 300 m and 150 m Cable Lengths, G = 1

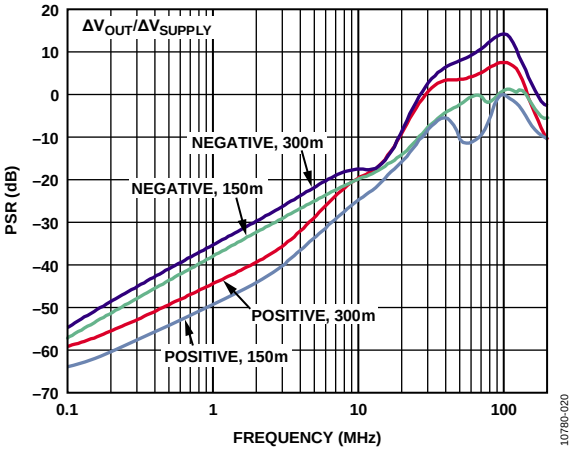


Figure 20. Power Supply Rejection vs. Frequency for 300 m and 150 m Cable Lengths, G = 2

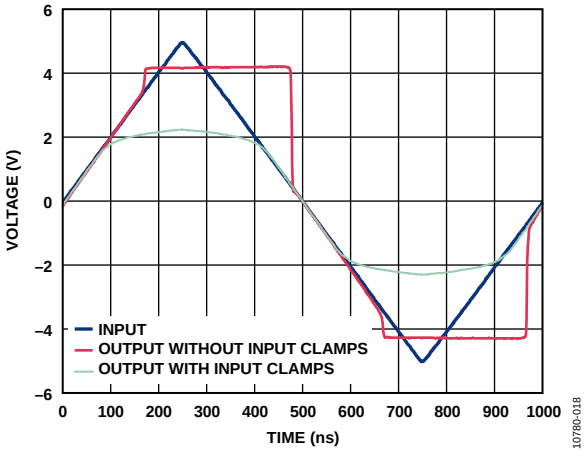


Figure 18. Overdrive Recovery, G = 1

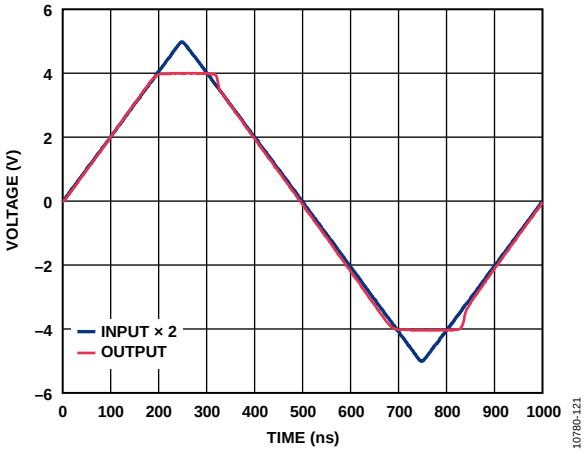


Figure 21. Overdrive Recovery, G = 2

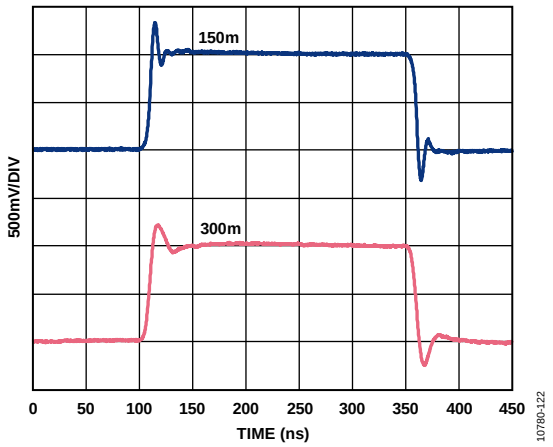


Figure 22. Equalized Pulse Response for 300 m and 150 m Cable Lengths (2 MHz), G = 1

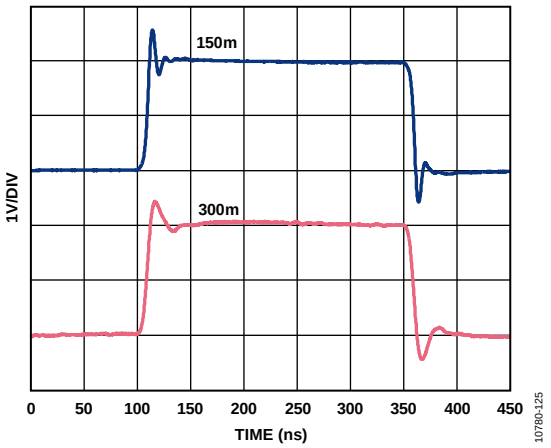


Figure 25. Equalized Pulse Response for 300 m and 150 m Cable Lengths (2 MHz), G = 2

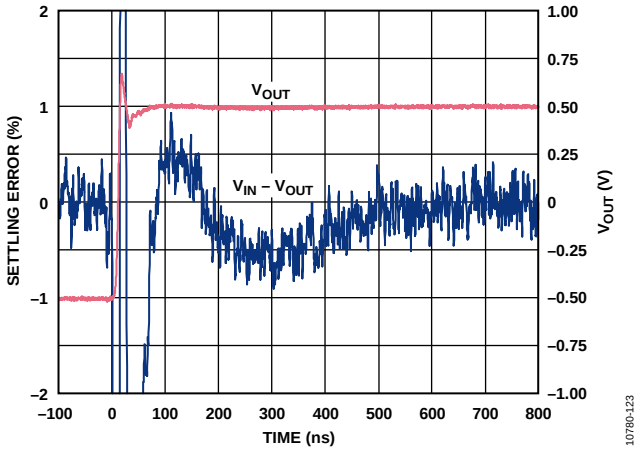


Figure 23. Settling Time to 1%, 300 m Cable Length, G = 1

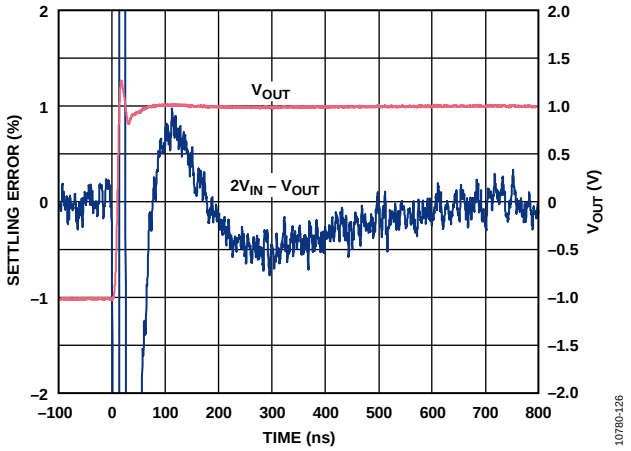


Figure 26. Settling Time to 1%, 300 m Cable Length, G = 2

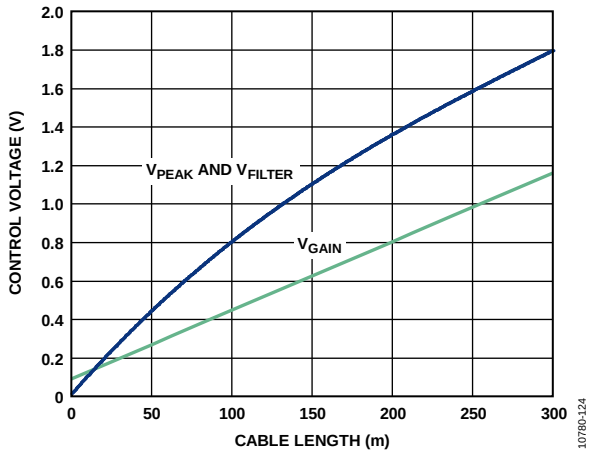


Figure 24. Recommended Settings for UTP Cable

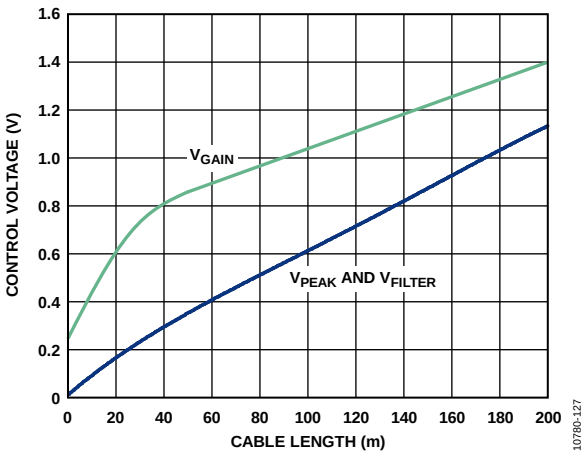


Figure 27. Recommended Settings for Coaxial Cable

THEORY OF OPERATION

The AD8122 is a triple, wideband, low noise analog line equalizer that compensates for losses in UTP cables up to 300 meters in length and coaxial cables up to 200 meters in length. The 3-channel architecture is targeted at high resolution RGB applications, but can be used in HD YPbPr applications as well. The transfer function of the AD8122 can be pin selected for UTP or coaxial cable, and the gain of each channel can be set to 1 or 2.

ADJUSTABLE CONTROL VOLTAGES

Four continuously adjustable control voltages, common to the RGB channels, are available to the designer to provide compensation for various cable lengths, as well as for variations in the cable itself.

- The V_{PEAK} pin is used to control the amount of high frequency peaking. The V_{PEAK} control is used to compensate for frequency dependent losses and cable length dependent losses that are present due to the skin effect of the cable.
- The V_{GAIN} pin is used to adjust broadband gain to compensate for low frequency flat losses present in the cable.
- The V_{FILTER} pin is used to adjust the cutoff frequency of the output low-pass filters.
- The V_{OFFSET} pin is an output offset adjustment control that allows the designer to shift the output dc level.

DIFFERENTIAL INPUTS

The AD8122 has high impedance differential inputs that make termination simple and allow dc-coupled signals to be received directly from the cable. The AD8122 inputs can also be used in a single-ended fashion in coaxial cable applications. For differential systems that require a very wide input common-mode range, the AD8143 high voltage, triple differential receiver can be placed in front of the AD8122. For more information, see the Input Common-Mode Range section.

OUTPUTS

The AD8122 has low impedance outputs that are capable of driving a 150 Ω load. In systems where the AD8122 must drive a high impedance capacitive load, it is recommended that a small series resistor be placed between the output and the load to buffer the capacitance. The resistor should not be so large as to reduce the overall bandwidth to an unacceptable level. For more information, see the Driving High Impedance Capacitive Loads section.

ON-CHIP COMPARATORS

Two on-chip comparators can be used for sync pulse extraction in systems that use common-mode sync pulse encoding (see the Sync Pulse Extraction Using Comparators section).

Each comparator can be used in a source-only cable termination scheme by placing a resistor in series with the comparator output. For more information, see the Comparator Applications section.

INPUT SINGLE-ENDED VOLTAGE RANGE CONSIDERATIONS

When using the AD8122 as a receiver, it is important to ensure that its single-ended input voltages stay within their specified ranges. The received single-ended level for each input is calculated by adding the common-mode level of the driver, the single-ended peak amplitude of the received signal, the amplitude of any sync pulses, and other induced common-mode signals, such as ground shifts between the driver and the AD8122 and pickup from external sources, such as power lines and fluorescent lights. For more information, see the Input Common-Mode Range section.

APPLICATIONS INFORMATION

BASIC OPERATION

The AD8122 is easy to apply because it contains on chip all components needed for cable loss compensation. Figure 30 shows a basic application circuit for common-mode sync pulse extraction that is compatible with the common-mode sync pulse encoding technique used in the AD8134, AD8142, AD8147, and AD8148 triple differential drivers. If sync pulse extraction is not required, the terminations can be single 100 Ω resistors, and the comparator inputs can be left floating.

INPUT OVERDRIVE RECOVERY AND PROTECTION

Occasional large differential transients can occur on the cable due to a number of causes, such as ESD and switching. When operating the AD8122 at G = 1, a differential input that exceeds +3.4 V or −3.4 V causes the output to "stick" at the associated power supply rail (positive rail for positive overdrive, negative rail for negative overdrive). The overdrive condition does not occur in applications with G = 2.

The AD8122 recovers from the overdrive condition when the magnitude of the differential input falls below 200 mV. Most video signals return to 0 V nominal during the blanking intervals; therefore, recovery from the overdrive condition in systems that use these signals occurs during the first blanking interval after the overdrive event has ended.

In systems with G = 1 and video signals that do not return to 0 V—for example, systems that include dc offsets—it is necessary to prevent the overdrive condition from occurring. Figure 28 shows a protection circuit that limits the differential input voltage to a little over ±2 V. This circuit should be placed between the termination resistors and each AD8122 differential input.

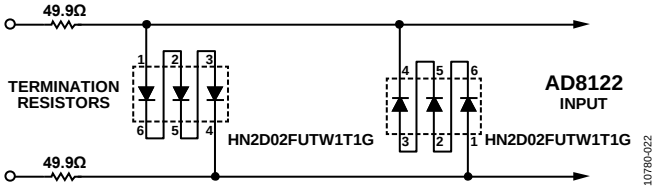


Figure 28. Required Input Protection for Applications with G = 1

COMPARATOR APPLICATIONS

The two on-chip comparators are most often used to extract video sync pulses from the received common-mode voltages (see the Sync Pulse Extraction Using Comparators section). However, the comparators can also be used to recover sync pulses in sync-on-color applications, to receive differential digital information received on other channels such as the fourth UTP pair, or as general-purpose comparators. Built-in hysteresis helps to eliminate false triggers from noise.

An ideal source terminated transmission line has a source resistance that exactly matches the characteristic impedance of the line and a load impedance that is infinite. When the signal is launched into the source termination, the initial value of the signal is one-half the source value because the signal amplitude is divided by 2 in the voltage divider formed by the source termination and the transmission line. At the load, the signal experiences 100% positive reflection due to the infinite load impedance and is restored to its full value. This technique is commonly used in PCB layouts that involve high speed digital logic.

The comparators are designed to drive source terminated transmission lines and have output resistances of 18 Ω in the low state and 1 Ω in the high state. Because the output resistances are different for each state, a compromise must be made in selecting the external source termination resistor value to match the transmission line impedance. The best approximation to a 50 Ω match that can be achieved in this case is with an external resistor value of approximately 41.2 Ω, which is available as a standard 1% value. See Figure 29 for an illustration of the source termination technique.

Impedance mismatches occur in both the high state and the low state due to the differences in output resistances, resulting in a reflection coefficient of approximately +8.4% (21.5 dB return loss) in the low state, where the total source resistance is 59.2 Ω, and −8.4% (21.5 dB return loss) in the high state, where the total source resistance is 42.2 Ω. This source match is acceptable for digital sync pulses.

Figure 29 shows how to apply source termination to the comparators when driving a 50 Ω transmission line that is high impedance at its receive end.

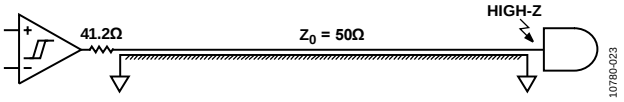


Figure 29. Using a Comparator with Source Termination

SYNC PULSE EXTRACTION USING COMPARATORS

The AD8122 is useful in many systems that transport computer video signals, which typically comprise red, green, and blue video signals, as well as separate horizontal and vertical sync signals (RGBHV). Because the sync signals are separate and not embedded in the color signals, it is advantageous to transmit them using a simple scheme that encodes them on the three common-mode voltages of the RGB signals. The AD8134, AD8142, AD8147, and AD8148 triple differential drivers are natural complements to the AD8122 because they perform the sync pulse encoding with the necessary circuitry on chip.

The sync encoding equations are as follows:

$$Red\ V_{CM} = \frac{K}{2}\left[V - H\right] \quad (1)$$

$$Green\ V_{CM} = \frac{K}{2}\left[-2\ \mathrm{V}\right] \quad (2)$$

$$Blue\ V_{CM} = \frac{K}{2}\left[V + H\right] \quad (3)$$

where:

Red V_{CM}, *Green* V_{CM}, and *Blue* V_{CM} are the transmitted common-mode voltages of the respective color signals.

K is an adjustable gain constant that is set by the driver.

V and H are the vertical and horizontal sync pulses, respectively, defined with a weight of −1 when the pulses are in their low states and a weight of +1 when the pulses are in their high states.

For more information about the encoding scheme, see the data sheets for the AD8134, AD8142, AD8147, and AD8148 drivers. Figure 30 shows how the AD8122 comparators can be used to extract the horizontal and vertical sync pulses that are encoded on the RGB common-mode voltages by the drivers.

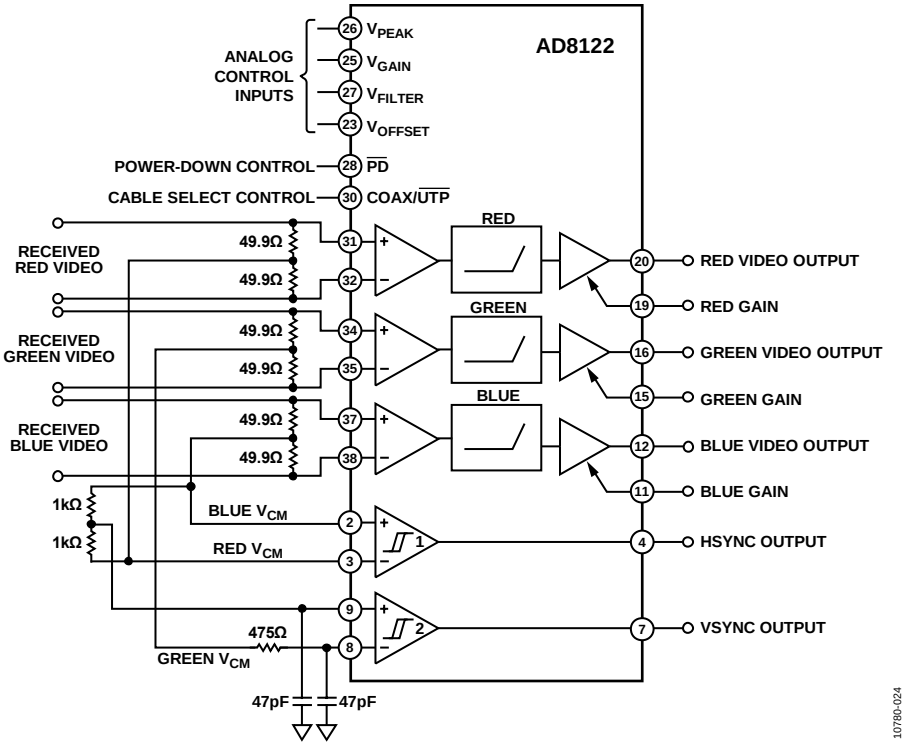


Figure 30. Basic Application Circuit with Common-Mode Sync Pulse Extraction (Supplies and Input Protection Not Shown)

USING THE V_{PEAK}, V_{GAIN}, V_{FILTER}, AND V_{OFFSET} INPUTS

The V_{PEAK} input is the main peaking control and is used to compensate for the low-pass roll-off in the cable response. The V_{GAIN} input controls the broadband flat gain and is used to compensate for the cable loss that is nominally flat.

The output of each channel contains an on-chip adjustable low-pass filter to reduce high frequency noise. In most applications, the filter cutoff frequency control, V_{FILTER}, is connected directly to the V_{PEAK} voltage to provide the maximum bandwidth and minimum noise for a given V_{PEAK} setting. External low-pass filters are generally not required.

The V_{OFFSET} input is used to produce an offset at the AD8122 output. The output offset is equal to the voltage applied to the V_{OFFSET} input, limited by the output swing limits.

USING THE COAX/$\overline{\text{UTP}}$ SELECTOR

Connect the COAX/$\overline{\text{UTP}}$ input to Logic 1 for coaxial cable or to Logic 0 for UTP cable (see Table 1 for the logic levels). This input has an internal pull-down resistor and can, therefore, be left floating in UTP applications.

DRIVING HIGH IMPEDANCE CAPACITIVE LOADS

In many applications that use RGB over UTP cable, delay correction is required to remove the skew that exists among the three pairs used to carry the RGB signals. The AD8120 is ideally suited to perform this skew correction and can be placed immediately following the AD8122 in the receiver signal chain. The AD8120 has a high input impedance and a fixed gain of 2. When using the AD8120 with the AD8122, configure the AD8122 for a gain of 1 by connecting each video output (OUT_R, OUT_G, and OUT_B) to its respective gain pin ($GAIN_R$, $GAIN_G$, and $GAIN_B$).

In systems where the AD8122 must drive a high impedance capacitive load, a small series resistor must be placed between each of the three AD8122 video outputs and the load to buffer the input capacitance of the device being driven. The resistor value must be small enough to preserve the required bandwidth.

DRIVING 75 Ω CABLE WITH THE AD8122

When the RGB outputs must drive a 75 Ω line instead of a high impedance load, an additional gain of 2 is required to make up for the double termination loss (75 Ω source and load terminations). Each output of the AD8122 (OUT_R, OUT_G, or OUT_B) is easily configured for a gain of 2 by grounding its respective gain pin ($GAIN_R$, $GAIN_G$, or $GAIN_B$).

LAYOUT AND POWER SUPPLY DECOUPLING CONSIDERATIONS

Standard high speed PCB layout practices should be adhered to when designing with the AD8122. A solid ground plane is required, and controlled impedance traces should be used when interconnecting the high speed signals. Place source termination resistors on all of the outputs as close as possible to the output pins.

The exposed pad on the underside of the AD8122 must be soldered to a pad on the PCB surface that is thermally connected to a solid plane (usually the ground plane) to achieve the specified θ_{JA}. Use several thermal vias to make the connection between the pad and the PCB planes.

Place high quality 0.1 µF power supply decoupling capacitors as close as possible to all of the supply pins; use small surface-mount ceramic capacitors. For bulk supply decoupling, tantalum capacitors are recommended.

INPUT COMMON-MODE RANGE

Most applications that use the AD8122 as a receiver use a driver powered from ±5 V supplies. (Suggested drivers include the AD8146, AD8147, AD8148, AD8133, and AD8134.) In such applications, the common-mode voltage on the line is placed at a nominal 0 V relative to the ground potential at the driver and provides optimum immunity from any common-mode anomalies picked up along the cable (including ground shifts between the driver and receiver ends).

The AD8122 input voltage range of ±4 V typical is sufficient for many of these applications. If a wider input range is required, the AD8143 triple receiver (with an input common-mode range of ±10.5 V on ±12 V supplies) can be placed in front of the AD8122. Figure 31 shows this configuration for one channel.

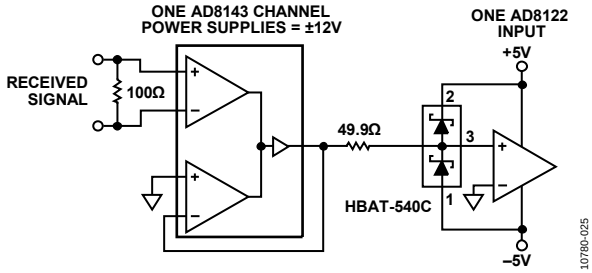


Figure 31. Optional Use of the AD8143 in Front of the AD8122 for Wide Input Common-Mode Range

The Schottky diodes are required to protect the AD8122 from any AD8143 outputs that exceed the AD8122 input limits. The 49.9 Ω resistor limits the fault current and produces a pole at approximately 800 MHz with the effective diode capacitance of 3 pF and the AD8122 input capacitance of 1 pF. The pole lowers the response by only 0.07 dB at 100 MHz and, therefore, has a negligible effect on the signal.

When using a single 5 V supply on the driver side, the common-mode voltage at the driver output is typically 2.5 V (in the case of the AD8142 driver, the common-mode voltage at the output is fixed at 1.5 V). The largest received differential video signal is approximately 700 mV p-p, which adds 175 mV_{PEAK} to each single-ended side of the differential signal and results in a worst-case peak voltage of 2.675 V or 1.675 V on an AD8122 single-ended input (assuming that there is no ground shift between the driver and receiver). Because these levels are within the AD8122 input voltage swing limits, such a system works well as long as the difference in ground potential between the driver and receiver does not cause the input voltage swing to exceed these limits.

When used, common-mode sync signals are generally applied with a peak deviation of 500 mV during the blanking intervals (video signal = 0 V), increasing the common-mode level from 2.5 V to 3.0 V (1.5 V to 2.0 V in the case of the AD8142 driver).

These common-mode levels are below the upper input voltage swing limit of 4 V and, therefore, leave a margin of 1 V or 2 V for ground shifts between the driver and receiver. To increase the common-mode range of the overall system, use one or both of these techniques:

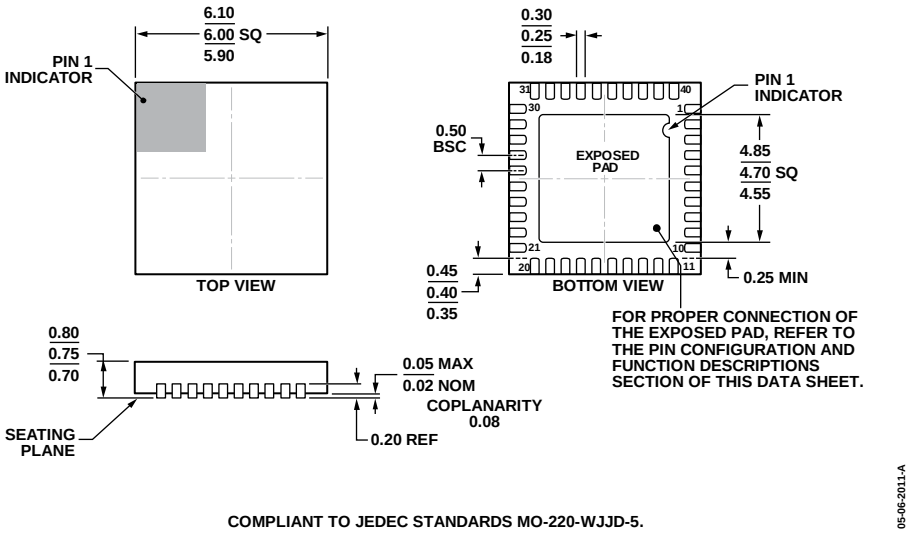
- Power the driver from dual supplies (output common-mode voltage = 0 V).
- Place an AD8143 in front of the AD8122, as shown in Figure 31.

These techniques can be combined or applied separately.

POWER-DOWN

The power-down feature can be used to reduce power consumption when a particular device is not in use. When asserted, the $\overline{PD}$ pin does not place the output in a high-Z state. The input logic levels and supply current in power-down mode are listed in Table 1.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD-5.

Figure 32. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8122ACPZ	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-12
AD8122ACPZ-R7	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-12
AD8122-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

NOTES

D10780-0-7/12(0)

AMEYA360
Components Supply Platform

Authorized Distribution Brand :

Website :

Welcome to visit www.ameya360.com

Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com