

## FEATURES

- Supports GR-1244 Stratum 3 stability in holdover mode
- Supports smooth reference switchover with virtually no disturbance on output phase
- Supports Telcordia GR-253 jitter generation, transfer, and tolerance for SONET/SDH up to OC-192 systems
- Supports ITU-T G.8262 synchronous Ethernet slave clocks
- Supports ITU-T G.823, ITU-T G.824, ITU-T G.825, and ITU-T G.8261
- Auto/manual holdover and reference switchover
- Adaptive clocking allows dynamic adjustment of feedback dividers for use in OTN mapping/demapping applications
- Quad digital phase-locked loop (DPLL) architecture with four reference inputs (single-ended or differential)
- 4 × 4 crosspoint allows any reference input to drive any PLL
- Input reference frequencies from 2 kHz to 1000 MHz
- Reference validation and frequency monitoring: 2 ppm
- Programmable input reference switchover priority
- 20-bit programmable input reference divider
- 4 differential clock outputs with each differential pair configurable as HCSL, LVDS compatible, or LVPECL compatible
- Output frequency range: 430 kHz to 941 MHz
- Programmable 18-bit integer and 24-bit fractional feedback divider in digital PLL
- Programmable loop bandwidths from 0.1 Hz to 4 kHz
- 56-lead (8 mm × 8 mm) LFCSP package

## APPLICATIONS

- Network synchronization, including synchronous Ethernet and synchronous digital hierarchy (SDH) to optical transport network (OTN) mapping/demapping
- Cleanup of reference clock jitter
- SONET/SDH clocks up to OC-192, including FEC
- Stratum 3 holdover, jitter cleanup, and phase transient control
- Cable infrastructure
- Data communications
- Professional video

## GENERAL DESCRIPTION

The [AD9554-1](#) is a low loop bandwidth clock translator that provides jitter cleanup and synchronization for many systems, including synchronous optical networks (SONET/SDH). The [AD9554-1](#) generates an output clock synchronized to up to four external input references. The digital PLLs (DPLLs) allow reduction of input time jitter or phase noise associated with the external references. The digitally controlled loop and holdover circuitry of the [AD9554-1](#) continuously generates a low jitter output clock even when all reference inputs have failed.

The [AD9554-1](#) operates over an industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . The [AD9554](#) is a version of this device with two outputs per PLL. If a single or dual DPLL version of this device is needed, refer to the [AD9557](#) or [AD9559](#), respectively.

## FUNCTIONAL BLOCK DIAGRAM

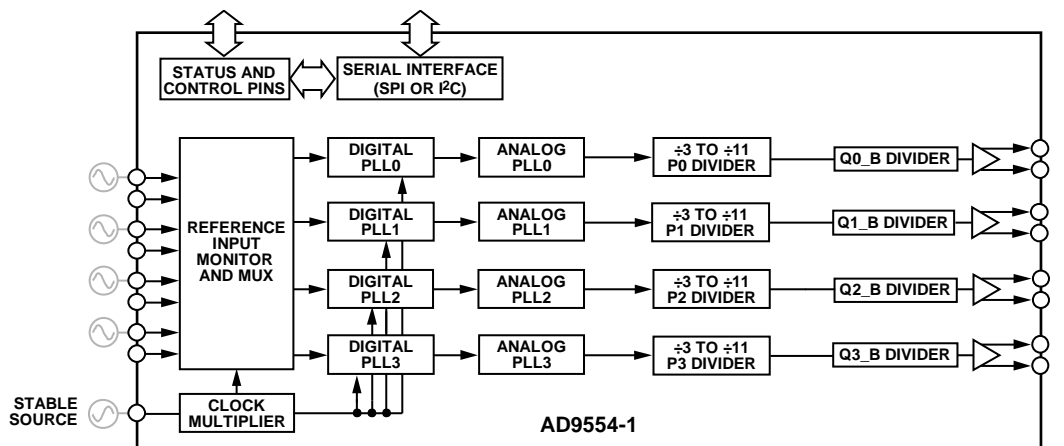


Figure 1.

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**REVISION HISTORY**

**8/14—Rev. 0 to Rev. A**

Added Bandwidth ( $f_{REF} = 19.44$  MHz;  $f_{OUT} = 156.25$  MHz;  
 $f_{LOOP} = 50$  Hz) Parameters; Table 18 ..... 15  
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**6/14—Revision 0: Initial Version**

## SPECIFICATIONS

Minimum (min) and maximum (max) values apply for the full range of supply voltage and operating temperature variations. Typical (typ) values apply for VDD = 1.8 V; T<sub>A</sub> = 25°C, unless otherwise noted.

### SUPPLY VOLTAGE

Table 1.

| Parameter                          | Min  | Typ | Max   | Unit |
|------------------------------------|------|-----|-------|------|
| SUPPLY VOLTAGE FOR 1.8 V OPERATION |      |     |       |      |
| VDD_SP                             | 1.47 | 1.8 | 2.625 | V    |
| VDD                                | 1.71 | 1.8 | 1.89  | V    |
| SUPPLY VOLTAGE FOR 1.5 V OPERATION |      |     |       |      |
| VDD_SP                             | 1.47 | 1.5 | 2.625 | V    |
| VDD                                | 1.47 | 1.5 | 1.53  | V    |

### SUPPLY CURRENT

The test conditions for the maximum (max) supply current are at the maximum supply voltage found in Table 1. The test conditions for the typical (typ) supply current are at the typical supply voltage found in Table 1. The test conditions for the minimum (min) supply current are at the minimum supply voltage found in Table 1.

Table 2.

| Parameter                                           | Min  | Typ  | Max | Unit | Test Conditions/Comments                                                                                               |
|-----------------------------------------------------|------|------|-----|------|------------------------------------------------------------------------------------------------------------------------|
| SUPPLY CURRENT FOR TYPICAL CONFIGURATION            |      |      |     |      |                                                                                                                        |
| I <sub>VDD_SP</sub>                                 | 0.01 | 0.04 | 0.1 | mA   | Typical values are for the Typical Configuration parameter listed in Table 3; valid for both 1.5 V and 1.8 V operation |
| I <sub>VDD</sub>                                    | 450  | 513  | 560 | mA   |                                                                                                                        |
| SUPPLY CURRENT FOR ALL BLOCKS RUNNING CONFIGURATION |      |      |     |      |                                                                                                                        |
| I <sub>VDD_SP</sub>                                 | 0.01 | 0.04 | 0.1 | mA   | Maximum values are for the All Blocks Running parameter listed in Table 3; valid for both 1.5 V and 1.8 V operation    |
| I <sub>VDD</sub>                                    | 450  | 566  | 650 | mA   |                                                                                                                        |

**POWER DISSIPATION**

Typical (typ) values apply for VDD = 1.8 V and maximum (max) values for VDD = 1.89 V.

Table 3.

| Parameter                         | Min | Typ  | Max | Unit | Test Conditions/Comments                                                                                                                                                                                   |
|-----------------------------------|-----|------|-----|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POWER DISSIPATION                 |     |      |     |      |                                                                                                                                                                                                            |
| Typical Configuration             |     | 0.92 | 1.1 | W    | System clock: 49.152 MHz crystal; four DPLLs active; two 19.44 MHz input references in differential mode; four ac-coupled output drivers in 21 mA mode at 644.53125 MHz;                                   |
| All Blocks Running                |     | 1.02 | 1.2 | W    | System clock: 49.152 MHz crystal; four DPLLs active, four 19.44 MHz input references in differential mode; eight ac-coupled output drivers in 28 mA mode at 750 MHz                                        |
| Full Power-Down                   |     | 164  |     | mW   | Measured using the Typical Configuration parameter (see Table 3) and then setting the full power-down bit                                                                                                  |
| Incremental Power Dissipation     |     |      |     |      | Typical configuration; table values show the change in power due to the indicated operation                                                                                                                |
| Complete DPLL/APLL On/Off         |     | 190  |     | mW   | Power delta computed relative to the typical configuration; the blocks powered down include one reference input, one DPLL, one APLL, one P divider, two channel dividers, two output drivers in 28 mA mode |
| Input Reference On/Off            |     |      |     |      |                                                                                                                                                                                                            |
| Differential (Normal Mode)        |     | 22.5 |     | mW   | $f_{REF} = 19.44$ MHz                                                                                                                                                                                      |
| Differential (DC-Coupled LVDS)    |     | 24.6 |     | mW   | $f_{REF} = 19.44$ MHz                                                                                                                                                                                      |
| Single-Ended                      |     | 14.3 |     | mW   | $f_{REF} = 19.44$ MHz                                                                                                                                                                                      |
| Output Distribution Driver On/Off |     |      |     |      |                                                                                                                                                                                                            |
| 28 mA Mode (at 644.53 MHz)        |     | 70   |     | mW   |                                                                                                                                                                                                            |
| 21 mA Mode (at 644.53 MHz)        |     | 48   |     | mW   |                                                                                                                                                                                                            |
| 14 mA mode (at 644.53 MHz)        |     | 23.6 |     | mW   |                                                                                                                                                                                                            |

**SYSTEM CLOCK INPUTS (XOA, XOB)**

Table 4.

| Parameter                              | Min  | Typ  | Max  | Unit       | Test Conditions/Comments                                                                                                                                                                                                                                                         |
|----------------------------------------|------|------|------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SYSTEM CLOCK MULTIPLIER                |      |      |      |            |                                                                                                                                                                                                                                                                                  |
| PLL Output Frequency Range             | 2250 |      | 2415 | MHz        | Voltage controlled oscillator (VCO) range can place limitations on nonstandard system clock input frequencies                                                                                                                                                                    |
| Phase Frequency Detector (PFD) Rate    | 10   |      | 300  | MHz        |                                                                                                                                                                                                                                                                                  |
| Frequency Multiplication Range         | 8    |      | 241  |            | Assumes valid system clock and PFD rates                                                                                                                                                                                                                                         |
| SYSTEM CLOCK REFERENCE INPUT PATH      |      |      |      |            |                                                                                                                                                                                                                                                                                  |
| Input Frequency Range                  |      |      |      |            | System clock input must be ac-coupled                                                                                                                                                                                                                                            |
| System Clock Input Doubler Disabled    | 10   |      | 268  | MHz        |                                                                                                                                                                                                                                                                                  |
| System Clock Input Doubler Enabled     | 16   |      | 150  | MHz        |                                                                                                                                                                                                                                                                                  |
| Minimum Input Slew Rate                | 250  |      |      | V/ $\mu$ s | Minimum limit imposed for jitter performance                                                                                                                                                                                                                                     |
| Self-Biased Common-Mode Voltage        |      | 0.72 |      | V          | Internally generated                                                                                                                                                                                                                                                             |
| Input High Voltage                     | 0.9  |      |      | V          | For ac-coupled single-ended operation                                                                                                                                                                                                                                            |
| Input Low Voltage                      |      |      | 0.5  | V          | For ac-coupled single-ended operation                                                                                                                                                                                                                                            |
| Differential Input Voltage Sensitivity | 250  |      |      | mV p-p     | Minimum voltage across pins required to ensure switching between logic states; the instantaneous voltage on either pin must not exceed 1.14 V; single-ended input can be accommodated by ac grounding complementary input; 800 mV p-p recommended for optimal jitter performance |
| System Clock Input Doubler Duty Cycle  |      |      |      |            | Amount of duty-cycle variation that can be tolerated on the system clock input to use the doubler                                                                                                                                                                                |
| System Clock Input = 20 MHz to 150 MHz | 43   | 50   | 57   | %          |                                                                                                                                                                                                                                                                                  |
| System Clock Input = 16 MHz to 20 MHz  | 47   | 50   | 53   | %          |                                                                                                                                                                                                                                                                                  |

| Parameter                           | Min | Typ | Max | Unit       | Test Conditions/Comments                                             |
|-------------------------------------|-----|-----|-----|------------|----------------------------------------------------------------------|
| Input Capacitance                   |     | 3   |     | pF         | Single-ended to ground, each pin                                     |
| Input Resistance                    |     | 5   |     | k $\Omega$ |                                                                      |
| CRYSTAL RESONATOR PATH              |     |     |     |            |                                                                      |
| Crystal Resonator Frequency Range   | 12  |     | 50  | MHz        | Fundamental mode, AT cut crystal<br>Single-ended to ground, each pin |
| Input Capacitance                   |     | 3   |     | pF         |                                                                      |
| Maximum Crystal Motional Resistance |     |     | 100 | $\Omega$   |                                                                      |

## REFERENCE INPUTS

Table 5.

| Parameter                              | Min   | Typ  | Max   | Unit       | Test Conditions/Comments                                                                                                                                                                               |
|----------------------------------------|-------|------|-------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DIFFERENTIAL MODE                      |       |      |       |            |                                                                                                                                                                                                        |
| Frequency Range                        |       |      |       |            | AC-couple inputs in differential mode                                                                                                                                                                  |
| Sinusoidal Input                       | 10    |      | 475   | MHz        |                                                                                                                                                                                                        |
| LVPECL Input                           | 0.002 |      | 1000  | MHz        | Assumes an LVDS minimum of 494 mV p-p differential amplitude<br>Minimum limit imposed for jitter performance                                                                                           |
| LVDS Input                             | 0.002 |      | 700   | MHz        |                                                                                                                                                                                                        |
| Minimum Input Slew Rate                |       |      |       |            |                                                                                                                                                                                                        |
| DPLL Loop Bandwidth = 50 Hz            | 40    |      |       | V/ $\mu$ s | Maximum loop bandwidth is $f_{\text{PFD}}/50$                                                                                                                                                          |
| DPLL Loop Bandwidth = 4 kHz            | 50    |      |       | V/ $\mu$ s |                                                                                                                                                                                                        |
| Common-Mode Input Voltage              |       | 0.64 |       | V          | Internally generated self-biased voltage                                                                                                                                                               |
| Differential Input Voltage Sensitivity |       |      |       |            | Peak-to-peak differential voltage swing across pins required to ensure switching between logic levels as measured with a differential probe; instantaneous voltage on either pin must not exceed 1.3 V |
| $f_{\text{IN}} < 400$ MHz              | 400   |      | 2100  | mV p-p     | Equivalent differential input resistance<br>Single-ended to ground, each pin                                                                                                                           |
| $f_{\text{IN}} = 400$ MHz to 750 MHz   | 500   |      | 2100  | mV p-p     |                                                                                                                                                                                                        |
| $f_{\text{IN}} = 750$ MHz to 1000 MHz  | 1000  |      | 2100  | mV p-p     |                                                                                                                                                                                                        |
| Differential Input Voltage Hysteresis  |       | 55   | 100   | mV         | Equivalent differential input resistance<br>Single-ended to ground, each pin                                                                                                                           |
| Input Resistance                       |       | 16   |       | k $\Omega$ |                                                                                                                                                                                                        |
| Input Capacitance                      |       | 9    |       | pF         | Minimum limit imposed for jitter performance                                                                                                                                                           |
| Minimum Pulse Width High               |       |      |       |            |                                                                                                                                                                                                        |
| LVPECL                                 | 460   |      |       | ps         | Maximum loop bandwidth is $f_{\text{PFD}}/50$                                                                                                                                                          |
| LVDS                                   | 560   |      |       | ps         |                                                                                                                                                                                                        |
| Minimum Pulse Width Low                |       |      |       |            | Differential voltage across pins required to ensure switching between logic levels; instantaneous voltage on either pin must not exceed the supply rails                                               |
| LVPECL                                 | 460   |      |       | ps         |                                                                                                                                                                                                        |
| LVDS                                   | 560   |      |       | ps         |                                                                                                                                                                                                        |
| DC-COUPLED LVDS MODE                   |       |      |       |            |                                                                                                                                                                                                        |
| Frequency Range                        | 0.002 |      | 10.24 | MHz        | Intended for dc-coupled LVDS $\leq 10.24$ MHz                                                                                                                                                          |
| Minimum Input Slew Rate                |       |      |       |            | Minimum limit imposed for jitter performance                                                                                                                                                           |
| DPLL Loop Bandwidth = 50 Hz            | 40    |      |       | V/ $\mu$ s | Maximum loop bandwidth is $f_{\text{PFD}}/50$                                                                                                                                                          |
| DPLL Loop Bandwidth = 4 kHz            | 150   |      |       | V/ $\mu$ s |                                                                                                                                                                                                        |
| Common-Mode Input Voltage              | 1.125 |      | 1.375 | V          | Differential voltage across pins required to ensure switching between logic levels; instantaneous voltage on either pin must not exceed the supply rails                                               |
| Differential Input Voltage Sensitivity | 400   |      | 1200  | mV         |                                                                                                                                                                                                        |
| Differential Input Voltage Hysteresis  |       | 55   | 100   | mV         | Differential voltage across pins required to ensure switching between logic levels; instantaneous voltage on either pin must not exceed the supply rails                                               |
| Input Resistance                       |       | 21   |       | k $\Omega$ |                                                                                                                                                                                                        |
| Input Capacitance                      |       | 7    |       | pF         | Minimum limit imposed for jitter performance                                                                                                                                                           |
| Minimum Pulse Width High               | 25    |      |       | ns         |                                                                                                                                                                                                        |
| Minimum Pulse Width Low                | 25    |      |       | ns         |                                                                                                                                                                                                        |

| Parameter                           | Min                   | Typ | Max | Unit       | Test Conditions/Comments                      |
|-------------------------------------|-----------------------|-----|-----|------------|-----------------------------------------------|
| SINGLE-ENDED MODE                   |                       |     |     |            | DC-coupled                                    |
| Frequency Range (CMOS)              | 0.002                 |     | 300 | MHz        |                                               |
| Minimum Input Slew Rate             |                       |     |     |            | Minimum limit imposed for jitter performance  |
| DPLL Loop Bandwidth = 50 Hz         | 40                    |     |     | V/ $\mu$ s |                                               |
| DPLL Loop Bandwidth = 4 kHz         | 175                   |     |     | V/ $\mu$ s | Maximum loop bandwidth is $f_{\text{PFD}}/50$ |
| Input Voltage High, $V_{\text{IH}}$ | $V_{\text{DD}} - 0.5$ |     |     | V          |                                               |
| Input Voltage Low, $V_{\text{IL}}$  |                       |     | 0.5 | V          |                                               |
| Input Resistance                    |                       | 30  |     | k $\Omega$ |                                               |
| Input Capacitance                   |                       | 5   |     | pF         |                                               |
| Minimum Pulse Width High            | 1.5                   |     |     | ns         |                                               |
| Minimum Pulse Width Low             | 1.5                   |     |     | ns         |                                               |

## REFERENCE MONITORS

Table 6.

| Parameter                        | Min   | Typ | Max    | Unit                            | Test Conditions/Comments                                                                                                                                                                 |
|----------------------------------|-------|-----|--------|---------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REFERENCE MONITORS               |       |     |        |                                 |                                                                                                                                                                                          |
| Reference Monitor                |       |     |        |                                 |                                                                                                                                                                                          |
| Loss of Reference Detection Time |       |     | 1.15   | DPLL PFD period                 | Nominal phase detector period = $R/f_{\text{REF}}$ , where R is the frequency division factor determined by the R divider, and $f_{\text{REF}}$ is the frequency of the active reference |
| Frequency Out-of Range Limits    | 2     |     | $10^5$ | $\Delta f/f_{\text{REF}}$ (ppm) | Programmable (lower bound subject to quality of the system clock [SYSCLK]); SYSCLK accuracy must be less than the lower bound                                                            |
| Validation Timer                 | 0.001 |     | 65.535 | sec                             | Programmable in 1 ms increments                                                                                                                                                          |

## REFERENCE SWITCHOVER SPECIFICATIONS

Table 7.

| Parameter                                                                | Min | Typ | Max      | Unit      | Test Conditions/Comments                                                                                                                                                                                                                |
|--------------------------------------------------------------------------|-----|-----|----------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MAXIMUM OUTPUT PHASE PERTURBATION<br>(PHASE BUILD-OUT SWITCHOVER)        |     |     |          |           | Assumes a jitter-free reference; satisfies Telcordia GR-1244-CORE requirements; base loop filter selection bit set to 1b or all active references                                                                                       |
| 50 Hz DPLL Loop Bandwidth                                                |     |     |          |           | High phase margin mode; 19.44 MHz to 174.70308 MHz; DPLL bandwidth = 50 Hz; 49.152 MHz signal generator used for the system clock source                                                                                                |
| Peak                                                                     |     |     | $\pm 20$ | $\pm 130$ | ps                                                                                                                                                                                                                                      |
| Steady State                                                             |     |     | $\pm 20$ | $\pm 130$ | ps                                                                                                                                                                                                                                      |
| Time Required to Switch to a New Reference<br>Phase Build-Out Switchover |     |     |          | 10        | DPLL PFD period<br>Calculated using the nominal phase detector period ( $\text{NPDP} = R/f_{\text{REF}}$ ); the total time required is the time plus the reference validation time, plus the time required to lock to the new reference |



## DISTRIBUTION CLOCK OUTPUTS

Table 8.

| Parameter                                                                           | Min   | Typ      | Max  | Unit             | Test Conditions/Comments                                                                                                                                                                                                                                                                                                      |
|-------------------------------------------------------------------------------------|-------|----------|------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14 mA (HCSL, LVDS-COMPATIBLE) MODE                                                  |       |          |      |                  |                                                                                                                                                                                                                                                                                                                               |
| Output Frequency                                                                    | 0.430 |          | 941  | MHz              | Unless otherwise stated, specifications dc-coupled with no output termination resistor; when ac-coupled, LVDS-compatible amplitudes are achieved with a 100 $\Omega$ resistor across the output pair; HCSL-compatible amplitudes achieved with no termination resistor across the output pair; output current setting = 14 mA |
| Continuous Output Frequency Range                                                   | 0.430 |          | 781  | MHz              | Frequency range all four PLLs can generate using unique VCO frequencies; frequencies outside this range are possible on some of the PLLs, but can result in increased VCO coupling due to multiple PLLs using the same VCO frequency                                                                                          |
| Maximum Output Frequency                                                            |       |          |      |                  | All four PLLs can generate this range at the same time while using unique VCO frequencies                                                                                                                                                                                                                                     |
| PLL0 to PLL3 Using Unique VCO Frequencies                                           |       | 941      |      | MHz              | Maximum frequency all four PLLs can generate using unique VCO frequencies                                                                                                                                                                                                                                                     |
| PLL0, PLL1, and PLL2                                                                |       | 1250     |      | MHz              | Limited by 1250 MHz maximum input frequency to channel divider (Q divider)                                                                                                                                                                                                                                                    |
| PLL3                                                                                |       | 1187     |      | MHz              | Limited by 4748 MHz maximum VCO frequency                                                                                                                                                                                                                                                                                     |
| Rise/Fall Time (20% to 80%) <sup>1</sup>                                            |       | 125      | 190  | ps               |                                                                                                                                                                                                                                                                                                                               |
| Duty Cycle                                                                          |       |          |      |                  |                                                                                                                                                                                                                                                                                                                               |
| Up to $f_{OUT} = 750$ MHz                                                           | 45    | 50       | 55   | %                |                                                                                                                                                                                                                                                                                                                               |
| Up to $f_{OUT} = 941$ MHz                                                           | 44    | 50       | 56   | %                |                                                                                                                                                                                                                                                                                                                               |
| Up to $f_{OUT} = 1250$ MHz                                                          |       | 50       |      | %                |                                                                                                                                                                                                                                                                                                                               |
| Differential Output Voltage Swing                                                   |       |          |      |                  | Differential voltage swing between output pins; measured with output driver static; peak-to-peak differential output amplitude 2 $\times$ this level with driver toggling; see Figure 11 for output amplitude vs. output frequency                                                                                            |
| Without 100 $\Omega$ Termination Resistor                                           | 635   | 840      | 1000 | mV               |                                                                                                                                                                                                                                                                                                                               |
| With 100 $\Omega$ Termination Resistor Across Outputs                               | 294   | 390      | 463  | mV               |                                                                                                                                                                                                                                                                                                                               |
| Common-Mode Output Voltage                                                          | 310   | 420      | 525  | mV               | Output driver static; no termination resistor                                                                                                                                                                                                                                                                                 |
| Reference Input-to-Output Delay Variation over Temperature                          |       | 600      |      | fs/ $^{\circ}$ C | DPLL locked to same input reference at all times; stable system clock source (noncrystal)                                                                                                                                                                                                                                     |
| Static Phase Offset Variation from Active Reference to Output over Voltage Extremes |       | $\pm 75$ |      | fs/mV            |                                                                                                                                                                                                                                                                                                                               |
| 21 mA MODE                                                                          |       |          |      |                  |                                                                                                                                                                                                                                                                                                                               |
| Output Frequency                                                                    | 0.430 |          | 941  | MHz              | Unless otherwise stated, specifications dc-coupled with 50 $\Omega$ output termination resistor to ground; output current setting = 21 mA                                                                                                                                                                                     |
| Continuous Output Frequency Range                                                   | 0.430 |          | 781  | MHz              | Frequency range all four PLLs can generate using unique VCO frequencies; frequencies outside this range are possible on some of the PLLs, but can result in increased VCO coupling due to multiple PLLs using the same VCO frequency                                                                                          |
| Maximum Output Frequency                                                            |       |          |      |                  | All four PLLs can generate this range at the same time while using unique VCO frequencies                                                                                                                                                                                                                                     |
| PLL0 to PLL3 Using Unique VCO Frequencies                                           |       | 941      |      | MHz              | Maximum frequency all four PLLs can generate using unique VCO frequencies                                                                                                                                                                                                                                                     |
| PLL0, PLL1, and PLL2                                                                |       | 1250     |      | MHz              | Limited by 1250 MHz maximum input frequency to channel divider (Q divider)                                                                                                                                                                                                                                                    |
| PLL3                                                                                |       | 1187     |      | MHz              | Limited by 4748 MHz maximum VCO frequency                                                                                                                                                                                                                                                                                     |

| Parameter                                                                           | Min   | Typ  | Max  | Unit  | Test Conditions/Comments                                                                                                                                                                                                                                                                                    |
|-------------------------------------------------------------------------------------|-------|------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rise/Fall Time (20% to 80%) <sup>1</sup>                                            |       | 125  | 190  | ps    |                                                                                                                                                                                                                                                                                                             |
| Duty Cycle                                                                          |       |      |      |       |                                                                                                                                                                                                                                                                                                             |
| Up to $f_{OUT} = 750$ MHz                                                           | 45    | 50   | 55   | %     |                                                                                                                                                                                                                                                                                                             |
| Up to $f_{OUT} = 941$ MHz                                                           | 44    | 50   | 56   | %     |                                                                                                                                                                                                                                                                                                             |
| Up to $f_{OUT} = 1250$ MHz                                                          |       | 50   |      | %     |                                                                                                                                                                                                                                                                                                             |
| Differential Output Voltage Swing                                                   |       |      |      |       | Differential voltage swing between output pins; measured with output driver static; peak-to-peak differential output amplitude 2× this level with driver toggling; see Figure 13 for output amplitude vs. output frequency                                                                                  |
| No External Termination Resistor                                                    | 779   | 1180 | 1510 | mV    |                                                                                                                                                                                                                                                                                                             |
| With 50 $\Omega$ Termination Resistor to Ground on Each Leg                         | 413   | 625  | 800  | mV    |                                                                                                                                                                                                                                                                                                             |
| Common-Mode Output Voltage                                                          | 206   | 312  | 400  | mV    | Output driver static with 50 $\Omega$ resistor to ground on each leg                                                                                                                                                                                                                                        |
| Reference Input-to-Output Delay Variation over Temperature                          |       | 600  |      | fs/°C | DPLL locked to same input reference at all times; stable system clock source (noncrystal)                                                                                                                                                                                                                   |
| Static Phase Offset Variation from Active Reference to Output over Voltage Extremes |       | ±75  |      | fs/mV |                                                                                                                                                                                                                                                                                                             |
| <b>28 mA (LVPECL-COMPATIBLE) MODE</b>                                               |       |      |      |       |                                                                                                                                                                                                                                                                                                             |
| Output Frequency                                                                    | 0.430 |      | 941  | MHz   | Specifications for dc-coupled, 50 $\Omega$ termination resistor from each leg to ground; ac coupling used in most applications; output current setting = 28 mA; in this mode, user must have either a 50 $\Omega$ resistor from each leg to ground, or a 100 $\Omega$ resistor across the differential pair |
| Continuous Output Frequency Range                                                   | 0.430 |      | 781  | MHz   | Frequency range all four PLLs can generate using unique VCO frequencies; frequencies outside this range are possible on some of the PLLs, but can result in increased VCO coupling due to multiple PLLs using the same VCO frequency                                                                        |
| Maximum Output Frequency                                                            |       |      |      |       | Frequency range for each PLL such that all four PLLs are using unique VCO frequencies with no frequency gaps                                                                                                                                                                                                |
| PLL0 to PLL3 Using Unique VCO Frequencies                                           |       | 941  |      | MHz   | Maximum frequency all four PLLs can generate using unique VCO frequencies                                                                                                                                                                                                                                   |
| PLL0, PLL1, and PLL2                                                                |       | 1250 |      | MHz   | Limited by 1250 MHz maximum input frequency to channel divider (Q divider)                                                                                                                                                                                                                                  |
| PLL3                                                                                |       | 1187 |      | MHz   | Limited by 4748 MHz maximum VCO frequency                                                                                                                                                                                                                                                                   |
| Rise/Fall Time (20% to 80%) <sup>1</sup>                                            |       | 185  | 280  | ps    |                                                                                                                                                                                                                                                                                                             |
| Duty Cycle                                                                          |       |      |      |       |                                                                                                                                                                                                                                                                                                             |
| Up to $f_{OUT} = 750$ MHz                                                           | 45    | 50   | 55   | %     |                                                                                                                                                                                                                                                                                                             |
| Up to $f_{OUT} = 941$ MHz                                                           | 44    | 50   | 56   | %     |                                                                                                                                                                                                                                                                                                             |
| Up to $f_{OUT} = 1250$ MHz                                                          |       | 50   |      | %     |                                                                                                                                                                                                                                                                                                             |
| Differential Output Voltage Swing                                                   | 540   | 830  | 1020 | mV    | Differential voltage swing between output pins; measured with output driver static; peak-to-peak differential output amplitude 2× this level with driver toggling; see Figure 10 for output amplitude vs. output frequency                                                                                  |
| Common-Mode Output Voltage                                                          | 275   | 415  | 510  | mV    | Output driver static; 50 $\Omega$ external termination resistor from each leg to ground                                                                                                                                                                                                                     |
| Reference Input-to-Output Delay Variation over Temperature                          |       | 600  |      | fs/°C | DPLL locked to same input reference at all times; stable system clock source (noncrystal)                                                                                                                                                                                                                   |
| Static Phase Offset Variation from Active Reference to Output over Voltage Extremes |       | ±75  |      | fs/mV |                                                                                                                                                                                                                                                                                                             |

<sup>1</sup> The listed values are for the slower edge (rising or falling).

## TIME DURATION OF DIGITAL FUNCTIONS

Table 9.

| Parameter                                                    | Min | Typ | Max | Unit | Test Conditions/Comments                                                                                                                                                                                                                |
|--------------------------------------------------------------|-----|-----|-----|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TIME DURATION OF DIGITAL FUNCTIONS                           |     |     |     |      |                                                                                                                                                                                                                                         |
| Power-Down Exit Time                                         |     | 51  |     | ms   | Time from power-down exit to system clock stable (including the system clock stability timer default of 50 ms); does not include time to validate input references or lock the DPLL<br>Mx refers to the M0, M1, M2, M3, M5, M6, M7 pins |
| Mx Pin to $\overline{\text{RESET}}$ Rising Edge Setup Time   |     |     | 1   | ns   |                                                                                                                                                                                                                                         |
| Mx Pin to $\overline{\text{RESET}}$ Rising Edge Hold Time    |     |     | 1   | ns   |                                                                                                                                                                                                                                         |
| $\overline{\text{RESET}}$ Falling Edge to Mx Pin High-Z Time |     |     | 10  | ns   |                                                                                                                                                                                                                                         |

## DIGITAL PLL (DPLL\_0, DPLL\_1, DPLL\_2, AND DPLL\_3)

Table 10.

| Parameter                                               | Min  | Typ | Max  | Unit    | Test Conditions/Comments                                                                                                                                                                                                                                      |
|---------------------------------------------------------|------|-----|------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DIGITAL PLL                                             |      |     |      |         |                                                                                                                                                                                                                                                               |
| Phase Frequency Detector (PFD)<br>Input Frequency Range | 2    |     | 200  | kHz     | Programmable design parameter; note that ( $f_{\text{PFD}}$ /loop bandwidth) $\geq$ 50<br>Programmable design parameter<br>Programmable design parameter; part can be programmed for <0.1 dB peaking in accordance with Telcordia GR-253-CORE jitter transfer |
| Loop Bandwidth                                          | 0.1  |     | 4000 | Hz      |                                                                                                                                                                                                                                                               |
| Phase Margin                                            | 45   |     | 89   | Degrees |                                                                                                                                                                                                                                                               |
| Closed Loop Peaking                                     | <0.1 |     |      | dB      |                                                                                                                                                                                                                                                               |

## ANALOG PLL (APLL\_0, APLL\_1, APLL\_2, AND APLL\_3)

Table 11.

| Parameter                                               | Min  | Typ | Max  | Unit    | Test Conditions/Comments                                                                                         |
|---------------------------------------------------------|------|-----|------|---------|------------------------------------------------------------------------------------------------------------------|
| ANALOG PLL0 (APLL_0)                                    |      |     |      |         |                                                                                                                  |
| VCO Frequency Range                                     | 2424 |     | 3132 | MHz     | The <a href="#">AD9554-1</a> evaluation software finds the optimal value for this setting based on user's input. |
| Phase Frequency Detector (PFD)<br>Input Frequency Range |      | 320 | 350  | MHz     |                                                                                                                  |
| Loop Bandwidth                                          |      | 240 |      | kHz     |                                                                                                                  |
| Phase Margin                                            |      | 68  |      | Degrees |                                                                                                                  |
| ANALOG PLL1 (APLL_1)                                    |      |     |      |         |                                                                                                                  |
| VCO Frequency Range                                     | 3232 |     | 3905 | MHz     | The <a href="#">AD9554-1</a> evaluation software finds the optimal value for this setting based on user's input. |
| Phase Frequency Detector (PFD)<br>Input Frequency Range |      | 320 | 350  | MHz     |                                                                                                                  |
| Loop Bandwidth                                          |      | 240 |      | kHz     |                                                                                                                  |
| Phase Margin                                            |      | 68  |      | Degrees |                                                                                                                  |
| ANALOG PLL2 (APLL_2)                                    |      |     |      |         |                                                                                                                  |
| VCO Frequency Range                                     | 4842 |     | 5650 | MHz     | The <a href="#">AD9554-1</a> evaluation software finds the optimal value for this setting based on user's input. |
| Phase Frequency Detector (PFD)<br>Input Frequency Range |      | 320 | 350  | MHz     |                                                                                                                  |
| Loop Bandwidth                                          |      | 240 |      | kHz     |                                                                                                                  |
| Phase Margin                                            |      | 68  |      | Degrees |                                                                                                                  |
| ANALOG PLL3 (APLL_3)                                    |      |     |      |         |                                                                                                                  |
| VCO Frequency Range                                     | 4040 |     | 4748 | MHz     | The <a href="#">AD9554-1</a> evaluation software finds the optimal value for this setting based on user's input. |
| Phase Frequency Detector (PFD)<br>Input Frequency Range |      | 320 | 350  | MHz     |                                                                                                                  |
| Loop Bandwidth                                          |      | 240 |      | kHz     |                                                                                                                  |
| Phase Margin                                            |      | 68  |      | Degrees |                                                                                                                  |

**DIGITAL PLL LOCK DETECTION**

Table 12.

| Parameter                   | Min | Typ | Max          | Unit | Test Conditions/Comments                |
|-----------------------------|-----|-----|--------------|------|-----------------------------------------|
| PHASE LOCK DETECTOR         |     |     |              |      |                                         |
| Threshold Programming Range | 10  |     | $2^{24} - 1$ | ps   | Reference-to-feedback phase difference  |
| Threshold Resolution        |     | 1   |              | ps   |                                         |
| FREQUENCY LOCK DETECTOR     |     |     |              |      |                                         |
| Threshold Programming Range | 10  |     | $2^{24} - 1$ | ps   | Reference-to-feedback period difference |
| Threshold Resolution        |     | 1   |              | ps   |                                         |

**HOLDOVER SPECIFICATIONS**

Table 13.

| Parameter                  | Min | Typ   | Max | Unit | Test Conditions/Comments                                                                                                                            |
|----------------------------|-----|-------|-----|------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| HOLDOVER SPECIFICATIONS    |     |       |     |      |                                                                                                                                                     |
| Initial Frequency Accuracy |     | <0.01 |     | ppm  | Excludes frequency drift of SYSCLK source; excludes frequency drift of input reference prior to entering holdover; compliant with GR-1244 Stratum 3 |

**SERIAL PORT SPECIFICATIONS—SERIAL PORT INTERFACE (SPI) MODE**

Table 14.

| Parameter              | Min          | Typ | Max | Unit | Test Conditions/Comments                                     |
|------------------------|--------------|-----|-----|------|--------------------------------------------------------------|
| CS                     |              |     |     |      | Valid for VDD_SP = 1.5 V, VDD_SP = 1.8 V, and VDD_SP = 2.5 V |
| Input Logic 1 Voltage  | VDD_SP – 0.4 |     |     | V    |                                                              |
| Input Logic 0 Voltage  |              |     | 0.4 | V    |                                                              |
| Input Logic 1 Current  |              | 1   |     | μA   |                                                              |
| Input Logic 0 Current  |              | 1   |     | μA   |                                                              |
| Input Capacitance      |              | 3   |     | pF   |                                                              |
| SCLK                   |              |     |     |      | No internal pull-up or pull-down resistor                    |
| Input Logic 1 Voltage  | VDD_SP – 0.4 |     |     | V    |                                                              |
| Input Logic 0 Voltage  |              |     | 0.4 | V    |                                                              |
| Input Logic 1 Current  |              | 1   |     | μA   |                                                              |
| Input Logic 0 Current  |              | 1   |     | μA   |                                                              |
| Input Capacitance      |              | 2   |     | pF   |                                                              |
| SDIO                   |              |     |     |      |                                                              |
| As an Input            |              |     |     |      |                                                              |
| Input Logic 1 Voltage  | VDD_SP – 0.4 |     |     | V    |                                                              |
| Input Logic 0 Voltage  |              |     | 0.4 | V    |                                                              |
| Input Logic 1 Current  |              | 1   |     | μA   |                                                              |
| Input Logic 0 Current  |              | 1   |     | μA   |                                                              |
| Input Capacitance      |              | 2   |     | pF   |                                                              |
| As an Output           |              |     |     |      |                                                              |
| Output Logic 1 Voltage | VDD_SP – 0.2 |     |     | V    | 1 mA load current                                            |
| Output Logic 0 Voltage |              |     | 0.1 | V    | 1 mA load current                                            |

| Parameter                                            | Min | Typ | Max | Unit | Test Conditions/Comments                                     |
|------------------------------------------------------|-----|-----|-----|------|--------------------------------------------------------------|
| TIMING                                               |     |     |     |      | Valid for VDD_SP = 1.5 V, VDD_SP = 1.8 V, and VDD_SP = 2.5 V |
| SCLK                                                 |     |     |     |      |                                                              |
| Clock Rate, 1/t <sub>CLK</sub>                       |     |     | 50  | MHz  |                                                              |
| Pulse Width High, t <sub>HIGH</sub>                  | 5   |     |     | ns   |                                                              |
| Pulse Width Low, t <sub>LOW</sub>                    | 8   |     |     | ns   |                                                              |
| SDIO to SCLK Setup, t <sub>DS</sub>                  | 1.5 |     |     | ns   |                                                              |
| SCLK to SDIO Hold, t <sub>DH</sub>                   | 0   |     |     | ns   |                                                              |
| SCLK to Valid SDIO, t <sub>DV</sub>                  |     | 8   |     | ns   |                                                              |
| $\overline{\text{CS}}$ to SCLK Setup, t <sub>S</sub> | 0   |     |     | ns   |                                                              |
| $\overline{\text{CS}}$ to SCLK Hold, t <sub>c</sub>  | 0   |     |     | ns   |                                                              |
| $\overline{\text{CS}}$ Minimum Pulse Width High      | 1.5 |     |     | ns   |                                                              |

## SERIAL PORT SPECIFICATIONS—I<sup>2</sup>C MODE

Table 15.

| Parameter                                                                | Min                       | Typ | Max          | Unit | Test Conditions/Comments                                     |
|--------------------------------------------------------------------------|---------------------------|-----|--------------|------|--------------------------------------------------------------|
| SDA, SCL (AS INPUTS)                                                     |                           |     |              |      | Valid for VDD_SP = 1.5 V, VDD_SP = 1.8 V, and VDD_SP = 2.5 V |
| Input Logic 1 Voltage                                                    | 0.7 × VDD_SP              |     |              | V    |                                                              |
| Input Logic 0 Voltage                                                    |                           |     | 0.3 × VDD_SP | V    |                                                              |
| Input Current                                                            | −10                       |     | +10          | μA   | For V <sub>IN</sub> = 10% to 90% of VDD                      |
| Hysteresis of Schmitt Trigger Inputs                                     | 0.015 × VDD               |     |              |      |                                                              |
| SDA (AS OUTPUT)                                                          |                           |     |              |      |                                                              |
| Output Logic 0 Voltage                                                   |                           |     | 0.2          | V    | I <sub>OUT</sub> = 3 mA                                      |
| Output Fall Time from V <sub>IH</sub> Minimum to V <sub>IL</sub> Maximum | 20 + 0.1 × C <sub>b</sub> |     | 250          | ns   | 10 pF ≤ C <sub>b</sub> ≤ 400 pF                              |
| TIMING                                                                   |                           |     |              |      |                                                              |
| SCL Clock Rate                                                           |                           |     | 400          | kHz  |                                                              |
| Bus-Free Time Between a Stop and Start Condition, t <sub>BUF</sub>       | 1.3                       |     |              | μs   |                                                              |
| Repeated Start Condition Setup Time, t <sub>SU; STA</sub>                | 0.6                       |     |              | μs   |                                                              |
| Repeated Hold Time Start Condition, t <sub>HD; STA</sub>                 | 0.6                       |     |              | μs   | After this period, the first clock pulse is generated        |
| Stop Condition Setup Time, t <sub>SU; STO</sub>                          | 0.6                       |     |              | μs   |                                                              |
| Low Period of the SCL Clock, t <sub>LOW</sub>                            | 1.3                       |     |              | μs   |                                                              |
| High Period of the SCL Clock, t <sub>HIGH</sub>                          | 0.6                       |     |              | μs   |                                                              |
| SCL/SDA Rise Time, t <sub>R</sub>                                        | 20 + 0.1 × C <sub>b</sub> |     | 300          | ns   |                                                              |
| SCL/SDA Fall Time, t <sub>F</sub>                                        | 20 + 0.1 × C <sub>b</sub> |     | 300          | ns   |                                                              |
| Data Setup Time, t <sub>SU; DAT</sub>                                    | 100                       |     |              | ns   |                                                              |
| Data Hold Time, t <sub>HD; DAT</sub>                                     | 100                       |     |              | ns   |                                                              |
| Capacitive Load for Each Bus Line, C <sub>b</sub>                        |                           |     | 400          | pF   |                                                              |

**LOGIC INPUTS ( $\overline{\text{RESET}}$ , M0 TO M3, M5 TO M7)**

Table 16.

| Parameter                               | Min          | Typ | Max  | Unit | Test Conditions/Comments                                     |
|-----------------------------------------|--------------|-----|------|------|--------------------------------------------------------------|
| $\overline{\text{RESET}}$ PIN           |              |     |      |      | Valid for VDD_SP = 1.5 V, VDD_SP = 1.8 V, and VDD_SP = 2.5 V |
| Input High Voltage ( $V_{IH}$ )         | VDD_SP – 0.5 |     |      | V    |                                                              |
| Input Low Voltage ( $V_{IL}$ )          |              |     | 0.5  | V    |                                                              |
| Input Current ( $I_{INH}$ , $I_{INL}$ ) |              | ±85 | ±125 | µA   |                                                              |
| Input Capacitance ( $C_{IN}$ )          |              | 3   |      | pF   |                                                              |
| LOGIC INPUTS (M0 TO M3 AND M5 TO M7)    |              |     |      |      | Valid for VDD = 1.5 V, and VDD = 1.8 V                       |
| Input High Voltage ( $V_{IH}$ )         | VDD – 0.5    |     |      | V    |                                                              |
| Input Low Voltage ( $V_{IL}$ )          |              |     | 0.6  | V    |                                                              |
| Input Current ( $I_{INH}$ , $I_{INL}$ ) |              | ±15 | ±25  | µA   |                                                              |
| Input Capacitance ( $C_{IN}$ )          |              | 5   |      | pF   |                                                              |

**LOGIC OUTPUTS (M0 TO M3 AND M5 TO M7)**

Table 17.

| Parameter                             | Min       | Typ | Max | Unit | Test Conditions/Comments                                        |
|---------------------------------------|-----------|-----|-----|------|-----------------------------------------------------------------|
| LOGIC OUTPUTS (M0 to M3 and M5 to M7) |           |     |     |      | VDD = 1.5 V and VDD = 1.8 V                                     |
| Output High Voltage ( $V_{OH}$ )      | VDD – 0.2 |     |     | V    | $I_{OH}$ = 1 mA using high drive strength (see Register 0x011E) |
| Output Low Voltage ( $V_{OL}$ )       |           |     | 0.2 | V    | $I_{OL}$ = 1 mA                                                 |

**JITTER GENERATION****Jitter Generation (Random Jitter)—49.152 MHz Crystal for System Clock Input**

Table 18.

| Parameter                                                                              | Min | Typ | Max | Unit   | Test Conditions/Comments                                                                                                                                                                                                                                          |
|----------------------------------------------------------------------------------------|-----|-----|-----|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| JITTER GENERATION                                                                      |     |     |     |        | System clock doubler enabled; high phase margin mode enabled; all PLLs are running with same output frequency; in cases where the four PLLs have different jitter, the higher jitter is listed; there is not a significant jitter difference between driver modes |
| $f_{REF} = 19.44 \text{ MHz}; f_{OUT} = 622.08 \text{ MHz}; f_{LOOP} = 50 \text{ Hz}$  |     |     |     |        |                                                                                                                                                                                                                                                                   |
| Bandwidth                                                                              |     |     |     |        |                                                                                                                                                                                                                                                                   |
| 5 kHz to 20 MHz                                                                        |     | 381 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 12 kHz to 20 MHz                                                                       |     | 375 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 20 kHz to 80 MHz                                                                       |     | 380 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 50 kHz to 80 MHz                                                                       |     | 365 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 4 MHz to 80 MHz                                                                        |     | 116 |     | fs rms |                                                                                                                                                                                                                                                                   |
| $f_{REF} = 19.44 \text{ MHz}; f_{OUT} = 644.53 \text{ MHz}; f_{LOOP} = 50 \text{ Hz}$  |     |     |     |        |                                                                                                                                                                                                                                                                   |
| Bandwidth                                                                              |     |     |     |        |                                                                                                                                                                                                                                                                   |
| 5 kHz to 20 MHz                                                                        |     | 388 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 12 kHz to 20 MHz                                                                       |     | 381 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 20 kHz to 80 MHz                                                                       |     | 385 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 50 kHz to 80 MHz                                                                       |     | 368 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 4 MHz to 80 MHz                                                                        |     | 106 |     | fs rms |                                                                                                                                                                                                                                                                   |
| $f_{REF} = 19.44 \text{ MHz}; f_{OUT} = 693.48 \text{ MHz}; f_{LOOP} = 50 \text{ Hz}$  |     |     |     |        |                                                                                                                                                                                                                                                                   |
| Bandwidth                                                                              |     |     |     |        |                                                                                                                                                                                                                                                                   |
| 5 kHz to 20 MHz                                                                        |     | 433 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 12 kHz to 20 MHz                                                                       |     | 427 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 20 kHz to 80 MHz                                                                       |     | 432 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 50 kHz to 80 MHz                                                                       |     | 419 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 4 MHz to 80 MHz                                                                        |     | 120 |     | fs rms |                                                                                                                                                                                                                                                                   |
| $f_{REF} = 19.44 \text{ MHz}; f_{OUT} = 156.25 \text{ MHz}; f_{LOOP} = 50 \text{ Hz}$  |     |     |     |        |                                                                                                                                                                                                                                                                   |
| Bandwidth                                                                              |     |     |     |        |                                                                                                                                                                                                                                                                   |
| 5 kHz to 20 MHz                                                                        |     | 420 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 12 kHz to 20 MHz                                                                       |     | 414 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 20 kHz to 80 MHz                                                                       |     | 461 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 50 kHz to 80 MHz                                                                       |     | 449 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 4 MHz to 80 MHz                                                                        |     | 260 |     | fs rms |                                                                                                                                                                                                                                                                   |
| $f_{REF} = 19.44 \text{ MHz}; f_{OUT} = 174.703 \text{ MHz}; f_{LOOP} = 50 \text{ Hz}$ |     |     |     |        |                                                                                                                                                                                                                                                                   |
| Bandwidth                                                                              |     |     |     |        |                                                                                                                                                                                                                                                                   |
| 5 kHz to 20 MHz                                                                        |     | 398 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 12 kHz to 20 MHz                                                                       |     | 393 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 20 kHz to 80 MHz                                                                       |     | 439 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 50 kHz to 80 MHz                                                                       |     | 427 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 4 MHz to 80 MHz                                                                        |     | 231 |     | fs rms |                                                                                                                                                                                                                                                                   |
| $f_{REF} = 25 \text{ MHz}; f_{OUT} = 161.1328 \text{ MHz}; f_{LOOP} = 100 \text{ Hz}$  |     |     |     |        |                                                                                                                                                                                                                                                                   |
| Bandwidth                                                                              |     |     |     |        |                                                                                                                                                                                                                                                                   |
| 5 kHz to 20 MHz                                                                        |     | 385 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 12 kHz to 20 MHz                                                                       |     | 379 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 20 kHz to 80 MHz                                                                       |     | 423 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 50 kHz to 80 MHz                                                                       |     | 412 |     | fs rms |                                                                                                                                                                                                                                                                   |
| 4 MHz to 80 MHz                                                                        |     | 250 |     | fs rms |                                                                                                                                                                                                                                                                   |

## ABSOLUTE MAXIMUM RATINGS

Table 19.

| Parameter                           | Rating                |
|-------------------------------------|-----------------------|
| 1.8 V Supply Voltage (VDD)          | 2 V                   |
| Serial Port Supply Voltage (VDD_SP) | 2.75 V                |
| Maximum Digital Input Voltage Range | -0.5 V to VDD + 0.5 V |
| Storage Temperature Range           | -65°C to +150°C       |
| Operating Temperature Range         | -40°C to +85°C        |
| Lead Temperature (Soldering 10 sec) | 300°C                 |
| Junction Temperature                | 115°C                 |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

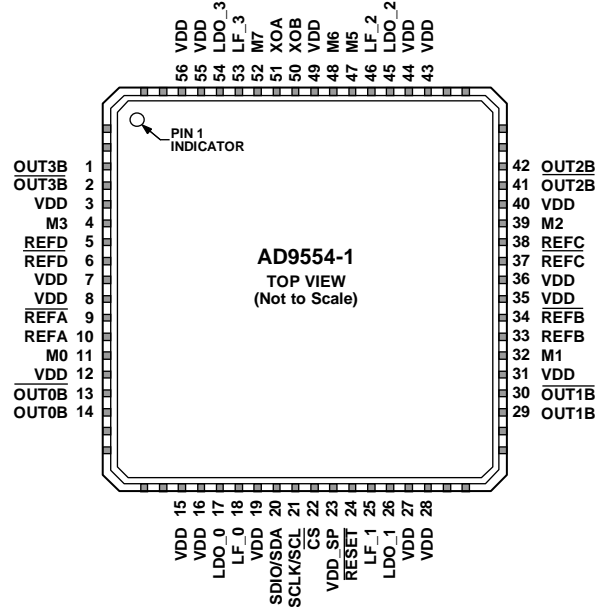
### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



**NOTES**  
 1. THE EXPOSED PAD IS THE GROUND CONNECTION ON THE CHIP. IT MUST BE SOLDERED TO THE ANALOG GROUND OF THE PCB TO ENSURE PROPER FUNCTIONALITY AND HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

12214-002

Figure 2. Pin Configuration

Table 20. Pin Function Descriptions

| Pin No.                                                             | Mnemonic                  | Input/Output | Pin Type                                 | Description                                                                                                                                                                                                                                                                                                                                                                             |
|---------------------------------------------------------------------|---------------------------|--------------|------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                                                                   | OUT3B                     | O            | HCSL, LVDS-compatible, LVPECL-compatible | PLL3 Output 3B. This HCSL output can be configured as a LVDS- or a LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.                                                                                                                  |
| 2                                                                   | $\overline{\text{OUT3B}}$ | O            | HCSL, LVDS-compatible, LVPECL-compatible | PLL3 Complementary Output 3B. Complementary signal to the output provided on Pin 1 (OUT3B).                                                                                                                                                                                                                                                                                             |
| 3, 7, 8, 12, 15, 16, 19, 27, 28, 31, 35, 36, 40, 43, 44, 49, 55, 56 | VDD                       | I            | Power                                    | 1.5 V or 1.8 V Power Supply. See the Power Supply Partitions section for information about the recommended grouping of the power supply pins.                                                                                                                                                                                                                                           |
| 4, 11, 32, 39                                                       | M3, M0, M1, M2            | I/O          | 1.5 V/1.8 V CMOS                         | Configurable Input/Output Pins. These pins are used for status and control of the AD9554-1. See the Multifunction Pins at Reset/Power-Up section for more information about the internal 100 kΩ pull-up or pull-down resistors. These pins are on the VDD power domain (Pin 7, Pin 8, Pin 35, and Pin 36), and the logic high voltage for this pin matches the voltage of the VDD pins. |
| 5                                                                   | REFD                      | I            | Differential input                       | Reference D Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with single-ended swing up to the VDD power supply. If dc-coupled, the input can be LVDS or single-ended CMOS provided that $V_{IH} \leq VDD$ .                                                                                          |
| 6                                                                   | $\overline{\text{REFD}}$  | I            | Differential input                       | Complementary Reference D Input. Complementary signal to the input provided on Pin 5 (REFD). This pin can be left floating if REFD is a single-ended input, or if REFD is not used.                                                                                                                                                                                                     |
| 9                                                                   | $\overline{\text{REFA}}$  | I            | Differential input                       | Complementary Reference A Input. Complementary signal to the input provided on Pin 10 (REFA). This pin can be left floating if REFA is a single-ended input or if REFA is not used.                                                                                                                                                                                                     |

| Pin No. | Mnemonic           | Input/<br>Output | Pin Type                                 | Description                                                                                                                                                                                                                                                                                                                                                                                              |
|---------|--------------------|------------------|------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10      | REFA               | I                | Differential input                       | Reference A Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with single-ended swing up to the VDD power supply. If dc-coupled, the input can be LVDS, or single-ended CMOS provided that $V_{IH} \leq VDD$ .                                                                                                          |
| 13      | $\overline{OUT0B}$ | O                | HCSL, LVDS-compatible, LVPECL-compatible | PLL0 Complementary Output 0B. Complementary signal to the output provided on Pin 14 (OUT0B).                                                                                                                                                                                                                                                                                                             |
| 14      | OUT0B              | O                | HCSL, LVDS-compatible, LVPECL-compatible | PLL0 Output 0B. This HCSL output can be configured as a LVDS- or a LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.                                                                                                                                   |
| 17      | LDO_0              | I                | LDO bypass                               | APLL_0 Loop Filter Voltage Regulator. Connect a 0.22 $\mu$ F capacitor from this pin to ground. This pin is also the ac ground reference for the integrated APLL_0 external loop filter.                                                                                                                                                                                                                 |
| 18      | LF_0               | I/O              | Loop filter for APLL_0                   | Loop Filter Node for the APLL_0. Connect an external 15 nF capacitor from this pin to Pin 17 (LDO_0).                                                                                                                                                                                                                                                                                                    |
| 20      | SDIO/SDA           | I/O              | CMOS                                     | Serial Data Input/Output (SDIO) in SPI Mode. In 4-wire SPI mode, data is written via this pin. In 3-wire SPI mode, data reads and writes both occur on this pin.<br>Serial Data Pin (SDA) in I <sup>2</sup> C Mode. There is no internal pull-up/pull-down resistor on this pin. The $V_{IH}/V_{OH}$ of this pin tracks the VDD_SP power supply (which can be 1.5 V, 1.8 V, or 2.5 V).                   |
| 21      | SCLK/SCL           | I                | CMOS                                     | Serial Programming Clock (SCLK) in SPI Mode. In I <sup>2</sup> C mode, this is the serial clock pin (SCL). The $V_{IH}/V_{OH}$ of this pin tracks the VDD_SP power supply (which can be 1.5 V, 1.8 V, or 2.5 V).                                                                                                                                                                                         |
| 22      | $\overline{CS}$    | I/O              | CMOS                                     | Chip Select in SPI Mode ( $\overline{CS}$ ). Active low input. When programming a device in SPI, this pin must be held low. In systems where more than one AD9554-1 is present, this pin enables individual programming of each AD9554-1. This pin has an internal 10 k $\Omega$ pull-up resistor. The $V_{IH}/V_{OH}$ of this pin tracks the VDD_SP power supply (which can be 1.5 V, 1.8 V, or 2.5 V). |
| 23      | VDD_SP             | I                | Power                                    | Serial Port Power Supply. The power supply can be 1.5 V, 1.8 V, or 2.5 V. If this pin is at the same voltage as VDD, it can be connected to VDD pins. See the Power Supply Partitions section for information about the recommended grouping of the power supply pins.                                                                                                                                   |
| 24      | $\overline{RESET}$ | I                | CMOS logic                               | Chip Reset. When this active low pin is asserted, the chip goes into reset. This pin has an internal 50 k $\Omega$ pull-up resistor.                                                                                                                                                                                                                                                                     |
| 25      | LF_1               | I/O              | Loop filter for APLL_1                   | Loop Filter Node for the APLL_1. Connect an external 15 nF capacitor from this pin to Pin 26 (LDO_1).                                                                                                                                                                                                                                                                                                    |
| 26      | LDO_1              | I                | LDO bypass                               | APLL_1 Loop Filter Voltage Regulator. Connect a 0.22 $\mu$ F capacitor from this pin to ground. This pin is also the ac ground reference for the integrated APLL_1 external loop filter.                                                                                                                                                                                                                 |
| 29      | OUT1B              | O                | HCSL, LVDS-compatible, LVPECL-compatible | PLL1 Output 1B. This HCSL output can be configured as a LVDS- or a LVPECL-compatible. LVPECL and LVDS levels can be achieved by ac coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.                                                                                                                                          |
| 30      | $\overline{OUT1B}$ | O                | HCSL, LVDS-compatible, LVPECL-compatible | PLL1 Complementary Output 1B. Complementary signal to the output provided on Pin 29 (OUT1B).                                                                                                                                                                                                                                                                                                             |
| 33      | REFB               | I                | Differential input                       | Reference B Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with single-ended swing up to the VDD power supply. If dc-coupled, the input can be LVDS, or single-ended CMOS provided that $V_{IH} \leq VDD$ .                                                                                                          |
| 34      | $\overline{REFB}$  | I                | Differential input                       | Complementary Reference B Input. Complementary signal to the input provided on Pin 33 (REFB). This pin can be left floating if REFB is a single-ended input or if REFB is not used.                                                                                                                                                                                                                      |
| 37      | $\overline{REFC}$  | I                | Differential input                       | Complementary Reference C Input. Complementary signal to the input provided on Pin 38 (REFC). This pin can be left floating if REFC is a single-ended input or if REFC is not used.                                                                                                                                                                                                                      |

| Pin No.    | Mnemonic           | Input/<br>Output | Pin Type                                 | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------------|--------------------|------------------|------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 38         | REFC               | I                | Differential input                       | Reference C Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with single-ended swing up to the VDD power supply. If dc-coupled, the input can be LVDS, or single-ended CMOS provided that $V_{IH} \leq VDD$ .                                                                                                                                                                        |
| 41         | $\overline{OUT2B}$ | O                | HCSL, LVDS-compatible, LVPECL-compatible | PLL2 Complementary Output 2B. Complementary signal to the output provided on Pin 42 (OUT2B).                                                                                                                                                                                                                                                                                                                                                                           |
| 42         | OUT2B              | O                | HCSL, LVDS-compatible, LVPECL-compatible | PLL2 Output 2B. This HCSL output can be configured as a LVDS- or a LVPECL-compatible. LVPECL and LVDS levels can be achieved by ac coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.                                                                                                                                                                                                        |
| 45         | LDO_2              | I                | LDO bypass                               | APLL_2 Loop Filter Voltage Regulator. Connect a 0.22 $\mu F$ capacitor from this pin to ground. This pin is also the ac ground reference for the integrated APLL_2 external loop filter.                                                                                                                                                                                                                                                                               |
| 46         | LF_2               | I/O              | Loop filter for APLL_2                   | Loop Filter Node for the APLL_2. Connect an external 15 nF capacitor from this pin to Pin 45 (LDO_2).                                                                                                                                                                                                                                                                                                                                                                  |
| 47, 48, 52 | M5, M6, M7         | I/O              | 1.5 V/1.8 V CMOS                         | Configurable Input/Output Pins. These pins are used for status and control of the AD9554-1. These pins are also used at power-up and reset to determine the serial port and address. See the Multifunction Pins at Reset/Power-Up section for more information about the internal 100 k $\Omega$ pull-up or pull-down resistors. These pins are on the VDD digital power domain (Pin 49), and the logic high voltage for this pin matches the voltage of the VDD pins. |
| 50         | XOB                | I                | Differential input                       | Complementary System Clock Input. Complementary signal to XOA. XOB contains internal dc biasing and must be ac-coupled with a 0.1 $\mu F$ capacitor except when using a crystal. When a crystal is used, connect the crystal across XOA and XOB.                                                                                                                                                                                                                       |
| 51         | XOA                | I                | Differential input                       | System Clock Input. XOA contains internal dc biasing and must be ac-coupled with a 0.1 $\mu F$ capacitor except when using a crystal. When a crystal is used, connect the crystal across XOA and XOB. Single-ended CMOS is also an option, but a spur may be introduced if the duty cycle is not 50%. When using XOA as a single-ended input, connect a 0.1 $\mu F$ capacitor from XOB to ground.                                                                      |
| 53         | LF_3               | I/O              | Loop filter for APLL_3                   | Loop Filter Node for the APLL_3. Connect an external 15 nF capacitor from this pin to Pin 54 (LDO_3).                                                                                                                                                                                                                                                                                                                                                                  |
| 54         | LDO_3              | I                | LDO bypass                               | APLL_3 Loop Filter Voltage Regulator. Connect a 0.22 $\mu F$ capacitor from this pin to ground. This pin is also the ac ground reference for the integrated APLL_3 external loop filter.                                                                                                                                                                                                                                                                               |
| 57         | EPAD               | GND              | Exposed pad                              | The exposed pad is the ground connection on the chip. It must be soldered to the analog ground of the printed circuit board (PCB) to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.                                                                                                                                                                                                                                        |

# TYPICAL PERFORMANCE CHARACTERISTICS

$f_R$  = input reference clock frequency,  $f_{OUT}$  = output clock frequency,  $f_{SYS}$  = SYSCLK input frequency, and VDD at 1.8 V.

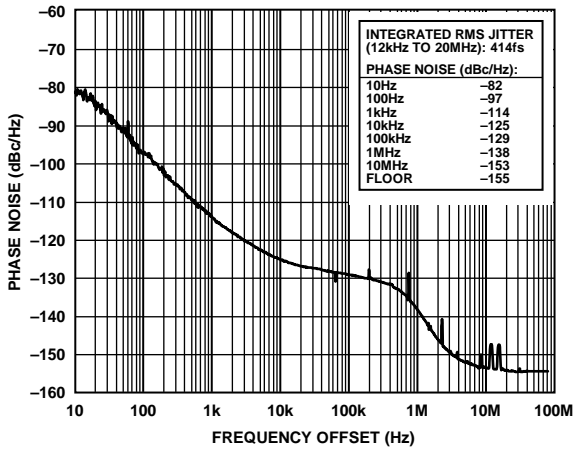


Figure 3. Absolute Phase Noise (Output Driver = 21 mA Mode),  $f_R = 19.44$  MHz,  $f_{OUT} = 156.25$  MHz, DPLL Loop Bandwidth = 50 Hz,  $f_{SYS} = 49.152$  MHz Crystal

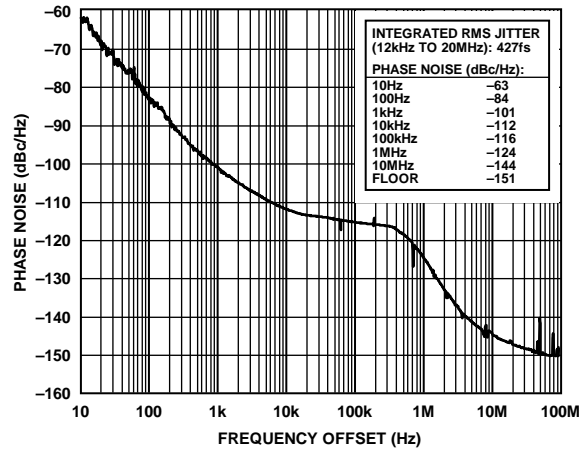


Figure 6. Absolute Phase Noise (Output Driver = 21 mA Mode),  $f_R = 19.44$  MHz,  $f_{OUT} = 693.482991$  MHz, DPLL Loop Bandwidth = 50 Hz,  $f_{SYS} = 49.152$  MHz Crystal

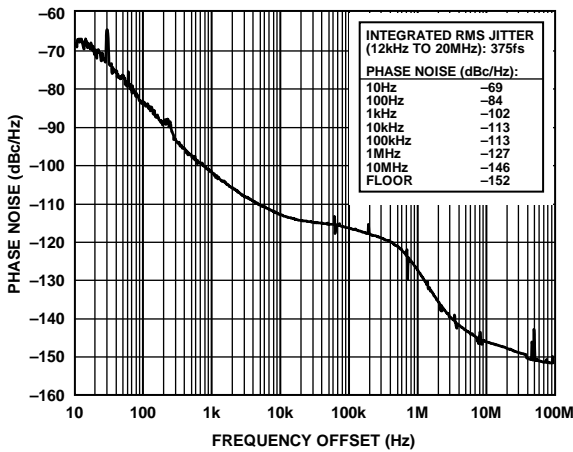


Figure 4. Absolute Phase Noise (Output Driver = 21 mA Mode),  $f_R = 19.44$  MHz,  $f_{OUT} = 622.08$  MHz, DPLL Loop Bandwidth = 50 Hz,  $f_{SYS} = 49.152$  MHz Crystal

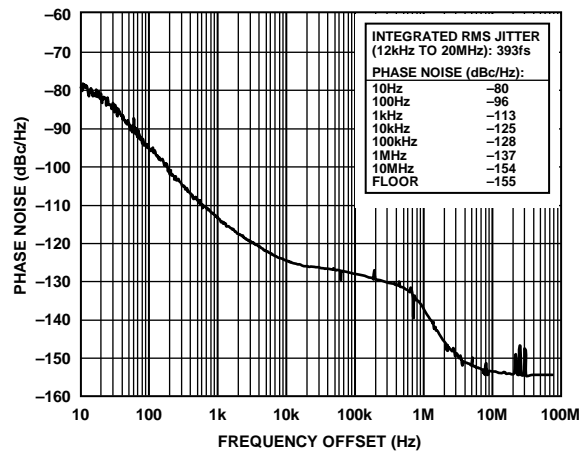


Figure 7. Absolute Phase Noise (Output Driver = 21 mA Mode),  $f_R = 19.44$  MHz,  $f_{OUT} = 174.703$  MHz, DPLL Loop Bandwidth = 1 kHz,  $f_{SYS} = 49.152$  MHz Crystal

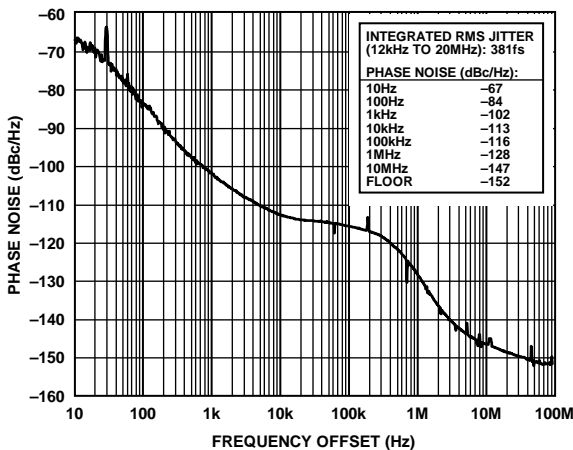


Figure 5. Absolute Phase Noise (Output Driver = 21 mA Mode),  $f_R = 19.44$  MHz,  $f_{OUT} = 644.53125$  MHz, DPLL Loop Bandwidth = 50 Hz,  $f_{SYS} = 49.152$  MHz Crystal

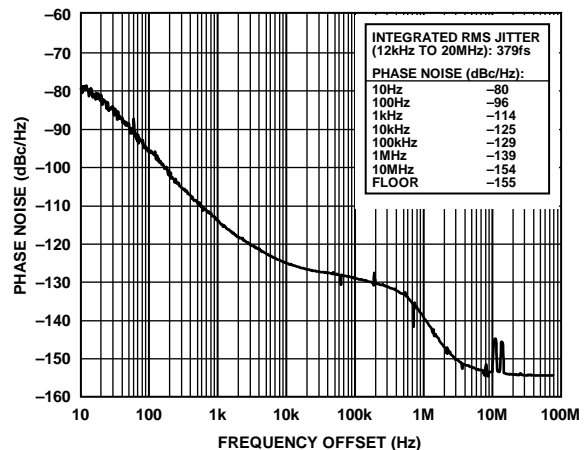


Figure 8. Absolute Phase Noise,  $f_R = 19.44$  MHz,  $f_{OUT} = 161.1328125$  MHz, DPLL Loop Bandwidth = 100 Hz,  $f_{SYS} = 49.152$  MHz Crystal

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12214-304

12214-302

12214-307

12214-303

12214-308

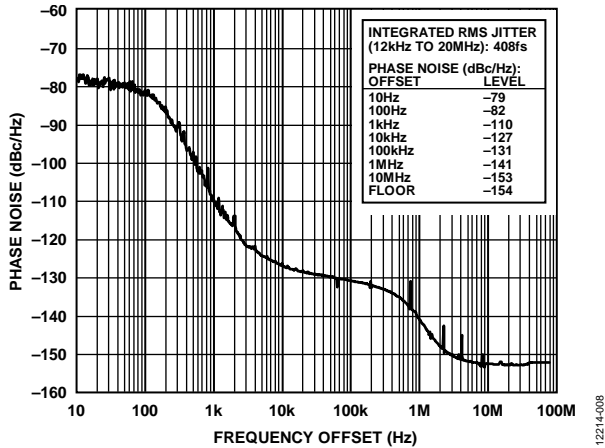


Figure 9. Absolute Phase Noise (Output Driver = 14 mA Mode),  $f_R = 2$  kHz,  $f_{OUT} = 125$  MHz, DPLL Loop Bandwidth = 100 Hz,  $f_{SYS} = 49.152$  MHz Crystal

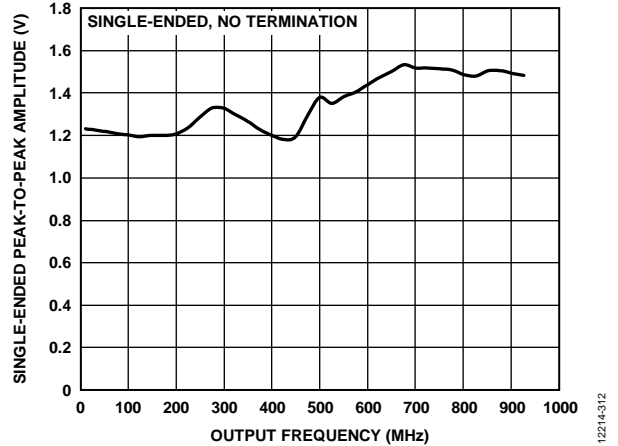


Figure 12. Single-Ended Peak-to-Peak Amplitude vs. Output Frequency, 21 mA Mode (No Termination)

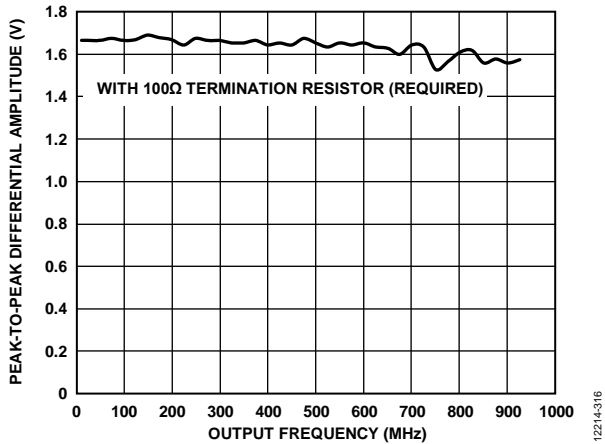


Figure 10. Peak-to-Peak Differential Amplitude vs. Output Frequency, 28 mA Mode (LVPECL-Compatible Mode) with 100  $\Omega$  Termination Resistor (Required)

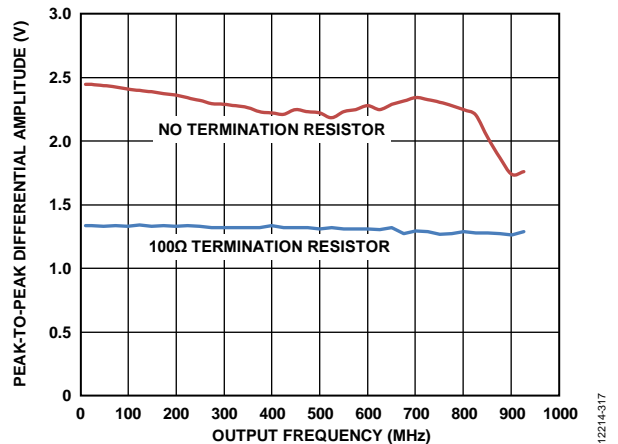


Figure 13. Peak-to-Peak Differential Amplitude vs. Output Frequency, 21 mA Mode

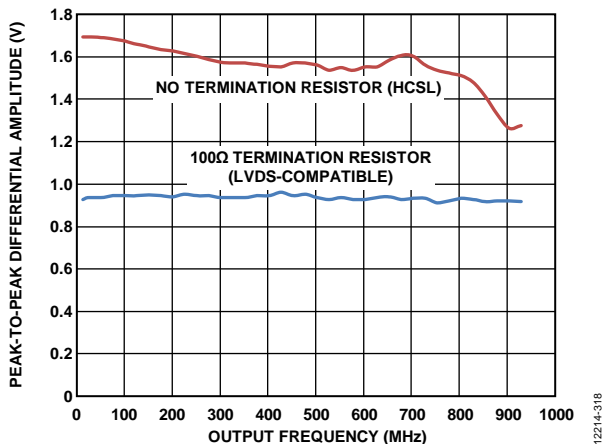


Figure 11. Peak-to-Peak Differential Amplitude vs. Output Frequency, 14 mA Mode

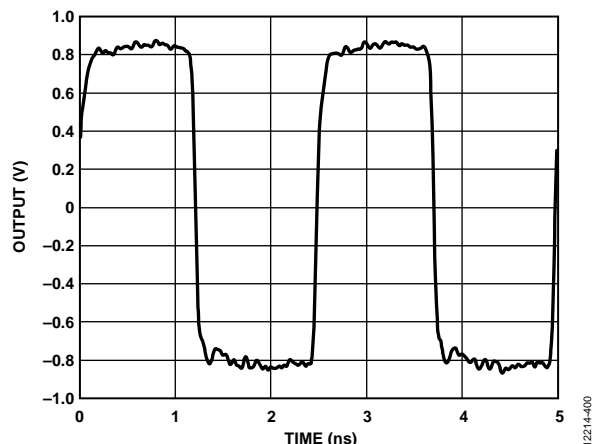


Figure 14. Output Waveform, 28 mA LVPECL-Compatible Mode (400 MHz) with 100  $\Omega$  Termination Resistor

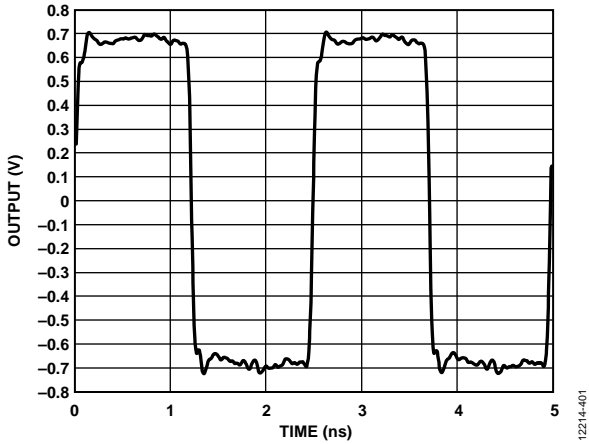


Figure 15. Output Waveform, 21 mA Mode (400 MHz) with 100 Ω Termination at Load

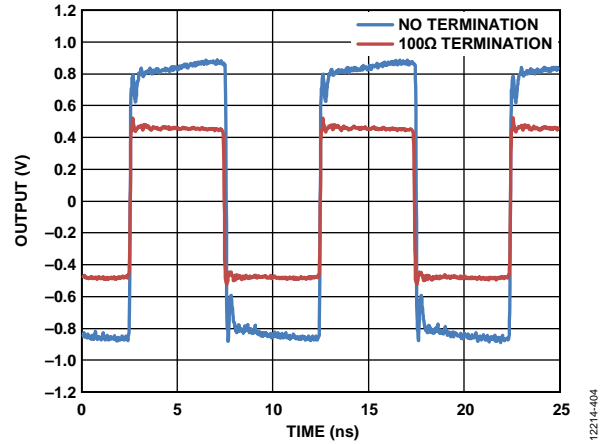


Figure 18. Output Waveform, 14 mA Mode (100 MHz)

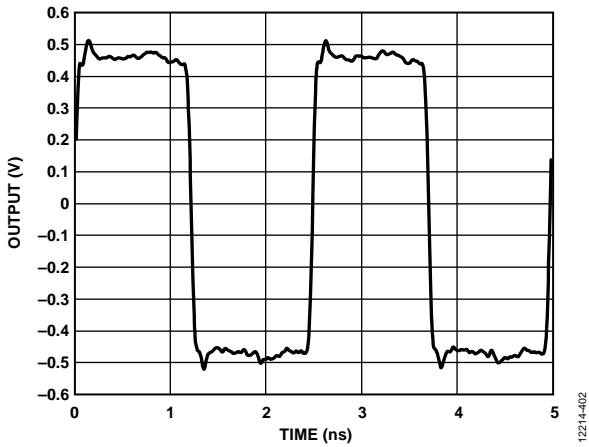


Figure 16. Output Waveform, 14 mA LVDS-Compatible Mode (400 MHz) with 100 Ω Termination at Load

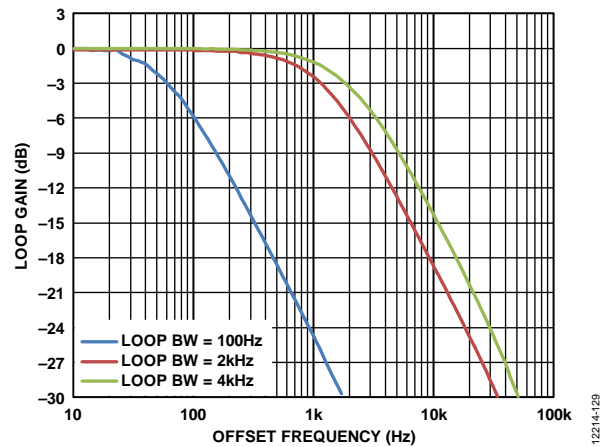


Figure 19. Closed-Loop Transfer Function for 100 Hz, 2 kHz, and 4 kHz Loop Bandwidth Settings; High Phase Margin Loop Filter Setting; Figure Compliant with Telcordia GR-253 Jitter Transfer Test for Loop Bandwidths < 2 kHz (Note that the bandwidth register setting is the point where the open-loop gain = 0 dB.)

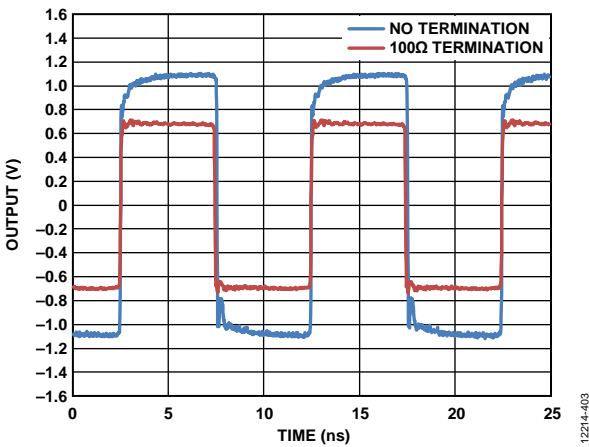


Figure 17. Output Waveform, 21 mA Mode (100 MHz)

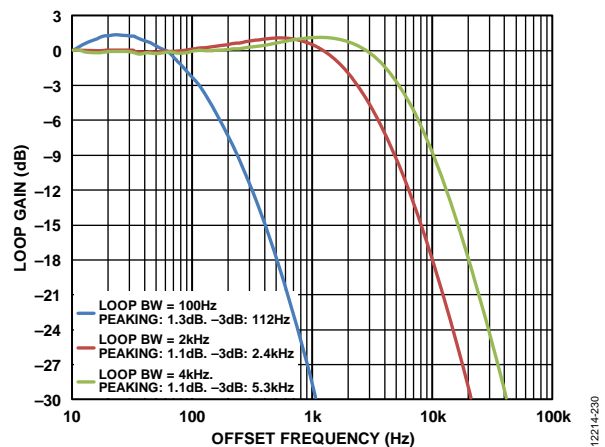


Figure 20. Closed-Loop Transfer Function for 100 Hz, 2 kHz, and 4 kHz Loop Bandwidth Settings; Normal Phase Margin Loop Filter Setting (Note that the bandwidth register setting is the point where the open-loop gain = 0 dB.)

# INPUT/OUTPUT TERMINATION RECOMMENDATIONS

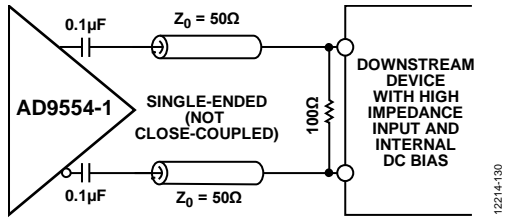


Figure 21. Destination Self-Biased Differential Receiver; Use 14 mA Mode for LVDS-Compatible Amplitude or 28 mA for LVPECL-Compatible Amplitudes (100Ω resistor must be as close to the destination receiver as possible.)

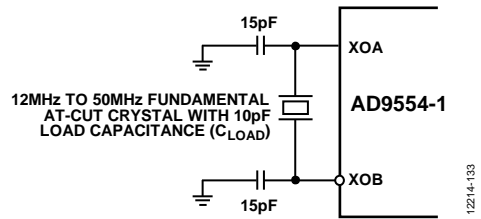


Figure 24. System Clock Input (XOA/XOB) in Crystal Mode (The recommended  $C_{LOAD} = 10\text{ pF}$  is shown. The 15 pF shunt capacitors shown in this figure must equal  $2 \times (C_{LOAD} - C_{STRAY})$ , where  $C_{STRAY}$  is typically 2 pF to 5 pF.)

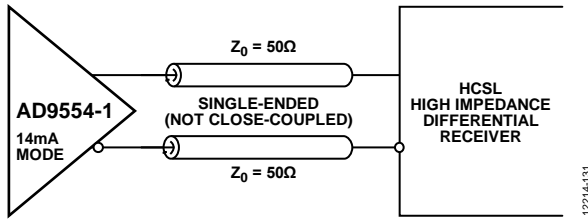


Figure 22. DC-Coupled HCSL Receiver

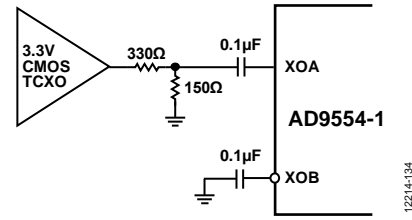


Figure 25. System Clock Input (XOA, XOB) When Using a TCXO/OCXO with 3.3 V CMOS Output

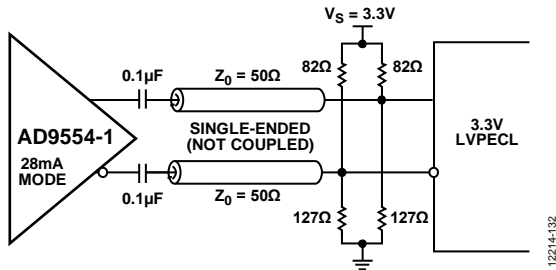


Figure 23. Interfacing the HCSL Driver to a 3.3 V LVPECL Input (This method incorporates impedance matching and dc-biasing for bipolar LVPECL receivers. If the receiver is self-biased, the termination scheme shown in Figure 21 is recommended.)

## GETTING STARTED

### CHIP POWER MONITOR AND STARTUP

The AD9554-1 monitors the voltage on the power supplies at power-up. The VDD pins provide power to the internal voltage regulators to provide a 1.2 V supply to the chip. When the internal 1.2 V supply is greater than  $0.96\text{ V} \pm 0.1\text{ V}$ , the device generates a 10 ms reset pulse. The power-up reset pulse is internal and independent of the RESET pin. This internal power-up reset sequence eliminates the need for the user to provide external power supply sequencing. The M0 through M3 and M5 through M7 values latch 10 ms after the internal reset pulse. Note that there is no M4 pin.

During a device reset (either via the power-up reset pulse or the RESET pin), the M7 to M5 and M3 to M0 multifunction pins behave as high impedance inputs. At the point where the reset condition is cleared, level-sensitive latches capture the logic pattern that is present on the multifunction pins.

### MULTIFUNCTION PINS AT RESET/POWER-UP

The AD9554-1 Mx pins have internal 100 k $\Omega$  pull-up/pull-down resistors.

**Table 21. Mx Pin Internal Pull-Up/Pull-Down Resistor**

| Mx Pin | Pull-Up/Pull-Down Resistor        | Startup Function                |
|--------|-----------------------------------|---------------------------------|
| M0     | 100 k $\Omega$ pull-down resistor | I <sup>2</sup> C address select |
| M1     | None                              | None                            |
| M2     | None                              | None                            |
| M3     | 100 k $\Omega$ pull-down resistor | None                            |
| M4     | Pin does not exist                | None                            |
| M5     | 100 k $\Omega$ pull-down resistor | SPI/I <sup>2</sup> C select     |
| M6     | 100 k $\Omega$ pull-up resistor   | I <sup>2</sup> C address select |
| M7     | 100 k $\Omega$ pull-down resistor | I <sup>2</sup> C address select |

**Table 22. SPI/I<sup>2</sup>C Serial Port Setup**

| M7         | M6 | M5 | M0         | SPI/I <sup>2</sup> C Address                  |
|------------|----|----|------------|-----------------------------------------------|
| Don't care | 0  | 0  | Don't care | Not applicable                                |
| Don't care | 1  | 0  | Don't care | Analog Devices, Inc., unified SPI (default)   |
| 0          | 0  | 1  | 0          | I <sup>2</sup> C, 1101000 (0x68)              |
| 0          | 1  | 1  | 0          | I <sup>2</sup> C, 1101001 (0x69) <sup>1</sup> |
| 1          | 0  | 1  | 0          | I <sup>2</sup> C, 1101010 (0x6A)              |
| 1          | 1  | 1  | 0          | I <sup>2</sup> C, 1101011 (0x6B)              |
| 0          | 0  | 1  | 1          | I <sup>2</sup> C, 1101100 (0x6C)              |
| 0          | 1  | 1  | 1          | I <sup>2</sup> C, 1101101 (0x6D)              |
| 1          | 0  | 1  | 1          | I <sup>2</sup> C, 1101110 (0x6E)              |
| 1          | 1  | 1  | 1          | I <sup>2</sup> C, 1101111 (0x6F)              |

<sup>1</sup> If M5 is high, the I<sup>2</sup>C power-on default is via internal pull-up/pull-down resistors. By pulling M5 high, the user selects I<sup>2</sup>C mode; the default I<sup>2</sup>C address is 0x69.

### DEVICE REGISTER PROGRAMMING USING A REGISTER SETUP FILE

The evaluation software contains a programming wizard and a convenient graphical user interface (GUI) that assists the user in determining the optimal configuration for the DPLLs, APLLs, and SYSCLK based on the desired input and output frequencies. It generates a register setup file with a .STP extension that is easily readable using a text editor.

The user can configure PLL\_0 through PLL\_3 independently. To do so, program the common registers (such as the system clock and reference inputs) first. Next, the registers that are unique to PLL\_0, PLL\_1, PLL\_2, or PLL\_3 can be configured independently.

After using the evaluation software to create the setup file, use the following sequence to program the AD9554-1:

1. Clear the existing voltage controlled oscillator (VCO) calibration: Register 0x0A00 = 0x00. Note that this step is not needed if the device has just been reset.
2. Write the registers in the .STP file starting from Register 0x000 to Register 0x208 to configure the system clock.
3. Write to the following registers:  
Register 0x0FFF = 0xF9 (enable manual V<sub>CAL</sub> reference settings)  
Register 0x1488 = 0x03  
Register 0x1588 = 0x03  
Register 0x1688 = 0x03  
Register 0x1788 = 0x03
4. Write Register 0x000F = 0x01 to update all registers (also referred to as IO\_UPDATE).
5. Write Register 0x0FFF = 0x00 to disable accidental writes to registers addresses above Register 0x0FFF.
6. Write Register 0x0A00 = 0x04 to calibrate the system clock on the next IO\_UPDATE.
7. Issue an IO\_UPDATE by writing Register 0x000F = 0x01.
8. Write the registers in the .STP file starting from Register 0x0300 to Register 0x0B01.
9. To have the outputs toggle (in free run mode) prior to DPLL phase or frequency lock, write Register 0x0A00 = 0x0C. Otherwise, write Register 0x0A00 = 0x04.
10. Issue an IO\_UPDATE by writing Register 0x000F = 0x01.
11. Write Register 0x0A00 = 0x06.
12. Issue an IO\_UPDATE by writing Register 0x000F = 0x01.

### REGISTER PROGRAMMING OVERVIEW

This section provides a programming overview of the register blocks of the AD9554-1, describing what they do and why they are important. This is supplemental information only needed when loading the registers without using the .STP file.

The AD9554-1 evaluation software contains a wizard that determines the register settings based on the input and output frequencies of the user. It is strongly recommended that the evaluation software be used to determine these settings.



**Multifunction Pins (Optional)**

To use any of the multifunction pins for status or control, this step is required. The multifunction pin parameters are located at Register 0x0100 to Register 0x010A.

Table 123 has a list of the Mx pin output functions, and Table 124 has a list of Mx pin input functions.

**IRQ Functions (Optional)**

To use the IRQ feature, this step is required. The IRQ functions are divided into five groups: common, PLL\_0, PLL\_1, PLL\_2, and PLL\_3.

First, choose the events that trigger an IRQ and then set them in Register 0x010F to Register 0x011D. Next, an Mx pin must be assigned to the IRQ function. The user can choose to dedicate one Mx pin to each of the five IRQ groups, or one Mx pin can be assigned for all IRQs.

The IRQ monitor registers are located at Register 0x0D08 to Register 0x0D16. If the desired bits in the IRQ mask registers at Register 0x010F to Register 0x011D are set high, the appropriate IRQ monitor bit at Register 0x0D08 to Register 0x0D16 is set high when the indicated event occurs.

Individual IRQ events are cleared by using the IRQ clearing registers at Register 0x0A05 to Register 0x0A14 or by setting the clear all IRQs bit (Register 0x0A05[0]) to 1b.

The default values of the IRQ mask registers are such that interrupts are not generated. The default IRQ pin (and Mx pins) mode is active high CMOS. The user can also select active low CMOS, open-drain PMOS, and open-drain NMOS independently on any of these pins.

**Watchdog Timer (Optional)**

To use the watchdog timer, this step is required. The watchdog timer control is located at Register 0x010D and Register 0x010E. The watchdog timer is disabled by default.

The watchdog timer is useful for generating an IRQ at a fixed interval. The timer is reset by setting the clear watchdog timer bit in Register 0x0A05[7] to 1.

The user can also program an Mx pin for the watchdog timer output. In this mode, the Mx pin generates a 40 ns pulse every time the watchdog timer expires.

**System Clock Configuration**

The system clock multiplier (SYSCLK) parameters are at Register 0x0200 to Register 0x0208. For optimal performance, use the following steps:

1. Set the system clock PLL input type and divider values.
2. Set the system clock period. It is essential to program the system clock period because many of the [AD9554-1](#) subsystems rely on this value.
3. Set the system clock stability timer. The system clock stability timer specifies the amount of time that the system clock PLL must be locked before the device declares that the system clock is stable. It is critical that the system clock stability

timer be set long enough to ensure that the external source is completely stable when the timer expires. For instance, a temperature compensated crystal oscillator (TCXO) can take longer than 50 ms (the default value for the stability timer) to stabilize after power is applied.

4. Update all registers (Register 0x000F = 0x01).
5. To calibrate the system clock on the next IO\_UPDATE, write Register 0x0A00 = 0x04.
6. Update all registers (Register 0x000F = 0x01).

**Important Notes**

If Bit 2 in Register 0x0A00 is set independently to initiate a system clock PLL calibration, leave this bit set to 1 in all subsequent writes to Register 0x0A00. If this bit is accidentally cleared, recalibrate the system clock VCO or issue a calibrate all command by setting Bit 1 in Register 0x0A00 and by issuing an IO\_UPDATE (Register 0x000F = 0x01).

In addition, the system clock PLL must be locked for the digital PLL blocks to function correctly and to read back the registers updated on the system clock domain. These registers include the status registers, as well as the free running tuning word. APLL calibration and input reference monitoring and validation require that the system clock be stable. Therefore, first ensure that the system clock is stable by checking Bit 1 in Register 0x0D01 when debugging the [AD9554-1](#).

**Reference Inputs**

The reference input parameters and reference dividers are common to all PLLs; there is only one reference divider (R divider) for each reference input. The register address for each reference input follows:

- Register 0x0300 to Register 0x031E for REFA
- Register 0x0320 to Register 0x033E for REFB
- Register 0x0340 to Register 0x035E for REFC
- Register 0x0360 to Register 0x037E for REFD

These registers include the following settings:

- Reference logic type (such as differential, single-ended)
- Reference divider (20-bit R divider value)
- Reference input period and tolerance
- Reference validation timer
- Phase and frequency lock detector settings
- Phase step threshold

Other reference input settings are at the following registers:

- Reference input enable information is found in the DPLL Feedback Dividers section.
- Reference power-down information is found in Register 0x0A01.
- Reference switching mode settings are found in Register 0x0A22 (DPLL\_0), Register 0x0A42 (DPLL\_1), Register 0x0A62 (DPLL\_2), and Register 0x0A82 (DPLL\_3).

### Digital PLL (DPLL) Controls and Settings

The DPLL control parameters are separate for DPLL\_0 through DPLL\_3. They reside in the following registers:

- Register 0x0400 to Register 0x041E (DPLL\_0)
- Register 0x0500 to Register 0x051E (DPLL\_1)
- Register 0x0600 to Register 0x061E (DPLL\_2)
- Register 0x0700 to Register 0x071E (DPLL\_3)

These registers include the following settings:

- 30-bit free running frequency
- DPLL pull-in range limits
- DPLL closed-loop phase offset
- Tuning word history control (for holdover operation)
- Phase slew control (for controlling the phase slew rate during a closed-loop phase adjustment)
- Demapping control

With the exception of the free running tuning word, the default values of these registers are fine for normal operation. The free running frequency of the DPLL determines the frequency that appears at the APLL input when user free run mode is selected. The correct free running frequency is required for the APLL to calibrate and lock correctly.

### Output PLLs (APLLs) and Output Drivers

The registers that control the APLLs and output drivers reside in the following registers:

- Register 0x0430 to Register 0x043E (APLL\_0)
- Register 0x0530 to Register 0x053E (APLL\_1)
- Register 0x0630 to Register 0x063E (APLL\_2)
- Register 0x0730 to Register 0x073E (APLL\_3)

The following functions are controlled in these registers:

- APLL settings (feedback divider, charge pump current)
- Output synchronization mode
- Output divider values
- Output enable/disable (disabled by default)
- Output logic type

The APLL calibration and synchronization bits reside in the following registers:

- Register 0x0A20 (APLL\_0)
- Register 0x0A40 (APLL\_1)
- Register 0x0A60 (APLL\_2)
- Register 0x0A80 (APLL\_3)

### DPLL Feedback Dividers

Each DPLL has separate feedback divider settings for each reference input, which allows the user to have each digital PLL perform a different frequency translation. However, there is only one reference divider (R divider) for each reference input.

The feedback divider register settings for DPLL\_0 reside in the following registers. Feedback divider registers for the remaining three DPLLs mimic the structure of the DPLL\_0 registers, but are offset by 0x0100 registers.

- Register 0x0440 to Register 0x44C (DPLL\_0 for REFA)
- Register 0x044D to Register 0x459 (DPLL\_0 for REFB)
- Register 0x045A to Register 0x466 (DPLL\_0 for REFC)
- Register 0x0467 to Register 0x473 (DPLL\_0 for REFD)
- DPLL\_1 for REFA to DPLL\_1 for REFD: Same as DPLL\_0 but offset by 0x0100 registers
- DPLL\_2 for REFA to DPLL\_2 for REFD: Same as DPLL\_0 but offset by 0x0200 registers
- DPLL\_3 for REFA to DPLL\_3 for REFD: Same as DPLL\_0 but offset by 0x0300 registers

These registers include the following settings:

- Reference priority
- Reference input enable (separate for each DPLL)
- DPLL loop bandwidth
- DPLL loop filter
- DPLL feedback divider (integer portion)
- DPLL feedback divider (fractional portion)
- DPLL feedback divider (modulus portion)

### Common Operational Controls

The common operational controls reside at Register 0x0A00 to Register 0x0A14 and include the following:

- Simultaneous calibration and synchronization of all PLLs
- Global power-down
- Reference power-down
- Reference validation override
- IRQ clearing (for all IRQs)

### PLL\_0 Through PLL\_3 Operational Controls

The PLL\_0 through PLL\_3 operational controls are located at Register 0x0A20 to Register 0x0A84 and include the following:

- APLL calibration and synchronization
- Output driver enable and power-down
- DPLL reference input switching modes
- DPLL open-loop phase stepping control

The user free run bits that enable user free run mode reside in the following registers:

- Register 0x0A22 = 0x01 (DPLL\_0)
- Register 0x0A42 = 0x01 (DPLL\_1)
- Register 0x0A62 = 0x01 (DPLL\_2)
- Register 0x0A82 = 0x01 (DPLL\_3)

### **APLL VCO Calibration**

VCO calibration ensures that the VCO has sufficient operating margin to function across the full temperature range. The user can calibrate each of the four VCOs independently of one another. When calibrating the APLL VCO, it is important to remember the following conditions:

- The APLL VCO calibration does not occur until the system clock is stable.
- The APLL VCO must have the correct frequency from the 30-bit digitally controlled oscillator (DCO) during calibration. The free running tuning word is found in Register 0x0400 to Register 0x0403 (DPLL\_0), Register 0x0500 to Register 0x0503 (DPLL\_1), Register 0x0600 to Register 0x0603 (DPLL\_2), and Register 0x0700 to Register 0x0703 (DPLL\_3).
- The APLL VCO must be recalibrated any time the APLL frequency changes.
- APLL VCO calibration occurs on the low to high transition of the APLL VCO calibration bit (Register 0x0A20[1] for APLL\_0, Register 0x0A40[1] for APLL\_1, Register 0x0A60[1] for APLL\_2, and Register 0x0A80[1] for APLL\_3).
- The VCO calibration bit is not an autoclearing bit. Therefore, this bit must be cleared (and an IO\_UPDATE issued) before the APLL is recalibrated.
- The best way to monitor successful APLL calibration is by monitoring the APLL locked bit in the following registers: Register 0x0D20[3] for APLL\_0, Register 0x0D40[3] for APLL\_1, Register 0x0D60[3] for APLL\_2, and Register 0x0D80[3] for APLL\_3.

### **Generate the Output Clock**

If Register 0x0435 (for PLL\_0), Register 0x0535 (for PLL\_1), Register 0x0635 (for PLL\_2), or Register 0x0735 (for PLL\_3) is programmed for automatic clock distribution synchronization via the DPLL phase or frequency lock, the synthesized output signal appears at the clock distribution outputs. Otherwise, set and then clear the soft sync bit (Bit 2 in Register 0x0A20 for APLL\_0, Bit 2 in Register 0x0A40 for APLL\_1, Bit 2 in Register 0x0A60 for APLL\_2, and Bit 2 in Register 0x0A80 for APLL\_3) or use a multifunction pin input (if programmed accordingly) to generate a clock distribution sync pulse. This sync pulse causes the synthesized output signal to appear at the clock distribution outputs. Note that the sync pulse is delayed until the APLL achieves lock following APLL calibration.

### **Generate the Reference Acquisition**

After the registers are programmed, the DPLLs lock to the reference input that has been manually selected (if any), or the first available reference that has the highest priority.

## THEORY OF OPERATION

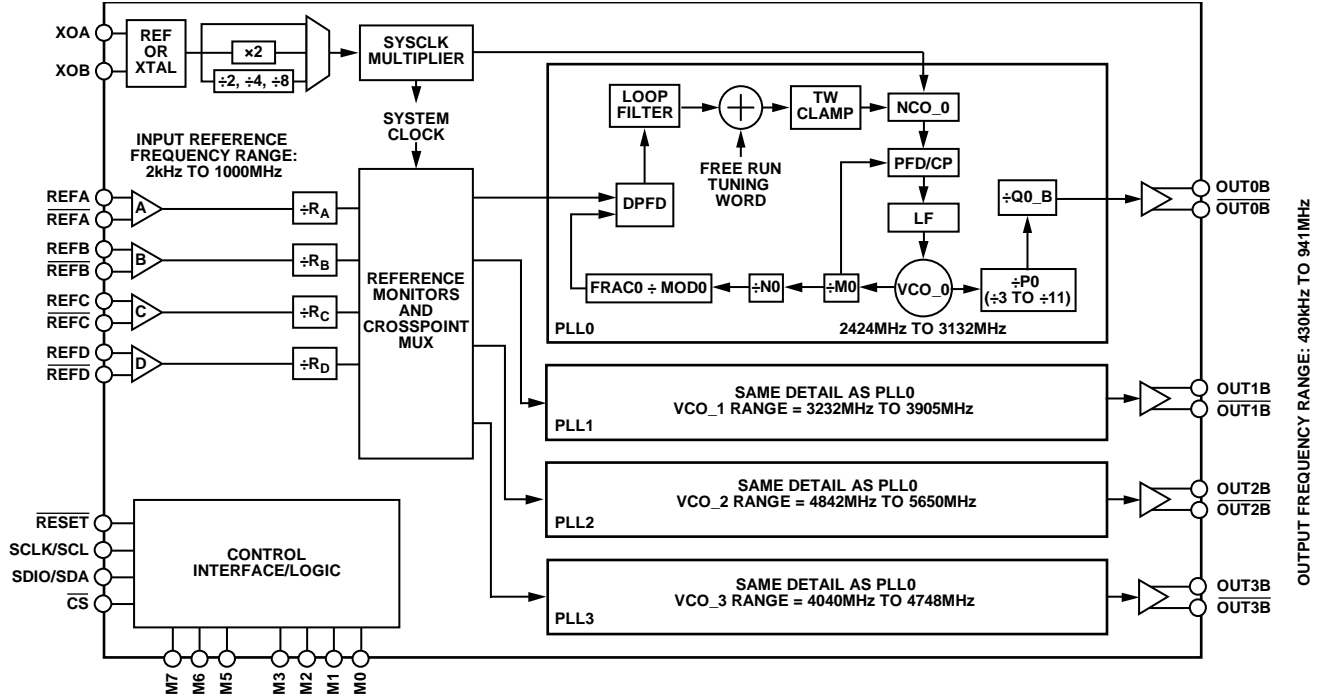


Figure 26. Detailed Block Diagram

## OVERVIEW

The **AD9554-1** provides clocking outputs that are directly related in phase and frequency to the selected (active) reference but with jitter characteristics governed by the system clock, the DCO, and the analog output PLL (APLL). The **AD9554-1** can be thought of as four copies of the **AD9557** inside one package, with a 4:4 crosspoint controlling the reference inputs. The **AD9554-1** supports up to four reference inputs and input frequencies ranging from 2 kHz to 1000 MHz. The cores of this device are four digital phase-locked loops (DPLLs). Each DPLL has a programmable digital loop filter that greatly reduces jitter transferred from the active reference to the output, and these four DPLLs operate completely independently of each other. The **AD9554-1** supports both manual and automatic holdover. While in holdover, the **AD9554-1** continues to provide an output as long as the system clock is present. The holdover output frequency is a time average of the output frequency history prior to the transition to the holdover condition. The device offers manual and automatic reference switchover capability if the active reference is degraded or fails completely. The **AD9554-1** also has adaptive clocking capability that allows the user to dynamically change the DPLL divide ratios while the DPLLs are locked.

The **AD9554-1** includes a system clock multiplier, four DPLLs, and four APLLs. The input signal goes first to the DPLL, which performs the jitter cleaning and most of the frequency translation. Each DPLL features a 30-bit DCO output that generates a signal in the range of 283 MHz to 345 MHz.

The DCO output goes to the APLL, which multiplies the signal up to a range of 2.4 GHz to 5.6 GHz. This signal is then sent to the clock distribution section, which consists of a P divider cascaded with 10-bit channel dividers (divide by 1 to divide by 1024).

The XOA and XOB inputs provide the input for the system clock. These pins accept a reference clock in the 10 MHz to 268 MHz range or a 12 MHz to 50 MHz crystal (XTAL) connected directly across the XOA and XOB inputs. The system clock provides the clocks to the frequency monitors, the DPLLs, and internal switching logic.

Each APLL on the **AD9554-1** has one differential output driver. Each of the four output drivers has a dedicated 10-bit programmable post divider. Each differential driver operates up to 1.25 GHz and is an HCSL driver with a 58  $\Omega$  internal termination resistor on each leg. There are three drive strengths:

- The 14 mA mode is used for HCSL and ac-coupled LVDS. When used as an LVDS-compatible driver, it must be ac-coupled and terminated with a 100  $\Omega$  resistor across the differential pair.
- The 28 mA mode produces a voltage swing and is compatible with LVPECL. If LVPECL signal levels are required, the designer must ac-couple the **AD9554-1** output.
- The 21 mA mode is halfway in between the two other settings.

The AD9554-1 also includes a demapping control function that allows the user to adjust each of the AD9554-1 output frequencies dynamically by periodically writing the actual level and desired level of a first in, first out (FIFO). These levels are intended to match the actual levels on the user's system.

### REFERENCE INPUT PHYSICAL CONNECTIONS

Four pairs of pins (REFA,  $\overline{\text{REFA}}$  to REFD,  $\overline{\text{REFD}}$ ) provide access to the reference clock receivers. To accommodate input signals with slow rising and falling edges, both the differential and single-ended input receivers employ hysteresis. Hysteresis also ensures that a disconnected or floating input does not cause the receiver to oscillate.

When configured for differential operation, the input receivers accommodate either ac- or dc-coupled input signals. If the input receiver is configured for dc-coupled LVDS mode, the input receivers are capable of accepting dc-coupled LVDS signals; however, only up to a maximum of 10.24 MHz. For frequencies greater than that, ac-couple the input clock and use ac-coupled differential mode. The receiver is internally dc biased to handle ac-coupled operation; however, there is no internal 50  $\Omega$  or 100  $\Omega$  termination.

When configured for single-ended operation, the input receivers exhibit a pull-down load of 47 k $\Omega$  (typical). See Register 0x0300 to Register 0x037E for the settings for the reference inputs.

### REFERENCE MONITORS

The accuracy of the input reference monitors depends on a known and accurate system clock period. Therefore, the function of the reference monitors is not operable until the system clock is stable.

#### Reference Period Monitor

Each reference input has a dedicated monitor that repeatedly measures the reference period. The AD9554-1 uses the reference period measurements to determine the validity of the reference based on a set of user provided parameters in the reference input area of the register map. See Register 0x0304 through Register 0x030E for the settings for Reference A, Register 0x0324 through Register 0x032E for the settings for Reference B, Register 0x0344 through Register 0x034E for the settings for Reference C, and Register 0x0364 through Register 0x036E for the settings for Reference D.

The monitor compares the measured period of a particular reference input with the parameters stored in the profile register assigned to that same reference input. The parameters include the reference period, an inner tolerance, and an outer tolerance. A 40-bit number defines the reference period in units of femtoseconds (fs). A 20-bit number defines the inner and outer tolerances. The value stored in the register is the reciprocal of the tolerance specification. For example, a tolerance specification of 50 ppm yields a register value of  $1/(50 \text{ ppm}) = 1/0.000050 = 20,000$  (0x04E20).

The use of two tolerance values provides hysteresis for the monitor decision logic. The inner tolerance applies to a previously faulted reference and specifies the largest period tolerance that a previously faulted reference can exhibit before it qualifies as unfaulted. The outer tolerance applies to an already unfaulted reference. It specifies the largest period tolerance that an unfaulted reference can exhibit before being faulted.

To produce decision hysteresis, the inner tolerance must be less than the outer tolerance. That is, a faulted reference must meet tighter requirements to become unfaulted than an unfaulted reference must meet to become faulted.

#### Reference Validation Timer

Each reference input has a dedicated validation timer. The validation timer establishes the amount of time that a previously faulted reference must remain unfaulted before the AD9554-1 declares that it is valid. The timeout period of the validation timer is programmable via a 16-bit register (Address 0x030F and Address 0x0310 for Reference A). The 16-bit number stored in the validation register represents units of milliseconds (ms), which yields a maximum timeout period of 65,535 ms.

It is possible to disable the validation timer by programming the validation timer to 0. With the validation timer disabled, the user must validate a reference manually via the manual reference validation override controls register (Register 0x0A02).

#### Reference Validation Override Control

The user can also override the reference validation logic and either force an invalid reference to be treated as valid or force a valid reference to be treated as an invalid reference. These controls are in Register 0x0A02 to Register 0x0A03.

### REFERENCE INPUT BLOCK

Unlike the AD9557, the AD9554-1 separates the DPLL reference dividers from the feedback dividers.

The reference input block includes the input receiver, the reference divider (R divider), and the reference input frequency monitor for each reference input. The reference input settings for REFA are grouped together in Register 0x0300 to Register 0x031E. The corresponding registers for REFB through REFD are the following: Register 0x0320 to Register 0x033E, Register 0x0340 to Register 0x035E, and Register 0x0360 to Register 0x037E, respectively.

These registers include the following settings:

- Reference logic type (such as differential, single-ended)
- Reference divider (20-bit R divider value)
- Reference input period and tolerance
- Reference validation timer
- Phase and frequency lock detector settings
- Phase step threshold

The reference prescaler reduces the frequency of this signal by an integer factor,  $R + 1$ , where  $R$  is the 20-bit value stored in the appropriate profile register and  $0 \leq R \leq 1,048,575$ . Therefore, the frequency at the output of the  $R$  divider (or the input to the time-to-digital converter [TDC]) is as follows:

$$f_{TDC} = \frac{f_R}{R+1}$$

After the  $R$  divider, the signal passes to a 4:4 crosspoint that allows any reference input signal to go to any DPLL.

Each DPLL on the [AD9554-1](#) has an independent set of feedback dividers for each reference input. A description of these settings can be found in the Digital PLL (DPLL) Core section.

The [AD9554-1](#) evaluation software includes a frequency planning wizard that configures the profile parameters based on the input and output frequencies.

## REFERENCE SWITCHOVER

An attractive feature of the [AD9554-1](#) is its versatile reference switchover capability. The flexibility of the reference switchover functionality resides in a sophisticated prioritization algorithm that is coupled with register-based controls. This scheme provides the user with maximum control over the state machine that handles the reference switchover.

The main reference switchover control resides in the user mode registers in the PLL\_0 through PLL\_3 operational controls registers. The reference switching mode bits for each DPLL include the following:

- Register 0x0A22[4:2] for DPLL\_0
- Register 0x0A42[4:2] for DPLL\_1
- Register 0x0A62[4:2] for DPLL\_2
- Register 0x0A82[4:2] for DPLL\_3

These bits allow the user to select one of the five operating modes of the reference switchover state machine that follows:

- Automatic revertive mode
- Automatic nonrevertive mode
- Manual with automatic fallback mode
- Manual with holdover fallback mode
- Full manual mode without holdover fallback

In automatic modes, a fully automatic priority-based algorithm selects the active reference. When programmed for automatic mode, the device chooses the highest priority valid reference. When two or more references have the same priority, REFA has preference over REFB, and so on in alphabetical order. However, the reference position is used as a tiebreaker only and does not initiate a reference switch.

An overview of the five operating modes follows:

- **Automatic revertive mode.** The device selects the highest priority valid reference and switches to a higher priority reference if it becomes available, even if the reference in use is still valid. In this mode, the user reference is ignored.
- **Automatic nonrevertive mode.** The device stays with the currently selected reference as long as it is valid, even if a higher priority reference becomes available. The user reference is ignored in this mode.
- **Manual with automatic fallback mode.** The device uses the user reference for as long as it is valid. If it becomes invalid, the reference input with the highest priority is chosen in accordance with the priority-based algorithm.
- **Manual with holdover fallback mode.** The user reference is the active reference until it becomes invalid. At that point, the device goes into holdover.
- **Full manual mode without holdover fallback.** The user reference is the active reference, regardless of whether it is valid.

The user also can force the device directly into holdover or free run operation via the user holdover and user free run bits. In free run mode, the free run frequency tuning word registers define the free run output frequency. In holdover mode, the output frequency depends on the holdover control settings (see the Holdover section).

### **Phase Build-Out Reference Switching**

The [AD9554-1](#) supports phase build-out reference switching, which refers to a reference switchover that completely masks any phase difference between the previous reference and the new reference. That is, there is virtually no phase change detectable at the output when a phase build-out switchover occurs.



### DPLL Digitally Controlled Oscillator (DCO) Free Run Frequency

The AD9554-1 uses a  $\Sigma$ - $\Delta$  modulator as a DCO. The DCO free run frequency can be calculated by

$$f_{DCO\_FREERUN} = f_{SYS} \times \frac{1}{DCOint + \frac{FTW0}{2^{30}}}$$

where:

$f_{SYS}$  is the system clock frequency. See the System Clock (SYSCLK) section for information on calculating the system clock frequency.

$DCOint$  is the DCO integer setting. The DCO integer is usually 7, and it can be found in Register 0x0404[3:0] for DPLL\_0.

$FTW0$  is the value in Register 0x0400 to Register 0x0403 for DPLL\_0 (see Table 31 for corresponding values for DPLL\_1 through DPLL\_3).

### Adaptive Clocking

The AD9554-1 supports adaptive clocking applications such as asynchronous mapping and demapping. For these applications, the output frequency can be dynamically adjusted by up to  $\pm 100$  ppm from the nominal output frequency without manually breaking the DPLL loop and reprogramming the device.

The following registers are used in this function:

- Register 0x0444 to Register 0x0446 (DPLL\_0 N0 divider)
- Register 0x0447 to Register 0x0449 (DPLL\_0 FRAC0 divider)
- Register 0x044A to Register 0x044C (DPLL\_0 MOD0 divider)

Note that the register values shown are for REFA/DPLL\_0. There are corresponding registers for all reference input and DPLL combinations.

Writing to these registers requires an IO\_UPDATE by writing 0x01 to Register 0x000F before the new values take effect.

To make small adjustments to the output frequency, vary the FRAC (FRAC0 through FRAC3) and issue an IO\_UPDATE. The advantage to using only FRAC to adjust the output frequency is that the DPLL does not briefly enter holdover. Therefore, the FRAC bit can be updated as quickly as the phase detector frequency of the DPLL.

Writing to the N (N0 through N3) and MOD (M0 through M3) dividers allows larger changes to the output frequency. When the AD9554-1 detects a write in the N or MOD value, it automatically enters and exits holdover for a brief instant without any disturbance in the output frequency. This limits how quickly the output frequency can be adapted.

It is important to note that the amount of frequency adjustment is limited to  $\pm 100$  ppm before the output PLL (APLL) needs a recalibration. Variations larger than  $\pm 100$  ppm are possible, but such variations can compromise the ability of the AD9554-1 to maintain lock over temperature extremes.

It is also important to remember that the rate of change in output frequency depends on the DPLL loop bandwidth.

### DPLL Phase Lock Detector

The DPLL contains an all-digital phase lock detector. The user controls the threshold sensitivity and hysteresis of the phase detector via the profile registers.

The lock detector behaves in a manner analogous to water in a tub (see Figure 29). The total capacity of the tub is 4096 units, with  $-2048$  denoting empty,  $0$  denoting the 50% point, and  $+2048$  denoting full. The tub also has a safeguard to prevent overflow. Furthermore, the tub has a low water mark at  $-1024$  and a high water mark at  $+1024$ . To change the water level, the user adds water with a fill bucket or removes water with a drain bucket. The user specifies the size of the fill and drain buckets via the 8-bit fill rate and drain rate values in the profile registers.

The water level in the tub is what the lock detector uses to determine the lock and unlock conditions. When the water level is below the low water mark ( $-1024$ ), the lock detector indicates an unlock condition. Conversely, when the water level is above the high water mark ( $+1024$ ), the lock detector indicates a lock condition. When the water level is between the marks, the lock detector holds its last condition. This concept appears graphically in Figure 29, with an overlay of an example of the instantaneous water level (vertical) vs. time (horizontal) and the resulting lock/unlock states.

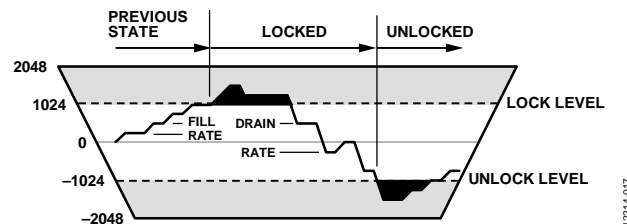


Figure 29. Lock Detector Diagram

During any given PFD phase error sample, the lock detector either adds water with the fill bucket or removes water with the drain bucket (one or the other but not both). The decision of whether to add or remove water depends on the threshold level specified by the user. The phase lock threshold value is a 24-bit number stored in the profile registers and is expressed in picoseconds. Thus, the phase lock threshold extends from 10 ns to  $\pm 16.7 \mu\text{s}$  and represents the magnitude of the phase error at the output of the PFD.

The lock detector compares each phase error sample at the output of the PFD to the programmed phase threshold value. If the absolute value of the phase error sample is less than or equal to the programmed phase threshold value, the lock detector control logic dumps one fill bucket into the tub. Otherwise, it removes one drain bucket from the tub. Note that it is the magnitude, relative to the phase threshold value, that determines whether to fill or drain the bucket, and not the polarity of the phase error sample.



If more filling is taking place than draining, the water level in the tub eventually rises above the high water mark (+1024), which causes the lock detector to indicate lock. If more draining is taking place than filling, the water level in the tub eventually falls below the low water mark (−1024), which causes the lock detector to indicate unlock. The ability to specify the threshold level, fill rate, and drain rate enables the user to tailor the operation of the lock detector to the statistics of the timing jitter associated with the input reference signal.

Note that whenever the AD9554-1 enters the free run or holdover mode, the DPLL phase lock detector indicates an unlocked state. However, when the AD9554-1 performs a reference switch, phase step detection, or loop bandwidth change, the state of the lock detector prior to the switch is preserved during the transition period.

#### **DPLL Frequency Lock Detector**

The operation of the frequency lock detector is identical to that of the phase lock detector. The only difference is that the fill or drain decision is based on the period deviation between the reference and feedback signals of the DPLL instead of the phase error at the output of the PFD.

The frequency lock detector uses a 24-bit frequency threshold register specified in units of picoseconds. Thus, the frequency threshold value extends from 10 ps to  $\pm 16.7 \mu\text{s}$ . It represents the magnitude of the difference in period between the reference and feedback signals at the input to the DPLL. For example, if the divided down reference signal is 80 kHz and the feedback signal is 79.32 kHz, the period difference is approximately 107.16 ns ( $|1/80,000 - 1/79,320| \approx 107.16 \text{ ns}$ ).

#### **Frequency Clamp**

The AD9554-1 digital PLL features a digital tuning word clamp that ensures that the digital PLL output frequency stays within a defined range. This feature is very useful to eliminate undesirable behavior in cases where the reference input clocks may be unpredictable. The tuning word clamp is also useful to guarantee that the APLL never loses lock by ensuring that the APLL VCO frequency stays within its tuning range.

#### **Frequency Tuning Word History**

The AD9554-1 has the ability to track the history of the tuning word samples generated by the DPLL digital loop filter output. It does so by periodically computing the average tuning word value over a user-specified interval. This average tuning word is used during holdover mode to maintain the average frequency when no input references are present.

### **LOOP CONTROL STATE MACHINE**

#### **Switchover**

Switchover occurs when the loop controller switches directly from one input reference to another. The AD9554-1 handles a reference switchover by briefly entering holdover mode, loading the new DPLL parameters, and then immediately recovering. During the switchover event, however, the AD9554-1 preserves the status of the lock detectors to avoid phantom unlock indications.

#### **Holdover**

The holdover state of the DPLL is typically used when none of the input references are present; although, the user can also manually engage holdover mode. In holdover mode, the output frequency remains constant. The accuracy of the AD9554-1 in holdover mode is dependent on the device programming and availability of the tuning word history.

#### **Recovery from Holdover**

When in holdover and a valid reference becomes available, the device exits holdover operation. The loop state machine restores the DPLL to closed-loop operation, locks to the selected reference, and sequences the recovery of all the loop parameters based on the profile settings for the active reference.

Note that, if the DPLL\_x user holdover bit is set, the device does not automatically exit holdover when a valid reference is available. However, automatic recovery can occur after clearing the user holdover bit.

## SYSTEM CLOCK (SYSCLK)

### SYSCLK INPUTS

#### Functional Description

The SYSCLK circuit provides a low jitter, stable, high frequency clock for use by the rest of the chip. The XOA and XOB pins connect to the internal SYSCLK multiplier. The SYSCLK multiplier can synthesize the system clock by connecting a crystal resonator across the XOA and XOB input pins or by connecting a low frequency clock source. The optimal signal for the system clock input is either a crystal in the 50 MHz range or an ac-coupled square wave with a 800 mV p-p amplitude.

#### SYSCLK Reference Frequency

For the AD9554-1 to function properly, enter the system clock reference frequency into Register 0x0202 to Register 0x0205. The ability of the AD9554-1 to accurately measure the frequency of the reference input depends on how accurately this register setting matches the frequency on the system clock input.

#### Choosing the SYSCLK Source

There are two internal paths for the SYSCLK input signal: crystal resonator (XTAL) and nonXTAL.

Using a TCXO for the system clock is a common use for the nonXTAL path. Applications requiring DPLL loop bandwidths of less than 50 Hz or high stability in holdover mode require a TCXO or oven controlled crystal oscillator (OCXO). As an alternative to the 49.152 MHz crystal for these applications, the AD9554-1 reference design uses a 19.2 MHz TCXO, which offers excellent holdover stability and a good combination of low jitter and low spurious content.

The differential receiver connected to the XOA and XOB pins is self-biased to a dc level of ~0.6 V, and ac coupling is strongly recommended to maintain a 50% input duty cycle. When a 3.3 V CMOS oscillator is in use, it is important to ac-couple and use a voltage divider to reduce the input high voltage to a maximum of 1.14 V. The target voltage swing must be 800 mV p-p. See Figure 25 for details on connecting a 3.3 V CMOS TCXO to the system clock input.

The nonXTAL input path permits the user to provide an LVPECL, LVDS, CMOS, or sinusoidal low frequency clock for multiplication by the integrated SYSCLK PLL. However, when using a sinusoidal input signal, it is best to use a frequency of  $\geq 20$  MHz. Otherwise, the resulting low slew rate can lead to poor noise performance. Note that there is an optional 2 $\times$  frequency multiplier to double the rate at the input to the SYSCLK PLL and potentially reduce the PLL in-band noise. However, to avoid exceeding the maximum PFD rate of 300 MHz, the 2 $\times$  frequency multiplier is only for input frequencies less than 150 MHz. Note that using the doubler when the duty is not close to 50% results in higher spurious noise and may prevent the system clock PLL from locking.

The nonXTAL path also includes an input divider (M) that is programmable for divide-by-1, -2, -4, or -8. The purpose of the divider is to allow additional flexibility in setting the system clock frequency to avoid spurs in the output clocks.

The XTAL path enables the connection of a crystal resonator (typically 12 MHz to 50 MHz) across the XOA and XOB pins. An internal amplifier provides the negative resistance required to induce oscillation. The internal amplifier expects an AT cut, fundamental mode crystal with a 100  $\Omega$  maximum motional resistance. The following crystals, listed in alphabetical order, may meet these criteria. Analog Devices does not guarantee their operation with the AD9554-1, nor does Analog Devices endorse one crystal supplier over another. The AD9554-1 reference design uses a 49.152 MHz crystal, which is high performance, low spurious content, and readily available.

- AVX/Kyocera CX3225SB
- ECS, Inc. ECX-32
- Epson/Toyocom TSX-3225
- Fox FX3225BS
- NDK NX3225SA
- Siward SX-3225
- Suntu SCM10B48-49.152 MHz

### SYSCLK MULTIPLIER

The SYSCLK PLL multiplier is an integer-N design with an integrated VCO. It provides a means to convert a low frequency clock input to the desired system clock frequency,  $f_{\text{SYS}}$  (2250 MHz to 2415 MHz). The SYSCLK PLL multiplier accepts input signals of between 10 MHz and 268 MHz. The PLL contains a feedback divider (K) that is programmable for divide values between 4 and 255.

$$f_{\text{SYS}} = f_{\text{OSC}} \times \frac{\text{SYSCLK\_KDIV}}{\text{SYSCLK\_JDIV}}$$

where:

$f_{\text{OSC}}$  is the frequency at the XOA and XOB pins.

SYSCLK\_KDIV is the K divider value stored in Register 0x0200.

SYSCLK\_JDIV is the system clock J1 divider that is determined by setting Register 0x0201[2:1].

If the system clock doubler is used, the value of SYSCLK\_KDIV should be half of its original value.

The system clock multiplier features a simple lock detector that compares the time difference between the reference and feedback edges. The most common cause of the SYSCLK multiplier not locking is a non-50% duty cycle at the SYSCLK input while the system clock doubler is enabled.

**System Clock Stability Timer**

Because multiple blocks inside the [AD9554-1](#) depend on the system clock being at a known frequency, the system clock must be stable before activating the monitors. At initial power-up, the system clock status is not known; therefore, it is reported as being unstable. After the system clock registers have been programmed and the SYSCLK VCO has been calibrated, the system clock PLL locks shortly thereafter.

When the SYSCLK PLL locks, a timer runs for the duration stored in the system clock stability period registers. If the locked condition

is violated any time during this waiting period, the timer is reset and halted until a locked condition is reestablished. After the specified period elapses, the internal logic of the [AD9554-1](#) reports the system clock as stable.

Note that any time the system clock stability timer is changed in Register 0x0206 through Register 0x0208, it is reset automatically. The system clock stability timer starts counting when the next IO\_UPDATE is issued (assuming that the system clock PLL is locked).

## OUTPUT ANALOG PLL (APLL)

There are four output analog PLLs (APLLs) on the AD9554-1. They provide the frequency upconversion from the digital PLL (DPLL) outputs. The frequency ranges for each APLL are in Table 11.

Each APLL also provides a noise filter on the DPLL output. The APLL reference input is the output of the DPLL. The feedback divider is an integer divider. The loop filter is partially integrated with one external 15 nF capacitor that connects to the internal LDO. In addition to the capacitor, there is an additional 0.22  $\mu$ F capacitor from the LDO pin to ground. The nominal loop bandwidth for all four APLLs is 240 kHz.

The APLL\_0 block diagram is shown in Figure 30. APLL\_1 through APLL\_3 are copies of APLL\_0 with different VCO ranges. Each APLL\_x input is connected to the respective DPLL\_x output, and each APLL\_x output is connected to the respective Px divider.

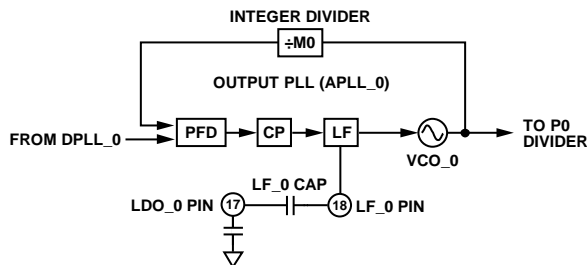


Figure 30. APLL\_0 Block Diagram

## APLL CONFIGURATION

The frequency wizard that is included in the evaluation software configures the APLL, and the user should not need to make changes to the APLL settings. However, there may be special cases where the user may want to adjust the APLL loop bandwidth to meet a specific phase noise requirement. The easiest way to change the APLL loop bandwidth is to adjust the APLL charge pump current which is controlled in the following registers:

- Register 0x0430 (APLL\_0)
- Register 0x0530 (APLL\_1)
- Register 0x0630 (APLL\_2)
- Register 0x0730 (APLL\_3)

There is sufficient stability ( $68^\circ$  of phase margin) in the APLL default settings to permit a broad range of adjustment without causing the APLL to be unstable.

## APLL CALIBRATION

Calibration of the APLLs must be performed at startup and whenever the nominal input frequency to the APLL changes by more than  $\pm 100$  ppm; although, the APLL maintains lock over voltage and temperature extremes without recalibration.

APLL calibration at startup is normally performed during initial register loading, see the detailed instructions in the Device Register Programming Using a Register Setup File section.

To recalibrate the APLL VCO after the chip has been running, first, input the new settings (if any). The user can calibrate APLL\_0 without disturbing any of the other three APLLs (APLL\_1, APLL\_2, and APLL\_3).

Use the following steps to recalibrate the APLL VCO. It is important to note that an IO\_UPDATE (Register 0x000F = 0x01) is needed after each of these steps.

1. Ensure that the DPLL free run tuning word is set (Register 0x0A22[0] = 1b for DPLL\_0, Register 0x0A42[0] = 1b for DPLL\_1, Register 0x0A62[0] = 1b for DPLL\_2, and Register 0x0A82[0] = 1b for DPLL\_3).
2. Clear the desired APLL calibration bit (Register 0x0A20[1] = 0b for APLL\_0, Register 0x0A40[1] = 0b for APLL\_1, Register 0x0A60[1] = 0b for APLL\_2, and Register 0x0A80[1] = 0b for APLL\_3). Alternatively, the user can write Register 0xA00 = 0x00 to clear the calibrate all bit. This allows the user to set this bit in the next step to calibrate all four VCOs at the same time.
3. Set the desired APLL calibration bit (Register 0x0A20[1] = 1b for APLL\_0, Register 0x0A40[1] = 1b for APLL\_1, Register 0x0A60[1] = 1b for APLL\_2, and Register 0x0A80[1] = 1b for APLL\_3). Alternatively, the user can write R0xA00=0x02 to calibrate all four VCOs at the same time.
4. To ensure that the APLLs have locked, poll the APLL lock status (Register 0x0D20[3] = 1b indicates lock for APLL\_0, Register 0x0D40[3] = 1b indicates lock for APLL\_1, Register 0x0D60[3] = 1b indicates lock for APLL\_2, and Register 0x0D80[3] = 1b indicates lock for APLL\_3).
5. Ensure that the DPLL free run tuning word is cleared (Register 0x0A22[0] = 0b for DPLL\_0, Register 0x0A42[0] = 0b for DPLL\_1, Register 0x0A62[0] = 0b for DPLL\_2, and Register 0x0A82[0] = 0b for DPLL\_3).

## CLOCK DISTRIBUTION

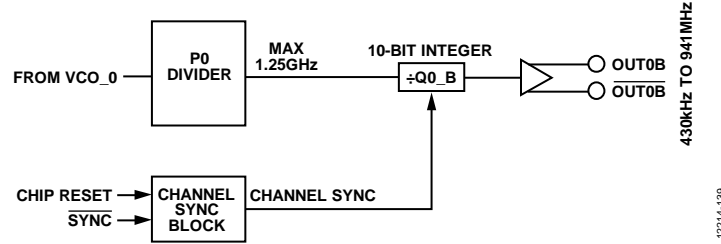


Figure 31. Clock Distribution Block Diagram from VCO\_0 for the PLL\_0

The AD9554-1 has four identical clock distribution sections for PLL\_0 through PLL\_3. See Figure 31 for a diagram of the clock distribution block for PLL\_0.

### CLOCK DIVIDERS

#### P Dividers

The first block in each clock distribution section is the P divider. The P divider divides the VCO output frequency down to a frequency of  $\leq 1.25$  GHz and has special circuitry to maintain a 50% duty cycle for any divide ratio.

The following registers contain the P divider settings:

- Register 0x0434[3:0] for PLL\_0, P0 divider
- Register 0x0534[3:0] for PLL\_1, P1 divider
- Register 0x0634[3:0] for PLL\_2, P2 divider
- Register 0x0734[3:0] for PLL\_3, P3 divider

#### Channel Dividers

The channel divider blocks, Q0\_B through Q3\_B are 10-bit integer dividers with a divide range of 1 to 1024. The channel divider block contains duty cycle correction that generates approximately 50% duty cycle for both even and odd divide ratios. The maximum input frequency to the channel dividers is 1.25 GHz.

The following registers contain the channel dividers:

- Register 0x043C to Register 0x043E for Q0\_B divider
- Same as Q0\_B but offset by 0x0100 registers for Q1\_B divider
- Same as Q0\_B but offset by 0x0200 registers for Q2\_B divider
- Same as Q0\_B but offset by 0x0300 registers for Q3\_B divider

### OUTPUT AMPLITUDE AND POWER-DOWN

The output drivers can be individually powered down. The output mode control (including power-down) can be found in the following registers:

- Register 0x043B[2:1] for OUT0B
- Register 0x053B[2:1] for OUT1B
- Register 0x063B[2:1] for OUT2B
- Register 0x073B[2:1] for OUT3B

The operating mode controls include the following:

- Output drive strength
- Output polarity
- Divide ratio
- Phase of each output channel

The HCSL drivers feature a programmable drive strength that allows the user to choose between a strong, high performance driver or a lower power setting with less electromagnetic interference (EMI) and crosstalk. The best setting is application dependent.

All outputs have three current settings that provide increased output amplitude in applications that require it. However, the only modes that support dc coupling without termination at the destination are the 14 mA HCSL and 21 mA modes. The 28 mA mode must have either 50  $\Omega$  to ground on each leg or 100  $\Omega$  across the differential pair.

For applications where LVPECL levels are required, the user must choose the 28 mA mode, ac-couple the output signal, and provide 100  $\Omega$  termination across the differential pair at the destination. Damage to the output drivers can result if 28 mA mode is used without external termination resistors (either to ground or across the differential pair). See the Input/Output Termination Recommendations section for recommended termination schemes.

## CLOCK DISTRIBUTION SYNCHRONIZATION

### *Divider Synchronization*

The dividers in the channels can be synchronized with each other. At power-up, they are held static until a synchronization signal is initiated through the serial port or a DPLL locked synchronization. This mode of operation provides time for APLL calibration before the outputs are enabled.

A user initiated sync signal can also be supplied to the dividers at any time (as a manual synchronization) using an Mx pin.

A channel can be programmed to ignore the sync function. When programmed to ignore the sync function, the channel sync block issues a sync pulse immediately, and the channel ignores all other sync signals.

The digital logic triggers a sync event from one of the following sources:

- Register programming through serial port
- A multifunction pin configured for the sync signal
- Other automatic conditions determined by the DPLL configuration: DPLL lock or reference clock synchronization

## STATUS AND CONTROL

### MULTIFUNCTION PINS (M0 TO M3 AND M5 TO M7)

The AD9554-1 has seven digital CMOS input/output pins (M0 to M3 and M5 to M7) that are configurable for a variety of uses. Note that there is no M4 pin for this device. To use these functions, the user must set them by writing to Register 0x0100 to Register 0x0101. The function of these pins is programmable via the register map. Each pin can control or monitor an assortment of internal functions based on Register 0x0103 to Register 0x010A.

The Mx pins feature a special write detection logic that prevents these pins from behaving unpredictably when the Mx pins function changes. When the user writes to these registers, the existing Mx pin function stops. The new Mx pin function takes effect on the next IO\_UPDATE (Register 0x000F = 0x01).

The Mx pins operate in one of four modes: active high CMOS, active low CMOS, open-drain PMOS, and open-drain NMOS.

**Table 23. Mx Pins Four Modes of Operation**

| Setting | Mode             | Description                                                                                                                                   |
|---------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 00      | Active high CMOS | When deasserted, the Mx pin is Logic 0.<br>When asserted, the Mx pin is Logic 1, which is the default operating mode.                         |
| 01      | Active low CMOS  | When deasserted, the Mx pin is Logic 1.<br>When asserted, the Mx pin is Logic 0.                                                              |
| 10      | Open-drain PMOS  | When deasserted, the Mx pin is high impedance.<br>When the Mx pin is asserted, it is active high; it requires an external pull-down resistor. |
| 11      | Open-drain NMOS  | When deasserted, the Mx pin is high impedance.<br>When the Mx pin is asserted, it is active low; it requires an external pull-up resistor.    |

To monitor an internal function with a multifunction pin, write a Logic 1 to the most significant bit of the register associated with the desired multifunction pin. The value of the seven least significant bits of the register defines the control function, as shown in Table 123.

To control an internal function with a multifunction pin, write a Logic 0 to the most significant bit of the register associated with the desired multifunction pin. The monitored function depends on the value of the seven least significant bits of the register, as shown in Table 124.

Note that each Mx pin has an open-drain mode that allows the user to perform logical AND and logical OR functions with the Mx pin outputs. For instance, it is possible to connect the IRQ lines of multiple AD9554-1s on one board together and to make the IRQ line the logical OR of each AD9554-1 IRQ line.

It is also possible to have an input function like IRQ clearing to be the logical combination of multiple inputs. For example, IRQ clearing is desired only if M2 is high and M3 is low, and either M0 is high or M1 is low.

In function form, this is the following:

$$Result = (M0 \parallel !M1) \&\& M2 \&\& !M3$$

To accomplish this, set the M0 through M3 pins as the IRQ clearing function, and set the Mx pin modes of operation as the following:

- M0 = OR true signal (Register 0x100[1:0] = 10)
- M1 = OR inverted signal (Register 0x100[3:2] = 11)
- M2 = AND true signal (Register 0x100[5:4] = 00)
- M3 = AND inverted signal (Register 0x100[7:6] = 01)

### IRQ FUNCTION

The AD9554-1 IRQ function can be assigned to any Mx pin. There are five IRQ categories: PLL0, PLL1, PLL2, PLL3, and common. This means an Mx pin can be set to respond only to IRQs that relate to one of the PLLs or to common functions. An Mx pin can also be set to respond to all IRQs.

The AD9554-1 asserts an IRQ when any bit in the IRQ monitor register (Register 0x0D08 to Register 0x0D16) is a Logic 1. Each bit in this register is associated with an internal function that is capable of producing an interrupt. Furthermore, each bit of the IRQ monitor register is the result of a logical AND of the associated internal interrupt signal and the corresponding bit in the IRQ mask register (Register 0x010F to Register 0x011D). That is, the bits in the IRQ mask registers have a one-to-one correspondence with the bits in the IRQ monitor registers. When an internal function produces an interrupt signal and the associated IRQ mask bit is set, the corresponding bit in the IRQ monitor register is set. Be aware that clearing a bit in the IRQ mask register removes only the mask associated with the internal interrupt signal. It does not clear the corresponding bit in the IRQ monitor register.

The IRQ function is edge triggered which means that if the condition that generated an IRQ (for example, loss of DPLL\_0 lock) still exists after an IRQ is cleared, the IRQ does not reactivate until DPLL\_0 lock is restored and lost again. However, if the IRQs are enabled when DPLL\_0 is not locked, an IRQ is generated.

The IRQ function of an Mx pin is the result of a logical OR of all the IRQ monitor register bits. The AD9554-1 asserts an IRQ as long as any of the IRQ monitor register bits is a Logic 1. Note that it is possible to have multiple bits set in the IRQ monitor registers. Therefore, when the AD9554-1 asserts an IRQ, it may indicate an interrupt from several different internal functions. The IRQ monitor registers provide a way to interrogate the AD9554-1 to determine which internal function(s) produced the interrupt.

Typically, when the AD9554-1 asserts an IRQ, the user interrogates the IRQ monitor registers to identify the source of the interrupt request. After servicing an indicated interrupt, the user must clear the associated IRQ monitor register bit via the IRQ clearing registers (Address 0x0A05 to Address 0x0A14). The bits in the IRQ clearing registers have a one-to-one correspondence with the bits in the IRQ monitor registers.

Note that the IRQ clearing registers are autoclearing. The Mx pin associated with an IRQ remains asserted until the user clears all of the bits in the IRQ monitor registers that indicate an interrupt.

All IRQ monitor register bits can be cleared by setting the clear all IRQs bit in the IRQ register (Register 0x0A05). Note that the bits in Register 0x0A05 are autoclearing. Setting Bit 0 results in the deassertion of all IRQs. Alternatively, the user can program any of the multifunction pins to clear all IRQs, which allows the user to clear all IRQs by means of a hardware pin rather than by a serial input/output port operation.

## WATCHDOG TIMER

The watchdog timer is a general-purpose programmable timer. To set the timeout period, the user writes to the 16-bit watchdog timer register (Address 0x010D to Address 0x010E). A value of 0x0000 in this register disables the timer. A nonzero value sets the timeout period in milliseconds, giving the watchdog timer a range of 1 ms to 65.535 sec. The relative accuracy of the timer is approximately 0.1% with an uncertainty of 0.5 ms.

If enabled, the timer runs continuously and generates a timeout event when the timeout period expires. The user has access to the watchdog timer status via the IRQ mechanism and the multifunction pins (M0 to M3 and M5 to M7). In the case of the multifunction pins, the timeout event of the watchdog timer is a pulse that lasts 96 system clock periods (which is approximately 40 ns).

There are two ways to reset the watchdog timer (thereby preventing it from causing a timeout event). The first method is to write a Logic 1 to the autoclearing clear watchdog timer bit in the clear IRQ groups register (Register 0x0A05, Bit 7). Alternatively, the user can program any of the multifunction pins to reset the watchdog timer. When used in this way, the user can reset the timer by means of a hardware pin rather than by a serial I/O port operation.



## SERIAL CONTROL PORT

The [AD9554-1](#) serial control port is a flexible, synchronous serial communications port that provides a convenient interface to many industry-standard microcontrollers and microprocessors. The [AD9554-1](#) serial control port is compatible with most synchronous transfer formats, including I<sup>2</sup>C, Motorola SPI, and Intel SSR protocols. The serial control port allows read/write access to the [AD9554-1](#) register map.

The [AD9554-1](#) uses the Analog Devices unified SPI protocol (see [Analog Devices Serial Control Interface Standard](#)). The unified SPI protocol guarantees that all new Analog Devices products using the unified protocol have consistent serial port characteristics. The SPI port configuration is programmable via Register 0x0000. This register is a part of the SPI control logic rather than in the register map and is distinct from the I<sup>2</sup>C Register 0x0000.

Unified SPI differs from the SPI port found on older products like the [AD9557](#) and [AD9558](#) in the following ways:

- Unified SPI does not have byte counts. A transfer is terminated when the  $\overline{\text{CS}}$  pin goes high. The W1 and W0 bits in the traditional SPI become the A12 and A13 bits of the register address. This is similar to streaming mode in the traditional SPI.
- The address ascension bit (Register 0x0000) controls whether register addresses are automatically incremented or decremented regardless of the LSB/MSB first setting. In traditional SPI, LSB first dictated autoincrements and MSB first dictated autodecrements of the register address.
- Devices that adhere to the unified serial port have a consistent structure of the first 16 register addresses.

Although the [AD9554-1](#) supports both the SPI and I<sup>2</sup>C serial port protocols, only one is active following power-up (as determined by the M0, M5, M6, and M7 multifunction pins during the start-up sequence). The only way to change the serial port protocol is to reset (or power cycle) the device.

### SPI/I<sup>2</sup>C PORT SELECTION

Because the [AD9554-1](#) supports both SPI and I<sup>2</sup>C protocols, the active serial port protocol depends on the logic state of M0, M5, M6, and M7 pins at reset or power-on. See Table 22 for the I<sup>2</sup>C address assignments.

## SPI SERIAL PORT OPERATION

### Pin Descriptions

The SCLK (serial clock) pin serves as the serial shift clock. This pin is an input. SCLK synchronizes serial control port read and write operations. The rising edge SCLK registers write data bits, and the falling edge registers read data bits. The SCLK pin supports a maximum clock rate of 50 MHz.

Data is transferred on the serial data input/output (SDIO) pin. The [AD9554-1](#) does not have a dedicated SDO pin, so it supports only bidirectional (3-wire) SPI mode.

The  $\overline{\text{CS}}$  (chip select) pin is an active low control that gates read and write operations. Assertion (active low) of the  $\overline{\text{CS}}$  pin initiates a write or read operation to the [AD9554-1](#) SPI port. Any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented based on the setting of the address ascension bit (Register 0x0000).  $\overline{\text{CS}}$  must be deasserted at the end of the last byte transferred, thereby ending the stream mode. This pin is internally connected to a 10 k $\Omega$  pull-up resistor. When  $\overline{\text{CS}}$  is high, the SDIO pin goes into a high impedance state.

### Implementation Specific Details

A detailed description of the unified SPI protocol can be found in the [Analog Devices Serial Control Interface Standard](#), which covers items such as timing, command format, and addressing.

The following product specific items are defined in the unified SPI protocol:

- Analog Devices unified SPI protocol revision: 1.0
- Chip type: 0x5
- Product ID: 0x009
- Physical layer: 3-wire supported and 1.5 V, 1.8 V, and 2.5 V operation supported
- Optional single-byte instruction mode: not supported
- Data link: not used
- Control: not used

### Communication Cycle—Instruction Plus Data

The unified SPI protocol consists of a two-part communication cycle. The first part is a 16-bit instruction word that is coincident with the first 16 SCLK rising edges and a payload. The instruction word provides the [AD9554-1](#) serial control port with information regarding the payload. The instruction word includes the R/W bit that indicates the direction of the payload transfer (that is, a read or write operation). The instruction word also indicates the starting register address of the first payload byte.

**Write**

If the instruction word indicates a write operation, the payload is written into the serial control port buffer of the AD9554-1. Data bits are registered on the rising edge of SCLK. Generally, it does not matter what data is written to blank registers; however, it is customary to use 0s. Note that the user must verify that all reserved registers within a specific range have a default value of 0x00; however, Analog Devices makes every effort to avoid having reserved registers with non-zero default values.

Most of the serial port registers are buffered (see the Buffered/Active Registers section for details on the difference between buffered and active registers). Therefore, data written into buffered registers does not take effect immediately. An additional operation is needed to transfer buffered serial control port contents to the registers that actually control the device. This transfer is accomplished with an IO\_UPDATE operation, which is performed in one of two ways. One method is to write a Logic 1 to Register 0x000F, Bit 0 (this bit is an autoclearing bit). The other method is to use an external signal via an appropriately programmed multifunction pin. The user can change as many register bits as desired before executing an IO\_UPDATE. The IO\_UPDATE operation transfers the buffer register contents to their active register counterparts.

**Read**

If the instruction word indicates a read operation, the next N × 8 SCLK cycles clock out the data starting from the address specified in the instruction word. N is the number of data bytes read. The readback data is driven to the pin on the falling edge and must be latched on the rising edge of SCLK. Blank registers are not skipped over during readback.

A readback operation takes data from either the serial control port buffer registers or the active registers, as determined by Register 0x0001, Bit 5.

**Table 25. Serial Control Port, 16-Bit Instruction Word**

| MSB |     |     |     |     |     |    |    |    |    |    |    |    |    | LSB |    |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|-----|----|
| I15 | I14 | I13 | I12 | I11 | I10 | I9 | I8 | I7 | I6 | I5 | I4 | I3 | I2 | I1  | I0 |
| R/W | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1  | A0 |

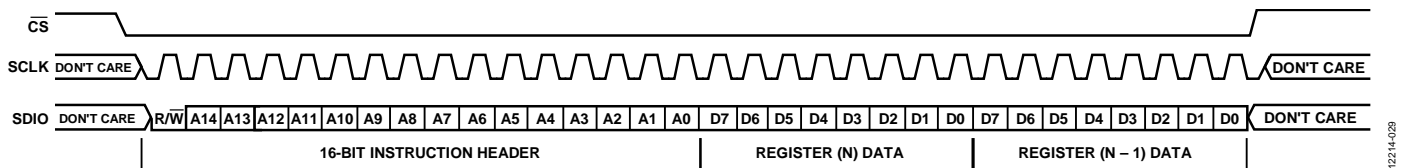


Figure 32. Serial Control Port Write—MSB First, Address Decrement, Two Bytes of Data

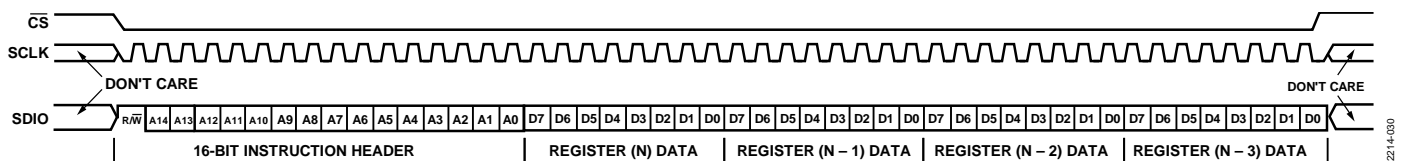


Figure 33. Serial Control Port Read—MSB First, Address Decrement, Four Bytes of Data

**SPI Instruction Word (16 Bits)**

The MSB of the 16-bit instruction word is R/W, which indicates whether the instruction is a read or a write. The next 15 bits are the register address (A14 to A0), which indicates the starting register address of the read/write operation (see Table 25). Note that A14 and A13 are ignored and treated as zeros in the AD9554-1 because there are no registers that require more than 13 address bits.

**SPI MSB-/LSB-First Transfers**

The AD9554-1 instruction word and payload can be MSB first or LSB first. The default for the AD9554-1 is MSB first. The LSB first mode can be set by writing a 1 to Register 0x0000, Bit 6. Immediately after the LSB first bit is set, subsequent serial control port operations are LSB first.

**Address Ascension**

If the address ascension bit (Register 0x0000, Bit 5) is zero, the serial control port register address decrements from the specified starting address toward Address 0x0000.

If the address ascension bit (Register 0x0000, Bit 5) is one, the serial control port register address increments from the starting address toward Address 0x0FFF. Reserved addresses are not skipped during multibyte input/output operations; therefore, write the default value to a reserved register and 0s to unmapped registers. Note that it is more efficient to issue a new write command than to write the default value to more than two consecutive reserved (or unmapped) registers.

**Table 24. Streaming Mode (No Addresses Skipped)**

| Address Ascension | Stop Sequence     |
|-------------------|-------------------|
| Increment         | 0x0000 ... 0x0FFF |
| Decrement         | 0x0FFF ... 0x0000 |

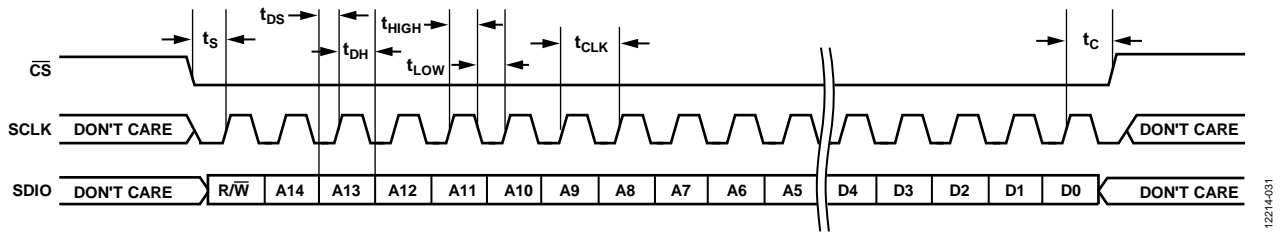


Figure 34. Timing Diagram for Serial Control Port Write—MSB First

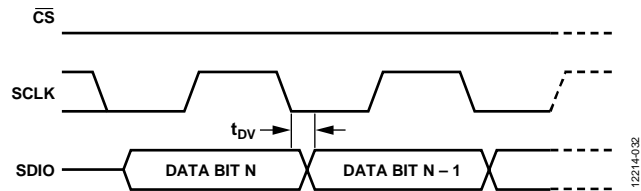


Figure 35. Timing Diagram for Serial Control Port Register Read—MSB First

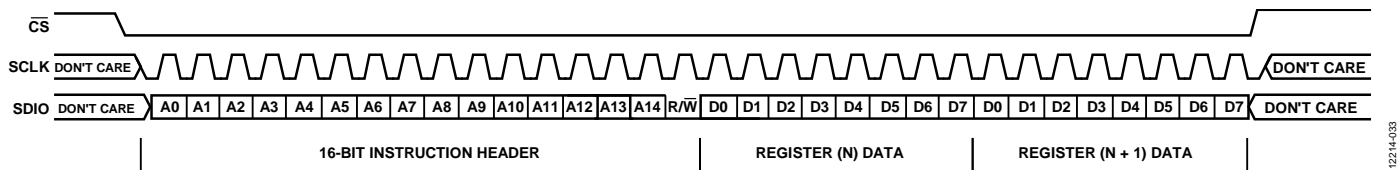


Figure 36. Serial Control Port Write—LSB First, Address Increment, Two Bytes of Data

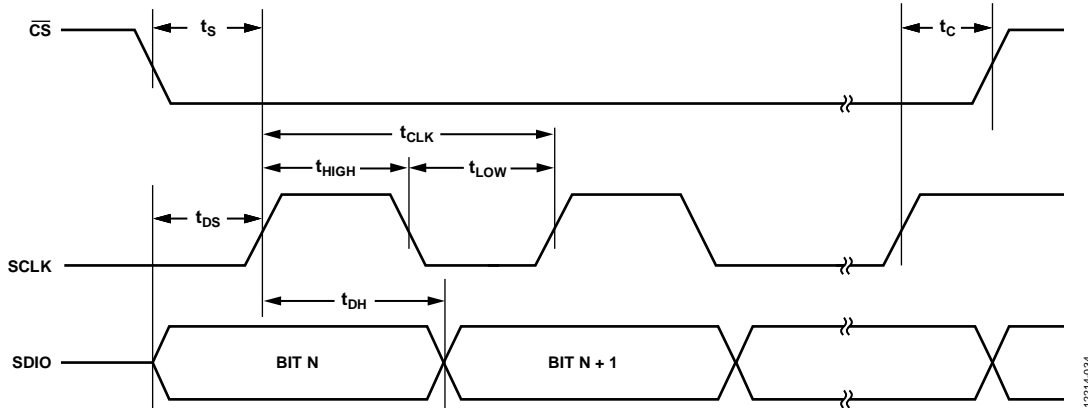


Figure 37. Serial Control Port Timing—Write

Table 26. Serial Control Port Timing

| Parameter  | Description                                                                                                     |
|------------|-----------------------------------------------------------------------------------------------------------------|
| $t_{DS}$   | Setup time between data and the rising edge of SCLK                                                             |
| $t_{DH}$   | Hold time between data and the rising edge of SCLK                                                              |
| $t_{CLK}$  | Period of the clock                                                                                             |
| $t_s$      | Setup time between the $\overline{CS}$ falling edge and the SCLK rising edge (start of the communication cycle) |
| $t_c$      | Setup time between the SCLK rising edge and $\overline{CS}$ rising edge (end of the communication cycle)        |
| $t_{HIGH}$ | Minimum period that SCLK should be in a logic high state                                                        |
| $t_{LOW}$  | Minimum period that SCLK should be in a logic low state                                                         |
| $t_{DV}$   | SCLK to valid SDIO (see Figure 35)                                                                              |

## I<sup>2</sup>C SERIAL PORT OPERATION

The I<sup>2</sup>C interface is popular because it requires only two pins and easily supports multiple devices on the same bus. Its main disadvantage is programming speed, which is 400 kbps maximum. The AD9554-1 I<sup>2</sup>C port design uses the I<sup>2</sup>C fast mode; however, it supports both the 100 kHz standard mode and 400 kHz fast mode.

In an effort to support 1.5 V, 1.8 V, and 2.5 V I<sup>2</sup>C operation, the AD9554-1 does not strictly adhere to every requirement in the original I<sup>2</sup>C specification. In particular, specifications such as slew rate limiting and glitch filtering are not implemented. Therefore, the AD9554-1 is I<sup>2</sup>C compatible, but may not be fully I<sup>2</sup>C compliant.

The AD9554-1 I<sup>2</sup>C port consists of a serial data line (SDA) and a serial clock line (SCL). In an I<sup>2</sup>C bus system, the AD9554-1 is connected to the serial bus (data bus SDA and clock bus SCL) as a slave device; that is, no clock is generated by the AD9554-1. The AD9554-1 uses direct 16-bit memory addressing instead of more common 8-bit memory addressing.

The AD9554-1 allows up to seven unique slave devices to occupy the I<sup>2</sup>C bus. These are accessed via a 7-bit slave address transmitted as part of an I<sup>2</sup>C packet. Only the device with a matching slave address responds to subsequent I<sup>2</sup>C commands. Table 22 lists the supported device slave addresses.

### I<sup>2</sup>C Bus Characteristics

A summary of the various I<sup>2</sup>C abbreviations appears in Table 27.

**Table 27. I<sup>2</sup>C Bus Abbreviation Definitions**

| Abbreviation | Definition     |
|--------------|----------------|
| S            | Start          |
| Sr           | Repeated start |
| P            | Stop           |
| A            | Acknowledge    |
| $\bar{A}$    | Nonacknowledge |
| $\bar{W}$    | Write          |
| R            | Read           |

The transfer of data is shown in Figure 38. One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can change only when the clock signal on the SCL line is low.

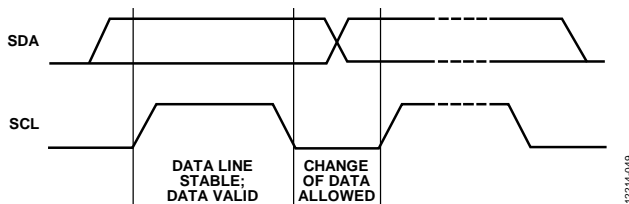


Figure 38. Valid Bit Transfer

Start/stop functionality is shown in Figure 39. The start condition is characterized by a high to low transition on the SDA line while SCL is high. The master always generates the start condition to initialize a data transfer. The stop condition is characterized by a low to high transition on the SDA line while SCL is high. The master always generates the stop condition to terminate a data transfer. Every byte on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit; bytes are sent MSB first.

The acknowledge bit (A) is the ninth bit attached to any 8-bit data byte. An acknowledge bit is always generated by the receiving device (receiver) to inform the transmitter that the byte has been received. It is done by pulling the SDA line low during the ninth clock pulse after each 8-bit data byte.

The nonacknowledge bit ( $\bar{A}$ ) is the ninth bit attached to any 8-bit data byte. A nonacknowledge bit is always generated by the receiving device (receiver) to inform the transmitter that the byte has not been received. It is done by leaving the SDA line high during the ninth clock pulse after each 8-bit data byte. After issuing a nonacknowledge bit, the AD9554-1 I<sup>2</sup>C state machine goes into an idle state.

### Data Transfer Process

The master initiates data transfer by asserting a start condition, which indicates that a data stream follows. All I<sup>2</sup>C slave devices connected to the serial bus respond to the start condition.

The master then sends an 8-bit address byte over the SDA line, consisting of a 7-bit slave address (MSB first) plus an R/ $\bar{W}$  bit. This bit determines the direction of the data transfer, that is, whether data is written to or read from the slave device (0 = write and 1 = read).

The peripheral whose address corresponds to the transmitted address responds by sending an acknowledge bit. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/ $\bar{W}$  bit is 0, the master (transmitter) writes to the slave device (receiver). If the R/ $\bar{W}$  bit is 1, the master (receiver) reads from the slave device (transmitter).

The format for these commands is described in the Data Transfer Format section.

Data is then sent over the serial bus in the format of nine clock pulses, one data byte (eight bits) from either master (write mode) or slave (read mode) followed by an acknowledge bit from the receiving device. The number of bytes that can be transmitted per transfer is unrestricted. In write mode, the first two data bytes immediately after the slave address byte are the internal memory (control registers) address bytes, with the high address byte first. This addressing scheme gives a memory address of up to  $2^{16} - 1 = 65,535$ . The data bytes after these two memory address bytes are register data written to or read from the control registers. In read mode, the data bytes after the slave address byte are register data written to or read from the control registers.

When all the data bytes are read or written, stop conditions are established. In write mode, the master (transmitter) asserts a stop condition to end data transfer during the clock pulse following the acknowledge bit for the last data byte from the slave device (receiver). In read mode, the master device (receiver) receives the last data byte from the slave device (transmitter) but does not pull SDA low during the ninth clock pulse. This is known as a nonacknowledge bit. By receiving the

nonacknowledge bit, the slave device knows that the data transfer is finished and enters idle mode. The master then takes the data line low during the low period before the 10<sup>th</sup> clock pulse, and high during the 10<sup>th</sup> clock pulse to assert a stop condition.

A start condition can be used in place of a stop condition. Furthermore, a start or stop condition can occur at any time, and partially transferred bytes are discarded.

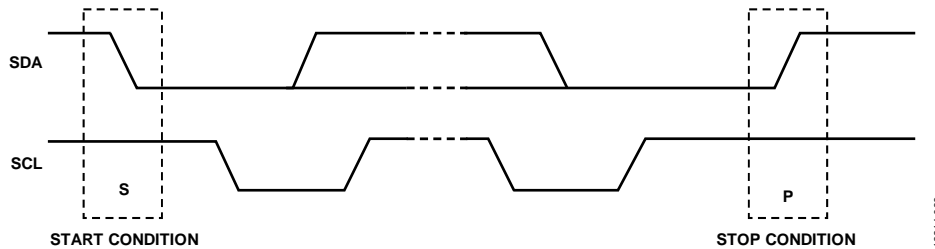


Figure 39. Start and Stop Conditions

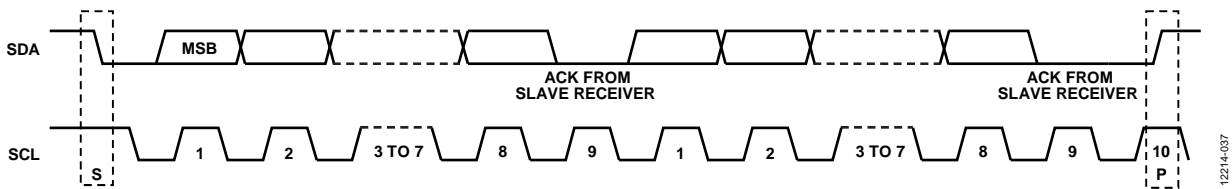


Figure 40. Acknowledge Bit

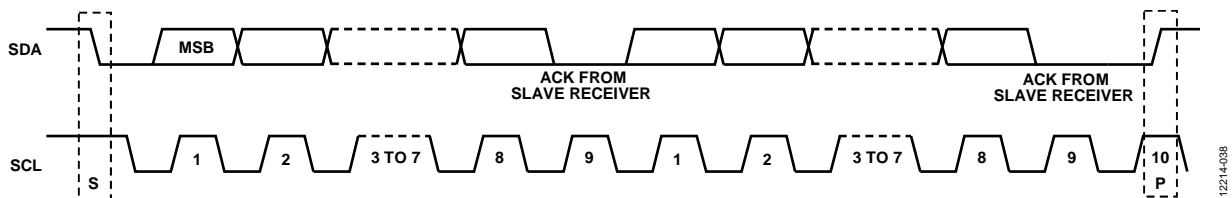


Figure 41. Data Transfer Process (Master Write Mode, 2-Byte Transfer)

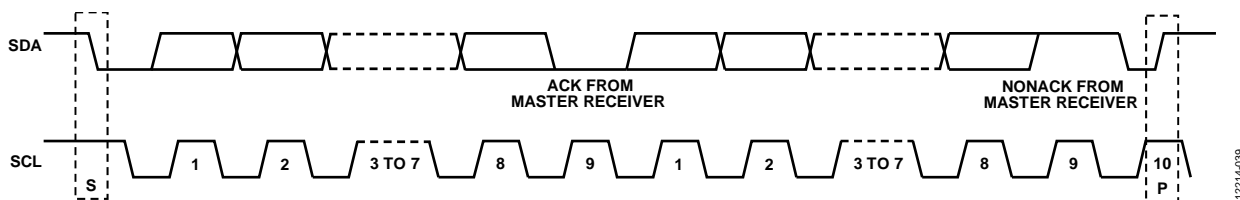


Figure 42. Data Transfer Process (Master Read Mode, 2-Byte Transfer), First Acknowledge From Slave

**Data Transfer Format**

The write byte format is used to write a register address to the RAM starting from the specified RAM address.

|   |               |                |   |                       |   |                      |   |            |   |            |   |            |   |   |
|---|---------------|----------------|---|-----------------------|---|----------------------|---|------------|---|------------|---|------------|---|---|
| S | Slave address | $\overline{W}$ | A | RAM address high byte | A | RAM address low byte | A | RAM Data 0 | A | RAM Data 1 | A | RAM Data 2 | A | P |
|---|---------------|----------------|---|-----------------------|---|----------------------|---|------------|---|------------|---|------------|---|---|

The send byte format is used to set up the register address for subsequent reads.

|   |               |                |   |                       |   |                      |   |   |
|---|---------------|----------------|---|-----------------------|---|----------------------|---|---|
| S | Slave address | $\overline{W}$ | A | RAM address high byte | A | RAM address low byte | A | P |
|---|---------------|----------------|---|-----------------------|---|----------------------|---|---|

The receive byte format is used to read the data byte(s) from RAM starting from the current address.

|   |               |   |   |            |   |            |   |            |                |   |
|---|---------------|---|---|------------|---|------------|---|------------|----------------|---|
| S | Slave address | R | A | RAM Data 0 | A | RAM Data 1 | A | RAM Data 2 | $\overline{A}$ | P |
|---|---------------|---|---|------------|---|------------|---|------------|----------------|---|

The read byte format is the combined format of the send byte and the receive byte.

|   |               |                |   |                       |   |                      |   |    |               |   |   |            |   |            |   |            |                |   |
|---|---------------|----------------|---|-----------------------|---|----------------------|---|----|---------------|---|---|------------|---|------------|---|------------|----------------|---|
| S | Slave address | $\overline{W}$ | A | RAM address high byte | A | RAM address low byte | A | Sr | Slave address | R | A | RAM Data 0 | A | RAM Data 1 | A | RAM Data 2 | $\overline{A}$ | P |
|---|---------------|----------------|---|-----------------------|---|----------------------|---|----|---------------|---|---|------------|---|------------|---|------------|----------------|---|

**I<sup>2</sup>C Serial Port Timing**

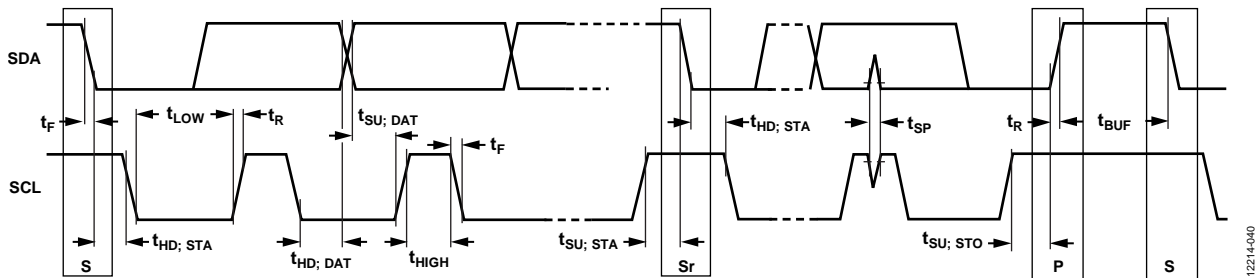


Figure 43. I<sup>2</sup>C Serial Port Timing

**Table 28. I<sup>2</sup>C Timing Definitions**

| Parameter            | Description                                                               |
|----------------------|---------------------------------------------------------------------------|
| f <sub>SCL</sub>     | Serial clock                                                              |
| t <sub>BUF</sub>     | Bus free time between stop and start conditions                           |
| t <sub>HD; STA</sub> | Repeated hold time start condition                                        |
| t <sub>SU; STA</sub> | Repeated start condition setup time                                       |
| t <sub>SU; STO</sub> | Stop condition setup time                                                 |
| t <sub>HD; DAT</sub> | Data hold time                                                            |
| t <sub>SU; DAT</sub> | Data setup time                                                           |
| t <sub>LOW</sub>     | SCL clock low period                                                      |
| t <sub>HIGH</sub>    | SCL clock high period                                                     |
| t <sub>R</sub>       | Minimum/maximum receive SCL and SDA rise time                             |
| t <sub>F</sub>       | Minimum/maximum receive SCL and SDA fall time                             |
| t <sub>SP</sub>      | Pulse width of voltage spikes that must be suppressed by the input filter |

## PROGRAMMING THE I/O REGISTERS

The register map (see Table 31) spans an address range from 0x0000 through 0x1788. Each address provides access to one byte (eight bits) of data. Each individual register is identified by its four digit hexadecimal address (for example, Register 0x0A23). In some cases, a group of addresses collectively defines a register.

In general, when a group of registers defines a control parameter, the LSB of the value resides in the D0 position of the register with the lowest address. The bit weight increases right to left, from the lowest register address to the highest register address.

### BUFFERED/ACTIVE REGISTERS

There are two copies of most registers: buffered and active. The value in the active registers is the one that is in use. The buffered registers are the ones that take effect the next time the user writes 0x01 to Register 0x000F (IO\_UPDATE). Buffering the registers allows the user to update a group of registers (like the APLL settings) simultaneously, avoiding the potential of unpredictable behavior in the device. Registers with an L in the option column of the register map (see Table 31) are live, meaning that they take effect the moment the serial port transfers that data byte.

### WRITE DETECT REGISTERS

A Wx (where x equals 1 to 8) in the option column of the register map (see Table 31) identifies a register with write detection. These registers contain additional logic to avoid glitches or unwanted operation.

**Table 29. Register Write Detection Description**

| Option | Register Operation                                                                                                                                                                                                                                                                     |
|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| W1     | When these registers are written to, the lock detector immediately declares it is unlocked. The lock detection restarts when the next IO_UPDATE occurs.                                                                                                                                |
| W2     | After these registers are written to, the DPLL faults the reference input and automatically enters holdover for one PFD cycle (and then exits) when an IO_UPDATE is issued. However, this action is only performed if the written register belongs to the actively selected reference. |
| W3     | After these registers are written to, the DPLL lock detector unlocks.                                                                                                                                                                                                                  |
| W5     | The watchdog timer resets automatically when these registers are written to and then resumes counting on the next IO_UPDATE.                                                                                                                                                           |
| W6     | The system clock stability timer is automatically reset when these registers are changed and then resumes counting on the next IO_UPDATE. (Note that the SYSCLK stability timer starts only after the system clock is locked.                                                          |
| W7     | If these registers are written to while they are assigned to an existing function, the existing function stops immediately. The new function starts when the next IO_UPDATE occurs.                                                                                                    |
| W8     | Almost identical to W2; however, the DPLL must be in demapping mode.                                                                                                                                                                                                                   |

### AUTOCLEAR REGISTERS

An A in the option column of the register map (see Table 31) identifies an autoclearing register. Typically, the active value for an autoclearing register takes effect following an IO\_UPDATE. The bit is cleared by the internal device logic upon completion of the prescribed action.

### REGISTER ACCESS RESTRICTIONS

Read and write access to the register map may be restricted, depending on the register in question, the source and direction of access, and the current state of the device. Each register can be classified into one or more access types. When more than one type applies, the most restrictive condition is the one that applies.

When access is denied to a register, all attempts to read the register return a 0 byte, and all attempts to write to the register are ignored. Access to nonexistent registers is handled in the same way as for a denied register.

#### *Regular Access*

Registers with regular access do not fall into any other category.

#### *Read Only Access*

An R in the option column of the register map (see Table 31) identifies read only registers. Serial port access is available at all times.

## THERMAL PERFORMANCE

Table 30. Thermal Parameters for the 56-Lead LFCSP Package

| Symbol         | Thermal Characteristic Using a JEDEC 51-7 Plus JEDEC 51-5 2S2P Test Board <sup>1</sup>                   | Value <sup>2</sup> | Unit |
|----------------|----------------------------------------------------------------------------------------------------------|--------------------|------|
| $\theta_{JA}$  | Junction-to-ambient thermal resistance, 0.0 m/sec airflow per JEDEC JESD51-2 (still air)                 | 25.3               | °C/W |
| $\theta_{JMA}$ | Junction-to-ambient thermal resistance, 1.0 m/sec airflow per JEDEC JESD51-6 (moving air)                | 21.8               | °C/W |
| $\theta_{JMA}$ | Junction-to-ambient thermal resistance, 2.5 m/sec airflow per JEDEC JESD51-6 (moving air)                | 20.4               | °C/W |
| $\theta_{JB}$  | Junction-to-board thermal resistance, 0.0 m/sec airflow per JEDEC JESD51-8 (still air)                   | 10.9               | °C/W |
| $\theta_{JC}$  | Junction-to-case thermal resistance (die-to-heat sink) per MIL-Standard 883, Method 1012.1               | 2.64               | °C/W |
| $\Psi_{JT}$    | Junction-to-top-of-package characterization parameter, 0 m/sec airflow per JEDEC JESD51-2 (still air)    | 0.16               | °C/W |
| $\Psi_{JT}$    | Junction-to-top-of-package characterization parameter, 1.0 m/sec airflow per JEDEC JESD51-6 (moving air) | 0.29               | °C/W |
| $\Psi_{JT}$    | Junction-to-top-of-package characterization parameter, 2.5 m/sec airflow per JEDEC JESD51-6 (moving air) | 0.37               | °C/W |

<sup>1</sup> The exposed pad on the bottom of the package must be soldered to analog ground of the PCB to achieve the specified thermal performance.

<sup>2</sup> Results are from simulations. The PCB is a JEDEC multilayer type. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine if they are similar to those assumed in these calculations.

The AD9554-1 is specified for a case temperature ( $T_{CASE}$ ). To ensure that  $T_{CASE}$  is not exceeded, an airflow source can be used. Use the following equation to determine the junction temperature on the application PCB:

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

where:

$T_J$  is the junction temperature (°C).

$T_{CASE}$  is the case temperature (°C) measured by the customer at the top center of the package.

$\Psi_{JT}$  is the value as indicated in Table 30.

$PD$  is the power dissipation (see Table 3).

Values of  $\theta_{JA}$  are provided for package comparison and PCB design considerations.  $\theta_{JA}$  can be used for a first-order approximation of  $T_J$  by the equation

$$T_J = T_A + (\theta_{JA} \times PD)$$

where  $T_A$  is the ambient temperature (°C).

Values of  $\theta_{JC}$  are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of  $\theta_{JB}$  are provided for package comparison and PCB design considerations.



## POWER SUPPLY PARTITIONS

The AD9554-1 power supplies are in two groups: VDD and VDD\_SP. All power and ground pins must be connected, even if certain blocks of the chip are powered down.

### VDD SUPPLIES

All of the VDD supplies can be connected to one common source that is either 1.5 V or 1.8 V.

Place the 0.1  $\mu$ F bypass capacitors as close as possible to each power supply pin.

In addition to these bypass capacitors, the AD9554-1 evaluation board uses four ferrite beads between the 1.8 V (or 1.5 V) source and Pin 15, Pin 28, Pin 43, and Pin 56.

Although these ferrite beads may not be needed for every application, the use of these ferrite beads is strongly recommended. At a minimum, include a place for the ferrite beads (as close to the bypass capacitors as possible) and populate the board with 0402, 0  $\Omega$  resistors. By doing so, there is a place for the ferrite beads, if needed.

The ferrite beads are required if the AD9554-1 is powered directly from a switching power supply.

Ferrite beads with low ( $<0.7 \Omega$ ) dc resistance and approximately 30  $\Omega$  impedance at 100 MHz are suitable for this application. For example, the Murata BLM15AX300SN1D is suitable.

### VDD\_SP SUPPLY

Pin 23 (VDD\_SP) is the serial port power supply pin and can be connected to a 2.5 V, 1.8 V, or 1.5 V power supply.

If the user needs to operate the serial port at the same voltage as the device itself, VDD\_SP can be joined to VDD.

## REGISTER MAP

Register addresses that are not listed in Table 31 are not used, and writing to those registers has no effect. Write the default value to sections of registers marked reserved. In the option column, R = read only; A = autoclear; W1, W2, W3, W5, W6, W7, and W8 = write detection (see Table 29 for more information); and L = live (IO\_UPDATE not required for register to take effect or for a read only register to be updated). N/A = not applicable.

Table 31.

| Reg. Addr. (Hex)                            | Option | Name            | D7                               | D6                     | D5                           | D4                      | D3                        | D2                           | D1                        | D0         | Def (Hex) |           |      |
|---------------------------------------------|--------|-----------------|----------------------------------|------------------------|------------------------------|-------------------------|---------------------------|------------------------------|---------------------------|------------|-----------|-----------|------|
| Serial Control Port and Part Identification |        |                 |                                  |                        |                              |                         |                           |                              |                           |            |           |           |      |
| 0x0000                                      | L      | SPI Config A    | Soft reset                       | LSB first (SPI only)   | Address ascension (SPI only) | Reserved                |                           | Address ascension (SPI only) | LSB first (SPI only)      | Soft reset | 0x00      |           |      |
| 0x0001                                      | L      | SPI Config B    | Reserved                         |                        | Read buffer register         | Reserved                |                           | Reset sans regmap            | Reserved                  |            | 0x00      |           |      |
| 0x0002                                      |        | Reserved        | Reserved                         |                        |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x0003                                      | R      | Chip type       | Reserved                         |                        |                              |                         | Chip type, Bits[3:0]      |                              |                           |            | 0x05      |           |      |
| 0x0004                                      | R      | Product ID      | Clock part serial ID, Bits[3:0]  |                        |                              |                         | Reserved                  |                              |                           |            | 0x9F      |           |      |
| 0x0005                                      | R      |                 | Clock part serial ID, Bits[11:4] |                        |                              |                         |                           |                              |                           |            | 0x00      |           |      |
| 0x0006                                      | R      | Revision        | Part version, Bits[7:0]          |                        |                              |                         |                           |                              |                           |            |           | 0x05      |      |
| 0x0007                                      |        | Reserved        | Reserved                         |                        |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x0008                                      |        | Reserved        | Reserved                         |                        |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x0009                                      |        | Reserved        | Reserved                         |                        |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x000A                                      |        | Reserved        | Reserved                         |                        |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x000B                                      | R      | SPI version     | SPI version, Bits[7:0]           |                        |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x000C                                      | R      | Vendor ID       | Vendor ID, Bits[7:0]             |                        |                              |                         |                           |                              |                           |            |           | 0x56      |      |
| 0x000D                                      | R      |                 | Vendor ID, Bits[15:8]            |                        |                              |                         |                           |                              |                           |            |           | 0x04      |      |
| 0x000E                                      |        | Reserved        | Reserved                         |                        |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x000F                                      | L, A   | IO_UPDATE       | Reserved                         |                        |                              |                         |                           |                              |                           |            |           | IO_UPDATE | 0x00 |
| General Configuration                       |        |                 |                                  |                        |                              |                         |                           |                              |                           |            |           |           |      |
| 0x0100                                      |        | Mx pin drivers  | M3 driver mode, Bits[1:0]        |                        | M2 driver mode, Bits[1:0]    |                         | M1 driver mode, Bits[1:0] |                              | M0 driver mode, Bits[1:0] |            | 0x00      |           |      |
| 0x0101                                      |        |                 | M7 driver mode, Bits[1:0]        |                        | M6 driver mode, Bits[1:0]    |                         | M5 driver mode, Bits[1:0] |                              | Reserved                  |            | 0x00      |           |      |
| 0x0102                                      |        |                 | Reserved                         |                        |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x0103                                      | W7     | M0FUNC          | M0 output/input                  | M0 function, Bits[6:0] |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x0104                                      | W7     | M1FUNC          | M1 output/input                  | M1 function, Bits[6:0] |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x0105                                      | W7     | M2FUNC          | M2 output/input                  | M2 function, Bits[6:0] |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x0106                                      | W7     | M3FUNC          | M3 output/input                  | M3 function, Bits[6:0] |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x0107                                      | W7     | Reserved        | Reserved                         |                        |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x0108                                      | W7     | M5FUNC          | M5 output/input                  | M5 function, Bits[6:0] |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x0109                                      | W7     | M6FUNC          | M6 output/input                  | M6 function, Bits[6:0] |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x010A                                      | W7     | M7FUNC          | M7 output/input                  | M7 function, Bits[6:0] |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x010B                                      | W7     | Reserved        | Reserved                         |                        |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x010C                                      | W7     | Reserved        | Reserved                         |                        |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x010D                                      | W5     | Watchdog timer  | Watchdog timer (ms), Bits[7:0]   |                        |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x010E                                      | W5     |                 | Watchdog timer (ms), Bits[15:8]  |                        |                              |                         |                           |                              |                           |            |           | 0x00      |      |
| 0x010F                                      |        | IRQ mask common | SYCLK unlocked                   | SYCLK stable           | SYCLK locked                 | SYCLK calibration ended | SYCLK calibration started | Watchdog timer               | Reserved                  |            |           | 0x00      |      |
| 0x0110                                      |        |                 | Reserved                         | REFB validated         | REFB fault cleared           | REFB fault              | Reserved                  | REFA validated               | REFA fault cleared        | REFA fault | 0x00      |           |      |
| 0x0111                                      |        |                 | Reserved                         | REFD validated         | REFD fault cleared           | REFD fault              | Reserved                  | REFC validated               | REFC fault cleared        | REFC fault | 0x00      |           |      |

| Reg. Addr. (Hex)  | Option | Name                                          | D7                                                                                                                        | D6                         | D5                       | D4                      | D3                                                 | D2               | D1                           | D0                 | Def (Hex)                          |      |
|-------------------|--------|-----------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|----------------------------|--------------------------|-------------------------|----------------------------------------------------|------------------|------------------------------|--------------------|------------------------------------|------|
| 0x0112            |        | IRQ mask DPLL_0                               | Frequency unclamped                                                                                                       | Frequency clamped          | Phase slew unlimited     | Phase slew limited      | Frequency unlocked                                 | Frequency locked | Phase unlocked               | Phase locked       | 0x00                               |      |
| 0x0113            |        |                                               | Switching                                                                                                                 | Free run                   | Holdover                 | History updated         | REFD activated                                     | REFC activated   | REFB activated               | REFA activated     | 0x00                               |      |
| 0x0114            |        |                                               | Phase step detected                                                                                                       | Demap controller unclamped | Demap controller clamped | Sync clock distribution | APLL_0 unlocked                                    | APLL_0 locked    | APLL_0 cal complete          | APLL_0 cal started | 0x00                               |      |
| 0x0115            |        | IRQ mask DPLL_1                               | Frequency unclamped                                                                                                       | Frequency clamped          | Phase slew unlimited     | Phase slew limited      | Frequency unlocked                                 | Frequency locked | Phase unlocked               | Phase locked       | 0x00                               |      |
| 0x0116            |        |                                               | Switching                                                                                                                 | Free run                   | Holdover                 | History updated         | REFD activated                                     | REFC activated   | REFB activated               | REFA activated     | 0x00                               |      |
| 0x0117            |        |                                               | Phase step detected                                                                                                       | Demap controller unclamped | Demap controller clamped | Sync clock distribution | APLL_1 unlocked                                    | APLL_1 locked    | APLL_1 cal complete          | APLL_1 cal started | 0x00                               |      |
| 0x0118            |        | IRQ mask DPLL_2                               | Frequency unclamped                                                                                                       | Frequency clamped          | Phase slew unlimited     | Phase slew limited      | Frequency unlocked                                 | Frequency locked | Phase unlocked               | Phase locked       | 0x00                               |      |
| 0x0119            |        |                                               | Switching                                                                                                                 | Free run                   | Holdover                 | History updated         | REFD activated                                     | REFC activated   | REFB activated               | REFA activated     | 0x00                               |      |
| 0x011A            |        |                                               | Phase step detected                                                                                                       | Demap controller unclamped | Demap controller clamped | Sync clock distribution | APLL_2 unlocked                                    | APLL_2 locked    | APLL_2 cal complete          | APLL_2 cal started | 0x00                               |      |
| 0x011B            |        | IRQ mask DPLL_3                               | Frequency unclamped                                                                                                       | Frequency clamped          | Phase slew unlimited     | Phase slew limited      | Frequency unlocked                                 | Frequency locked | Phase unlocked               | Phase locked       | 0x00                               |      |
| 0x011C            |        |                                               | Switching                                                                                                                 | Free run                   | Holdover                 | History updated         | REFD activated                                     | REFC activated   | REFB activated               | REFA activated     | 0x00                               |      |
| 0x011D            |        |                                               | Phase step detected                                                                                                       | Demap controller unclamped | Demap controller clamped | Sync clock distribution | APLL_3 unlocked                                    | APLL_3 locked    | APLL_3 cal complete          | APLL_3 cal started | 0x00                               |      |
| 0x011E            | L      | Pad control                                   | M7 config                                                                                                                 | M6 config                  | M5 config                | Reserved                | M3 config                                          | M2 config        | M1 config                    | M0 config          | 0x00                               |      |
| 0x011F            | L      |                                               | Reserved                                                                                                                  |                            |                          |                         | SPI config                                         |                  | Reserved                     |                    | 0x00                               |      |
| System Clock      |        |                                               |                                                                                                                           |                            |                          |                         |                                                    |                  |                              |                    |                                    |      |
| 0x0200            |        | SYSCLK PLL feedback divider and configuration | System clock K divider, Bits[7:0]                                                                                         |                            |                          |                         |                                                    |                  |                              |                    |                                    | 0x00 |
| 0x0201            |        |                                               | Reserved                                                                                                                  |                            |                          |                         | SYSCLK XTAL enable                                 |                  | SYSCLK J1 divider, Bits[1:0] |                    | SYSCLK doubler enable (J0 divider) | 0x08 |
| 0x0202            | W6     | SYSCLK reference frequency                    | System clock reference frequency (Hz), Bits[7:0]                                                                          |                            |                          |                         |                                                    |                  |                              |                    | 0x00                               |      |
| 0x0203            | W6     |                                               | System clock reference frequency (Hz), Bits[15:8]                                                                         |                            |                          |                         |                                                    |                  |                              |                    | 0x00                               |      |
| 0x0204            | W6     |                                               | System clock reference frequency (Hz), Bits[23:16]                                                                        |                            |                          |                         |                                                    |                  |                              |                    | 0x00                               |      |
| 0x0205            | W6     |                                               | Reserved                                                                                                                  |                            |                          |                         | System clock reference frequency (Hz), Bits[27:24] |                  |                              |                    | 0x00                               |      |
| 0x0206            | W6     | SYSCLK stability                              | System clock stability period (ms), Bits[7:0]                                                                             |                            |                          |                         |                                                    |                  |                              |                    | 0x32                               |      |
| 0x0207            | W6     |                                               | System clock stability period (ms), Bits[15:8]                                                                            |                            |                          |                         |                                                    |                  |                              |                    | 0x00                               |      |
| 0x0208            | W6     |                                               | Reserved                                                                                                                  |                            |                          |                         | System clock stability period (ms), Bits[19:16]    |                  |                              |                    | 0x00                               |      |
| Reference Input A |        |                                               |                                                                                                                           |                            |                          |                         |                                                    |                  |                              |                    |                                    |      |
| 0x0300            | W1, L  | REFA logic type                               | Reserved                                                                                                                  |                            |                          |                         |                                                    |                  | REFA logic type, Bits[1:0]   |                    | 0x00                               |      |
| 0x0301            | W1, L  | REFA R divider (20 bits)                      | R divider, Bits[7:0]                                                                                                      |                            |                          |                         |                                                    |                  |                              |                    | 0x00                               |      |
| 0x0302            | W1, L  |                                               | R divider, Bits[15:8]                                                                                                     |                            |                          |                         |                                                    |                  |                              |                    | 0x00                               |      |
| 0x0303            | W1, L  |                                               | Reserved                                                                                                                  |                            |                          |                         | R divider, Bits[19:16]                             |                  |                              |                    | 0x00                               |      |
| 0x0304            | W2, L  | REFA period                                   | Nominal reference period (fs), Bits[7:0]                                                                                  |                            |                          |                         |                                                    |                  |                              |                    | 0x00                               |      |
| 0x0305            | W2, L  |                                               | Nominal reference period (fs), Bits[15:8]                                                                                 |                            |                          |                         |                                                    |                  |                              |                    | 0x00                               |      |
| 0x0306            | W2, L  |                                               | Nominal reference period (fs), Bits[23:16]                                                                                |                            |                          |                         |                                                    |                  |                              |                    | 0x00                               |      |
| 0x0307            | W2, L  |                                               | Nominal reference period (fs), Bits[31:24]                                                                                |                            |                          |                         |                                                    |                  |                              |                    | 0x00                               |      |
| 0x0308            | W2, L  |                                               | Nominal reference period (fs), Bits[39:32]                                                                                |                            |                          |                         |                                                    |                  |                              |                    | 0x00                               |      |
| 0x0309            | W2, L  | REFA frequency tolerance                      | Inner tolerance (1/(ppm error)), Bits[7:0] (for invalid to valid condition; maximum: 6.55%, minimum: 2 ppm) (default: 5%) |                            |                          |                         |                                                    |                  |                              |                    | 0x14                               |      |
| 0x030A            | W2, L  |                                               | Inner tolerance (1/(ppm error)), Bits[15:8] (for invalid to valid condition; maximum: 6.55%, minimum: 2 ppm)              |                            |                          |                         |                                                    |                  |                              |                    | 0x00                               |      |
| 0x030B            | W2, L  |                                               | Reserved                                                                                                                  |                            |                          |                         | Inner tolerance (1/(ppm error)), Bits[19:16]       |                  |                              |                    | 0x00                               |      |
| 0x030C            | W2, L  |                                               | Outer tolerance (1/(ppm error)), Bits[7:0] (for valid to invalid; maximum: 6.55%, minimum: 2 ppm) (default: 10%)          |                            |                          |                         |                                                    |                  |                              |                    | 0x0A                               |      |
| 0x030D            | W2, L  |                                               | Outer tolerance (1/(ppm error)), Bits[15:8] (for valid to invalid; max: 6.55%, min: 2 ppm)                                |                            |                          |                         |                                                    |                  |                              |                    | 0x00                               |      |
| 0x030E            | W2, L  |                                               | Reserved                                                                                                                  |                            |                          |                         | Outer tolerance (1/(ppm error)), Bits[19:16]       |                  |                              |                    | 0x00                               |      |
| 0x030F            | W2, L  | REFA validation timer                         | Validation timer (ms), Bits[7:0] (up to 65.5 sec)                                                                         |                            |                          |                         |                                                    |                  |                              |                    | 0x0A                               |      |
| 0x0310            | W2, L  |                                               | Validation timer (ms), Bits[15:8] (up to 65.5 sec)                                                                        |                            |                          |                         |                                                    |                  |                              |                    | 0x00                               |      |

| Reg. Addr. (Hex)        | Option | Name                                                                          | D7                                                                                                                                                               | D6 | D5 | D4 | D3                                                     | D2                 | D1                              | D0   | Def (Hex)               |      |
|-------------------------|--------|-------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|--------------------------------------------------------|--------------------|---------------------------------|------|-------------------------|------|
| 0x0311                  | W3, L  | REFA phase lock detector                                                      | Phase lock threshold (ps), Bits[7:0]                                                                                                                             |    |    |    |                                                        |                    |                                 |      | 0xBC                    |      |
| 0x0312                  | W3, L  |                                                                               | Phase lock threshold (ps), Bits[15:8]                                                                                                                            |    |    |    |                                                        |                    |                                 |      | 0x02                    |      |
| 0x0313                  | W3, L  |                                                                               | Phase lock threshold (ps), Bits [23:16]                                                                                                                          |    |    |    |                                                        |                    |                                 |      | 0x00                    |      |
| 0x0314                  | W3, L  |                                                                               | Phase lock fill rate, Bits[7:0]                                                                                                                                  |    |    |    |                                                        |                    |                                 |      | 0x0A                    |      |
| 0x0315                  | W3, L  |                                                                               | Phase lock drain rate, Bits[7:0]                                                                                                                                 |    |    |    |                                                        |                    |                                 |      | 0x0A                    |      |
| 0x0316                  | W3, L  | REFA frequency lock detector                                                  | Frequency lock threshold (ps), Bits[7:0]                                                                                                                         |    |    |    |                                                        |                    |                                 |      | 0xBC                    |      |
| 0x0317                  | W3, L  |                                                                               | Frequency lock threshold (ps), Bits[15:8]                                                                                                                        |    |    |    |                                                        |                    |                                 |      | 0x02                    |      |
| 0x0318                  | W3, L  |                                                                               | Frequency lock threshold (ps), Bits[23:16]                                                                                                                       |    |    |    |                                                        |                    |                                 |      | 0x00                    |      |
| 0x0319                  | W3, L  |                                                                               | Frequency lock fill rate, Bits[7:0]                                                                                                                              |    |    |    |                                                        |                    |                                 |      | 0x0A                    |      |
| 0x031A                  | W3, L  |                                                                               | Frequency lock drain rate, Bits[7:0]                                                                                                                             |    |    |    |                                                        |                    |                                 |      | 0x0A                    |      |
| 0x031B                  | W3, L  | REFA phase step threshold                                                     | Phase step threshold (ps), Bits[7:0]                                                                                                                             |    |    |    |                                                        |                    |                                 |      | 0x00                    |      |
| 0x031C                  | W3, L  |                                                                               | Phase step threshold (ps), Bits[15:8]                                                                                                                            |    |    |    |                                                        |                    |                                 |      | 0x00                    |      |
| 0x031D                  | W3, L  |                                                                               | Phase step threshold (ps), Bits[23:16]                                                                                                                           |    |    |    |                                                        |                    |                                 |      | 0x00                    |      |
| 0x031E                  | W3, L  |                                                                               | Reserved                                                                                                                                                         |    |    |    | Phase step threshold (ps), Bits[27:24]                 |                    |                                 |      | 0x00                    |      |
| Reference Input B       |        |                                                                               |                                                                                                                                                                  |    |    |    |                                                        |                    |                                 |      |                         |      |
| 0x0320 to 0x033E        |        |                                                                               | These registers mimic the Reference Input A registers (0x0300 through 0x031E) but the register addresses are offset by 0x0020. All default values are identical. |    |    |    |                                                        |                    |                                 |      |                         |      |
| Reference Input C       |        |                                                                               |                                                                                                                                                                  |    |    |    |                                                        |                    |                                 |      |                         |      |
| 0x0340 to 0x035E        |        |                                                                               | These registers mimic the Reference Input A registers (0x0300 through 0x031E) but register addresses are offset by 0x0040. All default values are identical.     |    |    |    |                                                        |                    |                                 |      |                         |      |
| Reference Input D       |        |                                                                               |                                                                                                                                                                  |    |    |    |                                                        |                    |                                 |      |                         |      |
| 0x0360 to 0x037E        |        |                                                                               | These registers mimic the Reference Input A registers (0x0300 through 0x031E) but the register addresses are offset by 0x0060. All default values are identical. |    |    |    |                                                        |                    |                                 |      |                         |      |
| DPLL_0 General Settings |        |                                                                               |                                                                                                                                                                  |    |    |    |                                                        |                    |                                 |      |                         |      |
| 0x0400                  |        | DPLL_0 free run frequency TW                                                  | 30-bit free running frequency tuning word, Bits[7:0]                                                                                                             |    |    |    |                                                        |                    |                                 |      | 0x00                    |      |
| 0x0401                  |        |                                                                               | 30-bit free running frequency tuning word, Bits[15:8]                                                                                                            |    |    |    |                                                        |                    |                                 |      | 0x00                    |      |
| 0x0402                  |        |                                                                               | 30-bit free running frequency tuning word, Bits[23:16]                                                                                                           |    |    |    |                                                        |                    |                                 |      | 0x00                    |      |
| 0x0403                  |        |                                                                               | Reserved                                                                                                                                                         |    |    |    | 30-bit free running frequency tuning word, Bits[29:24] |                    |                                 |      | 0x00                    |      |
| 0x0404                  |        | DPLL_0 DCO integer                                                            | Reserved                                                                                                                                                         |    |    |    | DCO integer, Bits[3:0]                                 |                    |                                 |      | 0x17                    |      |
| 0x0405                  |        | DPLL_0 frequency clamp                                                        | Lower limit of pull-in range, Bits[7:0]                                                                                                                          |    |    |    |                                                        |                    |                                 |      | 0xCC                    |      |
| 0x0406                  |        |                                                                               | Lower limit of pull-in range, Bits[15:8]                                                                                                                         |    |    |    |                                                        |                    |                                 |      | 0xCC                    |      |
| 0x0407                  |        |                                                                               | Reserved                                                                                                                                                         |    |    |    | Lower limit of pull-in range, Bits[19:16]              |                    |                                 |      | 0x00                    |      |
| 0x0408                  |        |                                                                               | Upper limit of pull-in range, Bits[7:0]                                                                                                                          |    |    |    |                                                        |                    |                                 |      | 0x33                    |      |
| 0x0409                  |        |                                                                               | Upper limit of pull-in range, Bits[15:8]                                                                                                                         |    |    |    |                                                        |                    |                                 |      | 0x33                    |      |
| 0x040A                  |        |                                                                               | Reserved                                                                                                                                                         |    |    |    | Upper limit of pull-in range, Bits[19:16]              |                    |                                 |      | 0x0F                    |      |
| 0x040B                  |        | DPLL_0 holdover history                                                       | History accumulation timer (ms), Bits[7:0] (up to 65 sec)                                                                                                        |    |    |    |                                                        |                    |                                 |      | 0x0A                    |      |
| 0x040C                  |        |                                                                               | History accumulation timer (ms), Bits[15:8] (up to 65 sec)                                                                                                       |    |    |    |                                                        |                    |                                 |      | 0x00                    |      |
| 0x040D                  |        | DPLL_0 history mode                                                           | Reserved                                                                                                                                                         |    |    |    | Single sample fallback                                 | Persistent history | Incremental average, Bits [2:0] |      | 0x00                    |      |
| 0x040E                  |        | DPLL_0 closed loop phase offset ( $\pm 0.5$ ms)                               | Fixed phase offset (signed; ps), Bits[7:0]                                                                                                                       |    |    |    |                                                        |                    |                                 |      | 0x00                    |      |
| 0x040F                  |        |                                                                               | Fixed phase offset (signed; ps), Bits[15:8]                                                                                                                      |    |    |    |                                                        |                    |                                 |      | 0x00                    |      |
| 0x0410                  |        |                                                                               | Fixed phase offset (signed; ps), Bits[23:16]                                                                                                                     |    |    |    |                                                        |                    |                                 |      | 0x00                    |      |
| 0x0411                  |        |                                                                               | Reserved                                                                                                                                                         |    |    |    | Fixed phase offset (signed; ps), Bits[29:24]           |                    |                                 |      | 0x00                    |      |
| 0x0412                  |        |                                                                               | Incremental phase offset step size (ps/step), Bits[7:0] (up to 65.5 ns/step)                                                                                     |    |    |    |                                                        |                    |                                 |      | 0x00                    |      |
| 0x0413                  |        | Incremental phase offset step size (ps/step), Bits[15:8] (up to 65.5 ns/step) |                                                                                                                                                                  |    |    |    |                                                        |                    |                                 | 0x00 |                         |      |
| 0x0414                  |        | DPLL_0 phase slew limit                                                       | Phase slew rate limit ( $\mu$ s/sec), Bits[7:0] (315 $\mu$ s/sec up to 65.536 ms/sec)                                                                            |    |    |    |                                                        |                    |                                 |      | 0x00                    |      |
| 0x0415                  |        |                                                                               | Phase slew rate limit ( $\mu$ s/sec), Bits[15:8] (315 $\mu$ s/sec up to 65.536 ms/sec)                                                                           |    |    |    |                                                        |                    |                                 |      | 0x00                    |      |
| 0x0416                  |        | Demap enable                                                                  | Reserved                                                                                                                                                         |    |    |    |                                                        |                    |                                 |      | Enable demap controller | 0x00 |

| Reg. Addr. (Hex)                                   | Option | Name                                                 | D7                                                                       | D6                                                  | D5 | D4 | D3                                 | D2                       | D1                                                          | D0                                           | Def (Hex) |
|----------------------------------------------------|--------|------------------------------------------------------|--------------------------------------------------------------------------|-----------------------------------------------------|----|----|------------------------------------|--------------------------|-------------------------------------------------------------|----------------------------------------------|-----------|
| 0x0417                                             |        | Demap sampled address                                | Sampled address, Bits[7:0]                                               |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x0418                                             |        |                                                      | Sampled address, Bits[15:8]                                              |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x0419                                             |        | Demap set point address                              | Set point address, Bits[7:0]                                             |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x041A                                             |        |                                                      | Set point address, Bits[15:8]                                            |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x041B                                             |        | Demap gain control                                   | Gain, Bits[7:0]                                                          |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x041C                                             |        |                                                      | Gain, Bits[15:8]                                                         |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x041D                                             |        |                                                      | Gain, Bits[23:16]                                                        |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x041E                                             |        | Demap clamp control                                  | Clamp value, Bits[7:0]                                                   |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| Output PLL_0 (APLL_0) and Channel 0 Output Drivers |        |                                                      |                                                                          |                                                     |    |    |                                    |                          |                                                             |                                              |           |
| 0x0430                                             |        | APLL_0 charge pump                                   | Reserved                                                                 | Output PLL0 (APLL_0) charge pump current, Bits[6:0] |    |    |                                    |                          |                                                             |                                              | 0x2E      |
| 0x0431                                             |        | APLL_0 M0 divider                                    | Output PLL0 (APLL_0) feedback (M0) divider, Bits[7:0]                    |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x0432                                             |        | APLL_0 loop filter control                           | APLL_0 loop filter control, Bits[7:0]                                    |                                                     |    |    |                                    |                          |                                                             |                                              | 0x7F      |
| 0x0433                                             |        |                                                      | Reserved                                                                 |                                                     |    |    |                                    |                          | P0 divider reset                                            | APLL_0 loop filter control, Bit 8            | 0x00      |
| 0x0434                                             |        | P0 divider                                           | Reserved                                                                 |                                                     |    |    | P0 divider divide ratio, Bits[3:0] |                          |                                                             |                                              | 0x00      |
| 0x0435                                             |        | OUT0 sync                                            | Reserved                                                                 |                                                     |    |    |                                    | Sync source selection    | Auto sync mode, Bits[1:0]                                   |                                              | 0x00      |
| 0x0436                                             |        |                                                      | Reserved                                                                 |                                                     |    |    |                                    | APLL_0 mask sync         | Mask OUT0B sync                                             | Reserved                                     | 0x00      |
| 0x0437                                             |        | Reserved                                             | Reserved                                                                 |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x0438                                             |        |                                                      | Reserved                                                                 |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x0439                                             |        |                                                      | Reserved                                                                 |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x043A                                             |        |                                                      | Reserved                                                                 |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x043B                                             |        | OUT0B                                                | Reserved                                                                 |                                                     |    |    |                                    | OUT0B mode, Bits[1:0]    | Invert polarity                                             | 0x08                                         |           |
| 0x043C                                             |        | Q0_B divider                                         | Q0_B divider, Bits[7:0]                                                  |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x043D                                             |        |                                                      | Reserved                                                                 |                                                     |    |    |                                    | Q0_B divider, Bits[9:8]  |                                                             |                                              | 0x00      |
| 0x043E                                             |        |                                                      | Reserved                                                                 | Q0_B divider phase, Bits[5:0]                       |    |    |                                    |                          |                                                             |                                              | 0x00      |
| DPLL_0 Settings for Reference Input A              |        |                                                      |                                                                          |                                                     |    |    |                                    |                          |                                                             |                                              |           |
| 0x0440                                             |        | Reference priority                                   | Reserved                                                                 |                                                     |    |    |                                    | REFA priority, Bits[1:0] | Enable REFA                                                 | 0x00                                         |           |
| 0x0441                                             | W2, L  | DPLL_0 loop BW (17 bits)                             | Digital PLL_0 loop bandwidth scaling factor, Bits[7:0] (unit of 0.1 Hz)  |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x0442                                             | W2, L  |                                                      | Digital PLL_0 loop bandwidth scaling factor, Bits[15:8] (unit of 0.1 Hz) |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x0443                                             | W2, L  |                                                      | Reserved                                                                 |                                                     |    |    |                                    |                          | Base loop filter selection                                  | Digital PLL_0 loop BW scaling factor, Bit 16 | 0x00      |
| 0x0444                                             | W2     | DPLL_0 N0 divider (18 bits)                          | Digital PLL_0 feedback divider—Integer Part N0, Bits[7:0]                |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x0445                                             | W2     |                                                      | Digital PLL_0 feedback divider—Integer Part N0, Bits[15:8]               |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x0446                                             | W2     |                                                      | Reserved                                                                 |                                                     |    |    |                                    |                          | Digital PLL_0 feedback divider—Integer Part N0, Bits[17:16] |                                              | 0x00      |
| 0x0447                                             | W8     | DPLL_0 fractional feedback divider (24 bits)         | Digital PLL_0 fractional feedback divider—FRAC0, Bits[7:0]               |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x0448                                             | W8     |                                                      | Digital PLL_0 fractional feedback divider—FRAC0, Bits[15:8]              |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x0449                                             | W8     |                                                      | Digital PLL_0 fractional feedback divider—FRAC0, Bits[23:16]             |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x044A                                             | W2     | DPLL_0 fractional feedback divider modulus (24 bits) | Digital PLL_0 feedback divider modulus—MOD0, Bits[7:0]                   |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x044B                                             | W2     |                                                      | Digital PLL_0 feedback divider modulus—MOD0, Bits[15:8]                  |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |
| 0x044C                                             | W2     |                                                      | Digital PLL_0 feedback divider modulus—MOD0, Bits[23:16]                 |                                                     |    |    |                                    |                          |                                                             |                                              | 0x00      |

| Reg. Addr. (Hex)                      | Option | Name                                                 | D7                                                                       | D6 | D5 | D4 | D3 | D2                       | D1                                                          | D0                                           | Def (Hex) |      |
|---------------------------------------|--------|------------------------------------------------------|--------------------------------------------------------------------------|----|----|----|----|--------------------------|-------------------------------------------------------------|----------------------------------------------|-----------|------|
| DPLL_0 Settings for Reference Input B |        |                                                      |                                                                          |    |    |    |    |                          |                                                             |                                              |           |      |
| 0x044D                                |        | Reference priority                                   | Reserved                                                                 |    |    |    |    | REFB priority, Bits[1:0] |                                                             | Enable REFB                                  | 0x00      |      |
| 0x044E                                | W2,L   | DPLL_0 loop BW (17 bits)                             | Digital PLL_0 loop bandwidth scaling factor, Bits[7:0] (unit of 0.1 Hz)  |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x044F                                | W2,L   |                                                      | Digital PLL_0 loop bandwidth scaling factor, Bits[15:8] (unit of 0.1 Hz) |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x0450                                | W2,L   |                                                      | Reserved                                                                 |    |    |    |    |                          | Base loop filter selection                                  | Digital PLL_0 loop BW scaling factor, Bit 16 | 0x00      |      |
| 0x0451                                | W2     | DPLL_0 N0 divider (18 bits)                          | Digital PLL_0 feedback divider—Integer Part N0, Bits[7:0]                |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x0452                                | W2     |                                                      | Digital PLL_0 feedback divider—Integer Part N0, Bits[15:8]               |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x0453                                | W2     |                                                      | Reserved                                                                 |    |    |    |    |                          | Digital PLL_0 feedback divider—Integer Part N0, Bits[17:16] |                                              |           | 0x00 |
| 0x0454                                | W8     | DPLL_0 fractional feedback divider (24 bits)         | Digital PLL_0 fractional feedback divider—FRAC0, Bits[7:0]               |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x0455                                | W8     |                                                      | Digital PLL_0 fractional feedback divider—FRAC0, Bits[15:8]              |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x0456                                | W8     |                                                      | Digital PLL_0 fractional feedback divider—FRAC0, Bits[23:16]             |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x0457                                | W2     | DPLL_0 fractional feedback divider modulus (24 bits) | Digital PLL_0 feedback divider modulus—MOD0, Bits[7:0]                   |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x0458                                | W2     |                                                      | Digital PLL_0 feedback divider modulus—MOD0, Bits[15:8]                  |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x0459                                | W2     |                                                      | Digital PLL_0 feedback divider modulus—MOD0, Bits[23:16]                 |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| DPLL_0 Settings for Reference Input C |        |                                                      |                                                                          |    |    |    |    |                          |                                                             |                                              |           |      |
| 0x045A                                |        | Reference priority                                   | Reserved                                                                 |    |    |    |    | REFC priority, Bits[1:0] |                                                             | Enable REFC                                  | 0x00      |      |
| 0x045B                                | W2,L   | DPLL_0 loop BW (17 bits)                             | Digital PLL_0 loop bandwidth scaling factor, Bits[7:0] (unit of 0.1 Hz)  |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x045C                                | W2,L   |                                                      | Digital PLL_0 loop bandwidth scaling factor, Bits[15:8] (unit of 0.1 Hz) |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x045D                                | W2,L   |                                                      | Reserved                                                                 |    |    |    |    |                          | Base loop filter selection                                  | Digital PLL_0 loop BW scaling factor, Bit 16 | 0x00      |      |
| 0x045E                                | W2     | DPLL_0 N0 divider (18 bits)                          | Digital PLL_0 feedback divider—Integer Part N0, Bits[7:0]                |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x045F                                | W2     |                                                      | Digital PLL_0 feedback divider—Integer Part N0, Bits[15:8]               |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x0460                                | W2     |                                                      | Reserved                                                                 |    |    |    |    |                          | Digital PLL_0 feedback divider—Integer Part N0, Bits[17:16] |                                              |           | 0x00 |
| 0x0461                                | W8     | DPLL_0 fractional feedback divider (24 bits)         | Digital PLL_0 fractional feedback divider—FRAC0, Bits[7:0]               |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x0462                                | W8     |                                                      | Digital PLL_0 fractional feedback divider—FRAC0, Bits[15:8]              |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x0463                                | W8     |                                                      | Digital PLL_0 fractional feedback divider—FRAC0, Bits[23:16]             |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x0464                                | W2     | DPLL_0 fractional feedback divider modulus (24 bits) | Digital PLL_0 feedback divider modulus—MOD0, Bits[7:0]                   |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x0465                                | W2     |                                                      | Digital PLL_0 feedback divider modulus—MOD0, Bits[15:8]                  |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x0466                                | W2     |                                                      | Digital PLL_0 feedback divider modulus—MOD0, Bits[23:16]                 |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| DPLL_0 Settings for Reference Input D |        |                                                      |                                                                          |    |    |    |    |                          |                                                             |                                              |           |      |
| 0x0467                                |        | Reference priority                                   | Reserved                                                                 |    |    |    |    | REFD priority, Bits[1:0] |                                                             | Enable REFD                                  | 0x00      |      |
| 0x0468                                | W2,L   | DPLL_0 loop BW (17 bits)                             | Digital PLL_0 loop bandwidth scaling factor, Bits[7:0] (unit of 0.1 Hz)  |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x0469                                | W2,L   |                                                      | Digital PLL_0 loop bandwidth scaling factor, Bits[15:8] (unit of 0.1 Hz) |    |    |    |    |                          |                                                             |                                              |           | 0x00 |
| 0x046A                                | W2,L   |                                                      | Reserved                                                                 |    |    |    |    |                          | Base loop filter selection                                  | Digital PLL_0 loop BW scaling factor, Bit 16 | 0x00      |      |

| Reg. Addr. (Hex)                                   | Option | Name                                                 | D7                                                                                                                                                                                    | D6 | D5 | D4 | D3 | D2 | D1 | D0                                                          | Def (Hex) |
|----------------------------------------------------|--------|------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|-------------------------------------------------------------|-----------|
| 0x046B                                             | W2     | DPLL_0 N0 divider (18 bits)                          | Digital PLL_0 feedback divider—Integer Part N0, Bits[7:0]                                                                                                                             |    |    |    |    |    |    |                                                             | 0x00      |
| 0x046C                                             | W2     |                                                      | Digital PLL_0 feedback divider—Integer Part N0, Bits[15:8]                                                                                                                            |    |    |    |    |    |    |                                                             | 0x00      |
| 0x046D                                             | W2     |                                                      | Reserved                                                                                                                                                                              |    |    |    |    |    |    | Digital PLL_0 feedback divider—Integer Part N0, Bits[17:16] | 0x00      |
| 0x046E                                             | W8     | DPLL_0 fractional feedback divider (24 bits)         | Digital PLL_0 fractional feedback divider—FRAC0, Bits[7:0]                                                                                                                            |    |    |    |    |    |    |                                                             | 0x00      |
| 0x046F                                             | W8     |                                                      | Digital PLL_0 fractional feedback divider—FRAC0, Bits[15:8]                                                                                                                           |    |    |    |    |    |    |                                                             | 0x00      |
| 0x0470                                             | W8     |                                                      | Digital PLL_0 fractional feedback divider—FRAC0, Bits[23:16]                                                                                                                          |    |    |    |    |    |    |                                                             | 0x00      |
| 0x0471                                             | W2     | DPLL_0 fractional feedback divider modulus (24 bits) | Digital PLL_0 feedback divider modulus—MOD0, Bits[7:0]                                                                                                                                |    |    |    |    |    |    |                                                             | 0x00      |
| 0x0472                                             | W2     |                                                      | Digital PLL_0 feedback divider modulus—MOD0, Bits[15:8]                                                                                                                               |    |    |    |    |    |    |                                                             | 0x00      |
| 0x0473                                             | W2     |                                                      | Digital PLL_0 feedback divider modulus—MOD0, Bits[23:16]                                                                                                                              |    |    |    |    |    |    |                                                             | 0x00      |
| DPLL_1 General Settings                            |        |                                                      |                                                                                                                                                                                       |    |    |    |    |    |    |                                                             |           |
| 0x0500 to 0x051E                                   |        |                                                      | These registers mimic the DPLL_0 general settings registers (0x0400 through 0x041E) but the register addresses are offset by 0x0100. All default values are identical.                |    |    |    |    |    |    |                                                             |           |
| Output PLL_1 (APLL_1) and Channel 1 Output Drivers |        |                                                      |                                                                                                                                                                                       |    |    |    |    |    |    |                                                             |           |
| 0x0530 to 0x053E                                   |        |                                                      | These registers mimic the output PLL_0 (APLL_0) general settings registers (0x0430 through 0x043E) but the register addresses are offset by 0x0100. All default values are identical. |    |    |    |    |    |    |                                                             |           |
| DPLL_1 Settings for Reference Input A              |        |                                                      |                                                                                                                                                                                       |    |    |    |    |    |    |                                                             |           |
| 0x0540 to 0x054C                                   |        |                                                      | These registers mimic the DPLL_0 settings for Reference Input A registers (0x0440 through 0x044C) but the register addresses are offset by 0x0100. All default values are identical.  |    |    |    |    |    |    |                                                             |           |
| DPLL_1 Settings for Reference Input B              |        |                                                      |                                                                                                                                                                                       |    |    |    |    |    |    |                                                             |           |
| 0x054D to 0x0559                                   |        |                                                      | These registers mimic the DPLL_0 settings for Reference Input B registers (0x044D through 0x0459) but the register addresses are offset by 0x0100. All default values are identical.  |    |    |    |    |    |    |                                                             |           |
| DPLL_1 Settings for Reference Input C              |        |                                                      |                                                                                                                                                                                       |    |    |    |    |    |    |                                                             |           |
| 0x055A to 0x0566                                   |        |                                                      | These registers mimic the DPLL_0 settings for Reference Input C registers (0x045A through 0x0466) but the register addresses are offset by 0x0100. All default values are identical.  |    |    |    |    |    |    |                                                             |           |
| DPLL_1 Settings for Reference Input D              |        |                                                      |                                                                                                                                                                                       |    |    |    |    |    |    |                                                             |           |
| 0x0567 to 0x0573                                   |        |                                                      | These registers mimic the DPLL_0 settings for Reference Input D registers (0x0467 through 0x0473) but the register addresses are offset by 0x0100. All default values are identical.  |    |    |    |    |    |    |                                                             |           |
| DPLL_2 General Settings                            |        |                                                      |                                                                                                                                                                                       |    |    |    |    |    |    |                                                             |           |
| 0x0600 to 0x061E                                   |        |                                                      | These registers mimic the DPLL_0 general settings registers (0x0400 through 0x041E) but the register addresses are offset by 0x0200. All default values are identical.                |    |    |    |    |    |    |                                                             |           |
| Output PLL_2 (APLL_2) and Channel 2 Output Drivers |        |                                                      |                                                                                                                                                                                       |    |    |    |    |    |    |                                                             |           |
| 0x0630 to 0x063E                                   |        |                                                      | These registers mimic the output PLL_0 (APLL_0) general settings registers (0x0430 through 0x043E) but the register addresses are offset by 0x0200. All default values are identical. |    |    |    |    |    |    |                                                             |           |
| DPLL_2 Settings for Reference Input A              |        |                                                      |                                                                                                                                                                                       |    |    |    |    |    |    |                                                             |           |
| 0x0640 to 0x064C                                   |        |                                                      | These registers mimic the DPLL_0 settings for Reference Input A registers (0x0440 through 0x044C) but the register addresses are offset by 0x0200. All default values are identical.  |    |    |    |    |    |    |                                                             |           |
| DPLL_2 Settings for Reference Input B              |        |                                                      |                                                                                                                                                                                       |    |    |    |    |    |    |                                                             |           |
| 0x064D to 0x0659                                   |        |                                                      | These registers mimic the DPLL_0 settings for Reference Input B registers (0x044D through 0x0459) but the register addresses are offset by 0x0200. All default values are identical.  |    |    |    |    |    |    |                                                             |           |
| DPLL_2 Settings for Reference Input C              |        |                                                      |                                                                                                                                                                                       |    |    |    |    |    |    |                                                             |           |
| 0x065A to 0x0666                                   |        |                                                      | These registers mimic the DPLL_0 settings for Reference Input C registers (0x045A through 0x0466) but the register addresses are offset by 0x0200. All default values are identical.  |    |    |    |    |    |    |                                                             |           |
| DPLL_2 Settings for Reference Input D              |        |                                                      |                                                                                                                                                                                       |    |    |    |    |    |    |                                                             |           |
| 0x0667 to 0x0673                                   |        |                                                      | These registers mimic the DPLL_0 settings for Reference Input D registers (0x0467 through 0x0473) but the register addresses are offset by 0x0200. All default values are identical.  |    |    |    |    |    |    |                                                             |           |

| Reg. Addr. (Hex)                                   | Option | Name                                                          | D7                                                                                                                                                                                    | D6                              | D5 | D4 | D3 | D2 | D1 | D0 | Def (Hex)               |      |      |
|----------------------------------------------------|--------|---------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|----|----|----|----|----|----|-------------------------|------|------|
| DPLL_3 General Settings                            |        |                                                               |                                                                                                                                                                                       |                                 |    |    |    |    |    |    |                         |      |      |
| 0x0700 to 0x071E                                   |        |                                                               | These registers mimic the DPLL_0 general settings registers (0x0400 through 0x041E) but the register addresses are offset by 0x0300. All default values are identical.                |                                 |    |    |    |    |    |    |                         |      |      |
| Output PLL_3 (APLL_3) and Channel 3 Output Drivers |        |                                                               |                                                                                                                                                                                       |                                 |    |    |    |    |    |    |                         |      |      |
| 0x0730 to 0x073E                                   |        |                                                               | These registers mimic the output PLL_0 (APLL_0) general settings registers (0x0430 through 0x043E) but the register addresses are offset by 0x0300. All default values are identical. |                                 |    |    |    |    |    |    |                         |      |      |
| DPLL_3 Settings for Reference Input A              |        |                                                               |                                                                                                                                                                                       |                                 |    |    |    |    |    |    |                         |      |      |
| 0x0740 to 0x074C                                   |        |                                                               | These registers mimic the DPLL_0 settings for Reference Input A registers (0x0440 through 0x044C) but the register addresses are offset by 0x0300. All default values are identical.  |                                 |    |    |    |    |    |    |                         |      |      |
| DPLL_3 Settings for Reference Input B              |        |                                                               |                                                                                                                                                                                       |                                 |    |    |    |    |    |    |                         |      |      |
| 0x074D to 0x0759                                   |        |                                                               | These registers mimic the DPLL_0 settings for Reference Input B registers (0x044D through 0x0459) but the register addresses are offset by 0x0300. All default values are identical.  |                                 |    |    |    |    |    |    |                         |      |      |
| DPLL_3 Settings for Reference Input C              |        |                                                               |                                                                                                                                                                                       |                                 |    |    |    |    |    |    |                         |      |      |
| 0x075A to 0x0766                                   |        |                                                               | These registers mimic the DPLL_0 Settings for Reference Input C registers (0x045A through 0x0466) but the register addresses are offset by 0x0300. All default values are identical.  |                                 |    |    |    |    |    |    |                         |      |      |
| DPLL_3 Settings for Reference Input D              |        |                                                               |                                                                                                                                                                                       |                                 |    |    |    |    |    |    |                         |      |      |
| 0x0767 to 0x0773                                   |        |                                                               | These registers mimic the DPLL_0 Settings for Reference Input D registers (0x0467 through 0x0473) but the register addresses are offset by 0x0300. All default values are identical.  |                                 |    |    |    |    |    |    |                         |      |      |
| Digital Loop Filter Coefficients                   |        |                                                               |                                                                                                                                                                                       |                                 |    |    |    |    |    |    |                         |      |      |
| 0x0800                                             | L      | Base loop filter coefficient set (normal phase margin of 70°) | NPM Alpha-0 linear, Bits[7:0]                                                                                                                                                         |                                 |    |    |    |    |    |    |                         | 0x24 |      |
| 0x0801                                             | L      |                                                               | NPM Alpha-0 linear, Bits[15:8]                                                                                                                                                        |                                 |    |    |    |    |    |    |                         | 0x8C |      |
| 0x0802                                             | L      |                                                               | Reserved                                                                                                                                                                              | NPM Alpha-1 exponent, Bits[6:0] |    |    |    |    |    |    |                         |      | 0x49 |
| 0x0803                                             | L      |                                                               | NPM Beta-0 linear, Bits[7:0]                                                                                                                                                          |                                 |    |    |    |    |    |    |                         | 0x55 |      |
| 0x0804                                             | L      |                                                               | NPM Beta-0 linear, Bits[15:8]                                                                                                                                                         |                                 |    |    |    |    |    |    |                         | 0xC9 |      |
| 0x0805                                             | L      |                                                               | Reserved                                                                                                                                                                              | NPM Beta-1 exponent, Bits[6:0]  |    |    |    |    |    |    |                         |      | 0x7B |
| 0x0806                                             | L      |                                                               | NPM Gamma-0 linear, Bits[7:0]                                                                                                                                                         |                                 |    |    |    |    |    |    |                         | 0x9C |      |
| 0x0807                                             | L      |                                                               | NPM Gamma-0 linear, Bits[15:8]                                                                                                                                                        |                                 |    |    |    |    |    |    |                         | 0xFA |      |
| 0x0808                                             | L      |                                                               | Reserved                                                                                                                                                                              | NPM Gamma-1 exponent, Bits[6:0] |    |    |    |    |    |    |                         |      | 0x55 |
| 0x0809                                             | L      |                                                               | NPM Delta-0 linear, Bits[7:0]                                                                                                                                                         |                                 |    |    |    |    |    |    |                         | 0xEA |      |
| 0x080A                                             | L      | NPM Delta-0 linear, Bits[15:8]                                |                                                                                                                                                                                       |                                 |    |    |    |    |    |    | 0xE2                    |      |      |
| 0x080B                                             | L      | Reserved                                                      | NPM Delta-1 exponent, Bits[6:0]                                                                                                                                                       |                                 |    |    |    |    |    |    |                         | 0x57 |      |
| 0x080C                                             | L      | Base loop filter coefficient set (high phase margin)          | HPM Alpha-0 linear, Bits[7:0]                                                                                                                                                         |                                 |    |    |    |    |    |    |                         | 0x8C |      |
| 0x080D                                             | L      |                                                               | HPM Alpha-0 linear, Bits[15:8]                                                                                                                                                        |                                 |    |    |    |    |    |    |                         | 0xAD |      |
| 0x080E                                             | L      |                                                               | Reserved                                                                                                                                                                              | HPM Alpha-1 exponent, Bits[6:0] |    |    |    |    |    |    |                         |      | 0x4C |
| 0x080F                                             | L      |                                                               | HPM Beta-0 linear, Bits[7:0]                                                                                                                                                          |                                 |    |    |    |    |    |    |                         | 0xF5 |      |
| 0x0810                                             | L      |                                                               | HPM Beta-0 linear, Bits[15:8]                                                                                                                                                         |                                 |    |    |    |    |    |    |                         | 0xCB |      |
| 0x0811                                             | L      |                                                               | Reserved                                                                                                                                                                              | HPM Beta-1 exponent, Bits[6:0]  |    |    |    |    |    |    |                         |      | 0x73 |
| 0x0812                                             | L      |                                                               | HPM Gamma-0 linear, Bits[7:0]                                                                                                                                                         |                                 |    |    |    |    |    |    |                         | 0x24 |      |
| 0x0813                                             | L      |                                                               | HPM Gamma-0 linear, Bits[15:8]                                                                                                                                                        |                                 |    |    |    |    |    |    |                         | 0xD8 |      |
| 0x0814                                             | L      |                                                               | Reserved                                                                                                                                                                              | HPM Gamma-1 exponent, Bits[6:0] |    |    |    |    |    |    |                         |      | 0x59 |
| 0x0815                                             | L      |                                                               | HPM Delta-0 linear, Bits[7:0]                                                                                                                                                         |                                 |    |    |    |    |    |    |                         | 0xD2 |      |
| 0x0816                                             | L      | HPM Delta-0 linear, Bits[15:8]                                |                                                                                                                                                                                       |                                 |    |    |    |    |    |    | 0x8D                    |      |      |
| 0x0817                                             | L      | Reserved                                                      | HPM Delta-1 exponent, Bits[6:0]                                                                                                                                                       |                                 |    |    |    |    |    |    |                         | 0x5A |      |
| Global Demapping Control                           |        |                                                               |                                                                                                                                                                                       |                                 |    |    |    |    |    |    |                         |      |      |
| 0x0900                                             | L      | Demap control IO_UPDATE                                       | Reserved                                                                                                                                                                              |                                 |    |    |    |    |    |    | Demap control IO_UPDATE | 0x00 |      |
| 0x0901                                             |        | DPLL_0                                                        | DPLL_0 sampled address, Bits[7:0]                                                                                                                                                     |                                 |    |    |    |    |    |    |                         | 0x00 |      |
| 0x0902                                             |        |                                                               | DPLL_0 sampled address, Bits[15:8]                                                                                                                                                    |                                 |    |    |    |    |    |    |                         | 0x00 |      |
| 0x0903                                             |        | DPLL_1                                                        | DPLL_1 sampled address, Bits[7:0]                                                                                                                                                     |                                 |    |    |    |    |    |    |                         | 0x00 |      |
| 0x0904                                             |        |                                                               | DPLL_1 sampled address, Bits[15:8]                                                                                                                                                    |                                 |    |    |    |    |    |    |                         | 0x00 |      |
| 0x0905                                             |        | DPLL_2                                                        | DPLL_2 sampled address, Bits[7:0]                                                                                                                                                     |                                 |    |    |    |    |    |    |                         | 0x00 |      |
| 0x0906                                             |        |                                                               | DPLL_2 sampled address, Bits[15:8]                                                                                                                                                    |                                 |    |    |    |    |    |    |                         | 0x00 |      |
| 0x0907                                             |        | DPLL_3                                                        | DPLL_3 sampled address, Bits[7:0]                                                                                                                                                     |                                 |    |    |    |    |    |    |                         | 0x00 |      |
| 0x0908                                             |        |                                                               | DPLL_3 sampled address, Bits[15:8]                                                                                                                                                    |                                 |    |    |    |    |    |    |                         | 0x00 |      |



| Reg. Addr. (Hex)            | Option | Name                    | D7                   | D6                      | D5                    | D4                    | D3                       | D2                                   | D1                    | D0                      | Def (Hex) |
|-----------------------------|--------|-------------------------|----------------------|-------------------------|-----------------------|-----------------------|--------------------------|--------------------------------------|-----------------------|-------------------------|-----------|
| 0x0909                      |        | Demap control IO_UPDATE | Reserved             |                         |                       |                       |                          |                                      |                       | Demap control IO_UPDATE | 0x00      |
| Common Operational Controls |        |                         |                      |                         |                       |                       |                          |                                      |                       |                         |           |
| 0x0A00                      |        | Global                  | Reserved             |                         |                       |                       | Soft sync all            | Calibrate SYSCLK                     | Calibrate all         | Power-down all          | 0x00      |
| 0x0A01                      |        | Reference inputs        | Reserved             |                         |                       |                       | REFD power-down          | REFC power-down                      | REFB power-down       | REFA power-down         | 0x00      |
| 0x0A02                      | A      |                         | Reserved             |                         |                       |                       | REFD timeout             | REFC timeout                         | REFB timeout          | REFA timeout            | 0x00      |
| 0x0A03                      |        |                         | Reserved             |                         |                       |                       | REFD fault               | REFC fault                           | REFB fault            | REFA fault              | 0x00      |
| 0x0A04                      |        |                         | Reserved             |                         |                       |                       | REFD monitor bypass      | REFC monitor bypass                  | REFB monitor bypass   | REFA monitor bypass     | 0x00      |
| 0x0A05                      | A      | Clear IRQ groups        | Clear watchdog timer | Reserved                | Clear DPLL_3 IRQs     | Clear DPLL_2 IRQs     | Clear DPLL_1 IRQs        | Clear DPLL_0 IRQs                    | Clear common IRQs     | Clear all IRQs          | 0x00      |
| 0x0A06                      | A      | Clear common IRQ        | SYSCLK unlocked      | SYSCLK stable           | SYSCLK locked         | SYSCLK cal ended      | SYSCLK cal started       | Watchdog timer                       | Reserved              |                         | 0x00      |
| 0x0A07                      | A      |                         | Reserved             | REFB validated          | REFB fault cleared    | REFB fault            | Reserved                 | REFA validated                       | REFA fault cleared    | REFA fault              | 0x00      |
| 0x0A08                      | A      |                         | Reserved             | REFD validated          | REFD fault cleared    | REFD fault            | Reserved                 | REFC validated                       | REFC fault cleared    | REFC fault              | 0x00      |
| 0x0A09                      | A      | Clear DPLL_0 IRQ        | Frequency unclamped  | Frequency clamped       | Phase slew unlimited  | Phase slew limited    | Frequency unlocked       | Frequency locked                     | Phase unlocked        | Phase locked            | 0x00      |
| 0x0A0A                      | A      |                         | DPLL_0 switching     | DPLL_0 free run         | DPLL_0 holdover       | History updated       | REFD activated           | REFC activated                       | REFB activated        | REFA activated          | 0x00      |
| 0x0A0B                      | A      |                         | Phase step detected  | Demap control unclamped | Demap control clamped | Clock dist sync'd     | APLL_0 unlocked          | APLL_0 locked                        | APLL_0 cal ended      | APLL_0 cal started      | 0x00      |
| 0x0A0C                      | A      | Clear DPLL_1 IRQ        | Frequency unclamped  | Frequency clamped       | Phase slew unlimited  | Phase slew limited    | Frequency unlocked       | Frequency locked                     | Phase unlocked        | Phase locked            | 0x00      |
| 0x0A0D                      | A      |                         | DPLL_1 switching     | DPLL_1 free run         | DPLL_1 holdover       | History updated       | REFD activated           | REFC activated                       | REFB activated        | REFA activated          | 0x00      |
| 0x0A0E                      | A      |                         | Phase step detected  | Demap control unclamped | Demap control clamped | Clock dist sync'd     | APLL_1 unlocked          | APLL_1 locked                        | APLL_1 cal ended      | APLL_1 cal started      | 0x00      |
| 0x0A0F                      | A      | Clear DPLL_2 IRQ        | Frequency unclamped  | Frequency clamped       | Phase slew unlimited  | Phase slew limited    | Frequency unlocked       | Frequency locked                     | Phase unlocked        | Phase locked            | 0x00      |
| 0x0A10                      | A      |                         | DPLL_2 switching     | DPLL_2 free run         | DPLL_2 holdover       | History updated       | REFD activated           | REFC activated                       | REFB activated        | REFA activated          | 0x00      |
| 0x0A11                      | A      |                         | Phase step detected  | Demap control unclamped | Demap control clamped | Clock dist sync'd     | APLL_2 unlocked          | APLL_2 locked                        | APLL_2 cal ended      | APLL_2 cal started      | 0x00      |
| 0x0A12                      | A      | Clear DPLL_3 IRQ        | Frequency unclamped  | Frequency clamped       | Phase slew unlimited  | Phase slew limited    | Frequency unlocked       | Frequency locked                     | Phase unlocked        | Phase locked            | 0x00      |
| 0x0A13                      | A      |                         | DPLL_3 switching     | DPLL_3 free run         | DPLL_3 holdover       | History updated       | REFD activated           | REFC activated                       | REFB activated        | REFA activated          | 0x00      |
| 0x0A14                      | A      |                         | Phase step detected  | Demap control unclamped | Demap control clamped | Clock dist sync'd     | APLL_3 unlocked          | APLL_3 locked                        | APLL_3 cal ended      | APLL_3 cal started      | 0x00      |
| PLL_0 Operational Controls  |        |                         |                      |                         |                       |                       |                          |                                      |                       |                         |           |
| 0x0A20                      |        | PLL_0 sync cal          | Reserved             |                         |                       |                       | APLL_0 soft sync         | APLL_0 calibrate (not self-clearing) | PLL_0 power-down      | 0x00                    |           |
| 0x0A21                      |        | PLL_0 output            | Reserved             |                         |                       | OUT0B disable         | Reserved                 | OUT0B power-down                     | Reserved              | 0x00                    |           |
| 0x0A22                      |        | PLL_0 user mode         | Reserved             | DPLL_0 manual reference |                       | DPLL_0 switching mode |                          | DPLL_0 user holdover                 | DPLL_0 user free run  | 0x00                    |           |
| 0x0A23                      | A      | PLL_0 reset             | Reserved             |                         |                       |                       | Reset DPLL_0 loop filter | Reset DPLL_0 TW history              | Reset DPLL_0 autosync | 0x00                    |           |

| Reg. Addr. (Hex)                                                                                                                       | Option | Name                  | D7                                                                                                                                                                        | D6                      | D5                    | D4                     | D3                 | D2                        | D1                            | D0                            | Def (Hex) |
|----------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|-----------------------|------------------------|--------------------|---------------------------|-------------------------------|-------------------------------|-----------|
| 0x0A24                                                                                                                                 | A      | PLL_0 phase           | Reserved                                                                                                                                                                  |                         |                       |                        |                    | DPLL_0 reset phase offset | DPLL_0 decrement phase offset | DPLL_0 increment phase offset | 0x00      |
| PLL_1 Operational Controls                                                                                                             |        |                       |                                                                                                                                                                           |                         |                       |                        |                    |                           |                               |                               |           |
| 0x0A40 to 0x0A44                                                                                                                       |        |                       | These registers mimic the PLL_0 operational controls registers (0x0A20 through 0x0A24) but the register addresses are offset by 0x0020. All default values are identical. |                         |                       |                        |                    |                           |                               |                               |           |
| PLL_2 Operational Controls                                                                                                             |        |                       |                                                                                                                                                                           |                         |                       |                        |                    |                           |                               |                               |           |
| 0x0A60 to 0x0A64                                                                                                                       |        |                       | These registers mimic the PLL_0 operational controls registers (0x0A20 through 0x0A24) but the register addresses are offset by 0x0040. All default values are identical. |                         |                       |                        |                    |                           |                               |                               |           |
| PLL_3 Operational Controls                                                                                                             |        |                       |                                                                                                                                                                           |                         |                       |                        |                    |                           |                               |                               |           |
| 0x0A80 to 0x0A84                                                                                                                       |        |                       | These registers mimic the PLL_0 operational controls registers (0x0A20 through 0x0A24) but the register addresses are offset by 0x0060. All default values are identical. |                         |                       |                        |                    |                           |                               |                               |           |
| Voltage Regulator                                                                                                                      |        |                       |                                                                                                                                                                           |                         |                       |                        |                    |                           |                               |                               |           |
| 0x0B00                                                                                                                                 | L      | Voltage regulator     | VREG, Bits[7:0]                                                                                                                                                           |                         |                       |                        |                    |                           |                               |                               | 0x00      |
| 0x0B01                                                                                                                                 | L      |                       | Reserved                                                                                                                                                                  |                         |                       |                        |                    | VREG, Bits[9:8]           |                               |                               | 0x00      |
| Read-Only Status Common Blocks (To show the latest status, Register 0x0D02 to Register 0x0D05 require an IO_UPDATE before being read.) |        |                       |                                                                                                                                                                           |                         |                       |                        |                    |                           |                               |                               |           |
| 0x0D00                                                                                                                                 | R, L   | Reserved              | Reserved                                                                                                                                                                  |                         |                       |                        |                    |                           |                               |                               | N/A       |
| 0x0D01                                                                                                                                 | R, L   | SYSCLK and PLL status | PLL_3 all locked                                                                                                                                                          | PLL_2 all locked        | PLL_1 all locked      | PLL_0 all locked       | Reserved           | SYSCLK calibration busy   | SYSCLK stable                 | SYSCLK lock detect            | N/A       |
| 0x0D02                                                                                                                                 | R      | Reference status      | DPLL_3 REFA active                                                                                                                                                        | DPLL_2 REFA active      | DPLL_1 REFA active    | DPLL_0 REFA active     | REFA valid         | REFA fault                | REFA fast                     | REFA slow                     | N/A       |
| 0x0D03                                                                                                                                 | R      |                       | DPLL_3 REFB active                                                                                                                                                        | DPLL_2 REFB active      | DPLL_1 REFB active    | DPLL_0 REFB active     | REFB valid         | REFB fault                | REFB fast                     | REFB slow                     | N/A       |
| 0x0D04                                                                                                                                 | R      |                       | DPLL_3 REFC active                                                                                                                                                        | DPLL_2 REFC active      | DPLL_1 REFC active    | DPLL_0 REFC active     | REFC valid         | REFC fault                | REFC fast                     | REFC slow                     | N/A       |
| 0x0D05                                                                                                                                 | R      |                       | DPLL_3 REFD active                                                                                                                                                        | DPLL_2 REFD active      | DPLL_1 REFD active    | DPLL_0 REFD active     | REFD valid         | REFD fault                | REFD fast                     | REFD slow                     | N/A       |
| 0x0D06                                                                                                                                 | R      |                       | Reserved                                                                                                                                                                  |                         |                       |                        |                    |                           |                               |                               | N/A       |
| 0x0D07                                                                                                                                 | R      | Reserved              |                                                                                                                                                                           |                         |                       |                        |                    |                           |                               | N/A                           |           |
| IRQ Monitor                                                                                                                            |        |                       |                                                                                                                                                                           |                         |                       |                        |                    |                           |                               |                               |           |
| 0x0D08                                                                                                                                 | R, L   | IRQ, common           | SYSCLK unlocked                                                                                                                                                           | SYSCLK stable           | SYSCLK locked         | SYSCLK cal ended       | SYSCLK cal started | Watchdog timer            | Reserved                      |                               | N/A       |
| 0x0D09                                                                                                                                 | R, L   |                       | Reserved                                                                                                                                                                  | REFB validated          | REFB fault cleared    | REFB fault             | Reserved           | REFA validated            | REFA fault cleared            | REFA fault                    | N/A       |
| 0x0D0A                                                                                                                                 | R, L   |                       | Reserved                                                                                                                                                                  | REFD validated          | REFD fault cleared    | REFD fault             | Reserved           | REFC validated            | REFC fault cleared            | REFC fault                    | N/A       |
| 0x0D0B                                                                                                                                 | R, L   | IRQ, DPLL_0           | Frequency unclamped                                                                                                                                                       | Frequency clamped       | Phase slew unlimited  | Phase slew limited     | Frequency unlocked | Frequency locked          | Phase unlocked                | Phase locked                  | N/A       |
| 0x0D0C                                                                                                                                 | R, L   |                       | DPLL_0 switching                                                                                                                                                          | DPLL_0 free run         | DPLL_0 holdover       | DPLL_0 history updated | REFD activated     | REFC activated            | REFB activated                | REFA activated                | N/A       |
| 0x0D0D                                                                                                                                 | R, L   |                       | Phase step direction                                                                                                                                                      | Demap control unclamped | Demap control clamped | Clock dist sync'd      | APLL_0 unlocked    | APLL_0 locked             | APLL_0 cal ended              | APLL_0 cal started            | N/A       |
| 0x0D0E                                                                                                                                 | R, L   | IRQ, DPLL_1           | Frequency unclamped                                                                                                                                                       | Frequency clamped       | Phase slew unlimited  | Phase slew limited     | Frequency unlocked | Frequency locked          | Phase unlocked                | Phase locked                  | N/A       |
| 0x0D0F                                                                                                                                 | R, L   |                       | DPLL_1 switching                                                                                                                                                          | DPLL_1 free run         | DPLL_1 holdover       | DPLL_1 history updated | REFD activated     | REFC activated            | REFB activated                | REFA activated                | N/A       |
| 0x0D10                                                                                                                                 | R, L   |                       | Phase step direction                                                                                                                                                      | Demap control unclamped | Demap control clamped | Clock dist sync'd      | APLL_1 unlocked    | APLL_1 locked             | APLL_1 cal ended              | APLL_1 cal started            | N/A       |

| Reg. Addr. (Hex) | Option | Name        | D7                   | D6                      | D5                    | D4                     | D3                 | D2               | D1               | D0                 | Def (Hex) |
|------------------|--------|-------------|----------------------|-------------------------|-----------------------|------------------------|--------------------|------------------|------------------|--------------------|-----------|
| 0x0D11           | R, L   | IRQ, DPLL_2 | Frequency unclamped  | Frequency clamped       | Phase slew unlimited  | Phase slew limited     | Frequency unlocked | Frequency locked | Phase unlocked   | Phase locked       | N/A       |
| 0x0D12           | R, L   |             | DPLL_2 switching     | DPLL_2 free run         | DPLL_2 holdover       | DPLL_2 history updated | REFD activated     | REFC activated   | REFB activated   | REFA activated     | N/A       |
| 0x0D13           | R, L   |             | Phase step direction | Demap control unclamped | Demap control clamped | Clock dist sync'd      | APLL_2 unlocked    | APLL_2 locked    | APLL_2 cal ended | APLL_2 cal started | N/A       |
| 0x0D14           | R, L   | IRQ, DPLL_3 | Frequency unclamped  | Frequency clamped       | Phase slew unlimited  | Phase slew limited     | Frequency unlocked | Frequency locked | Phase unlocked   | Phase locked       | N/A       |
| 0x0D15           | R, L   |             | DPLL_3 switching     | DPLL_3 free run         | DPLL_3 holdover       | DPLL_3 history updated | REFD activated     | REFC activated   | REFB activated   | REFA activated     | N/A       |
| 0x0D16           | R, L   |             | Phase step direction | Demap control unclamped | Demap control clamped | Clock dist sync'd      | APLL_3 unlocked    | APLL_3 locked    | APLL_3 cal ended | APLL_3 cal started | N/A       |

PLL\_0 Read-Only Status (To show the latest status, these registers require an IO\_UPDATE before being read.)

|        |      |                                     |                                                      |                                          |  |                        |                                                       |                           |                          |                          |     |
|--------|------|-------------------------------------|------------------------------------------------------|------------------------------------------|--|------------------------|-------------------------------------------------------|---------------------------|--------------------------|--------------------------|-----|
| 0x0D20 | R, L | PLL_0 lock status                   | Reserved                                             |                                          |  | APLL_0 cal in progress | APLL_0 freq lock                                      | DPLL_0 freq lock          | DPLL_0 phase lock        | PLL_0 all locked         | N/A |
| 0x0D21 | R    | DPLL_0 loop state                   | Reserved                                             |                                          |  | DPLL_0 active ref      |                                                       | DPLL_0 switching          | DPLL_0 holdover          | DPLL_0 free run          | N/A |
| 0x0D22 | R    |                                     | Reserved                                             |                                          |  |                        | Demap controller clamped                              | DPLL_0 phase slew limited | DPLL_0 frequency clamped | DPLL_0 history available | N/A |
| 0x0D23 | R    | DPLL_0 holdover history             | DPLL_0 tuning word readback, Bits[7:0]               |                                          |  |                        |                                                       |                           |                          |                          | N/A |
| 0x0D24 | R    |                                     | DPLL_0 tuning word readback, Bits[15:8]              |                                          |  |                        |                                                       |                           |                          |                          | N/A |
| 0x0D25 | R    |                                     | DPLL_0 tuning word readback, Bits[23:16]             |                                          |  |                        |                                                       |                           |                          |                          | N/A |
| 0x0D26 | R    |                                     | Reserved                                             | DPLL_0 tuning word readback, Bits[29:24] |  |                        |                                                       |                           |                          |                          | N/A |
| 0x0D27 | R    | DPLL_0 phase lock detect bucket     | Reserved                                             |                                          |  |                        | DPLL_0 phase lock detect bucket level, Bits[7:0]      |                           |                          |                          | N/A |
| 0x0D28 | R    |                                     | Reserved                                             |                                          |  |                        | DPLL_0 phase lock detect bucket level, Bits[11:8]     |                           |                          |                          | N/A |
| 0x0D29 | R    | DPLL_0 frequency lock detect bucket | DPLL_0 frequency lock detect bucket level, Bits[7:0] |                                          |  |                        |                                                       |                           |                          |                          | N/A |
| 0x0D2A | R    |                                     | Reserved                                             |                                          |  |                        | DPLL_0 frequency lock detect bucket level, Bits[11:8] |                           |                          |                          | N/A |

PLL\_1 Read-Only Status (To show the latest status, these registers require an IO\_UPDATE before being read.)

|                  |  |  |                                                                                                                                                                       |  |  |  |  |  |  |  |     |
|------------------|--|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|-----|
| 0x0D40 to 0x0D4A |  |  | These registers mimic the PLL_0 read-only status registers (0x0D20 through 0x0D2A) but the register addresses are offset by 0x0020. All default values are identical. |  |  |  |  |  |  |  | N/A |
|------------------|--|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|-----|

PLL\_2 Read-Only Status (To show the latest status, these registers require an IO\_UPDATE before being read.)

|                  |  |  |                                                                                                                                                                       |  |  |  |  |  |  |  |     |
|------------------|--|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|-----|
| 0x0D60 to 0x0D6A |  |  | These registers mimic the PLL_0 read-only status registers (0x0D20 through 0x0D2A) but the register addresses are offset by 0x0040. All default values are identical. |  |  |  |  |  |  |  | N/A |
|------------------|--|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|-----|

PLL\_3 Read-Only Status (To show the latest status, these registers require an IO\_UPDATE before being read.)

|                  |  |  |                                                                                                                                                                       |  |  |  |  |  |  |  |     |
|------------------|--|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|-----|
| 0x0D80 to 0x0D8A |  |  | These registers mimic the PLL_0 Read-Only Status registers (0x0D20 through 0x0D2A) but the register addresses are offset by 0x0060. All default values are identical. |  |  |  |  |  |  |  | N/A |
|------------------|--|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|-----|

V<sub>CAL</sub> Reference Control

|        |  |                                   |                                   |  |  |  |                                    |  |                         |  |      |
|--------|--|-----------------------------------|-----------------------------------|--|--|--|------------------------------------|--|-------------------------|--|------|
| 0x0FFF |  | V <sub>CAL</sub> reference access | V <sub>CAL</sub> reference access |  |  |  |                                    |  |                         |  | 0x00 |
| 0x1488 |  | APLL_0 V <sub>CAL</sub> reference | Reserved                          |  |  |  | APLL_0 manual cal level, Bits[1:0] |  | En APLL_0 man cal level |  | 0x00 |
| 0x1588 |  | APLL_1 V <sub>CAL</sub> reference | Reserved                          |  |  |  | APLL_1 manual cal level, Bits[1:0] |  | En APLL_1 man cal level |  | 0x00 |
| 0x1688 |  | APLL_2 V <sub>CAL</sub> reference | Reserved                          |  |  |  | APLL_2 manual cal level, Bits[1:0] |  | En APLL_2 Man Cal Level |  | 0x00 |
| 0x1788 |  | APLL_3 V <sub>CAL</sub> reference | Reserved                          |  |  |  | APLL_3 manual cal level, Bits[1:0] |  | En APLL_3 man cal level |  | 0x00 |

## REGISTER MAP BIT DESCRIPTIONS

### SERIAL CONTROL PORT CONFIGURATION (REGISTER 0x0000 TO REGISTER 0x0001)

Table 32. SPI Configuration A

| Address | Bits  | Bit Name                     | Description                                                                                                                                                                                                                                                                                                                                                                                                    |
|---------|-------|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0000  | 7     | Soft reset                   | Device reset.                                                                                                                                                                                                                                                                                                                                                                                                  |
|         | 6     | LSB first (SPI only)         | Bit order for SPI port. This bit has no effect in I <sup>2</sup> C mode.<br>1 = least significant bit first.<br>0 (default) = most significant bit first.                                                                                                                                                                                                                                                      |
|         | 5     | Address ascension (SPI only) | This bit controls whether the register address is automatically incremented during a multibyte transfer. This bit has no effect in I <sup>2</sup> C mode.<br>1 = Register addresses are automatically incremented in multibyte transfers.<br>0 (default) = Register addresses are automatically decremented in multibyte transfers.                                                                            |
|         | 4     | Reserved                     | Default: 0b.                                                                                                                                                                                                                                                                                                                                                                                                   |
|         | [3:0] |                              | These bits are mirrors of Bits[7:4] of this register so that when the serial port is configured, the pattern written is independent of an MSB first/LSB first setting interpretation. The <a href="#">AD9554-1</a> internal logic performs a logical OR on the corresponding bits.<br>Bit 3 corresponds to Bit 4.<br>Bit 2 corresponds to Bit 5.<br>Bit 1 corresponds to Bit 6.<br>Bit 0 corresponds to Bit 7. |

Table 33. SPI Configuration B

| Address | Bits  | Bit Name             | Description                                                                                                                                                                                                                                                                                                              |
|---------|-------|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0001  | [7:6] | Reserved             | Reserved.                                                                                                                                                                                                                                                                                                                |
|         | 5     | Read buffer register | For buffered registers, this bit controls whether the value read from the serial port is from the actual (active) registers or the buffered copy.<br>1 = reads buffered values that take effect on the next assertion of IO_UPDATE.<br>0 (default) = reads values currently applied to the internal logic of the device. |
|         | [4:3] | Reserved             | Reserved.                                                                                                                                                                                                                                                                                                                |
|         | 2     | Reset sans regmap    | This bit resets the device while maintaining the current register settings.<br>1 = resets the device.<br>0 (default) = no action.                                                                                                                                                                                        |
|         | [1:0] | Reserved             | Reserved.                                                                                                                                                                                                                                                                                                                |

### CLOCK PART FAMILY ID (REGISTER 0x0003 TO REGISTER 0x0006)

Table 34. Clock Part Family ID

| Address | Bits  | Bit Name                         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|---------|-------|----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0003  | [7:4] | Reserved                         | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|         | [3:0] | Chip type, Bits[3:0]             | The Analog Devices unified SPI protocol reserves this read only register location for identifying the type of device. The default value of 0x05 identifies the <a href="#">AD9554-1</a> as a clock IC.                                                                                                                                                                                                                                        |
| 0x0004  | [7:4] | Clock part serial ID, Bits[3:0]  | The Analog Devices unified SPI protocol reserves this read only register location as the lower four bits of the clock part serial ID that (along with Register 0x0005) uniquely identifies the <a href="#">AD9554-1</a> within the Analog Devices clock chip family. No other Analog Devices chip that adheres to the Analog Devices unified SPI have these values for Register 0x0003, Register 0x0004, and Register 0x0005. Default: 0x9E.  |
|         | [3:0] | Reserved                         | Default: 0xF.                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 0x0005  | [7:0] | Clock part serial ID, Bits[11:4] | The Analog Devices unified SPI protocol reserves this read only register location as the upper eight bits of the clock part serial ID that (along with Register 0x0004) uniquely identifies the <a href="#">AD9554-1</a> within the Analog Devices clock chip family. No other Analog Devices chip that adheres to the Analog Devices unified SPI have these values for Register 0x0003, Register 0x0004, and Register 0x0005. Default: 0x00. |
| 0x0006  | [7:0] | Part version, Bits[7:0]          | The Analog Devices unified SPI protocol reserves this read only register location for identifying the die revision. Default: 0x05.                                                                                                                                                                                                                                                                                                            |

**SPI VERSION (REGISTER 0x000B)**

Table 35. SPI Version

| Address | Bits  | Bit Name               | Description                                                                                                                                               |
|---------|-------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x000B  | [7:0] | SPI version, Bits[7:0] | The Analog Devices unified SPI protocol reserves this read only register location for identifying the version of the unified SPI protocol. Default: 0x00. |

**VENDOR ID (REGISTER 0x000C TO REGISTER 0x000D)**

Table 36. Vendor ID

| Address | Bits  | Bit Name              | Description                                                                                                                                                                                                                                                                         |
|---------|-------|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x000C  | [7:0] | Vendor ID, Bits[7:0]  | The Analog Devices unified SPI protocol reserves this read only register location for identifying Analog Devices as the chip vendor of this device. All Analog Devices parts adhering to the unified serial port specification have the same value in this register. Default: 0x56. |
| 0x000D  | [7:0] | Vendor ID, Bits[15:8] | The Analog Devices unified SPI protocol reserves this read-only register location for identifying Analog Devices as the chip vendor of this part. All Analog Devices parts adhering to the unified serial port specification have the same value in this register. Default: 0x04.   |

**IO\_UPDATE (REGISTER 0x000F)**

Table 37. IO\_UPDATE

| Address | Bits  | Bit Name  | Description                                                                                                                                                          |
|---------|-------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x000F  | [7:1] | Reserved  | Reserved. Default: 0000000b                                                                                                                                          |
|         | 0     | IO_UPDATE | Writing a 1 to this bit transfers the data in the serial input/output buffer registers to the internal control registers of the device. This is an autoclearing bit. |

**GENERAL CONFIGURATION (REGISTER 0x0100 TO REGISTER 0x010E)****Multifunction Pin Control (M0 to M3 and M5 to M7) and Watchdog Timer**

Note that there is no M4 pin for this device.

Table 38. Multifunction Pins (M0 to M3 and M5 to M7) Control

| Address | Bits  | Bit Name                  | Description                                                                                                                                                                                                       |
|---------|-------|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0100  | [7:6] | M3 driver mode, Bits[1:0] | 00 (default) = active high CMOS.<br>01 = active low CMOS.<br>10 = open-drain PMOS (requires an external pull-down resistor).<br>11 = open-drain NMOS (requires an external pull-up resistor).                     |
|         | [5:4] | M2 driver mode, Bits[1:0] | The settings of these bits are identical to Register 0x0100, Bits[7:6].                                                                                                                                           |
|         | [3:2] | M1 driver mode, Bits[1:0] | The settings of these bits are identical to Register 0x0100, Bits[7:6].                                                                                                                                           |
|         | [1:0] | M0 driver mode, Bits[1:0] | The settings of these bits are identical to Register 0x0100, Bits[7:6].                                                                                                                                           |
| 0x0101  | [7:6] | M7 driver mode, Bits[1:0] | The settings of these bits are identical to Register 0x0100, Bits[7:6].                                                                                                                                           |
|         | [5:4] | M6 driver mode, Bits[1:0] | The settings of these bits are identical to Register 0x0100, Bits[7:6].                                                                                                                                           |
|         | [3:2] | M5 driver mode, Bits[1:0] | The settings of these bits are identical to Register 0x0100, Bits[7:6].                                                                                                                                           |
|         | [1:0] | Reserved                  | Default: 00b.                                                                                                                                                                                                     |
| 0x0102  | [7:0] | Reserved                  | Default: 0x00.                                                                                                                                                                                                    |
| 0x0103  | 7     | M0 output/input           | Input/output control for M0 pin.<br>0 (default) = input (control pin).<br>1 = output (status pin).                                                                                                                |
|         | [6:0] | M0 function, Bits[6:0]    | These bits control the function of the M0 pin. See Table 123 and Table 124 for details about the input and output functions that are available. Default: 0x00 = high impedance control pin, no function assigned. |
| 0x0104  | 7     | M1 output/input           | Input/output control for M1 pin (same as for the M0 pin, Register 0x0103, Bit 7).                                                                                                                                 |
|         | [6:0] | M1 function, Bits[6:0]    | These bits control the function of the M1 pin and are the same as Register 0x0103, Bits[6:0]. Default: 0x00 = high impedance control pin, no function assigned.                                                   |

| Address | Bits  | Bit Name               | Description                                                                                                                                                                                                      |
|---------|-------|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0105  | 7     | M2 output/input        | Input/output control for M2 pin (same as for the M0 pin, Register 0x0103, Bit 7).                                                                                                                                |
|         | [6:0] | M2 function, Bits[6:0] | These bits control the function of the M2 pin and are the same as Register 0x0103, Bits[6:0]. Default: 0x00 = high impedance control pin, no function assigned.                                                  |
| 0x0106  | 7     | M3 output/input        | Input/output control for M3 pin (same as for the M0 pin, Register 0x0103, Bit 7).                                                                                                                                |
|         | [6:0] | M3 function, Bits[6:0] | These bits control the function of the M3 pin and are the same as Register 0x0103, Bits[6:0]. Default: 0x00 = high impedance control pin, no function assigned.                                                  |
| 0x0107  | [7:0] | Reserved               | Default: 0x00.                                                                                                                                                                                                   |
| 0x0108  | 7     | M5 output/input        | Input/output control for M5 pin (same as for the M0 pin, Register 0x0103, Bit 7).                                                                                                                                |
|         | [6:0] | M5 function, Bits[6:0] | These bits control the function of the M5 pin and are the same as Register 0x0103, Bits[6:0]. Default: 0x00 = high impedance control pin, no function assigned.                                                  |
| 0x0109  | 7     | M6 output/input        | Input/output control for M6 pin (same as for the M0 pin, Register 0x0103, Bit 7).                                                                                                                                |
|         | [6:0] | M6 function, Bits[6:0] | These bits control the function of the M6 pin and are the same as Register 0x0103, Bits[6:0]. Default: 0x00 = high impedance control pin, no function assigned.                                                  |
| 0x010A  | 7     | M7 output/input        | Input/output control for M7 pin (same as for the M0 pin, Register 0x0103, Bit 7).                                                                                                                                |
|         | [6:0] | M7 function, Bits[6:0] | These bits control the function of the M7 pin and are the same as Register 0x0103, Bits[6:0]. Default: 0x00 = high impedance control pin, no function assigned.                                                  |
| 0x010B  | [7:0] | Reserved               | Default: 0x00.                                                                                                                                                                                                   |
| 0x010C  | [7:0] | Reserved               | Default: 0x00.                                                                                                                                                                                                   |
| 0x010D  | [7:0] | Watchdog timer         | Watchdog timer, Bits[7:0]. The watchdog timer stops when this register is written and restarts on the next IO_UPDATE (Register 0x000F = 0x01). Default: 0x00 (0x0000 = disabled). The units are in milliseconds. |
| 0x010E  | [7:0] |                        | Watchdog timer, Bits[15:8]. The watchdog timer stops when this register is written and restarts on the next IO_UPDATE (Register 0x000F = 0x01). Default: 0x00.                                                   |

### IRQ MASK (REGISTER 0x010F TO REGISTER 0x011F)

The IRQ mask register bits form a one-to-one correspondence with the bits of the IRQ monitor register (0x0D08 to 0x0D16). When set to Logic 1, the IRQ mask bits enable the corresponding IRQ monitor bits to indicate an IRQ event. The default for all IRQ mask bits is Logic 0, which prevents the IRQ monitor from detecting any internal interrupts.

**Table 39. IRQ Mask for SYSCLK and Watchdog Timer**

| Address | Bits  | Bit Name                   | Description                                                                     |
|---------|-------|----------------------------|---------------------------------------------------------------------------------|
| 0x010F  | 7     | SYSCLK unlocked            | Enables IRQ to indicate that the system clock has gone from locked to unlocked. |
|         | 6     | SYSCLK stable              | Enables IRQ to indicate that the system clock has gone from unstable to stable. |
|         | 5     | SYSCLK locked              | Enables IRQ to indicate that the system clock has gone from unlocked to locked. |
|         | 4     | SYSCLK calibration ended   | Enables IRQ to indicate that the system clock calibration sequence has ended.   |
|         | 3     | SYSCLK calibration started | Enables IRQ to indicate that the system clock calibration sequence has started. |
|         | 2     | Watchdog timer             | Enables IRQ to indicate expiration of the watchdog timer.                       |
|         | [1:0] | Reserved                   | Default: 00b.                                                                   |

**Table 40. IRQ Mask for Reference Inputs**

| Address | Bits | Bit Name           | Description                                                             |
|---------|------|--------------------|-------------------------------------------------------------------------|
| 0x0110  | 7    | Reserved           | Reserved.                                                               |
|         | 6    | REFB validated     | Enables IRQ to indicate that REFB has been validated.                   |
|         | 5    | REFB fault cleared | Enables IRQ to indicate that REFB has been cleared of a previous fault. |
|         | 4    | REFB fault         | Enables IRQ to indicate that REFB has been faulted.                     |
|         | 3    | Reserved           | Reserved.                                                               |
|         | 2    | REFA validated     | Enables IRQ to indicate that REFA has been validated.                   |
|         | 1    | REFA fault cleared | Enables IRQ to indicate that REFA has been cleared of a previous fault. |
|         | 0    | REFA fault         | Enables IRQ to indicate that REFA has been faulted.                     |

| Address | Bits | Bit Name           | Description                                                             |
|---------|------|--------------------|-------------------------------------------------------------------------|
| 0x0111  | 7    | Reserved           | Reserved.                                                               |
|         | 6    | REFD validated     | Enables IRQ to indicate that REFD has been validated.                   |
|         | 5    | REFD fault cleared | Enables IRQ to indicate that REFD has been cleared of a previous fault. |
|         | 4    | REFD fault         | Enables IRQ to indicate that REFD has been faulted.                     |
|         | 3    | Reserved           | Reserved.                                                               |
|         | 2    | REFC validated     | Enables IRQ to indicate that REFC has been validated.                   |
|         | 1    | REFC fault cleared | Enables IRQ to indicate that REFC has been cleared of a previous fault. |
|         | 0    | REFC fault         | Enables IRQ to indicate that REFC has been faulted.                     |

Table 41. IRQ Mask for the Digital PLL0 (DPLL\_0)

| Address | Bits | Bit Name                    | Description                                                                                    |
|---------|------|-----------------------------|------------------------------------------------------------------------------------------------|
| 0x0112  | 7    | Frequency unclamped         | Enables IRQ to indicate that DPLL_0 has exited a frequency clamped state.                      |
|         | 6    | Frequency clamped           | Enables IRQ to indicate that DPLL_0 has entered a frequency clamped state.                     |
|         | 5    | Phase slew unlimited        | Enables IRQ to indicate that DPLL_0 has exited a phase slew limited state.                     |
|         | 4    | Phase slew limited          | Enables IRQ to indicate that DPLL_0 has entered a phase slew limited state.                    |
|         | 3    | Frequency unlocked          | Enables IRQ to indicate that DPLL_0 has lost frequency lock.                                   |
|         | 2    | Frequency locked            | Enables IRQ to indicate that DPLL_0 has acquired frequency lock.                               |
|         | 1    | Phase unlocked              | Enables IRQ to indicate that DPLL_0 has lost phase lock.                                       |
|         | 0    | Phase locked                | Enables IRQ to indicate that DPLL_0 has acquired phase lock.                                   |
| 0x0113  | 7    | Switching                   | Enables IRQ to indicate that DPLL_0 is switching to a new reference.                           |
|         | 6    | Free run                    | Enables IRQ to indicate that DPLL_0 has entered free run mode.                                 |
|         | 5    | Holdover                    | Enables IRQ to indicate that DPLL_0 has entered holdover mode.                                 |
|         | 4    | History updated             | Enables IRQ to indicate that DPLL_0 has updated its tuning word history.                       |
|         | 3    | REFD activated              | Enables IRQ to indicate that DPLL_0 has activated REFD.                                        |
|         | 2    | REFC activated              | Enables IRQ to indicate that DPLL_0 has activated REFC.                                        |
|         | 1    | REFB activated              | Enables IRQ to indicate that DPLL_0 has activated REFB.                                        |
|         | 0    | REFA activated              | Enables IRQ to indicate that DPLL_0 has activated REFA.                                        |
| 0x0114  | 7    | Phase step detection        | Enables IRQ to indicate that DPLL_0 has detected a large phase step at the reference input.    |
|         | 6    | Demap control unclamped     | Enables IRQ to indicate that the DPLL_0 demapping controller tuning word has become unclamped. |
|         | 5    | Demap control clamped       | Enables IRQ to indicate that the DPLL_0 demapping controller tuning word has become clamped.   |
|         | 4    | Sync clock distribution     | Enables IRQ for indicating a distribution sync event.                                          |
|         | 3    | APLL_0 unlocked             | Enables IRQ for APLL_0 unlocked.                                                               |
|         | 2    | APLL_0 locked               | Enables IRQ for APLL_0 locked.                                                                 |
|         | 1    | APLL_0 calibration complete | Enables IRQ for APLL_0 calibration complete.                                                   |
|         | 0    | APLL_0 calibration started  | Enables IRQ for APLL_0 calibration started.                                                    |

Table 42. IRQ Mask for the Digital PLL1 (DPLL\_1)

| Address | Bits  | Bit Name     | Description                                                                                                                                                |
|---------|-------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0115  | [7:0] | See Table 41 | IRQ mask for DPLL_1, same as IRQ mask for the digital PLL0 (DPLL_0) registers (Register 0x0112 through Register 0x0114). All default values are identical. |
| 0x0116  | [7:0] | See Table 41 |                                                                                                                                                            |
| 0x0117  | [7:0] | See Table 41 |                                                                                                                                                            |

Table 43. IRQ Mask for the Digital PLL2 (DPLL\_2)

| Address | Bits  | Bit Name     | Description                                                                                                                                                |
|---------|-------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0118  | [7:0] | See Table 41 | IRQ mask for DPLL_2, same as IRQ mask for the digital PLL0 (DPLL_0) registers (Register 0x0112 through Register 0x0114). All default values are identical. |
| 0x0119  | [7:0] | See Table 41 |                                                                                                                                                            |
| 0x011A  | [7:0] | See Table 41 |                                                                                                                                                            |

Table 44. IRQ Mask for the Digital PLL3 (DPLL\_3)

| Address | Bits  | Bit Name     | Description                                                                                                                                                |
|---------|-------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x011B  | [7:0] | See Table 41 | IRQ mask for DPLL_3, same as IRQ mask for the digital PLL0 (DPLL_0) registers (Register 0x0112 through Register 0x0114). All default values are identical. |
| 0x011C  | [7:0] | See Table 41 |                                                                                                                                                            |
| 0x011D  | [7:0] | See Table 41 |                                                                                                                                                            |

Table 45. Pad Control for Mx Pins

| Address | Bits  | Bit Name          | Description                                                                                                                              |
|---------|-------|-------------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 0x011E  | 7     | M7 configuration  | M7 pin output drive strength.<br>0 (default) = high (approximately 6 mA) drive strength.<br>1 = low (approximately 3 mA) drive strength. |
|         | 6     | M6 configuration  | Same as Bit 7 of this register, except that it applies to the M6 pin.                                                                    |
|         | 5     | M5 configuration  | Same as Bit 7 of this register, except that it applies to the M5 pin.                                                                    |
|         | 4     | Reserved          | Default: 0b.                                                                                                                             |
|         | 3     | M3 configuration  | Same as Bit 7 of this register, except that it applies to the M3 pin.                                                                    |
|         | 2     | M2 configuration  | Same as Bit 7 of this register, except that it applies to the M2 pin.                                                                    |
|         | 1     | M1 configuration  | Same as Bit 7 of this register, except that it applies to the M1 pin.                                                                    |
|         | 0     | M0 configuration  | Same as Bit 7 of this register, except that it applies to the M0 pin.                                                                    |
| 0x011F  | [7:3] | Reserved          | Default: 00000b.                                                                                                                         |
|         | 2     | SPI configuration | Same as Bit 7 of Register 0x011E, except that it applies to the SDIO pin.                                                                |
|         | [1:0] | Reserved          | Default: 00b.                                                                                                                            |

**SYSTEM CLOCK (REGISTER 0x0200 TO REGISTER 0x0208)**

Table 46. System Clock PLL Feedback Divider (K Divider) and Configuration

| Address | Bits  | Bit Name                          | Description                                                                    |
|---------|-------|-----------------------------------|--------------------------------------------------------------------------------|
| 0x0200  | [7:0] | System clock K divider, Bits[7:0] | System clock PLL feedback divider value = $4 \leq K \leq 255$ . Default: 0x00. |

Table 47. SYSCLK Configuration

| Address | Bits  | Bit Name                           | Description                                                                                                                                                                                                                                                          |
|---------|-------|------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0201  | [7:4] | Reserved                           | Reserved.                                                                                                                                                                                                                                                            |
|         | 3     | SYSCLK XTAL enable                 | Enables the crystal maintaining amplifier for the system clock input.<br>1 (default) = crystal mode (crystal maintaining amplifier enabled).<br>0 = external crystal oscillator or other system clock source.                                                        |
|         | [2:1] | SYSCLK J1 divider, Bits[1:0]       | System clock input divider.<br>00 (default): $\div 1$ .<br>01: $\div 2$ .<br>10: $\div 4$ .<br>11: $\div 8$ .                                                                                                                                                        |
|         | 0     | SYSCLK doubler enable (J0 divider) | Enables the clock doubler on the system clock input to reduce noise. Setting this bit may prevent the SYSCLK PLL from locking if the input duty cycle is not close enough to 50%. See Table 4 for the limits on duty cycle.<br>0 (default) = disable.<br>1 = enable. |



Table 48. System Clock Reference Frequency

| Address | Bits  | Bit Name                                           | Description                                                   |
|---------|-------|----------------------------------------------------|---------------------------------------------------------------|
| 0x0202  | [7:0] | System clock reference frequency (Hz), Bits[23:0]  | System clock reference frequency, Bits[7:0]. Default: 0x00.   |
| 0x0203  | [7:0] |                                                    | System clock reference frequency, Bits[15:8]. Default: 0x00.  |
| 0x0204  | [7:0] |                                                    | System clock reference frequency, Bits[23:16]. Default: 0x00. |
| 0x0205  | [7:4] | Reserved                                           | Default: 0x0.                                                 |
|         | [3:0] | System clock reference frequency (Hz), Bits[27:24] | System clock reference frequency, Bits[27:24]. Default: 0x0.  |

Table 49. System Clock Stability Period

| Address | Bits  | Bit Name                                        | Description                                                                                                                                                                                                                                                                                                                                                                               |
|---------|-------|-------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0206  | [7:0] | System clock stability period (ms), Bits[15:0]  | System clock period, Bits[7:0]. The system clock stability period is the amount of time that the system clock PLL must be locked before it is declared stable. The system clock stability period is reset automatically if the user writes to this register. The system clock stability period restarts on the next IO_UPDATE (Register 0x000F = 0x01). Default: 0x32 (0x000032 = 50 ms). |
| 0x0207  | [7:0] |                                                 | System clock period, Bits[15:8]. The system clock stability period is reset automatically if the user writes to this register. The system clock stability timer restarts on the next IO_UPDATE (Register 0x000F = 0x01). Default: 0x00.                                                                                                                                                   |
| 0x0208  | [7:4] | Reserved                                        | Default: 0x0.                                                                                                                                                                                                                                                                                                                                                                             |
|         | [3:0] | System clock stability period (ms), Bits[19:16] | System clock period, Bits[19:16]. The system clock stability period is reset automatically if the user writes to this register. The system clock stability period restarts on the next IO_UPDATE (Register 0x000F = 0x01). Default: 0x0. The units are in milliseconds.                                                                                                                   |

## REFERENCE INPUT A (REGISTER 0x0300 TO REGISTER 0x031E)

Table 50. REFA Logic Type

| Address | Bits  | Bit Name                   | Description                                                                                                                                                                                                                                        |
|---------|-------|----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0300  | [7:2] | Reserved                   | Default: 000000b.                                                                                                                                                                                                                                  |
|         | [1:0] | REFA logic type, Bits[1:0] | Selects logic family for REFA input receiver; only the REFA pin is used in CMOS mode.<br>00b (default) = 1.8 V or 1.5 V single-ended CMOS.<br>01b = ac-coupled differential.<br>10b = dc-coupled LVDS ( $f_{IN} \leq 10.24$ MHz).<br>11b = unused. |

Table 51. REFA R Divider (20 Bits) DPLL

| Address | Bits  | Bit Name               | Description                                                                                                          |
|---------|-------|------------------------|----------------------------------------------------------------------------------------------------------------------|
| 0x0301  | [7:0] | R divider, Bits[15:0]  | DPLL integer reference divider (minus 1), Bits[7:0]. Default: 0x00. (For example, 0x00000 equals an R divider of 1.) |
| 0x0302  | [7:0] |                        | DPLL integer reference divider (minus 1), Bits[15:8]. Default: 0x00.                                                 |
| 0x0303  | [7:4] | Reserved               | Default: 0x0.                                                                                                        |
|         | [3:0] | R divider, Bits[19:16] | DPLL integer reference divider (minus 1), Bits[19:16]. Default: 0x0.                                                 |

Table 52. Nominal Period of REFA Input Clock

| Address | Bits  | Bit Name                     | Description                                           |
|---------|-------|------------------------------|-------------------------------------------------------|
| 0x0304  | [7:0] | REFA period (fs), Bits[39:0] | Nominal reference period, Bits[7:0]. Default: 0x00.   |
| 0x0305  | [7:0] |                              | Nominal reference period, Bits[15:8]. Default: 0x00.  |
| 0x0306  | [7:0] |                              | Nominal reference period, Bits[23:16]. Default: 0x00. |
| 0x0307  | [7:0] |                              | Nominal reference period, Bits[31:24]. Default: 0x00. |
| 0x0308  | [7:0] |                              | Nominal reference period, Bits[39:32]. Default: 0x00. |

Table 53. REFA Frequency Tolerance

| Address | Bits  | Bit Name                                     | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|---------|-------|----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0309  | [7:0] | Inner tolerance (1/(ppm error)), Bits[15:0]  | Input reference frequency monitor inner tolerance, Bits[7:0]. Default: 0x14.                                                                                                                                                                                                                                                                                                                                     |
| 0x030A  | [7:0] |                                              | Input reference frequency monitor inner tolerance, Bits[15:8]. Default: 0x00.                                                                                                                                                                                                                                                                                                                                    |
| 0x030B  | [7:4] | Reserved                                     | Default: 0x0.                                                                                                                                                                                                                                                                                                                                                                                                    |
|         | [3:0] | Inner tolerance (1/(ppm error)), Bits[19:16] | Input reference frequency monitor inner tolerance, Bits[19:16]. Default for Register 0x0309 to Register 0x30B: 0x000014 = 20 (5% or 50,000 ppm). The Stratum 3 clock requires an inner tolerance of $\pm 9.2$ ppm and an outer tolerance of $\pm 12$ ppm. An SMC clock requires an outer tolerance of $\pm 48$ ppm. The allowable range for the inner tolerance is 0x00A (10%) to 0x8FF (2 ppm).                 |
| 0x030C  | [7:0] | Outer tolerance (1/(ppm error)), Bits[15:0]  | Input reference frequency monitor outer tolerance, Bits[7:0]. Default: 0x0A.                                                                                                                                                                                                                                                                                                                                     |
| 0x030D  | [7:0] |                                              | Input reference frequency monitor outer tolerance, Bits[15:8]. Default: 0x00.                                                                                                                                                                                                                                                                                                                                    |
| 0x030E  | [7:4] | Reserved                                     | Default: 0x0.                                                                                                                                                                                                                                                                                                                                                                                                    |
|         | [3:0] | Outer tolerance (1/(ppm error)), Bits[19:16] | Input reference frequency monitor outer tolerance, Bits[19:16]. Default for Register 0x030C to Register 0x30E = 0x00000A = 10 (10% or 100,000 ppm). The Stratum 3 clock requires an inner tolerance of $\pm 9.2$ ppm and an outer tolerance of $\pm 12$ ppm. An SMC clock requires an outer tolerance of $\pm 48$ ppm. The outer tolerance must be greater than the inner tolerance so that there is hysteresis. |

Table 54. REFA Validation Timer

| Address | Bits  | Bit Name                                           | Description                                                                                                                                                                            |
|---------|-------|----------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x030F  | [7:0] | Validation timer (ms), Bits[15:0] (up to 65.5 sec) | Validation timer, Bits[7:0]. Default: 0x0A. This is the amount of time a reference input must be unfaulted before it is declared valid by the reference input monitor. Default: 10 ms. |
| 0x0310  | [7:0] |                                                    | Validation timer, Bits[15:8]. Default: 0x00.                                                                                                                                           |

Table 55. REFA Phase/Frequency Lock Detectors

| Address | Bits  | Bit Name                                  | Description                                                                                                                   |
|---------|-------|-------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| 0x0311  | [7:0] | Phase lock threshold (ps), Bits[23:0]     | Phase lock threshold, Bits[7:0]. Default: 0xBC. Default of 0x0002BC for Register 0x0311 through Register 0x313 = 700 ps.      |
| 0x0312  | [7:0] |                                           | Phase lock threshold, Bits[15:8]. Default: 0x02.                                                                              |
| 0x0313  | [7:0] |                                           | Phase lock threshold, Bits[23:16]. Default: 0x00.                                                                             |
| 0x0314  | [7:0] | Phase lock fill rate, Bits[7:0]           | Phase lock fill rate, Bits[7:0]. Default: 0x0A = 10 code/PFD cycle.                                                           |
| 0x0315  | [7:0] | Phase lock drain rate, Bits[7:0]          | Phase lock drain rate, Bits[7:0]. Default: 0x0A = 10 code/PFD cycle.                                                          |
| 0x0316  | [7:0] | Frequency lock threshold (ps), Bits[23:0] | Frequency lock threshold, Bits[7:0]. Default: 0xBC. Default of 0x0002BC for Register 0x0316 through Register 0x0318 = 700 ps. |
| 0x0317  | [7:0] |                                           | Frequency lock threshold, Bits[15:8]. Default: 0x02.                                                                          |
| 0x0318  | [7:0] |                                           | Frequency lock threshold, Bits[23:16]. Default: 0x00.                                                                         |
| 0x0319  | [7:0] | Frequency lock fill rate, Bits[7:0]       | Frequency lock fill rate, Bits[7:0]. Default: 0x0A = 10 code/PFD cycle.                                                       |
| 0x031A  | [7:0] | Frequency lock drain rate, Bits[7:0]      | Frequency lock drain rate, Bits[7:0]. Default: 0x0A = 10 code/PFD cycle.                                                      |

Table 56. REFA Phase Step Threshold

| Address | Bits  | Bit Name                               | Description                                                                                                                       |
|---------|-------|----------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 0x031B  | [7:0] | Phase step threshold (ps), Bits[23:0]  | Phase step threshold, Bits[7:0]. Default: 0x00. Note that a phase step threshold of 0x000000 means that this feature is disabled. |
| 0x031C  | [7:0] |                                        | Phase step threshold, Bits[15:8]. Default: 0x00.                                                                                  |
| 0x031D  | [7:0] |                                        | Phase step threshold, Bits[23:16]. Default: 0x00.                                                                                 |
| 0x031E  | [7:4] | Reserved                               | Default: 0x0.                                                                                                                     |
|         | [3:0] | Phase step threshold (ps), Bits[27:24] | Phase step threshold, Bits[27:24].                                                                                                |

**REFERENCE INPUT B (REGISTER 0x0320 TO REGISTER 0x033E)**

These registers mimic the Reference Input A registers (Register 0x0300 through Register 0x031E) but the register addresses are offset by 0x0020. All default values are identical.

**REFERENCE INPUT C (REGISTER 0x0340 TO REGISTER 0x035E)**

These registers mimic the Reference Input A registers (Register 0x0300 through Register 0x031E) but the register addresses are offset by 0x0040. All default values are identical.

**REFERENCE INPUT D (REGISTER 0x0360 TO REGISTER 0x037E)**

These registers mimic the Reference Input A registers (Register 0x0300 through Register 0x031E) but the register addresses are offset by 0x0060. All default values are identical.

**DPLL\_0 CONTROLS (REGISTER 0x0400 TO REGISTER 0x041E)****Table 57. DPLL\_0 Free Run Frequency Tuning Word**

| Address | Bits  | Bit Name                                                 | Description                                                     |
|---------|-------|----------------------------------------------------------|-----------------------------------------------------------------|
| 0x0400  | [7:0] | 30-bit free running frequency tuning word<br>Bits[23:0]  | Free running frequency tuning word, Bits[7:0]. Default: 0x00.   |
| 0x0401  | [7:0] |                                                          | Free running frequency tuning word, Bits[15:8]. Default: 0x00.  |
| 0x0402  | [7:0] |                                                          | Free running frequency tuning word, Bits[23:16]. Default: 0x00. |
| 0x0403  | [7:6] | Reserved                                                 | Default: 00b.                                                   |
|         | [5:0] | 30-bit free running frequency tuning word<br>Bits[29:24] | Free running frequency tuning word, Bits[29:24]. Default: 0x00. |

**Table 58. DPLL\_0 DCO Integer**

| Address | Bits  | Bit Name                  | Description                                                                                                                                                                                                                           |
|---------|-------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0404  | [7:4] | Reserved                  | This register is used internally. It is usually 0x1 but may differ depending on how the device is configured. When writing to this register, read the current value and write the same value back to this register.                   |
|         | [3:0] | DCO integer,<br>Bits[3:0] | This register contains the integer part of the DCO frequency divider. Valid values are 0x7 to 0xD, and the <a href="#">AD9554-1</a> evaluation software frequency planning wizard can help determine the optimal value. Default: 0x7. |

**Table 59. DPLL\_0 Frequency Clamp**

| Address | Bits  | Bit Name                                     | Description                                                                                                                                                             |
|---------|-------|----------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0405  | [7:0] | Lower limit of pull-in range,<br>Bits[15:0]  | Lower limit pull-in range, Bits[7:0]. The value in these registers is the 20 most significant bits of the lowest allowable tuning word used by the DPLL. Default: 0xCC. |
| 0x0406  | [7:0] |                                              | Lower limit pull-in range, Bits[15:8]. Default: 0xCC.                                                                                                                   |
| 0x0407  | [7:4] | Reserved                                     | Default: 0x0.                                                                                                                                                           |
|         | [3:0] | Lower limit of pull-in range,<br>Bits[19:16] | Lower limit pull-in range, Bits[19:16]. Default: 0x0.                                                                                                                   |
| 0x0408  | [7:0] | Upper limit of pull-in range,<br>Bits[15:0]  | Upper limit pull-in range, Bits[7:0]. Default: 0x33.                                                                                                                    |
| 0x0409  | [7:0] | Upper limit of pull-in range,<br>Bits[15:0]  | Upper limit pull-in range, Bits[15:8]. Default: 0x33.                                                                                                                   |
| 0x040A  | [7:4] | Reserved                                     | Default: 0x0.                                                                                                                                                           |
|         | [3:0] | Upper limit of pull-in range,<br>Bits[19:16] | Upper limit pull-in range, Bits[19:16]. Default: 0xF.                                                                                                                   |

**Table 60. DPLL\_0 Holdover History**

| Address | Bits  | Bit Name                                                 | Description                                                                                                                                                                                                                                                                                                                 |
|---------|-------|----------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x040B  | [7:0] | DPLL_0 history<br>accumulation timer (ms),<br>Bits[15:0] | History accumulation timer, Bits[7:0]. Default: 0x0A. For Register 0x040B and Register 0x040C, 0x000A = 10 ms. Maximum: 65 sec. This register controls the amount of tuning word averaging used to determine the tuning word used in holdover. Behavior is undefined for a timer value of 0. Default value: 0x000A = 10 ms. |
| 0x040C  | [7:0] |                                                          | History accumulation timer, Bits[15:8]. Default: 0x00.                                                                                                                                                                                                                                                                      |

Table 61. DPLL\_0 History Mode

| Address | Bits  | Bit Name                       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|---------|-------|--------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x040D  | [7:5] | Reserved                       | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|         | 4     | Single sample fallback         | Controls holdover history. If tuning word history is not available for the reference that was active just prior to holdover, then the following:<br>0 (default) = uses the free running frequency tuning word register value.<br>1 = uses the last tuning word from the DPLL.                                                                                                                                                                                                                                                                              |
|         | 3     | Persistent history             | Controls holdover history initialization. When switching to a new reference:<br>0 (default) = clears the tuning word history.<br>1 = retains the previous tuning word history.                                                                                                                                                                                                                                                                                                                                                                             |
|         | [2:0] | Incremental average, Bits[2:0] | History mode value from 0 to 7. Default: 0. When set to nonzero, causes the first history accumulation to update prior to the first complete averaging period. After the first full interval, updates occur only at the full period.<br>0 (default) = update only after the full interval has elapsed.<br>1 = update at 1/2 the full interval.<br>2 = update at 1/4 and 1/2 of the full interval.<br>3 = update at 1/8, 1/4, and 1/2 of the full interval.<br>...<br>7 = update at 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, and 1/2 of the full interval. |

Table 62. DPLL\_0 Fixed Closed Loop Phase Offset

| Address | Bits  | Bit Name                                     | Description                                     |
|---------|-------|----------------------------------------------|-------------------------------------------------|
| 0x040E  | [7:0] | Fixed phase offset (signed; ps), Bits[23:0]  | Fixed phase offset, Bits[7:0]. Default: 0x00.   |
| 0x040F  | [7:0] |                                              | Fixed phase offset, Bits[15:8]. Default: 0x00.  |
| 0x0410  | [7:0] |                                              | Fixed phase offset, Bits[23:16]. Default: 0x00. |
| 0x0411  | [7:6] | Reserved                                     | Reserved; default: 0x0.                         |
|         | [5:0] | Fixed phase offset (signed; ps), Bits[29:24] | Fixed phase offset, Bits[29:24]. Default: 0x00. |

Table 63. DPLL\_0 Incremental Closed-Loop Phase Offset Step Size

| Address | Bits  | Bit Name                                            | Description                                                                                                                                                                                                                                    |
|---------|-------|-----------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0412  | [7:0] | Incremental phase offset step size (ps), Bits[15:0] | Incremental phase offset step size, Bits[7:0]. Default: 0x00. This register controls the static phase offset step size of the DPLL while it is locked. See Register 0x0A24 for the bits that increment, decrement, and reset the phase offset. |
| 0x0413  | [7:0] |                                                     | Incremental phase offset step size, Bits[15:8]. Default: 0x00. This register controls the static phase offset step size of the DPLL while it is locked.                                                                                        |

Table 64. DPLL\_0 Phase Slew Rate Limit

| Address | Bits  | Bit Name                                                       | Description                                                                                                                                                                                                                                                                                                           |
|---------|-------|----------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0414  | [7:0] | Phase slew rate limit ( $\mu\text{s}/\text{sec}$ ), Bits[15:0] | Phase slew rate limit, Bits[7:0]. Default: 0x00. This register controls the maximum allowable phase slewing during phase adjustment. (The phase adjustment controls are in Register 0x040E to Register 0x0411.) Default phase slew rate limit: 0, or disabled. Minimum useful value is 100 $\mu\text{s}/\text{sec}$ . |
| 0x0415  | [7:0] |                                                                | Phase slew rate limit, Bits[15:8]. Default = 0x00.                                                                                                                                                                                                                                                                    |

Table 65. DPLL\_0 Demapping Control

| Address | Bits  | Bit Name                      | Description                                                                                                                          |
|---------|-------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 0x0416  | [7:1] | Reserved                      | Reserved, Bits[7:1] (default: 0x00)                                                                                                  |
|         | 0     | Enable demap controller       | Enables the demapping controller.<br>0 (default) = The demapping controller is disabled.<br>1 = The demapping controller is enabled. |
| 0x0417  | [7:0] | Sampled address, Bits[15:0]   | Sampled address, Bits[7:0]. Default: 0x00.                                                                                           |
| 0x0418  | [7:0] |                               | Sampled address, Bits[15:8]. Default: 0x00.                                                                                          |
| 0x0419  | [7:0] | Set point address, Bits[15:0] | Set point address, Bits[7:0]. Default: 0x00.                                                                                         |
| 0x041A  | [7:0] |                               | Set point address, Bits[15:8]. Default: 0x00.                                                                                        |
| 0x041B  | [7:0] |                               | Gain, Bits[7:0]. Default: 0x00.                                                                                                      |
| 0x041C  | [7:0] | Gain, Bits[23:0]              | Gain, Bits[15:8]. Default: 0x00.                                                                                                     |
| 0x041D  | [7:0] |                               | Gain, Bits[23:16]. Default: 0x00.                                                                                                    |
| 0x041E  | [7:0] | Clamp value, Bits[7:0]        | Clamp value, Bits[7:0]. Default: 0x00.                                                                                               |

**APLL\_0 CONFIGURATION (REGISTER 0x0430 TO REGISTER 0x0434)**Table 66. Output PLL\_0 (APLL\_0) Setting<sup>1</sup>

| Address       | Bits                               | Bit Name                                            | Description                                                                                                                                     |              |              |              |
|---------------|------------------------------------|-----------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|--------------|--------------|--------------|
| 0x0430        | 7                                  | Reserved                                            | Default: 0b.                                                                                                                                    |              |              |              |
|               | [6:0]                              | Output PLL0 (APLL_0) charge pump current, Bits[6:0] | LSB: 3.5 $\mu$ A. 0000001b = 1 $\times$ LSB; 0000010b = 2 $\times$ LSB; 1111111b = 127 $\times$ LSB.<br>Default: 0x2E = 451 $\mu$ A CP current. |              |              |              |
| 0x0431        | [7:0]                              | Output PLL0 (APLL_0) feedback M0 divider, Bits[7:0] | Division: 14 to 255. Default: 0x00.                                                                                                             |              |              |              |
| 0x0432        | [7:6]                              | APLL_0 loop filter control, Bits[7:0]               | Second-pole resistor ( $R_{P2}$ ). Default: 0x7F.                                                                                               |              |              |              |
|               |                                    |                                                     | <b><math>R_{P2}</math> (<math>\Omega</math>)</b>                                                                                                | <b>Bit 7</b> | <b>Bit 6</b> |              |
|               |                                    |                                                     | 500                                                                                                                                             | 0            | 0            |              |
|               |                                    |                                                     | 333 (default)                                                                                                                                   | 0            | 1            |              |
|               |                                    |                                                     | 250                                                                                                                                             | 1            | 0            |              |
|               | 200                                | 1                                                   | 1                                                                                                                                               |              |              |              |
|               | [5:3]                              | Zero resistor ( $R_{ZERO}$ ).                       | <b><math>R_{ZERO}</math> (<math>\Omega</math>)</b>                                                                                              | <b>Bit 5</b> | <b>Bit 4</b> | <b>Bit 3</b> |
|               |                                    |                                                     | 1500                                                                                                                                            | 0            | 0            | 0            |
|               |                                    |                                                     | 1250                                                                                                                                            | 0            | 0            | 1            |
|               |                                    |                                                     | 1000                                                                                                                                            | 0            | 1            | 0            |
|               |                                    |                                                     | 930                                                                                                                                             | 0            | 1            | 1            |
|               |                                    |                                                     | 1250                                                                                                                                            | 1            | 0            | 0            |
|               |                                    |                                                     | 1000                                                                                                                                            | 1            | 0            | 1            |
|               |                                    |                                                     | 750                                                                                                                                             | 1            | 1            | 0            |
| 680 (default) |                                    |                                                     | 1                                                                                                                                               | 1            | 1            |              |
| [2:0]         | First-pole capacitor ( $C_{P1}$ ). | <b><math>C_{P1}</math> (pF)</b>                     | <b>Bit 2</b>                                                                                                                                    | <b>Bit 1</b> | <b>Bit 0</b> |              |
|               |                                    | 10                                                  | 0                                                                                                                                               | 0            | 0            |              |
|               |                                    | 30                                                  | 0                                                                                                                                               | 0            | 1            |              |
|               |                                    | 40                                                  | 0                                                                                                                                               | 1            | 0            |              |
|               |                                    | 70                                                  | 0                                                                                                                                               | 1            | 1            |              |
|               |                                    | 90                                                  | 1                                                                                                                                               | 0            | 0            |              |
|               |                                    | 110                                                 | 1                                                                                                                                               | 0            | 1            |              |
|               |                                    | 130                                                 | 1                                                                                                                                               | 1            | 0            |              |
|               |                                    | 150 (default)                                       | 1                                                                                                                                               | 1            | 1            |              |

| Address | Bits  | Bit Name                          | Description                                                                                                                                                                                                                                                                                           |
|---------|-------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0433  | [7:2] | Reserved                          | Default: 0x00.                                                                                                                                                                                                                                                                                        |
|         | 1     | P0 divider reset                  | 0 (default) = normal operation for the P0 divider.<br>1 = P0 divider held in reset.                                                                                                                                                                                                                   |
|         | 0     | APLL_0 loop filter control, Bit 8 | Bypass internal R <sub>ZERO</sub> .<br><br>0 (default) = use the internal R <sub>ZERO</sub> resistor.<br>1 = bypass the internal R <sub>ZERO</sub> resistor (makes R <sub>ZERO</sub> = 0 Ω and requires the use of an external zero resistor in addition to the capacitor to ground on the LF_0 pin). |

<sup>1</sup> Note that the default APLL loop bandwidth is 240 kHz.

## OUTPUT PLL\_0 (APLL\_0) SYNC AND CLOCK DISTRIBUTION (REGISTER 0x0434 TO REGISTER 0x043E)

Table 67. P0 Divider Settings

| Address | Bits  | Bit Name                           | Description                                                                                                                                                                                                                              |
|---------|-------|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0434  | [7:4] | Reserved                           | Default: 0x0.                                                                                                                                                                                                                            |
|         | [3:0] | P0 divider divide ratio, Bits[3:0] | 0000b (default)/0001b: undefined.<br>0010b: ÷2. This setting is permitted only if the APLL VCO frequency is ≤2500 MHz.<br>0011b: ÷3.<br>0101b: ÷5.<br>0110b: ÷6.<br>0111b: ÷7.<br>1000b: ÷8.<br>1001b: ÷9.<br>1010b: ÷10.<br>1011b: ÷11. |

Table 68. Distribution Output Synchronization Settings (OUT0)

| Address | Bits  | Bit Name                       | Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---------|-------|--------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0435  | [7:3] | Reserved                       | Default: 0x00.                                                                                                                                                                                                                                                                                                                                                                                                                           |
|         | 2     | Sync source selection          | Selects the sync source for the clock distribution output channels.<br>0 (default) = direct. The sync pulse is gated only by APLL calibration and lock.<br>1 = active reference. This mode is similar to direct mode except that the sync pulse occurs on the next edge of the actively selected reference.                                                                                                                              |
|         | [1:0] | Automatic sync mode, Bits[1:0] | Auto sync mode.<br>00 = (default) disabled.<br>01 = sync on DPLL frequency lock.<br>10 = sync on DPLL phase lock.<br>11 = reserved.                                                                                                                                                                                                                                                                                                      |
| 0x0436  | [7:3] | Reserved                       | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                |
|         | 2     | APLL_0 mask sync               | 0 (default) = the clock distribution SYNC function is delayed until the APLL has been calibrated and is locked. After APLL calibration and lock, the output clock distribution sync is armed, and the SYNC function for the clock outputs is under the control of Register 0x0435.<br>1 = overrides the lock detector state of the APLL; allows Register 0x0435 to control the output SYNC function, regardless of the APLL lock status. |
|         | 1     | Mask OUT0B sync                | Masks the synchronous reset to the OUT0B divider.<br>0 (default) = unmasked.<br>1 = masked. Setting this bit asynchronously releases the OUT0B divider from static sync state, thus allowing the OUT0B divider to toggle. OUT0B ignores all sync events while this bit is set. Setting this bit does not enable the output drivers connected to this channel.                                                                            |
|         | 0     | Reserved                       | Default: 0b.                                                                                                                                                                                                                                                                                                                                                                                                                             |

Table 69. Distribution OUT0B Settings

| Address | Bits  | Bit Name        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|---------|-------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x043B  | [7:3] | Reserved        | Reserved. Default: 0x00                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|         | [2:1] | OUT0B mode      | Selects the operating mode of OUT0B.<br>00 (default) = 14 mA (used for ac-coupled LVDS and dc-coupled HCSL).<br>01 = 21 mA (intended as an intermediate amplitude setting).<br>10 = 28 mA (used for ac-coupled LVPECL-compatible amplitudes with 100 $\Omega$ termination).<br>Note that damage to the output drivers can result if 28 mA mode is used without external termination resistors (either to ground or across the differential pair).<br>11 = power down and tristate outputs. |
|         | 0     | Invert polarity | Controls the OUT0B polarity.<br>0 (default) = normal polarity.<br>1 = inverted polarity.                                                                                                                                                                                                                                                                                                                                                                                                   |

Table 70. Q0\_B Divider Setting

| Address | Bits  | Bit Name                      | Description                                                                                                                                                                                                                                                      |
|---------|-------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x043C  | [7:0] | Q0_B divider, Bits[7:0]       | 10-bit channel divider, Bits[7:0] (LSB). Default: 0x00.<br>Division equals channel divider, Bits[9:0] + 1.<br>[9:0] = 0 is divide-by-1.<br>[9:0] = 1 is divide-by-2.<br>...<br>[9:0] = 1023 is divide-by-1024.                                                   |
| 0x043D  | [7:2] | Reserved                      | Default: 0x00.                                                                                                                                                                                                                                                   |
|         | [1:0] | Q0_B divider, Bits[9:8]       | 10-bit channel divider, Bits[9:8] (MSB).                                                                                                                                                                                                                         |
| 0x043E  | [7:6] | Reserved                      | Default: 0x0.                                                                                                                                                                                                                                                    |
|         | [5:0] | Q0_B divider phase, Bits[5:0] | Divider initial phase after sync relative to the divider input clock (from the P0 divider output).<br>LSB is $\frac{1}{2}$ of a period of the divider input clock. Default: 0x0.<br>Phase = 0 is no phase offset.<br>Phase = 1 is $\frac{1}{2}$ a period offset. |

**DPLL\_0 SETTINGS FOR REFERENCE INPUT A (REFA) (REGISTER 0x0440 TO REGISTER 0x044C)**

Table 71. DPLL\_0 REFA Priority Setting

| Address | Bits  | Bit Name      | Description                                                                                                                                                |
|---------|-------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0440  | [7:3] | Reserved      | Default: 00000b.                                                                                                                                           |
|         | [2:1] | REFA priority | These bits set the priority level (0 to 3) of REFA relative to the other input references.<br>00 (default) = 0 (highest).<br>01 = 1.<br>10 = 2.<br>11 = 3. |
|         | 0     | Enable REFA   | This bit enables DPLL_0 to lock to REFA.<br>0 (default) = REFA is not enabled for use by DPLL_0.<br>1 = REFA is enabled for use by DPLL_0.                 |

Table 72. DPLL\_0 REFA Loop Bandwidth Scaling Factor

| Address | Bits  | Bit Name                                                         | Description                                                                                                                                                                                                                                                                                                                                                                                               |
|---------|-------|------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0441  | [7:0] | Digital PLL_0 loop BW scaling factor, Bits[15:0] (unit of 0.1Hz) | Digital PLL loop bandwidth scaling factor, Bits[7:0]. Default: 0x0.                                                                                                                                                                                                                                                                                                                                       |
| 0x0442  | [7:0] | Digital PLL_0 loop BW scaling factor, Bits[15:0] (unit of 0.1Hz) | Digital PLL loop bandwidth scaling factor, Bits[15:8]. Default: 0x00. The default for Register 0x0441 to Register 0x0443 = 0x000000. The loop bandwidth must always be less than the DPLL phase detector frequency divided by 50. The DPLL may not lock reliably if the DPLL loop bandwidth is <50 Hz and a crystal is used for the system clock. See the Choosing the SYSCLK Source section for details. |
| 0x0443  | [7:2] | Reserved                                                         | Default: 0x00.                                                                                                                                                                                                                                                                                                                                                                                            |
|         | 1     | Base loop filter selection                                       | 0 = base loop filter with normal (70°) phase margin (default).<br>1 = base loop filter with high phase margin. (For loop bandwidth ≤ 2 kHz, there is ≤ 0.1 dB peaking in the closed-loop transfer function. Setting this bit is also recommended for loop bandwidths > 2 kHz.)                                                                                                                            |
|         | 0     | Digital PLL_0 loop BW scaling factor, Bit[16] (unit of 0.1 Hz)   | Digital PLL loop bandwidth scaling factor, Bit 16. Default: 0x0.                                                                                                                                                                                                                                                                                                                                          |

Table 73. DPLL\_0 REFA Integer Part of Feedback (N0) Divider

| Address | Bits  | Bit Name                                                    | Description                                                                                                                                                                         |
|---------|-------|-------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0444  | [7:0] | Digital PLL_0 feedback divider—Integer Part N0, Bits[15:0]  | DPLL integer feedback divider (minus 1), Bits[7:0]. Default: 0x00. (For example, an N0 divider value of one is achieved by writing 0x000000 to Register 0x0444 to Register 0x0446.) |
| 0x0445  | [7:0] |                                                             | DPLL integer feedback divider, Bits[15:8]. Default: 0x00.                                                                                                                           |
| 0x0446  | [7:2] | Reserved                                                    | Default: 0x00.                                                                                                                                                                      |
|         | [1:0] | Digital PLL_0 feedback divider—Integer Part N0, Bits[17:16] | DPLL integer feedback divider, Bits[17:16]. Default: 0b.<br><br>Default for Register 0x0444 to Register 0x0446: 0x000000.                                                           |

Table 74. DPLL\_0 REFA Fractional Part of Fractional Feedback Divider—FRAC0

| Address | Bits  | Bit Name                                                    | Description                                                                     |
|---------|-------|-------------------------------------------------------------|---------------------------------------------------------------------------------|
| 0x0447  | [7:0] | Digital PLL_0 fractional feedback divider—FRAC0, Bits[23:0] | The numerator of the fractional-N feedback divider, Bits[7:0]. Default: 0x00.   |
| 0x0448  | [7:0] |                                                             | The numerator of the fractional-N feedback divider, Bits[15:8]. Default: 0x00.  |
| 0x0449  | [7:0] |                                                             | The numerator of the fractional-N feedback divider, Bits[23:16]. Default: 0x00. |

Table 75. DPLL\_0 REFA Modulus of Fractional Feedback Divider—MOD0

| Address | Bits  | Bit Name                                                | Description                                                                                                                                            |
|---------|-------|---------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x044A  | [7:0] | Digital PLL_0 feedback divider modulus—MOD0, Bits[23:0] | The denominator of the fractional-N feedback divider, Bits[7:0]. Default: 0x00. Setting MOD0 to 0x000000 disables and bypasses the fractional divider. |
| 0x044B  | [7:0] |                                                         | The denominator of the fractional-N feedback divider, Bits[15:8]. Default: 0x00.                                                                       |
| 0x044C  | [7:0] |                                                         | The denominator of the fractional-N feedback divider, Bits[23:16]. Default: 0x00.                                                                      |



**DPLL\_0 SETTINGS FOR REFERENCE INPUT B (REFB) (REGISTER 0x044D TO REGISTER 0x0459)****Table 76. DPLL\_0 REFB Priority Setting**

| Address | Bits  | Bit Name                 | Description                                                                                                                                                |
|---------|-------|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x044D  | [7:3] | Reserved                 | Default: 0x00.                                                                                                                                             |
|         | [2:1] | REFB priority, Bits[1:0] | These bits set the priority level (0 to 3) of REFB relative to the other input references.<br>00 (default) = 0 (highest).<br>01 = 1.<br>10 = 2.<br>11 = 3. |
|         | 0     | Enable REFB              | This bit enables DPLL_0 to lock to REFB.<br>0 (default) = REFB is not enabled for use by DPLL_0.<br>1 = REFB is enabled for use by DPLL_0.                 |

**Table 77. DPLL\_0 REFB Loop Bandwidth Scaling Factor**

| Address | Bits  | Bit Name                                                                 | Description                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------|-------|--------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x044E  | [7:0] | Digital PLL_0 loop bandwidth scaling factor, Bits[7:0]                   | Digital PLL_0 loop bandwidth scaling factor, Bits[7:0]. Default: 0x00. Operation with the digital PLL_0 loop bandwidth scaling factor set to zero is undefined.                                                                                                                                                                                                                                             |
| 0x044F  | [7:0] | Digital PLL_0 loop bandwidth scaling factor, Bits[15:0] (unit of 0.1 Hz) | Digital PLL_0 loop bandwidth scaling factor, Bits[15:8]. Default: 0x00. The default for Register 0x044E to Register 0x0450 = 0x000000. The loop bandwidth must always be less than the DPLL phase detector frequency divided by 20. The DPLL may not lock reliably if the DPLL loop bandwidth is <50 Hz and a crystal is used for the system clock. See the Choosing the SYSCLK Source section for details. |
| 0x0450  | [7:2] | Reserved                                                                 | Default: 0x00.                                                                                                                                                                                                                                                                                                                                                                                              |
|         | 1     | Base loop filter selection                                               | 0 = base loop filter with normal (70°) phase margin (default).<br>1 = base loop filter with high phase margin. (For loop bandwidths ≤2 kHz, there is ≤0.1 dB peaking in the closed-loop transfer function. Setting this bit is also recommended for loop bandwidths >2 kHz.)                                                                                                                                |
|         | 0     | Digital PLL_0 loop bandwidth scaling factor, Bit 16 (unit of 0.1 Hz)     | Digital PLL loop bandwidth scaling factor, Bit 16. Default: 0b.                                                                                                                                                                                                                                                                                                                                             |

**Table 78. DPLL\_0 REFB Integer Part of Feedback (N0) Divider**

| Address | Bits  | Bit Name                                                    | Description                                                                 |
|---------|-------|-------------------------------------------------------------|-----------------------------------------------------------------------------|
| 0x0451  | [7:0] | Digital PLL_0 feedback divider—Integer Part N0, Bits[15:0]  | Digital PLL_0 integer feedback divider (minus 1), Bits[7:0]. Default: 0x00. |
| 0x0452  | [7:0] |                                                             | Digital PLL_0 integer feedback divider, Bits[15:8]. Default: 0x00.          |
| 0x0453  | [7:2] | Reserved                                                    | Default: 0x00.                                                              |
|         | [1:0] | Digital PLL_0 feedback divider—Integer Part N0, Bits[17:16] | Digital PLL_0 integer feedback divider, Bits[17:16]. Default: 00.           |

**Table 79. DPLL\_0 REFB Fractional Part of Fractional Feedback Divider—FRAC0**

| Address | Bits  | Bit Name                                                    | Description                                                                     |
|---------|-------|-------------------------------------------------------------|---------------------------------------------------------------------------------|
| 0x0454  | [7:0] | Digital PLL_0 fractional feedback divider—FRAC0, Bits[23:0] | The numerator of the fractional-N feedback divider, Bits[7:0]. Default: 0x00.   |
| 0x0455  | [7:0] |                                                             | The numerator of the fractional-N feedback divider, Bits[15:8]. Default: 0x00.  |
| 0x0456  | [7:0] |                                                             | The numerator of the fractional-N feedback divider, Bits[23:16]. Default: 0x00. |

**Table 80. DPLL\_0 REFB Modulus of Fractional Feedback Divider—MOD0**

| Address | Bits  | Bit Name                                                | Description                                                                       |
|---------|-------|---------------------------------------------------------|-----------------------------------------------------------------------------------|
| 0x0457  | [7:0] | Digital PLL_0 feedback divider modulus—MOD0, Bits[23:0] | The denominator of the fractional-N feedback divider, Bits[7:0]. Default: 0x00.   |
| 0x0458  | [7:0] |                                                         | The denominator of the fractional-N feedback divider, Bits[15:8]. Default: 0x00.  |
| 0x0459  | [7:0] |                                                         | The denominator of the fractional-N feedback divider, Bits[23:16]. Default: 0x00. |

**DPLL\_0 SETTINGS FOR REFERENCE INPUT C (REFC) (REGISTER 0x045A TO REGISTER 0x0466)****Table 81. DPLL\_0 REFC Priority Setting**

| Address | Bits  | Bit Name      | Description                                                                                                                                                |
|---------|-------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x045A  | [7:3] | Reserved      | Default: 00000b.                                                                                                                                           |
|         | [2:1] | REFC priority | These bits set the priority level (0 to 3) of REFC relative to the other input references.<br>00 (default) = 0 (highest).<br>01 = 1.<br>10 = 2.<br>11 = 3. |
|         | 0     | Enable REFC   | This bit enables DPLL_0 to lock to REFC.<br>0 (default) = REFC is not enabled for use by DPLL_0.<br>1 = REFC is enabled for use by DPLL_0.                 |

**Table 82. DPLL\_0 REFC Loop Bandwidth Scaling Factor**

| Address | Bits  | Bit Name                                                             | Description                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------|-------|----------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x045B  | [7:0] | Digital PLL_0 loop bandwidth scaling factor,                         | Digital PLL_0 loop bandwidth scaling factor, Bits[7:0]. Default: 0x00.                                                                                                                                                                                                                                                                                                                                      |
| 0x045C  | [7:0] | Bits[15:0] (unit of 0.1 Hz)                                          | Digital PLL_0 loop bandwidth scaling factor, Bits[15:8]. Default: 0x00. The default for Register 0x045B to Register 0x045D = 0x000000. The loop bandwidth must always be less than the DPLL phase detector frequency divided by 20. The DPLL may not lock reliably if the DPLL loop bandwidth is <50 Hz and a crystal is used for the system clock. See the Choosing the SYSCLK Source section for details. |
| 0x045D  | [7:2] | Reserved                                                             | Default: 0x00.                                                                                                                                                                                                                                                                                                                                                                                              |
|         | 1     | Base loop filter selection                                           | 0 = base loop filter with normal (70°) phase margin (default).<br>1 = base loop filter with high phase margin. For loop bandwidth ≤2 kHz, there is ≤0.1 dB peaking in the closed-loop transfer function. Setting this bit is also recommended for loop bandwidths >2 kHz.)                                                                                                                                  |
|         | 0     | Digital PLL_0 loop bandwidth scaling factor, Bit 16 (unit of 0.1 Hz) | Digital PLL_0 loop bandwidth scaling factor, Bit 16 (default: 0b).                                                                                                                                                                                                                                                                                                                                          |

**Table 83. DPLL\_0 REFC Integer Part of Feedback (N0) Divider**

| Address | Bits  | Bit Name                                                    | Description                                                                                                                     |
|---------|-------|-------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|
| 0x045E  | [7:0] | Digital PLL_0 feedback divider—Integer Part N0,             | Digital PLL_0 integer feedback divider (minus 1), Bits[7:0]. Default: 0x00.                                                     |
| 0x045F  | [7:0] | Bits[15:0]                                                  | Digital PLL_0 integer feedback divider, Bits[15:8]. Default: 0x00.                                                              |
| 0x0460  | [7:2] | Reserved                                                    | Default: 0x00.                                                                                                                  |
|         | [1:0] | Digital PLL_0 feedback divider—Integer Part N0, Bits[17:16] | Digital PLL_0 integer feedback divider, Bits[17:16]. Default: 00b. The default for Register 0x045E to Register 0x460: 0x000000. |

**Table 84. DPLL\_0 REFC Fractional Part of Fractional Feedback Divider—FRAC0**

| Address | Bits  | Bit Name                                         | Description                                                                     |
|---------|-------|--------------------------------------------------|---------------------------------------------------------------------------------|
| 0x0461  | [7:0] | Digital PLL_0 fractional feedback divider—FRAC0, | The numerator of the fractional-N feedback divider, Bits[7:0]. Default: 0x00.   |
| 0x0462  | [7:0] | Bits[23:0]                                       | The numerator of the fractional-N feedback divider, Bits[15:8]. Default: 0x00.  |
| 0x0463  | [7:0] |                                                  | The numerator of the fractional-N feedback divider, Bits[23:16]. Default: 0x00. |

**Table 85. DPLL\_0 REFC Modulus of Fractional Feedback Divider—MOD0**

| Address | Bits  | Bit Name                                     | Description                                                                       |
|---------|-------|----------------------------------------------|-----------------------------------------------------------------------------------|
| 0x0464  | [7:0] | Digital PLL_0 feedback divider modulus—MOD0, | The denominator of the fractional-N feedback divider, Bits[7:0]. Default: 0x00.   |
| 0x0465  | [7:0] | Bits[23:0]                                   | The denominator of the fractional-N feedback divider, Bits[15:8]. Default: 0x00.  |
| 0x0466  | [7:0] |                                              | The denominator of the fractional-N feedback divider, Bits[23:16]. Default: 0x00. |

**DPLL\_0 SETTINGS FOR REFERENCE INPUT D (REFD) (REGISTER 0x0467 TO REGISTER 0x0473)****Table 86. DPLL\_0 REFD Priority Setting**

| Address | Bits  | Bit Name                 | Description                                                                                                                                                |
|---------|-------|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0467  | [7:3] | Reserved                 | Default: 00000b.                                                                                                                                           |
|         | [2:1] | REFD priority, Bits[1:0] | These bits set the priority level (0 to 3) of REFD relative to the other input references.<br>00 (default) = 0 (highest).<br>01 = 1.<br>10 = 2.<br>11 = 3. |
|         | 0     | Enable REFD              | This bit enables DPLL_0 to lock to REFD.<br>0 (default) = REFD is not enabled for use by DPLL_0.<br>1 = REFD is enabled for use by DPLL_0.                 |

**Table 87. DPLL\_0 REFD Loop Bandwidth Scaling Factor**

| Address | Bits  | Bit Name                                                                 | Description                                                                                                                                                                                                                                                                                                                                  |
|---------|-------|--------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0468  | [7:0] | Digital PLL_0 loop bandwidth scaling factor, Bits[15:0] (unit of 0.1 Hz) | Digital PLL_0 loop bandwidth scaling factor, Bits[7:0]. Default: 0x00.                                                                                                                                                                                                                                                                       |
| 0x0469  | [7:0] |                                                                          | Digital PLL_0 loop bandwidth scaling factor, Bits[15:8]. Default: 0x00. The loop bandwidth must always be less than the DPLL phase detector frequency divided by 20. The DPLL may not lock reliably if the DPLL loop bandwidth is <50 Hz and a crystal is used for the system clock. See the Choosing the SYSCLK Source section for details. |
| 0x046A  | [7:2] | Reserved                                                                 | Default: 0x00.                                                                                                                                                                                                                                                                                                                               |
|         | 1     | Base loop filter selection                                               | 0 = base loop filter with normal (70°) phase margin (default).<br>1 = base loop filter with high phase margin. For loop bandwidths ≤2 kHz, there is ≤0.1 dB peaking in the closed-loop transfer function. Setting this bit is also recommended for loop bandwidths >2 kHz.                                                                   |
|         | 0     | Digital PLL_0 loop bandwidth scaling factor, Bit 16 (unit of 0.1 Hz)     | Digital PLL loop bandwidth scaling factor, Bit 16. Default: 0b.                                                                                                                                                                                                                                                                              |

**Table 88. DPLL\_0 REFD Integer Part of Feedback (N0) Divider**

| Address | Bits  | Bit Name                                                    | Description                                                                 |
|---------|-------|-------------------------------------------------------------|-----------------------------------------------------------------------------|
| 0x046B  | [7:0] | Digital PLL_0 feedback divider—Integer Part N0, Bits[15:0]  | Digital PLL_0 integer feedback divider (minus 1), Bits[7:0]. Default: 0x00. |
| 0x046C  | [7:0] |                                                             | Digital PLL_0 integer feedback divider, Bits[15:8]. Default: 0x00.          |
| 0x046D  | [7:2] | Reserved                                                    | Default: 0x00.                                                              |
|         | [1:0] | Digital PLL_0 feedback divider—Integer Part N0, Bits[17:16] | Digital PLL_0 integer feedback divider, Bits[17:16]. Default: 00b.          |

**Table 89. DPLL\_0 REFD Fractional Part of Fractional Feedback Divider—FRAC0**

| Address | Bits  | Bit Name                                                    | Description                                                                     |
|---------|-------|-------------------------------------------------------------|---------------------------------------------------------------------------------|
| 0x046E  | [7:0] | Digital PLL_0 fractional feedback divider—FRAC0, Bits[23:0] | The numerator of the fractional-N feedback divider, Bits[7:0]. Default: 0x00.   |
| 0x046F  | [7:0] |                                                             | The numerator of the fractional-N feedback divider, Bits[15:8]. Default: 0x00.  |
| 0x0470  | [7:0] |                                                             | The numerator of the fractional-N feedback divider, Bits[23:16]. Default: 0x00. |

**Table 90. DPLL\_0 REFD Modulus of Fractional Feedback Divider—MOD0**

| Address | Bits  | Bit Name                                                | Description                                                                       |
|---------|-------|---------------------------------------------------------|-----------------------------------------------------------------------------------|
| 0x0471  | [7:0] | Digital PLL_0 feedback divider modulus—MOD0, Bits[23:0] | The denominator of the fractional-N feedback divider, Bits[7:0]. Default: 0x00.   |
| 0x0472  | [7:0] |                                                         | The denominator of the fractional-N feedback divider, Bits[15:8]. Default: 0x00.  |
| 0x0473  | [7:0] |                                                         | The denominator of the fractional-N feedback divider, Bits[23:16]. Default: 0x00. |

**DPLL\_1 CONTROLS (REGISTER 0x0500 TO REGISTER 0x051E)**

These registers mimic the DPLL\_0 general settings registers (Register 0x0400 through Register 0x041E) but the register addresses are offset by 0x0100. All default values are identical.

**APLL\_1 CONFIGURATION (REGISTER 0x0530 TO REGISTER 0x0533)**

These registers mimic the APLL\_0 configuration registers (Register 0x0430 through Register 0x0433) but the register addresses are offset by 0x0100. All default values are identical.

**PLL\_1 OUTPUT SYNC AND CLOCK DISTRIBUTION (REGISTER 0x0534 TO REGISTER 0x053E)**

These registers mimic the PLL\_0 output SYNC and clock distribution registers (Register 0x0434 through Register 0x043E) but the register addresses are offset by 0x0100. All default values are identical.

**DPLL\_1 SETTINGS FOR REFERENCE INPUT A (REFA) (REGISTER 0x0540 TO REGISTER 0x054C)**

These registers mimic the DPLL\_0 settings for the Reference Input A (REFA) registers (Register 0x0440 through Register 0x044C) but the register addresses are offset by 0x0100. All default values are identical.

**DPLL\_1 SETTINGS FOR REFERENCE INPUT B (REFB) (REGISTER 0x054D TO REGISTER 0x0559)**

These registers mimic the DPLL\_0 settings for the Reference Input B (REFB) registers (Register 0x044D through Register 0x0459) but the register addresses are offset by 0x0100. All default values are identical.

**DPLL\_1 SETTINGS FOR REFERENCE INPUT C (REFC) (REGISTER 0x055A TO REGISTER 0x0566)**

These registers mimic the DPLL\_0 settings for the Reference Input C (REFC) registers (Register 0x045A through Register 0x0466) but the register addresses are offset by 0x0100. All default values are identical.

**DPLL\_1 SETTINGS FOR REFERENCE INPUT D (REFD) (REGISTER 0x0567 TO REGISTER 0x0573)**

These registers mimic the DPLL\_0 settings for the Reference Input D (REFD) registers (Register 0x0467 through Register 0x0473) but the register addresses are offset by 0x0100. All default values are identical.

**DPLL\_2 CONTROLS (REGISTER 0x0600 TO REGISTER 0x061E)**

These registers mimic the DPLL\_0 controls registers (Register 0x0400 through Register 0x041E) but the register addresses are offset by 0x0200. All default values are identical.

**APLL\_2 CONFIGURATION (REGISTER 0x0630 TO REGISTER 0x0633)**

These registers mimic the APLL\_0 configuration registers (Register 0x0430 through Register 0x0433) but the register addresses are offset by 0x0200. All default values are identical.

**PLL\_2 OUTPUT SYNC AND CLOCK DISTRIBUTION (REGISTER 0x0634 TO REGISTER 0x063E)**

These registers mimic the PLL\_0 output SYNC and clock distribution registers (Register 0x0434 through Register 0x043E) but the register addresses are offset by 0x0200. All default values are identical.

**DPLL\_2 SETTINGS FOR REFERENCE INPUT A (REFA) (REGISTER 0x0640 TO REGISTER 0x064C)**

These registers mimic the DPLL\_0 settings for the Reference Input A (REFA) registers (Register 0x0440 through Register 0x044C) but the register addresses are offset by 0x0200. All default values are identical.

**DPLL\_2 SETTINGS FOR REFERENCE INPUT B (REFB) (REGISTER 0x064D TO REGISTER 0x0659)**

These registers mimic the DPLL\_0 settings for the Reference Input B (REFB) registers (Register 0x044D through Register 0x0459) but the register addresses are offset by 0x0200. All default values are identical.

**DPLL\_2 SETTINGS FOR REFERENCE INPUT C (REFC) (REGISTER 0x065A TO REGISTER 0x0666)**

These registers mimic the DPLL\_0 settings for the Reference Input C (REFC) registers (Register 0x045A through Register 0x0466) but the register addresses are offset by 0x0200. All default values are identical.

**DPLL\_2 SETTINGS FOR REFERENCE INPUT D (REFD) (REGISTER 0x0667 TO REGISTER 0x0673)**

These registers mimic the DPLL\_0 settings for the Reference Input D (REFD) registers (Register 0x0467 through Register 0x0473) but the register addresses are offset by 0x0200. All default values are identical.

**DPLL\_3 CONTROLS (REGISTER 0x0700 TO REGISTER 0x071E)**

These registers mimic the DPLL\_0 controls registers (Register 0x0400 through Register 0x041E) but the register addresses are offset by 0x0300. All default values are identical.

**APLL\_3 CONFIGURATION (REGISTER 0x0730 TO REGISTER 0x0733)**

These registers mimic the APLL\_0 configuration registers (Register 0x0430 through Register 0x0433) but the register addresses are offset by 0x0300. All default values are identical.

**PLL\_3 OUTPUT SYNC AND CLOCK DISTRIBUTION (REGISTER 0x0734 TO REGISTER 0x073E)**

These registers mimic the PLL\_0 output SYNC and clock distribution registers (Register 0x0434 through Register 0x043E) but the register addresses are offset by 0x0300. All default values are identical.

**DPLL\_3 SETTINGS FOR REFERENCE INPUT A (REFA) (REGISTER 0x0740 TO REGISTER 0x074C)**

These registers mimic the DPLL\_0 settings for the Reference Input A (REFA) registers (Register 0x0440 through Register 0x044C) but the register addresses are offset by 0x0300. All default values are identical.

**DPLL\_3 SETTINGS FOR REFERENCE INPUT B (REFB) (REGISTER 0x074D TO REGISTER 0x0759)**

These registers mimic the DPLL\_0 settings for the Reference Input B (REFB) registers (Register 0x044D through Register 0x0459) but the register addresses are offset by 0x0300. All default values are identical.

**DPLL\_3 SETTINGS FOR REFERENCE INPUT C (REFC) (REGISTER 0x075A TO REGISTER 0x0766)**

These registers mimic the DPLL\_0 settings for the Reference Input C (REFC) registers (Register 0x045A through Register 0x0466) but the register addresses are offset by 0x0300. All default values are identical.

**DPLL\_3 SETTINGS FOR REFERENCE INPUT D (REFD) (REGISTER 0x0767 TO REGISTER 0x0773)**

These registers mimic the DPLL\_0 settings for the Reference Input D (REFD) registers (Register 0x0467 through Register 0x0473) but the register addresses are offset by 0x0300. All default values are identical.

**DIGITAL LOOP FILTER COEFFICIENTS (REGISTER 0x0800 TO REGISTER 0x0817)**

Note that the digital loop filter base coefficients ( $\alpha$ ,  $\beta$ ,  $\gamma$ , and  $\delta$ ) have the general form:  $x(2^y)$ , where  $x$  is the linear component, and  $y$  is the exponential component of the coefficient. The value of the linear component ( $x$ ) constitutes a fraction, where  $0 \leq x \leq 1$ . The exponential component ( $y$ ) is a signed integer. These are live registers; therefore, an IO\_UPDATE is not needed. However, the updated coefficients do not take effect while the loop is active.

**Table 91. Base Digital Loop Filter with Normal Phase Margin (PM = 70°)**

| Address | Bits  | Bit Name                        | Description                                             |
|---------|-------|---------------------------------|---------------------------------------------------------|
| 0x0800  | [7:0] | NPM Alpha-0 linear, Bits[15:0]  | Alpha-0 coefficient linear, Bits[7:0]. Default: 0x24.   |
| 0x0801  | [7:0] |                                 | Alpha-0 coefficient linear, Bits[15:8]. Default: 0x8C.  |
| 0x0802  | 7     | Reserved                        | Default: 0b.                                            |
|         | [6:0] | NPM Alpha-1 exponent, Bits[6:0] | Alpha-1 coefficient exponent, Bits[6:0]. Default: 0x49. |
| 0x0803  | [7:0] | NPM Beta-0 linear, Bits[15:0]   | Beta-0 coefficient linear, Bits[7:0]. Default: 0x55.    |
| 0x0804  | [7:0] |                                 | Beta-0 coefficient linear, Bits[15:8]. Default: 0xC9.   |
| 0x0805  | 7     | Reserved                        | Default: 0b.                                            |
|         | [6:0] | NPM Beta-1 exponent, Bits[6:0]  | Beta-1 coefficient exponent, Bits[6:0]. Default: 0x7B.  |
| 0x0806  | [7:0] | NPM Gamma-0 linear, Bits[15:0]  | Gamma-0 coefficient linear, Bits[7:0]. Default: 0x9C.   |
| 0x0807  | [7:0] |                                 | Gamma-0 coefficient linear, Bits[15:8]. Default: 0xFA.  |
| 0x0808  | 7     | Reserved                        | Default: 0b.                                            |
|         | [6:0] | NPM Gamma-1 exponent, Bits[6:0] | Gamma-1 coefficient exponent, Bits[6:0]. Default: 0x55. |
| 0x0809  | [7:0] | NPM Delta-0 linear, Bits[15:0]  | Delta-0 coefficient linear, Bits[7:0]. Default: 0xEA.   |
| 0x080A  | [7:0] |                                 | Delta-0 coefficient linear, Bits[15:8]. Default: 0xE2.  |
| 0x080B  | 7     | Reserved                        | Default: 0b.                                            |
|         | [6:0] | NPM Delta-1 exponent, Bits[6:0] | Delta-1 coefficient exponent, Bits[6:0]. Default: 0x57. |

Note that the base digital loop filter coefficients ( $\alpha$ ,  $\beta$ ,  $\gamma$ , and  $\delta$ ) have the general form:  $x(2^y)$ , where  $x$  is the linear component, and  $y$  is the exponential component of the coefficient. The value of the linear component ( $x$ ) constitutes a fraction, where  $0 \leq x \leq 1$ . The exponential component ( $y$ ) is a signed integer. These are live registers; therefore, an IO\_UPDATE is not needed. However, the updated coefficients do not take effect while the loop is active.

**Table 92. Base Digital Loop Filter with High Phase Margin (PM = 88.5°)**

| Address | Bits  | Bit Name                        | Description                                             |
|---------|-------|---------------------------------|---------------------------------------------------------|
| 0x080C  | [7:0] | HPM Alpha-0 linear, Bits[15:0]  | Alpha-0 coefficient linear, Bits[7:0]. Default = 0x8C.  |
| 0x080D  | [7:0] |                                 | Alpha-0 coefficient linear, Bits[15:8]. Default: 0xAD.  |
| 0x080E  | 7     | Reserved                        | Default: 0b.                                            |
|         | [6:0] | HPM Alpha-1 exponent, Bits[6:0] | Alpha-1 coefficient exponent, Bits[6:0]. Default: 0x4C. |
| 0x080F  | [7:0] | HPM Beta-0 linear, Bits[15:0]   | Beta-0 coefficient linear, Bits[7:0]. Default: 0xF5.    |
| 0x0810  | [7:0] |                                 | Beta-0 coefficient linear, Bits[15:8]. Default: 0xCB.   |
| 0x0811  | 7     | Reserved                        | Default: 0b.                                            |
|         | [6:0] | HPM Beta-1 exponent, Bits[6:0]  | Beta-1 coefficient exponent, Bits[6:0]. Default: 0x73.  |
| 0x0812  | [7:0] | HPM Gamma-0 linear, Bits[15:0]  | Gamma-0 coefficient linear, Bits[7:0]. Default: 0x24.   |
| 0x0813  | [7:0] |                                 | Gamma-0 coefficient linear, Bits[15:8]. Default: 0xD8.  |
| 0x0814  | 7     | Reserved                        | Default: 0b.                                            |
|         | [6:0] | HPM Gamma-1 exponent, Bits[6:0] | Gamma-1 coefficient exponent, Bits[6:0]. Default: 0x59. |
| 0x0815  | [7:0] | HPM Delta-0 linear, Bits[15:0]  | Delta-0 coefficient linear, Bits[7:0]. Default: 0xD2.   |
| 0x0816  | [7:0] |                                 | Delta-0 coefficient linear, Bits[15:8]. Default: 0x8D.  |
| 0x0817  | 7     | Reserved                        | Default: 0b.                                            |
|         | [6:0] | HPM Delta-1 exponent            | Delta-1 coefficient exponent, Bits[6:0]. Default: 0x5A. |

**Table 93. Global Demapping Control**

| Address | Bits  | Bit Name                           | Description                                        |
|---------|-------|------------------------------------|----------------------------------------------------|
| 0x0900  | [7:1] | Reserved                           | Reserved, Bits[7:1]. Default = 0x00.               |
|         | 0     | Demap control IO_UPDATE            | Demap control IO_UPDATE, Bit 0. Default = 0b.      |
| 0x0901  | [7:0] | DPLL_0 sampled address, Bits[15:0] | DPLL_0 sampled address, Bits[7:0]. Default = 0x00. |
| 0x0902  | [7:0] |                                    | DPLL_0 sampled address, Bits[15:8]. Default: 0x00. |
| 0x0903  | [7:0] | DPLL_1 sampled address, Bits[15:0] | DPLL_1 sampled address, Bits[7:0]. Default = 0x00. |
| 0x0904  | [7:0] |                                    | DPLL_1 sampled address, Bits[15:8]. Default: 0x00. |
| 0x0905  | [7:0] | DPLL_2 sampled address, Bits[15:0] | DPLL_2 sampled address, Bits[7:0]. Default = 0x00. |
| 0x0906  | [7:0] |                                    | DPLL_2 sampled address, Bits[15:8]. Default: 0x00  |
| 0x0907  | [7:0] | DPLL_3 sampled address, Bits[15:0] | DPLL_3 sampled address, Bits[7:0]. Default = 0x00. |
| 0x0908  | [7:0] |                                    | DPLL_3 sampled address, Bits[15:8]. Default: 0x00. |
| 0x0909  | [7:1] | Reserved                           | Reserved, Bits[7:1]. Default = 0x00.               |
|         | 0     | Demap control IO_UPDATE            | Demap control IO_UPDATE, Bit 0. Default = 0b.      |

## COMMON OPERATIONAL CONTROLS (REGISTER 0x0A00 TO REGISTER 0x0A0E)

**Table 94. Global Operational Controls**

| Address | Bits  | Bit Name         | Description                                                                                                                                                                                                                                                                                                                  |
|---------|-------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0A00  | [7:4] | Reserved         | Default: 0x0.                                                                                                                                                                                                                                                                                                                |
|         | 3     | Soft sync all    | Setting this bit initiates synchronization of all clock distribution outputs (default = 0b). Nonmasked outputs stall when value is 1; restart is initialized on a 1-to-0 transition. Note that like all buffered registers, an IO_UPDATE (0x000F = 0x01) is needed every time there is a change for this bit to take effect. |
|         | 2     | Calibrate SYSCLK | A 0-to-1 transition of this bit (followed by an IO_UPDATE) calibrates the SYSCLK PLL. Default: 0b.                                                                                                                                                                                                                           |
|         | 1     | Calibrate all    | A 0-to-1 transition of this bit (followed by an IO_UPDATE) calibrates the system clock PLL, as well as all four output PLLs (APLL_0, APLL_1, APLL_2, APLL_3). Default: 0b.                                                                                                                                                   |
|         | 0     | Power-down all   | Places the entire device in deep sleep mode. Default: device is not powered down.                                                                                                                                                                                                                                            |

Table 95. Power Down of Reference Inputs

| Address | Bits  | Bit Name        | Description                                                                           |
|---------|-------|-----------------|---------------------------------------------------------------------------------------|
| 0x0A01  | [7:4] | Reserved        | Default: 0x0                                                                          |
|         | 3     | REFD power-down | Powers down REFD input receiver<br>0 (default) = not powered down<br>1 = powered down |
|         | 2     | REFC power-down | Powers down REFC input receiver<br>0 (default) = not powered down<br>1 = powered down |
|         | 1     | REFB power-down | Powers down REFB input receiver<br>0 (default) = not powered down<br>1 = powered down |
|         | 0     | REFA power-down | Powers down REFA input receiver<br>0 (default) = not powered down<br>1 = powered down |

Table 96. Reference Input Validation Timeout

| Address | Bits  | Bit Name     | Description                                                                                                                                                 |
|---------|-------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0A02  | [7:4] | Reserved     | Default: 0x0.                                                                                                                                               |
|         | 3     | REFD timeout | If REFD is unfaulted, setting this autoclearing bit forces the reference validation timer for REFD to zero, thus making it valid immediately. Default = 0b. |
|         | 2     | REFC timeout | If REFC is unfaulted, setting this autoclearing bit forces the reference validation timer for REFC to zero, thus making it valid immediately. Default = 0b. |
|         | 1     | REFB timeout | If REFB is unfaulted, setting this autoclearing bit forces the reference validation timer for REFB to zero, thus making it valid immediately. Default = 0b. |
|         | 0     | REFA timeout | If REFA is unfaulted, setting this autoclearing bit forces the reference validation timer for REFA to zero, thus making it valid immediately. Default = 0b. |

Table 97. Force Reference Input Fault

| Address | Bits  | Bit Name   | Description                                                                               |
|---------|-------|------------|-------------------------------------------------------------------------------------------|
| 0x0A03  | [7:4] | Reserved   | Default: 0x0                                                                              |
|         | 3     | REFD fault | Faults REFD input receiver<br>0 (default) = not faulted<br>1 = faulted (REFD is not used) |
|         | 2     | REFC fault | Faults REFC input receiver<br>0 (default) = not faulted<br>1 = faulted (REFC is not used) |
|         | 1     | REFB fault | Faults REFB input receiver<br>0 (default) = not faulted<br>1 = faulted (REFB is not used) |
|         | 0     | REFA fault | Faults REFA input receiver<br>0 (default) = not faulted<br>1 = faulted (REFA is not used) |

Table 98. Reference Input Monitor Bypass

| Address | Bits  | Bit Name            | Description                                                                                                                                                                                                                                                  |
|---------|-------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0A04  | [7:4] | Reserved            | Default: 0x0                                                                                                                                                                                                                                                 |
|         | 3     | REFD monitor bypass | Bypasses REFD input receiver frequency monitor; setting this bit to 1 forces REFD to be unfaulted as long as the REFD fault bit in Register 0x0A03 is not set.<br>0 (default) = REFD frequency monitor not bypassed.<br>1 = REFD frequency monitor bypassed. |
|         | 2     | REFC monitor bypass | Bypasses REFC input receiver frequency monitor; setting this bit to 1 forces REFC to be unfaulted as long as the REFC fault bit in Register 0x0A03 is not set.<br>0 (default) = REFC frequency monitor not bypassed.<br>1 = REFC frequency monitor bypassed. |
|         | 1     | REFB monitor bypass | Bypasses REFB input receiver frequency monitor; setting this bit to 1 forces REFB to be unfaulted as long as the REFB fault bit in Register 0x0A03 is not set.<br>0 (default) = REFB frequency monitor not bypassed.<br>1 = REFB frequency monitor bypassed. |
|         | 0     | REFA monitor bypass | Bypasses REFA input receiver frequency monitor; setting this bit to 1 forces REFA to be unfaulted as long as the REFA fault bit in Register 0x0A03 is not set.<br>0 (default) = REFA frequency monitor not bypassed.<br>1 = REFA frequency monitor bypassed. |

**IRQ CLEARING (REGISTER 0x0A05 TO REGISTER 0x0A14)**

The IRQ clearing registers are identical in format to the IRQ monitor registers (Register 0x0D08 to Register 0x0D16). When set to Logic 1, an IRQ clearing bit resets the corresponding IRQ monitor bit, thereby cancelling the interrupt request for the indicated event. The IRQ clearing registers are autoclearing.

Table 99. Clear IRQ Groups

| Address | Bits | Bit Name             | Description                                      |
|---------|------|----------------------|--------------------------------------------------|
| 0x0A05  | 7    | Clear watchdog timer | Clears watchdog timer alert                      |
|         | 6    | Reserved             | Reserved                                         |
|         | 5    | Clear DPLL_3 IRQs    | Clears all IRQs associated with DPLL_3           |
|         | 4    | Clear DPLL_2 IRQs    | Clears all IRQs associated with DPLL_2           |
|         | 3    | Clear DPLL_1 IRQs    | Clears all IRQs associated with DPLL_1           |
|         | 2    | Clear DPLL_0 IRQs    | Clears all IRQs associated with DPLL_0           |
|         | 1    | Clear common IRQs    | Clears all IRQs associated with common IRQ group |
|         | 0    | Clear all IRQs       | Clears all IRQs                                  |

Table 100. IRQ Clearing for SYSCLK

| Address | Bits  | Bit Name           | Description                                                                                                     |
|---------|-------|--------------------|-----------------------------------------------------------------------------------------------------------------|
| 0x0A06  | 7     | SYSCLK unlocked    | Clears IRQ indicating a SYSCLK PLL state transition from locked to unlocked                                     |
|         | 6     | SYSCLK stable      | Clears IRQ indicating that SYSCLK stability time has expired and that the SYSCLK PLL is considered to be stable |
|         | 5     | SYSCLK locked      | Clears IRQ indicating a SYSCLK PLL state transition from unlocked to locked                                     |
|         | 4     | SYSCLK cal ended   | Clears IRQ indicating a SYSCLK PLL calibration has ended                                                        |
|         | 3     | SYSCLK cal started | Clears IRQ indicating a SYSCLK PLL calibration has started                                                      |
|         | 2     | Watchdog timer     | Clears IRQ indicating expiration of the watchdog timer                                                          |
|         | [1:0] | Reserved           | Default: 00b                                                                                                    |



Table 101. IRQ Clearing for Reference Inputs

| Address | Bits | Bit Name           | Description                                                          |
|---------|------|--------------------|----------------------------------------------------------------------|
| 0x0A07  | 7    | Reserved           | Reserved                                                             |
|         | 6    | REFB validated     | Clears IRQ indicating that REFB has been validated                   |
|         | 5    | REFB fault cleared | Clears IRQ indicating that REFB has been cleared of a previous fault |
|         | 4    | REFB fault         | Clears IRQ indicating that REFB has been faulted                     |
|         | 3    | Reserved           | Reserved                                                             |
|         | 2    | REFA validated     | Clears IRQ indicating that REFA has been validated                   |
|         | 1    | REFA fault cleared | Clears IRQ indicating that REFA has been cleared of a previous fault |
|         | 0    | REFA fault         | Clears IRQ indicating that REFA has been faulted                     |
| 0x0A08  | 7    | Reserved           | Reserved                                                             |
|         | 6    | REFD validated     | Clears IRQ indicating that REFD has been validated                   |
|         | 5    | REFD fault cleared | Clears IRQ indicating that REFD has been cleared of a previous fault |
|         | 4    | REFD fault         | Clears IRQ indicating that REFD has been faulted                     |
|         | 3    | Reserved           | Reserved                                                             |
|         | 2    | REFC validated     | Clears IRQ indicating that REFC has been validated                   |
|         | 1    | REFC fault cleared | Clears IRQ indicating that REFC has been cleared of a previous fault |
|         | 0    | REFC fault         | Clears IRQ indicating that REFC has been faulted                     |

Table 102. IRQ Clearing for Digital PLL0 (DPLL\_0)

| Address | Bits | Bit Name                | Description                                                                       |
|---------|------|-------------------------|-----------------------------------------------------------------------------------|
| 0x0A09  | 7    | Frequency unclamped     | Clears IRQ indicating that DPLL_0 has exited a frequency unclamped state          |
|         | 6    | Frequency clamped       | Clears IRQ indicating that DPLL_0 has entered a frequency clamped state           |
|         | 5    | Phase slew unlimited    | Clears IRQ indicating that DPLL_0 has exited a phase slew limited state           |
|         | 4    | Phase slew limited      | Clears IRQ indicating that DPLL_0 has entered a phase slew limited state          |
|         | 3    | Frequency unlocked      | Clears IRQ indicating that DPLL_0 has lost frequency lock                         |
|         | 2    | Frequency locked        | Clears IRQ indicating that DPLL_0 has acquired frequency lock                     |
|         | 1    | Phase unlocked          | Clears IRQ indicating that DPLL_0 has lost phase lock                             |
|         | 0    | Phase locked            | Clears IRQ indicating that DPLL_0 has acquired phase lock                         |
| 0x0A0A  | 7    | DPLL_0 switching        | Clears IRQ indicating that DPLL_0 is switching to a new reference                 |
|         | 6    | DPLL_0 free run         | Clears IRQ indicating that DPLL_0 has entered free run mode                       |
|         | 5    | DPLL_0 holdover         | Clears IRQ indicating that DPLL_0 has entered holdover mode                       |
|         | 4    | History updated         | Clears IRQ indicating that DPLL_0 has updated its tuning word history             |
|         | 3    | REFD activated          | Clears IRQ indicating that DPLL_0 has activated REFD                              |
|         | 2    | REFC activated          | Clears IRQ indicating that DPLL_0 has activated REFC                              |
|         | 1    | REFB activated          | Clears IRQ indicating that DPLL_0 has activated REFB                              |
|         | 0    | REFA activated          | Clears IRQ indicating that DPLL_0 has activated REFA                              |
| 0x0A0B  | 7    | Phase step detected     | Clears IRQ indicating that DPLL_0 has detected a large phase step at its input    |
|         | 6    | Demap control unclamped | Clears IRQ indicating that the DPLL_0 demapping controller has an unclamped state |
|         | 5    | Demap control clamped   | Clears IRQ indicating that the DPLL_0 demapping controller has a clamped state    |
|         | 4    | Clock dist sync'd       | Clears IRQ indicating a distribution sync event                                   |
|         | 3    | APLL_0 unlocked         | Clears IRQ indicating that APLL_0 has been unlocked                               |
|         | 2    | APLL_0 locked           | Clears IRQ indicating that APLL_0 has been locked                                 |
|         | 1    | APLL_0 cal ended        | Clears IRQ indicating that APLL_0 calibration complete                            |
|         | 0    | APLL_0 cal started      | Clears IRQ indicating that APLL_0 calibration started                             |

Table 103. IRQ Clearing for Digital PLL1 (DPLL\_1)

| Address | Bits | Bit Name                | Description                                                                       |
|---------|------|-------------------------|-----------------------------------------------------------------------------------|
| 0x0A0C  | 7    | Frequency unclamped     | Clears IRQ indicating that DPLL_1 has exited a frequency unclamped state          |
|         | 6    | Frequency clamped       | Clears IRQ indicating that DPLL_1 has entered a frequency clamped state           |
|         | 5    | Phase slew unlimited    | Clears IRQ indicating that DPLL_1 has exited a phase slew limited state           |
|         | 4    | Phase slew limited      | Clears IRQ indicating that DPLL_1 has entered a phase slew limited state          |
|         | 3    | Frequency unlocked      | Clears IRQ indicating that DPLL_1 has lost frequency lock                         |
|         | 2    | Frequency locked        | Clears IRQ indicating that DPLL_1 has acquired frequency lock                     |
|         | 1    | Phase unlocked          | Clears IRQ indicating that DPLL_1 has lost phase lock                             |
|         | 0    | Phase locked            | Clears IRQ indicating that DPLL_1 has acquired phase lock                         |
| 0x0A0D  | 7    | DPLL_1 switching        | Clears IRQ indicating that DPLL_1 is switching to a new reference                 |
|         | 6    | DPLL_1 free run         | Clears IRQ indicating that DPLL_1 has entered free run mode                       |
|         | 5    | DPLL_1 holdover         | Clears IRQ indicating that DPLL_1 has entered holdover mode                       |
|         | 4    | History updated         | Clears IRQ indicating that DPLL_1 has updated its tuning word history             |
|         | 3    | REFD activated          | Clears IRQ indicating that DPLL_1 has activated REFD                              |
|         | 2    | REFC activated          | Clears IRQ indicating that DPLL_1 has activated REFC                              |
|         | 1    | REFB activated          | Clears IRQ indicating that DPLL_1 has activated REFB                              |
|         | 0    | REFA activated          | Clears IRQ indicating that DPLL_1 has activated REFA                              |
| 0x0A0E  | 7    | Phase step detected     | Clears IRQ indicating that DPLL_1 has detected a large phase step at its input    |
|         | 6    | Demap control unclamped | Clears IRQ indicating that the DPLL_1 demapping controller has an unclamped state |
|         | 5    | Demap control clamped   | Clears IRQ indicating that the DPLL_1 demapping controller has a clamped state    |
|         | 4    | Clock dist sync'd       | Clears IRQ indicating a distribution sync event                                   |
|         | 3    | APLL_1 unlocked         | Clears IRQ indicating that APLL_1 has been unlocked                               |
|         | 2    | APLL_1 locked           | Clears IRQ indicating that APLL_1 has been locked                                 |
|         | 1    | APLL_1 cal ended        | Clears IRQ indicating that APLL_1 calibration complete                            |
|         | 0    | APLL_1 cal started      | Clears IRQ indicating that APLL_1 calibration started                             |

Table 104. IRQ Clearing for Digital PLL2 (DPLL\_2)

| Address | Bits | Bit Name             | Description                                                              |
|---------|------|----------------------|--------------------------------------------------------------------------|
| 0x0A0F  | 7    | Frequency unclamped  | Clears IRQ indicating that DPLL_2 has exited a frequency unclamped state |
|         | 6    | Frequency clamped    | Clears IRQ indicating that DPLL_2 has entered a frequency clamped state  |
|         | 5    | Phase slew unlimited | Clears IRQ indicating that DPLL_2 has exited a phase slew limited state  |
|         | 4    | Phase slew limited   | Clears IRQ indicating that DPLL_2 has entered a phase slew limited state |
|         | 3    | Frequency unlocked   | Clears IRQ indicating that DPLL_2 has lost frequency lock                |
|         | 2    | Frequency locked     | Clears IRQ indicating that DPLL_2 has acquired frequency lock            |
|         | 1    | Phase unlocked       | Clears IRQ indicating that DPLL_2 has lost phase lock                    |
|         | 0    | Phase locked         | Clears IRQ indicating that DPLL_2 has acquired phase lock                |
| 0x0A10  | 7    | DPLL_2 switching     | Clears IRQ indicating that DPLL_2 is switching to a new reference        |
|         | 6    | DPLL_2 free run      | Clears IRQ indicating that DPLL_2 has entered free run mode              |
|         | 5    | DPLL_2 holdover      | Clears IRQ indicating that DPLL_2 has entered holdover mode              |
|         | 4    | History updated      | Clears IRQ indicating that DPLL_2 has updated its tuning word history    |
|         | 3    | REFD activated       | Clears IRQ indicating that DPLL_2 has activated REFD                     |
|         | 2    | REFC activated       | Clears IRQ indicating that DPLL_2 has activated REFC                     |
|         | 1    | REFB activated       | Clears IRQ indicating that DPLL_2 has activated REFB                     |
|         | 0    | REFA activated       | Clears IRQ indicating that DPLL_2 has activated REFA                     |

| Address | Bits | Bit Name                | Description                                                                    |
|---------|------|-------------------------|--------------------------------------------------------------------------------|
| 0x0A11  | 7    | Phase step detected     | Clears IRQ indicating that DPLL_2 has detected a large phase step at its input |
|         | 6    | Demap control unclamped | Clears IRQ indicating that the DPLL_2 demapping controller is unclamped        |
|         | 5    | Demap control clamped   | Clears IRQ indicating that the DPLL_2 demapping controller is clamped          |
|         | 4    | Clock dist sync'd       | Clears IRQ indicating a distribution sync event                                |
|         | 3    | APLL_2 unlocked         | Clears IRQ indicating that APLL_2 has been unlocked                            |
|         | 2    | APLL_2 locked           | Clears IRQ indicating that APLL_2 has been locked                              |
|         | 1    | APLL_2 cal ended        | Clears IRQ indicating that APLL_2 calibration complete                         |
|         | 0    | APLL_2 cal started      | Clears IRQ indicating that APLL_2 calibration started                          |

Table 105. IRQ Clearing for Digital PLL3 (DPLL\_3)

| Address | Bits | Bit Name                | Description                                                                    |
|---------|------|-------------------------|--------------------------------------------------------------------------------|
| 0x0A12  | 7    | Frequency unclamped     | Clears IRQ indicating that DPLL_3 has exited a frequency unclamped state       |
|         | 6    | Frequency clamped       | Clears IRQ indicating that DPLL_3 has entered a frequency clamped state        |
|         | 5    | Phase slew unlimited    | Clears IRQ indicating that DPLL_3 has exited a phase slew limited state        |
|         | 4    | Phase slew limited      | Clears IRQ indicating that DPLL_3 has entered a phase slew limited state       |
|         | 3    | Frequency unlocked      | Clears IRQ indicating that DPLL_3 has lost frequency lock                      |
|         | 2    | Frequency locked        | Clears IRQ indicating that DPLL_3 has acquired frequency lock                  |
|         | 1    | Phase unlocked          | Clears IRQ indicating that DPLL_3 has lost phase lock                          |
|         | 0    | Phase locked            | Clears IRQ indicating that DPLL_3 has acquired phase lock                      |
| 0x0A13  | 7    | DPLL_3 switching        | Clears IRQ indicating that DPLL_3 is switching to a new reference              |
|         | 6    | DPLL_3 free run         | Clears IRQ indicating that DPLL_3 has entered free run mode                    |
|         | 5    | DPLL_3 holdover         | Clears IRQ indicating that DPLL_3 has entered holdover mode                    |
|         | 4    | History updated         | Clears IRQ indicating that DPLL_3 has updated its tuning word history          |
|         | 3    | REFD activated          | Clears IRQ indicating that DPLL_3 has activated REFD                           |
|         | 2    | REFC activated          | Clears IRQ indicating that DPLL_3 has activated REFC                           |
|         | 1    | REFB activated          | Clears IRQ indicating that DPLL_3 has activated REFB                           |
|         | 0    | REFA activated          | Clears IRQ indicating that DPLL_3 has activated REFA                           |
| 0x0A14  | 7    | Phase step detected     | Clears IRQ indicating that DPLL_3 has detected a large phase step at its input |
|         | 6    | Demap control unclamped | Clears IRQ indicating that the DPLL_3 demapping controller is unclamped        |
|         | 5    | Demap control clamped   | Clears IRQ indicating that the DPLL_3 demapping controller is clamped          |
|         | 4    | Clock dist sync'd       | Clears IRQ indicating a distribution sync event                                |
|         | 3    | APLL_3 unlocked         | Clears IRQ indicating that APLL_3 has been unlocked                            |
|         | 2    | APLL_3 locked           | Clears IRQ indicating that APLL_3 has been locked                              |
|         | 1    | APLL_3 cal ended        | Clears IRQ indicating that APLL_3 calibration complete                         |
|         | 0    | APLL_3 cal started      | Clears IRQ indicating that APLL_3 calibration started                          |

## PLL\_0 OPERATIONAL CONTROLS (REGISTER 0x0A20 TO REGISTER 0x0A24)

Table 106. PLL\_0 Sync and Calibration

| Address | Bits  | Bit Name                             | Description                                                                                                                                                                                       |
|---------|-------|--------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0A20  | [7:3] | Reserved                             | Default: 0x0.                                                                                                                                                                                     |
|         | 2     | APLL_0 soft sync                     | Setting this bit initiates synchronization of the clock distribution output.<br>0 (default) = normal operation.<br>1 = nonmasked PLL_0 outputs stall; restart initialized on a 1-to-0 transition. |
|         | 1     | APLL_0 calibrate (not self-clearing) | 1 = initiates VCO calibration (calibration occurs on the IO_UPDATE following a 0-to-1 transition of this bit). This bit is not autoclearing.<br>0 (default) = does nothing.                       |
|         | 0     | PLL_0 power-down                     | Places DPLL_0, APLL_0, and PLL_0 clock in deep sleep mode.<br>0 (default) = normal operation.<br>1 = powered down.                                                                                |

Table 107. PLL\_0 Output

| Address | Bits  | Bit Name         | Description                                                                                                                                                    |
|---------|-------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0A21  | [7:4] | Reserved         | Default 0x0                                                                                                                                                    |
|         | 3     | OUT0B disable    | Setting this bit puts the OUT0B driver into power-down. Default: 0b. Channel synchronization is maintained, but runt pulses may be generated.                  |
|         | 2     | Reserved         | Default: 0b.                                                                                                                                                   |
|         | 1     | OUT0B power-down | Setting this bit puts the OUT0B divider and driver into power-down. Default: 0b. This mode saves the most power, but runt pulses may be generated during exit. |
|         | 0     | Reserved         | Default: 0b.                                                                                                                                                   |

Table 108. PLL\_0 User Mode

| Address                              | Bits                                                      | Bit Name                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                                      |                          |      |                           |      |                              |      |                                                         |      |                                                        |      |                                                           |      |           |      |
|--------------------------------------|-----------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|--------------------------|------|---------------------------|------|------------------------------|------|---------------------------------------------------------|------|--------------------------------------------------------|------|-----------------------------------------------------------|------|-----------|------|
| 0x0A22                               | 7                                                         | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Default: 0b.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                      |                          |      |                           |      |                              |      |                                                         |      |                                                        |      |                                                           |      |           |      |
|                                      | [6:5]                                                     | DPLL_0 manual reference                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Input reference when user selection mode = 00, 01, 10, or 11.<br>00 (default) = Input Reference A.<br>01 = Input Reference B.<br>10 = Input Reference C.<br>11 = Input Reference D.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                      |                          |      |                           |      |                              |      |                                                         |      |                                                        |      |                                                           |      |           |      |
|                                      | [4:2]                                                     | DPLL_0 switching mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Selects the operating mode of the reference switching state machine.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                                      |                          |      |                           |      |                              |      |                                                         |      |                                                        |      |                                                           |      |           |      |
|                                      |                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | <table border="1"> <thead> <tr> <th>Reference Switchover Mode, Bits[2:0]</th> <th>Reference Selection Mode</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Automatic revertive mode.</td> </tr> <tr> <td>001b</td> <td>Automatic nonrevertive mode.</td> </tr> <tr> <td>010b</td> <td>Manual reference select mode (with automatic fallback).</td> </tr> <tr> <td>011b</td> <td>Manual reference select mode (with holdover fallback).</td> </tr> <tr> <td>100b</td> <td>Manual reference select mode (without holdover fallback).</td> </tr> <tr> <td>101b</td> <td>Not used.</td> </tr> <tr> <td>110b</td> <td>Not used.</td> </tr> <tr> <td>111b</td> <td>Not used.</td> </tr> </tbody> </table> | Reference Switchover Mode, Bits[2:0] | Reference Selection Mode | 000b | Automatic revertive mode. | 001b | Automatic nonrevertive mode. | 010b | Manual reference select mode (with automatic fallback). | 011b | Manual reference select mode (with holdover fallback). | 100b | Manual reference select mode (without holdover fallback). | 101b | Not used. | 110b |
| Reference Switchover Mode, Bits[2:0] | Reference Selection Mode                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                      |                          |      |                           |      |                              |      |                                                         |      |                                                        |      |                                                           |      |           |      |
| 000b                                 | Automatic revertive mode.                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                      |                          |      |                           |      |                              |      |                                                         |      |                                                        |      |                                                           |      |           |      |
| 001b                                 | Automatic nonrevertive mode.                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                      |                          |      |                           |      |                              |      |                                                         |      |                                                        |      |                                                           |      |           |      |
| 010b                                 | Manual reference select mode (with automatic fallback).   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                      |                          |      |                           |      |                              |      |                                                         |      |                                                        |      |                                                           |      |           |      |
| 011b                                 | Manual reference select mode (with holdover fallback).    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                      |                          |      |                           |      |                              |      |                                                         |      |                                                        |      |                                                           |      |           |      |
| 100b                                 | Manual reference select mode (without holdover fallback). |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                      |                          |      |                           |      |                              |      |                                                         |      |                                                        |      |                                                           |      |           |      |
| 101b                                 | Not used.                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                      |                          |      |                           |      |                              |      |                                                         |      |                                                        |      |                                                           |      |           |      |
| 110b                                 | Not used.                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                      |                          |      |                           |      |                              |      |                                                         |      |                                                        |      |                                                           |      |           |      |
| 111b                                 | Not used.                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                      |                          |      |                           |      |                              |      |                                                         |      |                                                        |      |                                                           |      |           |      |
| 1                                    | DPLL_0 user holdover                                      | Forces DPLL_0 into holdover mode. Note that the <a href="#">AD9554-1</a> enters free run mode if this bit is set when there is no holdover history available.<br>0 (default) = normal operation.<br>1 = DPLL_0 is forced into holdover mode until this bit is cleared. Note that holdover mode is used if the holdover history is available. User free run mode is used if the holdover history is not available. See Register 0x0D22, Bit 0 for the DPLL_0 history available indication. |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                      |                          |      |                           |      |                              |      |                                                         |      |                                                        |      |                                                           |      |           |      |
| 0                                    | DPLL_0 user free run                                      | Forces DPLL_0 into free run mode.<br>0 (default) = normal operation.<br>1 = DPLL_0 is forced into free run mode until this bit is cleared.                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                      |                          |      |                           |      |                              |      |                                                         |      |                                                        |      |                                                           |      |           |      |

Table 109. PLL\_0 Reset

| Address | Bits  | Bit Name                 | Description                                                                                                                                                                               |
|---------|-------|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0A23  | [7:3] | Reserved                 | Default: 00000b.                                                                                                                                                                          |
|         | 2     | Reset DPLL_0 loop filter | Resets the digital loop filter.<br>0 (default) = normal operation.<br>1 = DPLL_0 digital loop filter is reset. This is an autoclearing bit.                                               |
|         | 1     | Reset DPLL_0 TW history  | Resets the tuning word history (part of holdover functionality).<br>0 (default) = normal operation.<br>1 = DPLL_0 tuning word history is reset. This is an autoclearing bit.              |
|         | 0     | Reset DPLL_0 autosync    | Resets the automatic synchronization logic (see Register 0x0435).<br>0 (default) = normal operation.<br>1 = DPLL_0 automatic synchronization logic is reset. This is an autoclearing bit. |

Table 110. PLL\_0 Phase

| Address | Bits  | Bit Name                      | Description                                                                                                                                                                                  |
|---------|-------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0A24  | [7:3] | Reserved                      | Default: 00000b.                                                                                                                                                                             |
|         | 2     | DPLL_0 reset phase offset     | Resets the incremental phase offset to zero. This is an autoclearing bit.                                                                                                                    |
|         | 1     | DPLL_0 decrement phase offset | Decrements the incremental phase offset by the amount specified in the incremental phase lock offset step size registers (Register 0x0412 and Register 0x0413). This is an autoclearing bit. |
|         | 0     | DPLL_0 increment phase offset | Increments the incremental phase offset by the amount specified in the incremental phase lock offset step size registers (Register 0x0412 and Register 0x0413). This is an autoclearing bit. |

### PLL\_1 OPERATIONAL CONTROLS (REGISTER 0x0A40 TO REGISTER 0x0A44)

These registers mimic the PLL\_0 controls registers (Register 0x0A20 through Register 0x0A24) but the register addresses are offset by 0x0020. All default values are identical.

### PLL\_2 OPERATIONAL CONTROLS (REGISTER 0x0A60 TO REGISTER 0x0A64)

These registers mimic the PLL\_0 controls registers (Register 0x0A20 through Register 0x0A24) but the register addresses are offset by 0x0040. All default values are identical.

### PLL\_3 OPERATIONAL CONTROLS (REGISTER 0x0A80 TO REGISTER 0x0A84)

These registers mimic the PLL\_0 controls registers (Register 0x0A20 through Register 0x0A24) but the register addresses are offset by 0x0060. All default values are identical.

### VOLTAGE REGULATOR (REGISTER 0x0B00 TO REGISTER 0x0B01)

The bits in these registers adjust the internal voltage regulator for 1.5 V input voltage operation.

Table 111. Voltage Regulator

| Address | Bits  | Bit Name           | Description                                                                                                                                                                                                                                                                                     |
|---------|-------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0B00  | [7:0] | VREG,<br>Bits[7:0] | Adjusts internal voltage regulators for 1.5 V operation. There are only two valid settings for this register, and all bits in VREG[9:0] must be all 1s or all 0s, depending on whether the device is powered at 1.5 V or 1.8 V.<br>0x00 (default) = 1.8 V operation.<br>0xFF = 1.5 V operation. |
| 0x0B01  | [7:2] | Reserved           | Default: 000000b.                                                                                                                                                                                                                                                                               |
|         | [1:0] | VREG,<br>Bits[9:8] | Adjusts internal voltage regulators for 1.5 V operation. There are only two valid settings for this register.<br>00b (default) = 1.8 V operation.<br>11b = 1.5 V operation.                                                                                                                     |

**STATUS READBACK (REGISTER 0x0D01 TO REGISTER 0x0D05)**

All bits in Register 0x0D01 to Register 0x0D05 are read only. To report the latest status, these bits require an IO\_UPDATE (Register 0x000F = 0x01) immediately before being read.

**Table 112. SYSCLK and PLL Status**

| Address | Bits | Bit Name                | Description                                                                                                                                                                             |
|---------|------|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0D01  | 7    | PLL_3 all locked        | Indicates the status of the system clock, APLL_3, and DPLL_3.<br>0 = system clock or APLL_3 or DPLL_3 is unlocked.<br>1 = all three PLLs (system clock, APLL_3, and DPLL_3) are locked. |
|         | 6    | PLL_2 all locked        | Indicates the status of the system clock, APLL_2, and DPLL_2.<br>0 = system clock or APLL_2 or DPLL_2 is unlocked.<br>1 = all three PLLs (system clock, APLL_2, and DPLL_2) are locked. |
|         | 5    | PLL_1 all locked        | Indicates the status of the system clock, APLL_1, and DPLL_1.<br>0 = system clock or APLL_1 or DPLL_1 is unlocked.<br>1 = all three PLLs (system clock, APLL_1, and DPLL_1) are locked. |
|         | 4    | PLL_0 all locked        | Indicates the status of the system clock, APLL_0, and DPLL_0.<br>0 = system clock or APLL_0 or DPLL_0 is unlocked.<br>1 = all three PLLs (system clock, APLL_0, and DPLL_0) are locked. |
|         | 3    | Reserved                | Default: 0b.                                                                                                                                                                            |
|         | 2    | SYSCLK calibration busy | Indicates the status of the system clock calibration.<br>0 (default) = normal operation.<br>1 = system clock calibration in progress.                                                   |
|         | 1    | SYSCLK stable           | The control logic sets this bit when the device considers the system clock to be stable (see the System Clock Stability Timer section).                                                 |
|         | 0    | SYSCLK lock detect      | Indicates the status of the system clock PLL.<br>0 = unlocked.<br>1 = locked.                                                                                                           |

**Table 113. Status of Reference Inputs**

| Address | Bits   | Bit Name           | Description                                                                                                                                                                 |
|---------|--------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0D02  | 7      | DPLL_3 REFA active | This bit is 1 if DPLL_3 is either locked to or attempting to lock to REFA.                                                                                                  |
|         | 6      | DPLL_2 REFA active | This bit is 1 if DPLL_2 is either locked to or attempting to lock to REFA.                                                                                                  |
|         | 5      | DPLL_1 REFA active | This bit is 1 if DPLL_1 is either locked to or attempting to lock to REFA.                                                                                                  |
|         | 4      | DPLL_0 REFA active | This bit is 1 if DPLL_0 is either locked to or attempting to lock to REFA.                                                                                                  |
|         | 3      | REFA valid         | This bit is 1 if the REFA frequency is within the programmed limits and the validation timer has expired.                                                                   |
|         | 2      | REFA fault         | This bit is 1 if the REFA frequency is outside of the programmed limits.                                                                                                    |
|         | 1      | REFA fast          | This bit is 1 if the REFA frequency is higher than allowed by its profile settings. (Note that if no REFA input is detected, the REFA fast and slow bits may both be high.) |
|         | 0      | REFA slow          | This bit is 1 if the REFA frequency is lower than allowed by its profile settings.                                                                                          |
|         | 0x0D03 | 7                  | DPLL_3 REFB active                                                                                                                                                          |
| 6       |        | DPLL_2 REFB active | This bit is 1 if DPLL_2 is either locked to or attempting to lock to REFB.                                                                                                  |
| 5       |        | DPLL_1 REFB active | This bit is 1 if DPLL_1 is either locked to or attempting to lock to REFB.                                                                                                  |
| 4       |        | DPLL_0 REFB active | This bit is 1 if DPLL_0 is either locked to or attempting to lock to REFB.                                                                                                  |
| 3       |        | REFB valid         | This bit is 1 if the REFB frequency is within the programmed limits and the validation timer has expired.                                                                   |
| 2       |        | REFB fault         | This bit is 1 if the REFB frequency is outside of the programmed limits.                                                                                                    |
| 1       |        | REFB fast          | This bit is 1 if the REFB frequency is higher than allowed by its profile settings. (Note that if no REFB input is detected, the REFB fast and slow bits may both be high.) |
| 0       |        | REFB slow          | This bit is 1 if the REFB frequency is lower than allowed by its profile settings.                                                                                          |

| Address | Bits | Bit Name           | Description                                                                                                                                                                 |
|---------|------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0D04  | 7    | DPLL_3 REFC active | This bit is 1 if DPLL_3 is either locked to or attempting to lock to REFC.                                                                                                  |
|         | 6    | DPLL_2 REFC active | This bit is 1 if DPLL_2 is either locked to or attempting to lock to REFC.                                                                                                  |
|         | 5    | DPLL_1 REFC active | This bit is 1 if DPLL_1 is either locked to or attempting to lock to REFC.                                                                                                  |
|         | 4    | DPLL_0 REFC active | This bit is 1 if DPLL_0 is either locked to or attempting to lock to REFC.                                                                                                  |
|         | 3    | REFC valid         | This bit is 1 if the REFC frequency is within the programmed limits and the validation timer has expired.                                                                   |
|         | 2    | REFC fault         | This bit is 1 if the REFC frequency is outside of the programmed limits.                                                                                                    |
|         | 1    | REFC fast          | This bit is 1 if the REFC frequency is higher than allowed by its profile settings. Note that if no REFC input is detected, the REFC fast and slow bits may both be high.)  |
|         | 0    | REFC slow          | This bit is 1 if the REFC frequency is lower than allowed by its profile settings.                                                                                          |
| 0x0D05  | 7    | DPLL_3 REFD active | This bit is 1 if DPLL_3 is either locked to or attempting to lock to REFD.                                                                                                  |
|         | 6    | DPLL_2 REFD active | This bit is 1 if DPLL_2 is either locked to or attempting to lock to REFD.                                                                                                  |
|         | 5    | DPLL_1 REFD active | This bit is 1 if DPLL_1 is either locked to or attempting to lock to REFD.                                                                                                  |
|         | 4    | DPLL_0 REFD active | This bit is 1 if DPLL_0 is either locked to or attempting to lock to REFD.                                                                                                  |
|         | 3    | REFD valid         | This bit is 1 if the REFD frequency is within the programmed limits and the validation timer has expired.                                                                   |
|         | 2    | REFD fault         | This bit is 1 if the REFD frequency is outside of the programmed limits.                                                                                                    |
|         | 1    | REFD fast          | This bit is 1 if the REFD frequency is higher than allowed by its profile settings. (Note that if no REFD input is detected, the REFD fast and slow bits may both be high.) |
|         | 0    | REFD slow          | This bit is 1 if the REFD frequency is lower than allowed by its profile settings.                                                                                          |

### IRQ MONITOR (REGISTER 0x0D08 TO REGISTER 0x0D16)

If not masked via the IRQ mask registers (Register 0x010F to Register 0x011D), the appropriate IRQ monitor bit is set to Logic 1 when the indicated event occurs. These bits can be cleared by writing a 1 to the corresponding bit in the IRQ clearing registers (Register 0x0A05 to Register 0x0A0E) by setting the clear all IRQs bit in Register 0x0A05 or by a device reset.

**Table 114. IRQ Common Functions**

| Address | Bits   | Bit Name           | Description                                                                                              |
|---------|--------|--------------------|----------------------------------------------------------------------------------------------------------|
| 0x0D08  | 7      | SYSCLK unlocked    | IRQ indicating a SYSCLK PLL state transition from locked to unlocked                                     |
|         | 6      | SYSCLK stable      | IRQ indicating that SYSCLK stability time has expired and that the SYSCLK PLL is considered to be stable |
|         | 5      | SYSCLK locked      | IRQ indicating a SYSCLK PLL state transition from unlocked to locked                                     |
|         | 4      | SYSCLK cal ended   | IRQ indicating a SYSCLK PLL has ended its calibration                                                    |
|         | 3      | SYSCLK cal started | IRQ indicating a SYSCLK PLL has started its calibration                                                  |
|         | 2      | Watchdog timer     | IRQ indicating expiration of the watchdog timer                                                          |
|         | [1:0]  | Reserved           | Reserved                                                                                                 |
|         | 0x0D09 | 7                  | Reserved                                                                                                 |
| 6       |        | REFB validated     | IRQ indicating that REFB has been validated                                                              |
| 5       |        | REFB fault cleared | IRQ indicating that REFB has been cleared of a previous fault                                            |
| 4       |        | REFB fault         | IRQ indicating that REFB has been faulted                                                                |
| 3       |        | Reserved           | Reserved                                                                                                 |
| 2       |        | REFA validated     | IRQ indicating that REFA has been validated                                                              |
| 1       |        | REFA fault cleared | IRQ indicating that REFA has been cleared of a previous fault                                            |
| 0       |        | REFA fault         | IRQ indicating that REFA has been faulted                                                                |
| 0x0D0A  | 7      | Reserved           | Reserved                                                                                                 |
|         | 6      | REFD validated     | IRQ indicating that REFD has been validated                                                              |
|         | 5      | REFD fault cleared | IRQ indicating that REFD has been cleared of a previous fault                                            |
|         | 4      | REFD fault         | IRQ indicating that REFD has been faulted                                                                |
|         | 3      | Reserved           | Reserved                                                                                                 |
|         | 2      | REFC validated     | IRQ indicating that REFC has been validated                                                              |
|         | 1      | REFC fault cleared | IRQ indicating that REFC has been cleared of a previous fault                                            |
|         | 0      | REFC fault         | IRQ indicating that REFC has been faulted                                                                |

Table 115. IRQ Monitor for Digital PLL0 (DPLL\_0)

| Address | Bits | Bit Name                | Description                                                              |
|---------|------|-------------------------|--------------------------------------------------------------------------|
| 0x0D0B  | 7    | Frequency unclamped     | IRQ indicating that DPLL_0 has exited a frequency clamped state          |
|         | 6    | Frequency clamped       | IRQ indicating that DPLL_0 has entered a frequency clamped state         |
|         | 5    | Phase slew unlimited    | IRQ indicating that DPLL_0 has exited a phase slew limited state         |
|         | 4    | Phase slew limited      | IRQ indicating that DPLL_0 has entered a phase slew limited state        |
|         | 3    | Frequency unlocked      | IRQ indicating that DPLL_0 has lost frequency lock                       |
|         | 2    | Frequency locked        | IRQ indicating that DPLL_0 has acquired frequency lock                   |
|         | 1    | Phase unlocked          | IRQ indicating that DPLL_0 has lost phase lock                           |
|         | 0    | Phase locked            | IRQ indicating that DPLL_0 has acquired phase lock                       |
| 0x0D0C  | 7    | DPLL_0 switching        | IRQ indicating that DPLL_0 is switching to a new reference               |
|         | 6    | DPLL_0 free run         | IRQ indicating that DPLL_0 has entered free run mode                     |
|         | 5    | DPLL_0 holdover         | IRQ indicating that DPLL_0 has entered holdover mode                     |
|         | 4    | DPLL_0 history updated  | IRQ indicating that DPLL_0 has updated its tuning word history           |
|         | 3    | REFD activated          | IRQ indicating that DPLL_0 has activated REFD                            |
|         | 2    | REFC activated          | IRQ indicating that DPLL_0 has activated REFC                            |
|         | 1    | REFB activated          | IRQ indicating that DPLL_0 has activated REFB                            |
|         | 0    | REFA activated          | IRQ indicating that DPLL_0 has activated REFA                            |
| 0x0D0D  | 7    | Phase step direction    | IRQ indicating that the DPLL_0 demapping controller phase step direction |
|         | 6    | Demap control unclamped | IRQ indicating that the DPLL_0 demapping controller is unclamped         |
|         | 5    | Demap control clamped   | IRQ indicating that the DPLL_0 demapping controller is clamped           |
|         | 4    | Clock dist sync'd       | IRQ indicating a distribution sync event                                 |
|         | 3    | APLL_0 unlocked         | IRQ indicating that APLL_0 has been unlocked                             |
|         | 2    | APLL_0 locked           | IRQ indicating that APLL_0 has been locked                               |
|         | 1    | APLL_0 cal ended        | IRQ indicating that APLL_0 calibration complete                          |
|         | 0    | APLL_0 cal started      | IRQ indicating that APLL_0 calibration started                           |

Table 116. IRQ Monitor for Digital PLL1 (DPLL\_1)

| Address | Bits | Bit Name               | Description                                                       |
|---------|------|------------------------|-------------------------------------------------------------------|
| 0x0D0E  | 7    | Frequency unclamped    | IRQ indicating that DPLL_1 has exited a frequency clamped state   |
|         | 6    | Frequency clamped      | IRQ indicating that DPLL_1 has entered a frequency clamped state  |
|         | 5    | Phase slew unlimited   | IRQ indicating that DPLL_1 has exited a phase slew limited state  |
|         | 4    | Phase slew limited     | IRQ indicating that DPLL_1 has entered a phase slew limited state |
|         | 3    | Frequency unlocked     | IRQ indicating that DPLL_1 has lost frequency lock                |
|         | 2    | Frequency locked       | IRQ indicating that DPLL_1 has acquired frequency lock            |
|         | 1    | Phase unlocked         | IRQ indicating that DPLL_1 has lost phase lock                    |
|         | 0    | Phase locked           | IRQ indicating that DPLL_1 has acquired phase lock                |
| 0x0D0F  | 7    | DPLL_1 switching       | IRQ indicating that DPLL_1 is switching to a new reference        |
|         | 6    | DPLL_1 free run        | IRQ indicating that DPLL_1 has entered free run mode              |
|         | 5    | DPLL_1 holdover        | IRQ indicating that DPLL_1 has entered holdover mode              |
|         | 4    | DPLL_1 history updated | IRQ indicating that DPLL_1 has updated its tuning word history    |
|         | 3    | REFD activated         | IRQ indicating that DPLL_1 has activated REFD                     |
|         | 2    | REFC activated         | IRQ indicating that DPLL_1 has activated REFC                     |
|         | 1    | REFB activated         | IRQ indicating that DPLL_1 has activated REFB                     |
|         | 0    | REFA activated         | IRQ indicating that DPLL_1 has activated REFA                     |



| Address | Bits | Bit Name                | Description                                                              |
|---------|------|-------------------------|--------------------------------------------------------------------------|
| 0x0D10  | 7    | Phase step direction    | IRQ indicating that the DPLL_1 demapping controller phase step direction |
|         | 6    | Demap control unclamped | IRQ indicating that the DPLL_1 demapping controller is unclamped         |
|         | 5    | Demap control clamped   | IRQ indicating that the DPLL_1 demapping controller is clamped           |
|         | 4    | Clock dist sync'd       | IRQ indicating a distribution sync event                                 |
|         | 3    | APLL_1 unlocked         | IRQ indicating that APLL_1 has been unlocked                             |
|         | 2    | APLL_1 locked           | IRQ indicating that APLL_1 has been locked                               |
|         | 1    | APLL_1 cal ended        | IRQ indicating that APLL_1 calibration complete                          |
|         | 0    | APLL_1 cal started      | IRQ indicating that APLL_1 calibration started                           |

Table 117. IRQ Monitor for Digital PLL2 (DPLL\_2)

| Address | Bits | Bit Name                | Description                                                              |
|---------|------|-------------------------|--------------------------------------------------------------------------|
| 0x0D11  | 7    | Frequency unclamped     | IRQ indicating that DPLL_2 has exited a frequency clamped state          |
|         | 6    | Frequency clamped       | IRQ indicating that DPLL_2 has entered a frequency clamped state         |
|         | 5    | Phase slew unlimited    | IRQ indicating that DPLL_2 has exited a phase slew limited state         |
|         | 4    | Phase slew limited      | IRQ indicating that DPLL_2 has entered a phase slew limited state        |
|         | 3    | Frequency unlocked      | IRQ indicating that DPLL_2 has lost frequency lock                       |
|         | 2    | Frequency locked        | IRQ indicating that DPLL_2 has acquired frequency lock                   |
|         | 1    | Phase unlocked          | IRQ indicating that DPLL_2 has lost phase lock                           |
|         | 0    | Phase locked            | IRQ indicating that DPLL_2 has acquired phase lock                       |
| 0x0D12  | 7    | DPLL_2 switching        | IRQ indicating that DPLL_2 is switching to a new reference               |
|         | 6    | DPLL_2 free run         | IRQ indicating that DPLL_2 has entered free run mode                     |
|         | 5    | DPLL_2 holdover         | IRQ indicating that DPLL_2 has entered holdover mode                     |
|         | 4    | DPLL_2 history updated  | IRQ indicating that DPLL_2 has updated its tuning word history           |
|         | 3    | REFD activated          | IRQ indicating that DPLL_2 has activated REFD                            |
|         | 2    | REFC activated          | IRQ indicating that DPLL_2 has activated REFC                            |
|         | 1    | REFB activated          | IRQ indicating that DPLL_2 has activated REFB                            |
|         | 0    | REFA activated          | IRQ indicating that DPLL_2 has activated REFA                            |
| 0x0D13  | 7    | Phase step direction    | IRQ indicating that the DPLL_2 demapping controller phase step direction |
|         | 6    | Demap control unclamped | IRQ indicating that the DPLL_2 demapping controller is unclamped         |
|         | 5    | Demap control clamped   | IRQ indicating that the DPLL_2 demapping controller is clamped           |
|         | 4    | Clock dist sync'd       | IRQ indicating a distribution sync event                                 |
|         | 3    | APLL_2 unlocked         | IRQ indicating that APLL_2 has been unlocked                             |
|         | 2    | APLL_2 locked           | IRQ indicating that APLL_2 has been locked                               |
|         | 1    | APLL_2 cal ended        | IRQ indicating that APLL_2 calibration complete                          |
|         | 0    | APLL_2 cal started      | IRQ indicating that APLL_2 calibration started                           |

Table 118. IRQ Monitor for Digital PLL3 (DPLL\_3)

| Address | Bits | Bit Name                | Description                                                              |
|---------|------|-------------------------|--------------------------------------------------------------------------|
| 0x0D14  | 7    | Frequency unclamped     | IRQ indicating that DPLL_3 has exited a frequency clamped state          |
|         | 6    | Frequency clamped       | IRQ indicating that DPLL_3 has entered a frequency clamped state         |
|         | 5    | Phase slew unlimited    | IRQ indicating that DPLL_3 has exited a phase slew limited state         |
|         | 4    | Phase slew limited      | IRQ indicating that DPLL_3 has entered a phase slew limited state        |
|         | 3    | Frequency unlocked      | IRQ indicating that DPLL_3 has lost frequency lock                       |
|         | 2    | Frequency locked        | IRQ indicating that DPLL_3 has acquired frequency lock                   |
|         | 1    | Phase unlocked          | IRQ indicating that DPLL_3 has lost phase lock                           |
|         | 0    | Phase locked            | IRQ indicating that DPLL_3 has acquired phase lock                       |
| 0x0D15  | 7    | DPLL_3 switching        | IRQ indicating that DPLL_3 is switching to a new reference               |
|         | 6    | DPLL_3 free run         | IRQ indicating that DPLL_3 has entered free run mode                     |
|         | 5    | DPLL_3 holdover         | IRQ indicating that DPLL_3 has entered holdover mode                     |
|         | 4    | DPLL_3 history updated  | IRQ indicating that DPLL_3 has updated its tuning word history           |
|         | 3    | REFD activated          | IRQ indicating that DPLL_3 has activated REFD                            |
|         | 2    | REFC activated          | IRQ indicating that DPLL_3 has activated REFC                            |
|         | 1    | REFB activated          | IRQ indicating that DPLL_3 has activated REFB                            |
|         | 0    | REFA activated          | IRQ indicating that DPLL_3 has activated REFA                            |
| 0x0D16  | 7    | Phase step direction    | IRQ indicating that the DPLL_3 demapping controller phase step direction |
|         | 6    | Demap control unclamped | IRQ indicating that the DPLL_3 demapping controller is unclamped         |
|         | 5    | Demap control clamped   | IRQ indicating that the DPLL_3 demapping controller is clamped           |
|         | 4    | Clock dist sync'd       | IRQ indicating a distribution sync event                                 |
|         | 3    | APLL_3 unlocked         | IRQ indicating that APLL_3 has been unlocked                             |
|         | 2    | APLL_3 locked           | IRQ indicating that APLL_3 has been locked                               |
|         | 1    | APLL_3 cal ended        | IRQ indicating that APLL_3 calibration complete                          |
|         | 0    | APLL_3 cal started      | IRQ indicating that APLL_3 calibration started                           |

**PLL\_0 READ ONLY STATUS (REGISTER 0x0D20 TO REGISTER 0x0D2A)**

All bits in Register 0x0D20 to Register 0x0D2A are read only. To report the latest status, these bits require an IO\_UPDATE (Register 0x000F = 0x01) immediately before being read.

Table 119. PLL\_0 Lock Status

| Address | Bits  | Bit Name               | Description                                                                                                                                                                                    |
|---------|-------|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0D20  | [7:5] | Reserved               | Default: 000b.                                                                                                                                                                                 |
|         | 4     | APLL_0 cal in progress | The control logic holds this bit set while the calibration of the APLL_0 VCO is in progress.                                                                                                   |
|         | 3     | APLL_0 frequency lock  | Indicates the status of APLL_0.<br>0 = unlocked.<br>1 = locked.                                                                                                                                |
|         | 2     | DPLL_0 frequency lock  | Indicates the frequency lock status of DPLL_0.<br>0 = unlocked.<br>1 = locked.                                                                                                                 |
|         | 1     | DPLL_0 phase lock      | Indicates the phase lock status of DPLL_0.<br>0 = unlocked.<br>1 = locked.                                                                                                                     |
|         | 0     | PLL_0 all locked       | Indicates the status of the system clock, APLL_0, and DPLL_0.<br>0 = system clock PLL, APLL_0, or DPLL_0 is unlocked.<br>1 = all three PLLs (system clock PLL, APLL_0, and DPLL_0) are locked. |

Table 120. DPLL\_0 Loop State

| Address | Bits  | Bit Name                  | Description                                                                                                                                                                                 |
|---------|-------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0D21  | [7:5] | Reserved                  | Default: 000b.                                                                                                                                                                              |
|         | [4:3] | DPLL_0 active ref         | Indicates the reference input that DPLL_0 is using.<br>00 = DPLL_0 has selected REFA.<br>01 = DPLL_0 has selected REFB.<br>10 = DPLL_0 has selected REFC.<br>11 = DPLL_0 has selected REFD. |
|         | 2     | DPLL_0 switching          | Indicates that DPLL_0 is switching input references.<br>0 = DPLL is not switching.<br>1 = DPLL is switching input references.                                                               |
|         | 1     | DPLL_0 holdover           | Indicates that DPLL_0 is in holdover mode.<br>0 = not in holdover.<br>1 = in holdover mode.                                                                                                 |
|         | 0     | DPLL_0 free run           | Indicates that DPLL_0 is in free run mode.<br>0 = not in free run mode.<br>1 = in free run mode.                                                                                            |
| 0x0D22  | [7:4] | Reserved                  | Default: 00000b.                                                                                                                                                                            |
|         | 3     | Demap controller clamped  | The control logic sets this bit when DPLL_0 demapping controller is clamped.                                                                                                                |
|         | 2     | DPLL_0 phase slew limited | The control logic sets this bit when DPLL_0 is phase slew limited.                                                                                                                          |
|         | 1     | DPLL_0 frequency clamped  | The control logic sets this bit when DPLL_0 is frequency clamped.                                                                                                                           |
|         | 0     | DPLL_0 history available  | The control logic sets this bit when the tuning word history of DPLL_0 is available.<br>(See Register 0x0D23 to Register 0x0D26 for the tuning word.)                                       |

Table 121. DPLL\_0 Holdover History

| Address | Bits  | Bit Name                                 | Description                                                                                                                                                                                                                                                                                                                                                                                     |
|---------|-------|------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0D23  | [7:0] | DPLL_0 tuning word readback, Bits[23:0]  | DPLL_0 tuning word readback bits, Bits[7:0]. This group of registers contains the averaged digital PLL tuning word used when the DPLL enters holdover. Setting the history accumulation timer to its minimal value allows the user to use these registers for a read back of the most recent DPLL tuning word with only 1 ms of averaging. Instantaneous tuning word readback is not available. |
| 0x0D24  | [7:0] |                                          | DPLL_0 tuning word readback, Bits[15:8].                                                                                                                                                                                                                                                                                                                                                        |
| 0x0D25  | [7:0] |                                          | DPLL_0 tuning word readback, Bits[23:16].                                                                                                                                                                                                                                                                                                                                                       |
| 0x0D26  | [7:6] | Reserved                                 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                       |
|         | [5:0] | DPLL_0 tuning word readback, Bits[29:24] | DPLL_0 tuning word readback, Bits[29:24].                                                                                                                                                                                                                                                                                                                                                       |

Table 122. DPLL\_0 Phase Lock and Frequency Lock Bucket Levels

| Address | Bits  | Bit Name                                              | Description                                                                                                           |
|---------|-------|-------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|
| 0x0D27  | [7:0] | DPLL_0 phase lock detect bucket level, Bits[7:0]      | Read only digital PLL lock detect bucket level, Bits[7:0]; see the DPLL Frequency Lock Detector section for details.  |
| 0x0D28  | [7:4] | Reserved                                              | Reserved.                                                                                                             |
|         | [3:0] | DPLL_0 phase lock detect bucket level, Bits[11:8]     | Read only digital PLL lock detect bucket level, Bits[11:8]; see the DPLL Frequency Lock Detector section for details. |
| 0x0D29  | [7:0] | DPLL_0 frequency lock detect bucket level, Bits[7:0]  | Read only digital PLL lock detect bucket level, Bits[7:0]; see the DPLL Phase Lock Detector section for details.      |
| 0x0D2A  | [7:4] | Reserved                                              | Reserved.                                                                                                             |
|         | [3:0] | DPLL_0 frequency lock detect bucket level, Bits[11:8] | Read only digital PLL lock detect bucket level, Bits[11:8]; see the DPLL Phase Lock Detector section for details.     |

**PLL\_1 READ ONLY STATUS (REGISTER 0x0D40 TO REGISTER 0x0D4A)**

These registers mimic the PLL\_0 controls registers (Register 0x0D20 through Register 0x0D2A) but the register addresses are offset by 0x0020. All default values are identical. All bits in Register 0x0D40 to Register 0x0D4A are read only. To report the latest status, these bits require an IO\_UPDATE (Register 0x000F = 0x01) immediately before being read.

**PLL\_2 READ ONLY STATUS (REGISTER 0x0D60 TO REGISTER 0x0D6A)**

These registers mimic the PLL\_0 controls registers (Register 0x0D20 through Register 0x0D2A) but the register addresses are offset by 0x0040. All bits in Register 0x0D60 to Register 0x0D6A are read only. To report the latest status, these bits require an IO\_UPDATE (Register 0x000F = 0x01) immediately before being read.

**PLL\_3 READ ONLY STATUS (REGISTER 0x0D80 TO REGISTER 0x0D8A)**

These registers mimic the PLL\_0 controls registers (Register 0x0D20 through Register 0x0D2A) but the register addresses are offset by 0x0060. All bits in Register 0x0D40 to Register 0x0D4A are read only. To report the latest status, these bits require an IO\_UPDATE (Register 0x000F = 0x01) immediately before being read.

**Table 123. Multifunction Pin Output Functions (D7 = 1)**

| Bits[D7:D0] Value   | Output Function                                                                                                 | Source Proxy                                                                  |
|---------------------|-----------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|
| 0x80                | Static Logic 0                                                                                                  | None                                                                          |
| 0x81                | Static Logic 1                                                                                                  | None                                                                          |
| 0x82                | System clock divided by 32                                                                                      | None                                                                          |
| 0x83                | Watchdog timer output; this is a strobe whose duration equals (32/(one system clock period)) when timer expires | None                                                                          |
| 0x84                | SYSCLK PLL calibration busy                                                                                     | Register 0x0D01, Bit 2                                                        |
| 0x85                | SYSCLK PLL lock detected                                                                                        | Register 0x0D01, Bit 0                                                        |
| 0x86                | SYSCLK PLL stable                                                                                               | Register 0x0D01, Bit 1                                                        |
| 0x87                | All PLLs locked (logical AND of 0x88, 0x89, 0x8A, 0x8B)                                                         | Register 0x0D01, Bits[7:4]                                                    |
| 0x88                | (DPLL_0 phase lock) AND (APLL_0 lock) AND (SYSCLK PLL lock)                                                     | Register 0x0D01, Bit 4                                                        |
| 0x89                | (DPLL_1 phase lock) AND (APLL_1 lock) AND (SYSCLK PLL lock)                                                     | Register 0x0D01, Bit 5                                                        |
| 0x8A                | (DPLL_2 phase lock) AND (APLL_2 lock) AND (SYSCLK PLL lock)                                                     | Register 0x0D01, Bit 6                                                        |
| 0x8B                | (DPLL_3 phase lock) AND (APLL_3 lock) AND (SYSCLK PLL lock)                                                     | Register 0x0D01, Bit 7                                                        |
| 0x8C                | Unused                                                                                                          |                                                                               |
| 0x8D                | Unused                                                                                                          |                                                                               |
| 0x8E                | Unused                                                                                                          |                                                                               |
| 0x90                | All IRQs: (IRQ_common) OR (IRQ_PLL_0) OR (IRQ_PLL_1) OR (IRQ_PLL_2) OR (IRQ_PLL_3)                              | None                                                                          |
| 0x91                | IRQ_common                                                                                                      | None                                                                          |
| 0x92/0x93/0x94/0x95 | IRQ_PLL_0/IRQ_PLL_1/IRQ_PLL_2/IRQ_PLL_3                                                                         | None                                                                          |
| 0xA0/0xA1/0xA2/0xA3 | REFA/REFB/REFC/REFD fault                                                                                       | Register 0x0D02/Register 0x0D03/<br>Register 0x0D04/Register 0x0D05, Bit 2    |
| 0xA8/0xA9/0xAA/0xAB | REFA/REFB/REFC/REFD valid                                                                                       | Register 0x0D02/Register 0x0D03/<br>Register 0x0D04/Register 0x0D05, Bit 3    |
| 0xB0                | REFA active (any PLL)                                                                                           | Register 0x0D02, Bit 4  Bit 5  Bit 6  Bit 7                                   |
| 0xB1                | REFB active (any PLL)                                                                                           | Register 0x0D03, Bit 4  Bit 5  Bit 6  Bit 7                                   |
| 0xB2                | REFC active (any PLL)                                                                                           | Register 0x0D04, Bit 4  Bit 5  Bit 6  Bit 7                                   |
| 0xB3                | REFD active (any PLL)                                                                                           | Register 0x0D05, Bit 4  Bit 5  Bit 6  Bit 7                                   |
| 0xC0                | DPLL_0 phase locked                                                                                             | Register 0x0D20, Bit 1                                                        |
| 0xC1                | DPLL_0 frequency locked                                                                                         | Register 0x0D20, Bit 2                                                        |
| 0xC2                | APLL_0 frequency lock                                                                                           | Register 0x0D20, Bit 3                                                        |
| 0xC3                | APLL_0 cal in process                                                                                           | Register 0x0D20, Bit 4                                                        |
| 0xC4                | DPLL_0 active                                                                                                   | Logical OR of Bit 4 in Register 0x0D02 through Register 0x0D05                |
| 0xC5                | DPLL_0 in free run mode                                                                                         | Register 0x0D21, Bit 0                                                        |
| 0xC6                | DPLL_0 in holdover                                                                                              | Register 0x0D21, Bit 1                                                        |
| 0xC7                | DPLL_0 switching                                                                                                | Register 0x0D21, Bit 2                                                        |
| 0xC8                | DPLL_0 history available                                                                                        | Register 0x0D22, Bit 0                                                        |
| 0xC9                | DPLL_0 history updated                                                                                          | Register 0x0D0C, Bit 4 (IRQ does not need to be set for this setting to work) |

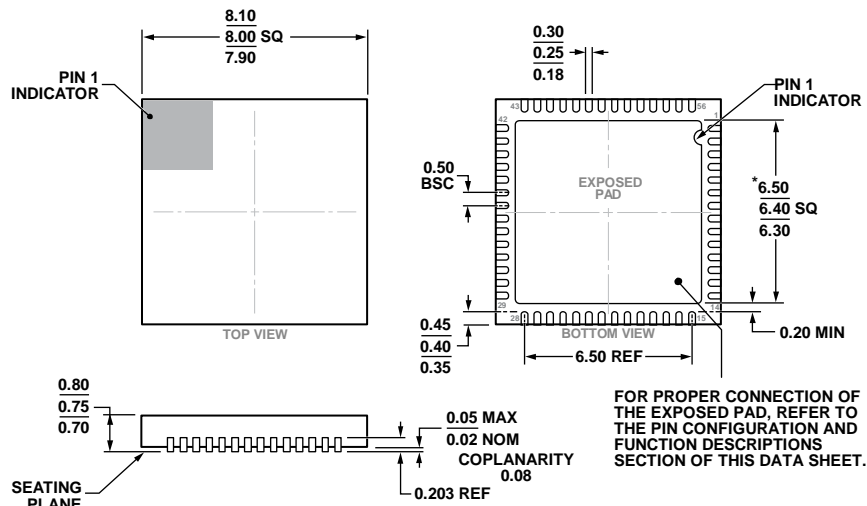
| Bits[D7:D0] Value | Output Function                     | Source Proxy                                                                  |
|-------------------|-------------------------------------|-------------------------------------------------------------------------------|
| 0xCA              | DPLL_0 clamp                        | Register 0x0D22, Bit 1                                                        |
| 0xCB              | DPLL_0 phase slew limited           | Register 0x0D22, Bit 2                                                        |
| 0xCC              | PLL_0 clock distribution sync pulse | None                                                                          |
| 0xCD              | DPLL_1 demapping controller clamped | Register 0x0D22, Bit 3                                                        |
| 0xD0              | DPLL_1 phase locked                 | Register 0x0D40, Bit 1                                                        |
| 0xD1              | DPLL_1 frequency locked             | Register 0x0D40, Bit 2                                                        |
| 0xD2              | APLL_1 frequency lock               | Register 0x0D40, Bit 3                                                        |
| 0xD3              | APLL_1 cal in process               | Register 0x0D40, Bit 4                                                        |
| 0xD4              | DPLL_1 active                       | Logical OR of Bit 5 in Register 0x0D02 through Register 0x0D05                |
| 0xD5              | DPLL_1 in free run mode             | Register 0x0D41, Bit 0                                                        |
| 0xD6              | DPLL_1 in holdover                  | Register 0x0D41, Bit 1                                                        |
| 0xD7              | DPLL_1 in switchover                | Register 0x0D41, Bit 2                                                        |
| 0xD8              | DPLL_1 history available            | Register 0x0D42, Bit 0                                                        |
| 0xD9              | DPLL_1 history updated              | Register 0x0D0F, Bit 4 (IRQ does not need to be set for this setting to work) |
| 0xDA              | DPLL_1 clamp                        | Register 0x0D42, Bit 1                                                        |
| 0xDB              | DPLL_1 phase slew limited           | Register 0x0D42, Bit 2                                                        |
| 0xDC              | PLL_1 clock distribution sync pulse | None                                                                          |
| 0xDD              | DPLL_1 demapping controller clamped | Register 0x0D42, Bit 3                                                        |
| 0xE0              | DPLL_2 phase locked                 | Register 0x0D60, Bit 1                                                        |
| 0xE1              | DPLL_2 frequency locked             | Register 0x0D60, Bit 2                                                        |
| 0xE2              | APLL_2 frequency lock               | Register 0x0D60, Bit 3                                                        |
| 0xE3              | APLL_2 cal in process               | Register 0x0D60, Bit 4                                                        |
| 0xE4              | DPLL_2 active                       | Logical OR of Bit 6 in Register 0x0D02 through Register 0x0D05                |
| 0xE5              | DPLL_2 in free run mode             | Register 0x0D61, Bit 0                                                        |
| 0xE6              | DPLL_2 in holdover                  | Register 0x0D61, Bit 1                                                        |
| 0xE7              | DPLL_2 switching                    | Register 0x0D61, Bit 2                                                        |
| 0xE8              | DPLL_2 history available            | Register 0x0D62, Bit 0                                                        |
| 0xE9              | DPLL_2 history update               | Register 0x0D0C, Bit 4 (IRQ does not need to be set for this setting to work) |
| 0xEA              | DPLL_2 clamp                        | Register 0x0D62, Bit 1                                                        |
| 0xEB              | DPLL_2 phase slew limited           | Register 0x0D62, Bit 2                                                        |
| 0xEC              | PLL_2 clock distribution sync pulse | None                                                                          |
| 0xED              | DPLL_2 demapping controller clamped | Register 0x0D62, Bit 4                                                        |
| 0xF0              | DPLL_3 phase locked                 | Register 0x0D80, Bit 1                                                        |
| 0xF1              | DPLL_3 frequency locked             | Register 0x0D80, Bit 2                                                        |
| 0xF2              | APLL_3 frequency lock               | Register 0x0D80, Bit 3                                                        |
| 0xF3              | APLL_3 cal in process               | Register 0x0D80, Bit 4                                                        |
| 0xF4              | DPLL_3 active                       | Logical OR of Bit 7 in Register 0x0D02 through Register 0x0D05                |
| 0xF5              | DPLL_3 in free run mode             | Register 0x0D81, Bit 0                                                        |
| 0xF6              | DPLL_3 in holdover                  | Register 0x0D81, Bit 1                                                        |
| 0xF7              | DPLL_3 switching                    | Register 0x0D81, Bit 2                                                        |
| 0xF8              | DPLL_3 history available            | Register 0x0D82, Bit 0                                                        |
| 0xF9              | DPLL_3 history update               | Register 0x0D0F, Bit 4 (IRQ does not need to be set for this setting to work) |
| 0xFA              | DPLL_3 clamp                        | Register 0x0D82, Bit 1                                                        |
| 0xFB              | DPLL_3 phase slew limited           | Register 0x0D82, Bit 2                                                        |
| 0xFC              | PLL_3 clock distribution sync pulse | None                                                                          |
| 0xFD              | DPLL_3 demapping controller clamped | Register 0x0D82, Bit 3                                                        |
| 0xFE to 0xFF      | Reserved                            | None                                                                          |

Table 124. Multifunction Pin Input Functions (D7 = 0)

| Bits[D7:D0] Value   | Input Function                                | Destination Proxy          |
|---------------------|-----------------------------------------------|----------------------------|
| 0x00                | No function                                   | None                       |
| 0x01                | IO_UPDATE                                     | Register 0x000F, Bit 0     |
| 0x02                | Full power-down                               | Register 0x0A00, Bit 0     |
| 0x03                | Clear watchdog timer                          | Register 0x0A05, Bit 7     |
| 0x04                | Soft sync all                                 | Register 0x0A00, Bit 3     |
| 0x10                | Clear all IRQs                                | Register 0x0A05, Bit 0     |
| 0x11                | Clear common IRQs                             | Register 0x0A05, Bit 1     |
| 0x12                | Clear DPLL_0 IRQs                             | Register 0x0A05, Bit 2     |
| 0x13                | Clear DPLL_1 IRQs                             | Register 0x0A05, Bit 3     |
| 0x14                | Clear DPLL_2 IRQs                             | Register 0x0A05, Bit 4     |
| 0x15                | Clear DPLL_3 IRQs                             | Register 0x0A05, Bit 5     |
| 0x20/0x21/0x22/0x23 | Force fault REFA/REFB/REFC/REFD               | Register 0x0A03, Bits[3:0] |
| 0x28/0x29/0x2A/0x2B | Force validation timeout REFA/REFB/REFC/REFD  | Register 0x0A02, Bits[3:0] |
| 0x40                | PLL_0 power-down                              | Register 0x0A20, Bit 0     |
| 0x41                | DPLL_0 user free run                          | Register 0x0A22, Bit 0     |
| 0x42                | DPLL_0 user holdover                          | Register 0x0A22, Bit 1     |
| 0x43                | DPLL_0 tuning word history reset              | Register 0x0A23, Bit 1     |
| 0x44                | DPLL_0 increment phase offset                 | Register 0x0A24, Bit 0     |
| 0x45                | DPLL_0 decrement phase offset                 | Register 0x0A24, Bit 1     |
| 0x46                | DPLL_0 reset phase offset                     | Register 0x0A24, Bit 2     |
| 0x48                | APLL_0 soft sync                              | Register 0x0A20, Bit 2     |
| 0x49                | PLL_0 disable OUT0B                           | Register 0x0A21, Bit 2     |
| 0x4A                | Unused                                        |                            |
| 0x4B                | PLL_0 disable OUT0B                           | Register 0x0A21, Bit 3     |
| 0x4C                | PLL_0 manual reference input selection, Bit 0 | Register 0x0A22, Bit 5     |
| 0x4D                | PLL_0 manual reference input selection, Bit 1 | Register 0x0A22, Bit 6     |
| 0x50                | PLL_1 power-down                              | Register 0x0A40, Bit 0     |
| 0x51                | DPLL_1 user free run                          | Register 0x0A42, Bit 0     |
| 0x52                | DPLL_1 user holdover                          | Register 0x0A42, Bit 1     |
| 0x53                | DPLL_1 tuning word history reset              | Register 0x0A43, Bit 1     |
| 0x54                | DPLL_1 increment phase offset                 | Register 0x0A44, Bit 0     |
| 0x55                | DPLL_1 decrement phase offset                 | Register 0x0A44, Bit 1     |
| 0x56                | DPLL_1 reset phase offset                     | Register 0x0A44, Bit 2     |
| 0x58                | APLL_1 soft sync                              | Register 0x0A40, Bit 2     |
| 0x59                | PLL_1 disable OUT1B                           | Register 0x0A41, Bit 2     |
| 0x5A                | Unused                                        |                            |
| 0x5B                | PLL_1 disable OUT1B                           | Register 0x0A41, Bit 3     |
| 0x5C                | PLL_1 manual reference input selection, Bit 0 | Register 0x0A42, Bit 5     |
| 0x5D                | PLL_1 manual reference input selection, Bit 1 | Register 0x0A42, Bit 6     |
| 0x60                | PLL_2 power-down                              | Register 0x0A60, Bit 0     |
| 0x61                | DPLL_2 user free run                          | Register 0x0A62, Bit 0     |
| 0x62                | DPLL_2 user holdover                          | Register 0x0A62, Bit 1     |
| 0x63                | DPLL_2 tuning word history reset              | Register 0x0A63, Bit 1     |
| 0x64                | DPLL_2 increment phase offset                 | Register 0x0A64, Bit 0     |
| 0x65                | DPLL_2 decrement phase offset                 | Register 0x0A64, Bit 1     |
| 0x66                | DPLL_2 reset phase offset                     | Register 0x0A64, Bit 2     |
| 0x68                | APLL_2 soft sync                              | Register 0x0A60, Bit 2     |
| 0x69                | PLL_2 disable OUT2B                           | Register 0x0A61, Bit 2     |
| 0x6A                | Unused                                        |                            |
| 0x6B                | PLL_2 disable OUT2B                           | Register 0x0A61, Bit 3     |
| 0x6C                | PLL_2 manual reference input selection, Bit 0 | Register 0x0A62, Bit 5     |
| 0x6D                | PLL_2 manual reference input selection, Bit 1 | Register 0x0A62, Bit 6     |

| Bits[D7:D0] Value | Input Function                                | Destination Proxy      |
|-------------------|-----------------------------------------------|------------------------|
| 0x70              | PLL_2 power-down                              | Register 0x0A60, Bit 0 |
| 0x71              | DPLL_3 user free run                          | Register 0x0A82, Bit 0 |
| 0x72              | DPLL_3 user holdover                          | Register 0x0A82, Bit 1 |
| 0x73              | DPLL_3 tuning word history reset              | Register 0x0A83, Bit 1 |
| 0x74              | DPLL_3 increment phase offset                 | Register 0x0A84, Bit 0 |
| 0x75              | DPLL_3 decrement phase offset                 | Register 0x0A84, Bit 1 |
| 0x76              | DPLL_3 reset phase offset                     | Register 0x0A84, Bit 2 |
| 0x78              | APLL_3 soft sync                              | Register 0x0A80, Bit 2 |
| 0x79              | PLL_3 disable OUT3B                           | Register 0x0A81, Bit 2 |
| 0x7A              | Unused                                        |                        |
| 0x7B              | PLL_3 disable OUT3B                           | Register 0x0A81, Bit 3 |
| 0x7C              | PLL_3 manual reference input selection, Bit 0 | Register 0x0A82, Bit 5 |
| 0x7D              | PLL_3 manual reference input selection, Bit 1 | Register 0x0A82, Bit 6 |
| 0x7E to 0x7F      | Reserved                                      | None                   |

OUTLINE DIMENSIONS



\*COMPLIANT TO JEDEC STANDARDS MO-220-WLLD-5 WITH EXCEPTION TO EXPOSED PAD DIMENSION.

Figure 44. 56-Lead Lead Frame Chip Scale Package [LFCSP\_WQ]  
8 mm × 8 mm Body, Very Very Thin Quad  
(CP-56-10)  
Dimensions shown in millimeters

ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                              | Package Option |
|--------------------|-------------------|--------------------------------------------------|----------------|
| AD9554-1BCPZ       | -40°C to +85°C    | 56-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-56-10       |
| AD9554-1BCPZ-REEL7 | -40°C to +85°C    | 56-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-56-10       |
| AD9554-1/PCBZ      |                   | Evaluation Board                                 |                |

<sup>1</sup> Z = RoHS Compliant Part.

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).