10-Bit, 125/105 MSPS, 1.8 V Dual Analog-to-Digital Converter (ADC)

Data Sheet **AD9608**

FEATURES

- 1.8 V analog supply operation
- 1.8 V CMOS or 1.8 V LVDS output
- SNR = 61.7 dBFS at 70 MHz
- SFDR = 85 dBc at 70 MHz
- Low power: 95 mW/channel at 125 MSPS
- Differential analog input with 650 MHz bandwidth
- IF sampling frequencies to 200 MHz
- On-chip voltage reference and sample-and-hold circuit
- 2 V p-p differential analog input
- DNL = ±0.13 LSB
- Serial port control options
  - Offset binary, Gray code, or twos complement data format
  - Optional clock duty cycle stabilizer
  - Integer 1-to-8 input clock divider
  - Data output multiplex option
  - Built-in selectable digital test pattern generation
  - Energy-saving power-down modes
  - Data clock out with programmable clock and data alignment

APPLICATIONS

- Communications
- Diversity radio systems
- I/Q demodulation systems
- Broadband data applications
- Battery-powered instruments
- Handheld scope meters
- Portable medical imaging
- Ultrasound

FUNCTIONAL BLOCK DIAGRAM

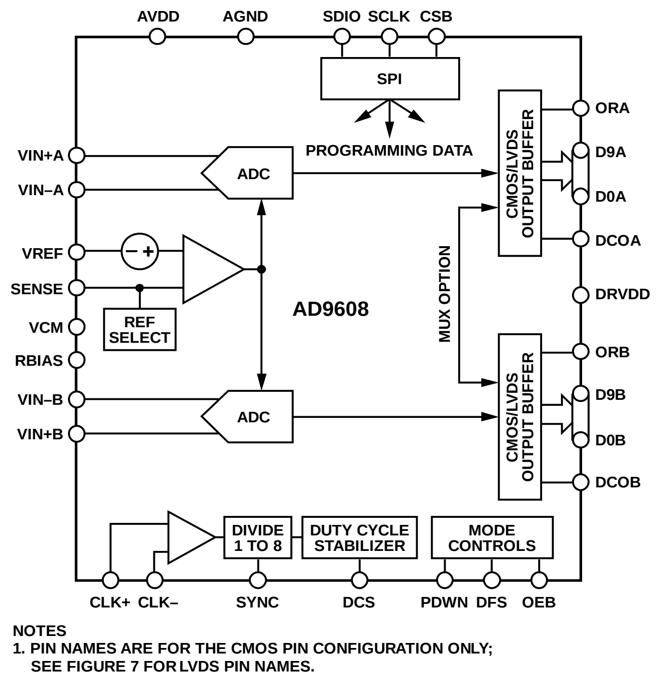

Figure 1.

PRODUCT HIGHLIGHTS

1. Operates from a single 1.8 V analog power supply and features a separate digital output driver supply to accommodate 1.8 V CMOS or 1.8 V LVDS logic families.
2. The patented sample-and-hold circuit maintains excellent performance for input frequencies up to 200 MHz and is designed for low cost, low power, and ease of use.
3. Includes a standard serial port interface that supports various product features and functions, such as data output formatting, internal clock divider, power-down, DCO/data timing, and offset adjustments.
4. Packaged in a 64-lead, RoHS-compliant LFCSP that is pin compatible with the AD9650, AD9269, and AD9268 16-bit ADCs, the AD9258 and AD9648 14-bit ADCs, the AD9628 and AD9231 12-bit ADCs, and the AD9204 10-bit ADC, enabling a simple migration path between 10-bit and 16-bit converters sampling from 20 MSPS to 125 MSPS.

Rev. C Document Feedback

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AD9608* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9608 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-282: Fundamentals of Sampled Data Systems
- AN-737: How ADIsimADC Models an ADC
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-803: Pin Compatible High Speed ADCs Simplify Design Tasks
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9608: 10-Bit, 125/105 MSPS, 1.8 V Dual Analog-to-Digital Converter (ADC) Data Sheet

User Guides

- UG-003: Evaluating the AD9650/AD9268/AD9258/AD9251/AD9231/AD9204 Analog-to-Digital Converters

TOOLS AND SIMULATIONS

- Visual Analog
- AD9608 IBIS Model
- AD9648/AD9628/AD9608 S-Parameters

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9608 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9608 EngineerZone Discussions.

SAMPLE AND BUY

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TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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11/15—Rev. B to Rev. C

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8/15—Rev. A to Rev. B

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7/11—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9608 is a monolithic, dual-channel, 1.8 V supply, 10-bit, 105 MSPS/125 MSPS analog-to-digital converter (ADC) that features a high performance sample-and-hold circuit and an on-chip voltage reference.

The product uses multistage differential pipeline architecture with output error correction logic to provide 10-bit accuracy at 125 MSPS data rates and to guarantee no missing codes over the full operating temperature range.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

A differential clock input controls all internal conversion cycles. An optional duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance.

The digital output data is presented in offset binary, Gray code, or twos complement format. A data output clock (DCO) is provided for each ADC channel to ensure proper latch timing with receiving logic. Logic levels of 1.8 V CMOS and 1.8 V LVDS are supported. Output data can also be multiplexed onto a single output bus.

The AD9608 is available in a 64-lead RoHS-compliant LFCSP and is specified over the industrial temperature range (−40°C to +85°C).

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 1.

Parameter	Temp	AD9608-105			AD9608-125			Unit
		Min	Typ	Max	Min	Typ	Max	
RESOLUTION	Full	10			10			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full	−1.0	−0.3	+0.4	−1.0	−0.3	+0.4	% FSR
Gain Error	Full	−2.8	±1.5	+9.0	−2.8	±1.5	+9.0	% FSR
Differential Nonlinearity (DNL)[1]	Full			±0.35			±0.35	LSB
	25°C		±0.12			±0.13		LSB
Integral Nonlinearity (INL)[1]	Full			±0.40			±0.40	LSB
	25°C		±0.14			±0.14		LSB
MATCHING CHARACTERISTIC								
Offset Error	Full		±0.1	±1.0		±0.1	±1.0	% FSR
Gain Error	Full		±0.5	±6.5		±0.5	±6.5	% FSR
TEMPERATURE DRIFT								
Offset Error	Full		±2			±2		ppm/°C
Gain Error	Full		±50			±50		ppm/°C
INTERNAL VOLTAGE REFERENCE								
Output Voltage (1 V Mode)	Full	0.98	1.00	1.02	0.98	1.00	1.02	V
Load Regulation Error at 1.0 mA	Full		2			2		mV
INPUT REFERRED NOISE								
VREF = 1.0 V	25°C		0.08			0.08		LSB rms
ANALOG INPUT								
Input Span, VREF = 1.0 V	Full		2			2		V p-p
Input Capacitance[2]	Full		5			5		pF
Input Resistance (Differential)	Full		7.5			7.5		kΩ
Input Common-Mode Voltage	Full		0.9			0.9		V
Input Common-Mode Range	Full	0.5		1.3	0.5		1.3	V
POWER SUPPLIES								
Supply Voltage								
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current								
I_{AVDD}[1]	Full		76.8	82.0		87.7	93.0	mA
I_{DRVDD}[1] (1.8 V CMOS)	Full		14.7			17.4		mA
I_{DRVDD}[1] (1.8 V LVDS)	Full		48.5			49.7		mA
POWER CONSUMPTION								
DC Input	Full		125			141		mW
Sine Wave Input[1] (DRVDD = 1.8 V CMOS Output Mode)	Full		165	174		189	199	mW
Sine Wave Input[1] (DRVDD = 1.8 V LVDS Output Mode)	Full		226			247		mW
Standby Power[3]	Full		108			120		mW
Power-Down Power	Full		2.0			2.0		mW

[1] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND.
[3] Standby power is measured with a dc input and with the CLK± pins active (1.8 V CMOS mode).

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 2.

Parameter[1]	Temp	AD9608-105 Min	AD9608-105 Typ	AD9608-105 Max	AD9608-125 Min	AD9608-125 Typ	AD9608-125 Max	Unit
SIGNAL-TO-NOISE-RATIO (SNR)								
f_{IN} = 9.7 MHz	25°C		61.7			61.7		dBFS
f_{IN} = 30.5 MHz	25°C		61.7			61.7		dBFS
f_{IN} = 70 MHz	25°C		61.7			61.7		dBFS
	Full	61.3			61.3			dBFS
f_{IN} = 100 MHz	25°C		61.6			61.6		dBFS
f_{IN} = 200 MHz	25°C		61.4			61.4		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)								
f_{IN} = 9.7 MHz	25°C		61.6			61.6		dBFS
f_{IN} = 30.5 MHz	25°C		61.6			61.6		dBFS
f_{IN} = 70 MHz	25°C		61.6			61.6		dBFS
	Full	61.1			61.1			dBFS
f_{IN} = 100 MHz	25°C		61.5			61.5		dBFS
f_{IN} = 200 MHz	25°C		61.3			61.3		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 9.7 MHz	25°C		9.9			9.9		Bits
f_{IN} = 30.5 MHz	25°C		9.9			9.9		Bits
f_{IN} = 70 MHz	25°C		9.9			9.9		Bits
f_{IN} = 100 MHz	25°C		9.9			9.9		Bits
f_{IN} = 200 MHz	25°C		9.9			9.9		Bits
WORST SECOND OR THIRD HARMONIC								
f_{IN} = 9.7 MHz	25°C		−90			−90		dBc
f_{IN} = 30.5 MHz	25°C		−89			−89		dBc
f_{IN} = 70 MHz	25°C		−89			−89		dBc
	Full			−75			−75	dBc
f_{IN} = 100 MHz	25°C		−89			−89		dBc
f_{IN} = 200 MHz	25°C		−84			−84		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 9.7 MHz	25°C		85			85		dBc
f_{IN} = 30.5 MHz	25°C		85			85		dBc
f_{IN} = 70 MHz	25°C		85			85		dBc
	Full	75			75			dBc
f_{IN} = 100 MHz	25°C		85			85		dBc
f_{IN} = 200 MHz	25°C		84			84		dBc
WORST OTHER (HARMONIC OR SPUR)								
f_{IN} = 9.7 MHz	25°C		−85			−85		dBc
f_{IN} = 30.5 MHz	25°C		−85			−85		dBc
f_{IN} = 70 MHz	25°C		−85			−85		dBc
	Full			−75			−75	dBc
f_{IN} = 100 MHz	25°C		−85			−85		dBc
f_{IN} = 200 MHz	25°C		−85			−85		dBc
TWO-TONE SFDR								
f_{IN} = 29 MHz (−7 dBFS), 32 MHz (−7 dBFS)	25°C		82			82		dBc
CROSSTALK[2]	Full		−95			−95		dB
ANALOG INPUT BANDWIDTH	25°C		650			650		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured at 100 MHz with −1.0 dBFS on one channel and no input on the alternate channel.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temp	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND − 0.3		AVDD + 0.2	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	−10		+10	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
LOGIC INPUT (CSB)[1]					
High Level Input Voltage	Full	1.22		DRVDD + 0.2	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		132	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK/DFS/SYNC)[2]					
High Level Input Voltage	Full	1.22		DRVDD + 0.2	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (VIN = 1.8 V)	Full	−92		−135	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT/OUTPUT (SDIO/DCS)[1]					
High Level Input Voltage	Full	1.22		DRVDD + 0.2	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	38		128	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
LOGIC INPUTS (OEB, PDWN)[2]					
High Level Input Voltage	Full	1.22		DRVDD + 0.2	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (VIN = 1.8 V)	Full	−90		−134	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS					
CMOS Mode—DRVDD = 1.8 V					
High Level Output Voltage					
I_{OH} = 50 µA	Full	1.79			V
I_{OH} = 0.5 mA	Full	1.75			V
Low Level Output Voltage					
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V

Parameter	Temp	Min	Typ	Max	Unit
LVDS Mode—DRVDD = 1.8 V					
Differential Output Voltage (V_{OD}), ANSI Mode	Full	290	345	400	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full	1.15	1.25	1.35	V
Differential Output Voltage (V_{OD}), Reduced Swing Mode	Full	160	200	230	mV
Output Offset Voltage (V_{OS}), Reduced Swing Mode	Full	1.15	1.25	1.35	V

[1] Pull up.
[2] Pull down.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

Table 4.

Parameter	Temp	AD9608-105			AD9608-125			Unit
		Min	Typ	Max	Min	Typ	Max	
CLOCK INPUT PARAMETERS								
Input Clock Rate	Full			1000			1000	MHz
Conversion Rate[1]								
DCS Enabled	Full	20		105	20		125	MSPS
DCS Disabled	Full	10		105	10		125	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full		9.52			8		ns
CLK Pulse Width High (t_{CH})	Full		4.76			4		ns
Aperture Delay (t_A)	Full		1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.137			0.137		ps rms
DATA OUTPUT PARAMETERS								
CMOS Mode								
CMOS Mode (DRVDD = 1.8 V)								
Data Propagation Delay (t_{PD})	Full	1.8	2.9	4.4	1.8	2.9	4.4	ns
DCO Propagation Delay (t_{DCO})[2]	Full	2.0	3.1	4.4	2.0	3.1	4.4	ns
DCO to Data Skew (t_{SKEW})	Full	−1.2	−0.1	+1.0	−1.2	−0.1	+1.0	ns
LVDS Mode (DRVDD = 1.8 V)								
Data Propagation Delay (t_{PD})	Full		2.4			2.4		ns
DCO Propagation Delay (t_{DCO})[2]	Full		4.4			4.4		ns
DCO to Data Skew (t_{SKEW})	Full	−0.1	+0.2	+0.5	−0.1	+0.2	+0.5	ns
CMOS Mode Pipeline Delay (Latency)	Full		16			16		Cycles
LVDS Mode Pipeline Delay (Latency) Channel A/Channel B	Full		16/16.5			16/16.5		Cycles
Wake-Up Time (Power-Down)[3]	Full		350			350		μs
Wake-Up Time (Standby)	Full		250			250		ns
Out-of-Range Recovery Time	Full		2			2		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Additional DCO delay can be added by writing to Bits[2:0] in SPI Register 0x17 (see Table 18).
[3] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Descriptions	Limit
SYNC TIMING REQUIREMENTS		
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	0.24 ns typ
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	0.40 ns typ
SPI TIMING REQUIREMENTS		
t_{DS}	Setup time between the data and the rising edge of SCLK	2 ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	40 ns min
t_{CLK}	Period of the SCLK	2 ns min
t_S	Setup time between CSB and SCLK	2 ns min
t_H	Hold time between CSB and SCLK	10 ns min
t_{HIGH}	SCLK pulse width high	10 ns min
t_{LOW}	SCLK pulse width low	10 ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10 ns min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	2 ns min

Timing Diagrams

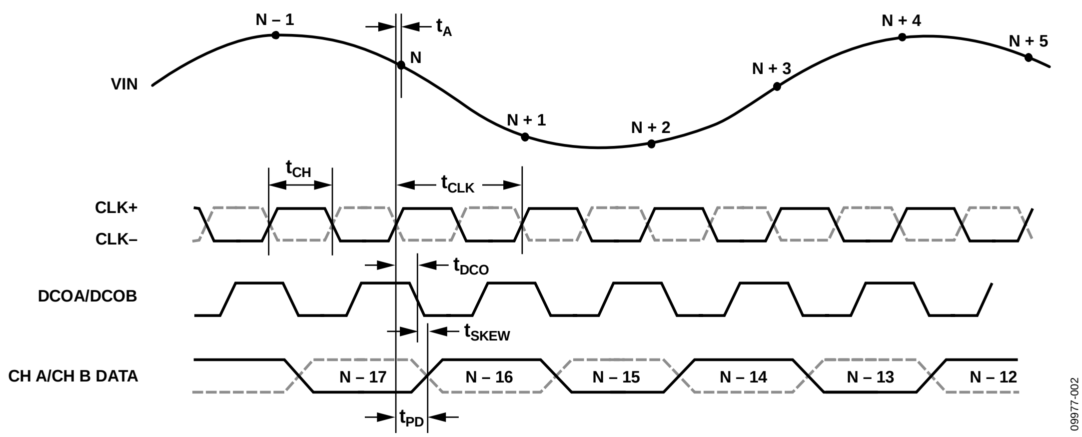


Figure 2. CMOS Default Output Mode Data Output Timing

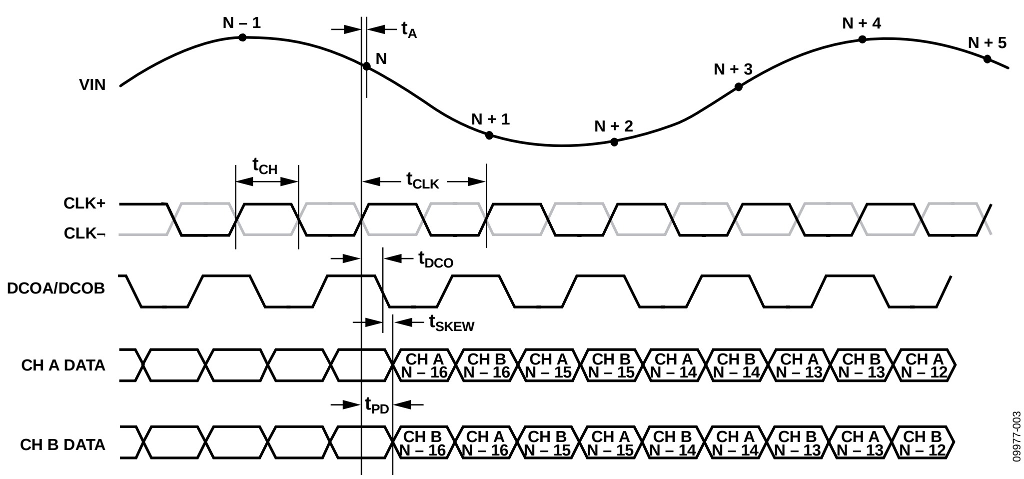


Figure 3. CMOS Interleaved Output Mode Data Output Timing

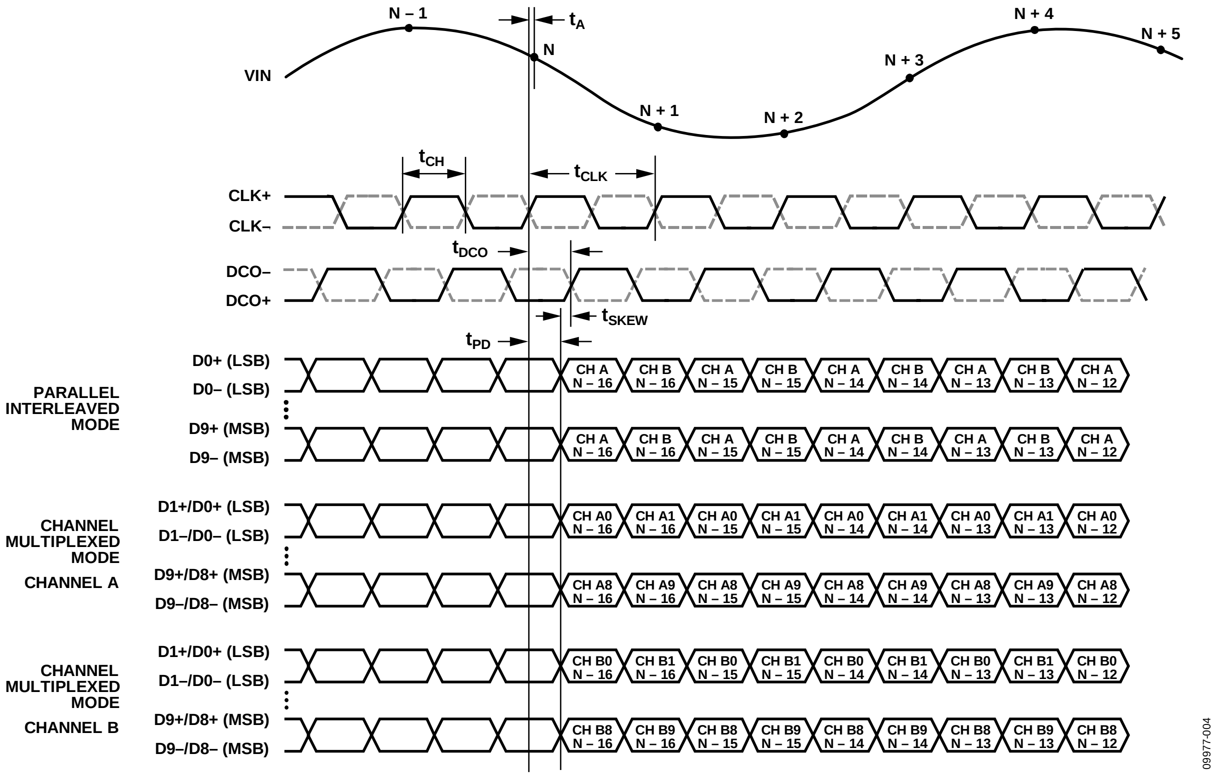


Figure 4. LVDS Modes for Data Output Timing

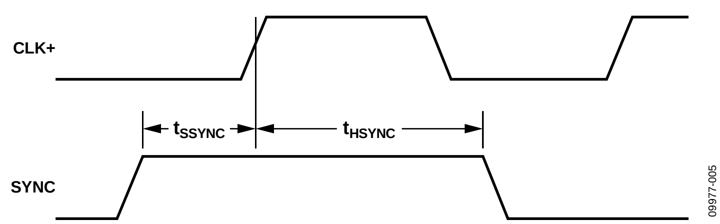


Figure 5. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
SYNC to DRVDD	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
RBIAS to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.2 V
SCLK/DFS to AGND	−0.3 V to DRVDD + 0.2 V
SDIO/DCS to AGND	−0.3 V to DRVDD + 0.2 V
OEB	−0.3 V to DRVDD + 0.2 V
PDWN	−0.3 V to DRVDD + 0.2 V
D0A, D0B through D9A, D9B to AGND	−0.3 V to DRVDD + 0.2 V
DCOA, DCOB to AGND	−0.3 V to DRVDD + 0.2 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP. Soldering the exposed paddle to the printed circuit board (PCB) increases the reliability of the solder joints and maximizes the thermal capability of the package.

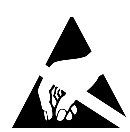
Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Ψ_{JT}[1, 2]	Unit
64-Lead LFCSP 9 mm × 9 mm (CP-64-4)	0	22.3	1.4	11.8	0.1	°C/W
	1.0	19.5	N/A[5]	N/A[5]	0.2	°C/W
	2.5	17.5	N/A[5]	N/A[5]	0.2	°C/W

[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).
[5] N/A means not applicable.

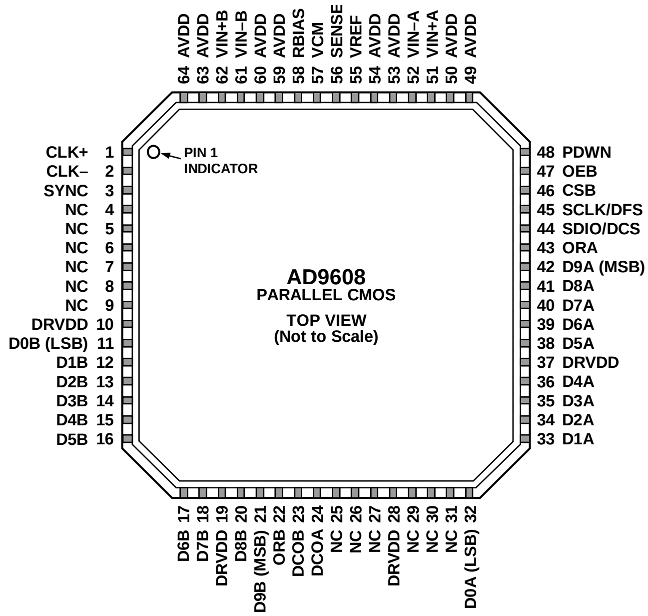
Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown Table 7, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

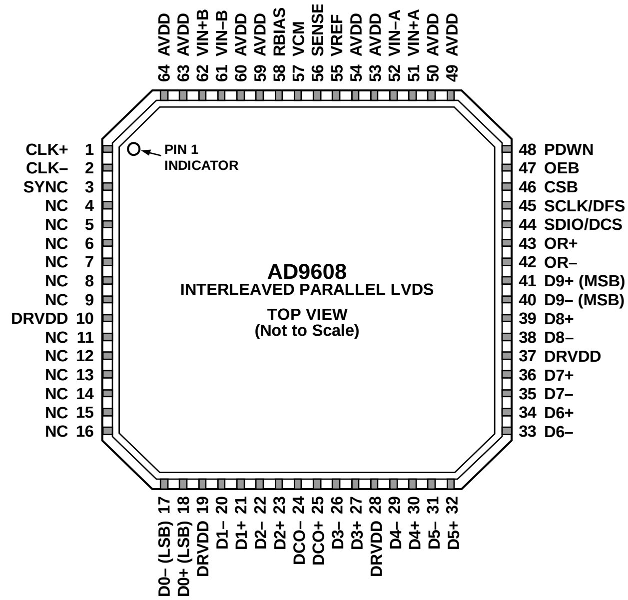
09977-006

Figure 6. Parallel CMOS Pin Configuration (Top View)

Table 8. Pin Function Descriptions (Parallel CMOS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
4, 5, 6, 7, 8, 9, 25, 26, 27, 29, 30, 31	NC		No Connect. Do not connect to this pin.
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
55	VREF	Input/Output	Voltage Reference Input/Output.
56	SENSE	Input	Reference Mode Selection.
58	RBIAS	Input/Output	External Reference Bias Resistor. Connect to 10 kΩ (1% tolerance) resistor to ground.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
1	CLK+	Input	ADC Clock Input—True.
2	CLK−	Input	ADC Clock Input—Complement.

Pin No.	Mnemonic	Type	Description
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
32	D0A (LSB)	Output	Channel A CMOS Output Data.
33	D1A	Output	Channel A CMOS Output Data.
34	D2A	Output	Channel A CMOS Output Data.
35	D3A	Output	Channel A CMOS Output Data.
36	D4A	Output	Channel A CMOS Output Data.
38	D5A	Output	Channel A CMOS Output Data.
39	D6A	Output	Channel A CMOS Output Data.
40	D7A	Output	Channel A CMOS Output Data.
41	D8A	Output	Channel A CMOS Output Data.
42	D9A (MSB)	Output	Channel A CMOS Output Data.
43	ORA	Output	Channel A Overrange Output.
11	D0B (LSB)	Output	Channel B CMOS Output Data.
12	D1B	Output	Channel B CMOS Output Data.
13	D2B	Output	Channel B CMOS Output Data.
14	D3B	Output	Channel B CMOS Output Data.
15	D4B	Output	Channel B CMOS Output Data.
16	D5B	Output	Channel B CMOS Output Data.
17	D6B	Output	Channel B CMOS Output Data.
18	D7B	Output	Channel B CMOS Output Data.
20	D8B	Output	Channel B CMOS Output Data.
21	D9B (MSB)	Output	Channel B CMOS Output Data.
22	ORB	Output	Channel B Overrange Output
24	DCOA	Output	Channel A Data Clock Output.
23	DCOB	Output	Channel B Data Clock Output.
SPI Control			
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
44	SDIO/DCS	Input/Output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
46	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
47	OEB	Input	Output Enable Input (Active Low).
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

09977-007

Figure 7. Interleaved Parallel LVDS Pin Configuration (Top View)

Table 9. Pin Function Descriptions (Interleaved Parallel LVDS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16	NC		No Connect. Do not connect to this pin.
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
55	VREF	Input/Output	Voltage Reference Input/Output.
56	SENSE	Input	Reference Mode Selection.
58	RBIAS	Input/Output	External Reference Bias Resistor. Connect to 10 kΩ (1% tolerance) resistor to ground.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
1	CLK+	Input	ADC Clock Input—True.
2	CLK−	Input	ADC Clock Input—Complement.
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.

Pin No.	Mnemonic	Type	Description
Digital Outputs			
18	D0+ (LSB)	Output	Channel A/Channel B LVDS Output Data 0—True.
17	D0− (LSB)	Output	Channel A/Channel B LVDS Output Data 0—Complement.
21	D1+	Output	Channel A/Channel B LVDS Output Data 1—True.
20	D1−	Output	Channel A/Channel B LVDS Output Data 1—Complement.
23	D2+	Output	Channel A/Channel B LVDS Output Data 2 —True.
22	D2−	Output	Channel A/Channel B LVDS Output Data 2—Complement.
27	D3+	Output	Channel A/Channel B LVDS Output Data 3—True.
26	D3−	Output	Channel A/Channel B LVDS Output Data 3—Complement.
30	D4+	Output	Channel A/Channel B LVDS Output Data 4—True.
29	D4−	Output	Channel A/Channel B LVDS Output Data 4—Complement.
32	D5+	Output	Channel A/Channel B LVDS Output Data 5—True.
31	D5−	Output	Channel A/Channel B LVDS Output Data 5—Complement.
34	D6+	Output	Channel A/Channel B LVDS Output Data 6—True.
33	D6−	Output	Channel A/Channel B LVDS Output Data 6—Complement.
36	D7+	Output	Channel A/Channel B LVDS Output Data 7—True.
35	D7−	Output	Channel A/Channel B LVDS Output Data 7—Complement.
39	D8+	Output	Channel A/Channel B LVDS Output Data 8—True.
38	D8−	Output	Channel A/Channel B LVDS Output Data 8—Complement.
41	D9+ (MSB)	Output	Channel A/Channel B LVDS Output Data 9—True.
40	D9− (MSB)	Output	Channel A/Channel B LVDS Output Data 9—Complement.
43	OR+	Output	Channel A/Channel B LVDS Overrange Output—True.
42	OR−	Output	Channel A/Channel B LVDS Overrange Output—Complement.
25	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
24	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
44	SDIO/DCS	Input/Output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
46	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
47	OEB	Input	Output Enable Input (Active Low).
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.

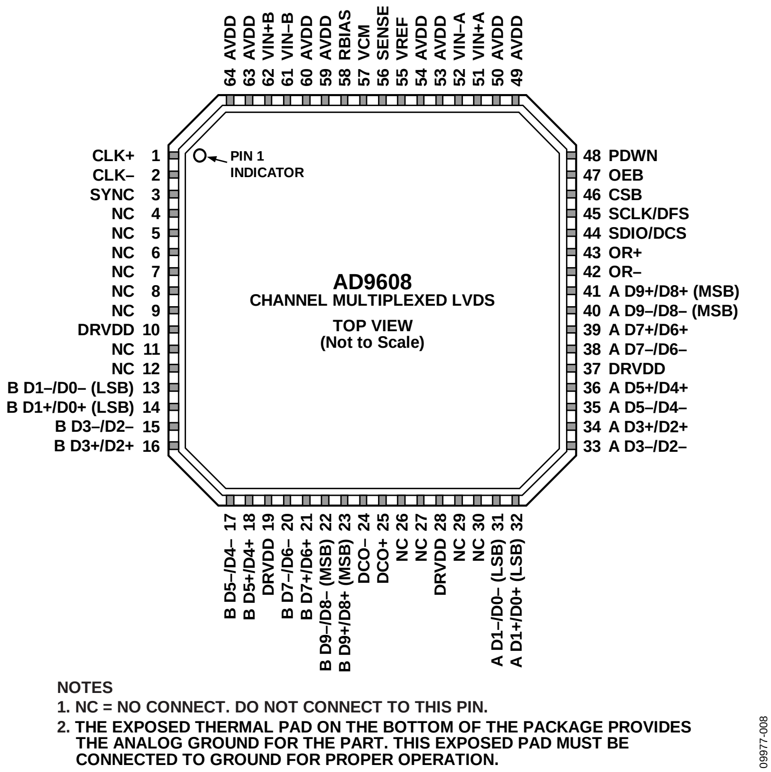


Figure 8. Channel Multiplexed LVDS Pin Configuration (Top View)

Table 10. Pin Function Descriptions (Channel Multiplexed Parallel LVDS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
4, 5, 6, 7, 8, 9, 11, 12, 26, 27, 29, 30	NC		No Connect. Do not connect to this pin.
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
55	VREF	Input/Output	Voltage Reference Input/Output.
56	SENSE	Input	Reference Mode Selection.
58	RBIAS	Input/Output	External Reference Bias Resistor. Connect to 10 kΩ (1% tolerance) resistor to ground.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
1	CLK+	Input	ADC Clock Input—True.
2	CLK−	Input	ADC Clock Input—Complement.
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.

Pin No.	Mnemonic	Type	Description
Digital Outputs			
14	B D1+/D0+ (LSB)	Output	Channel B LVDS Output Data 1/ Data 0—True.
13	B D1−/D0− (LSB)	Output	Channel B LVDS Output Data 1/ Data 0—Complement.
16	B D3+/D2+	Output	Channel B LVDS Output Data 3/ Data 2—True.
15	B D3−/D2−	Output	Channel B LVDS Output Data 3/ Data 2—Complement.
18	B D5+/D4+	Output	Channel B LVDS Output Data 5/ Data 4—True.
17	B D5−/D4−	Output	Channel B LVDS Output Data 5/ Data 4—Complement.
21	B D7+/D6+	Output	Channel B LVDS Output Data 7/ Data 6—True.
20	B D7−/D6−	Output	Channel B LVDS Output Data 7/ Data 6—Complement.
23	B D9+/D8+ (MSB)	Output	Channel B LVDS Output Data 9/ Data 8—True.
22	B D9−/D8− (MSB)	Output	Channel B LVDS Output Data 9/ Data 8—Complement.
32	A D1+/D0+ (LSB)	Output	Channel A LVDS Output Data 1/ Data 0—True.
31	A D1−/D0− (LSB)	Output	Channel A LVDS Output Data 1/ Data 0—Complement.
34	A D3+/D2+	Output	Channel A LVDS Output Data 3/ Data 2—True.
33	A D3−/D2−	Output	Channel A LVDS Output Data 3/ Data 2—Complement.
36	A D5+/D4+	Output	Channel A LVDS Output Data 5/ Data 4—True.
35	A D5−/D4−	Output	Channel A LVDS Output Data 5/ Data 4—Complement.
39	A D7+/D6+	Output	Channel A LVDS Output Data 7/ Data 6—True.
38	A D7−/D6−	Output	Channel A LVDS Output Data 7/ Data 6—Complement.
41	A D9+/D8+ (MSB)	Output	Channel A LVDS Output Data 9/ Data 8—True.
40	A D9−/D8− (MSB)	Output	Channel A LVDS Output Data 9/ Data 8—Complement.
43	OR+	Output	Channel A/Channel B LVDS Overrange Output—True.
42	OR−	Output	Channel A/Channel B LVDS Overrange Output—Complement.
25	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
24	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
44	SDIO/DCS	Input/Output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
46	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
47	OEB	Input	Output Enable Input (Active Low).
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.

TYPICAL PERFORMANCE CHARACTERISTICS

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AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

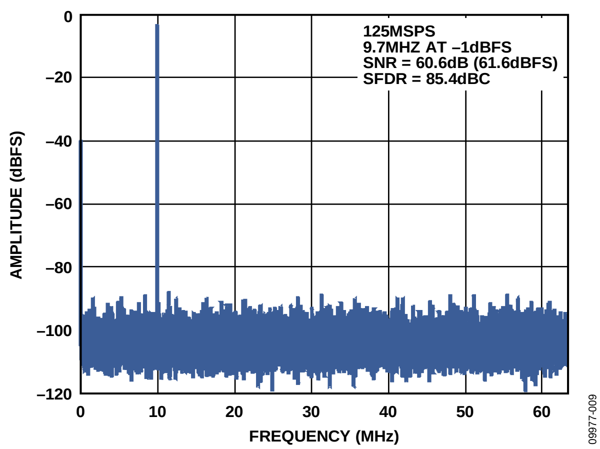

Figure 9. Single-Tone FFT with f_{IN} = 9.7 MHz

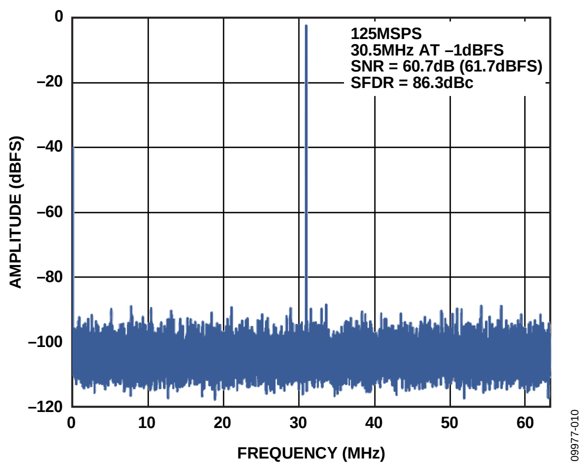

Figure 10. Single-Tone FFT with f_{IN} = 30.5 MHz

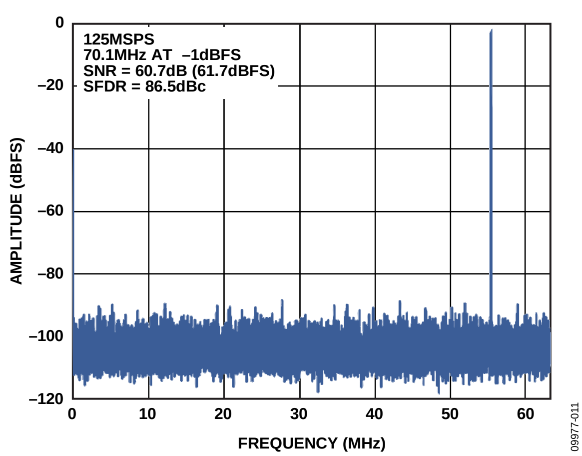

Figure 11. Single-Tone FFT with f_{IN} = 70.1 MHz

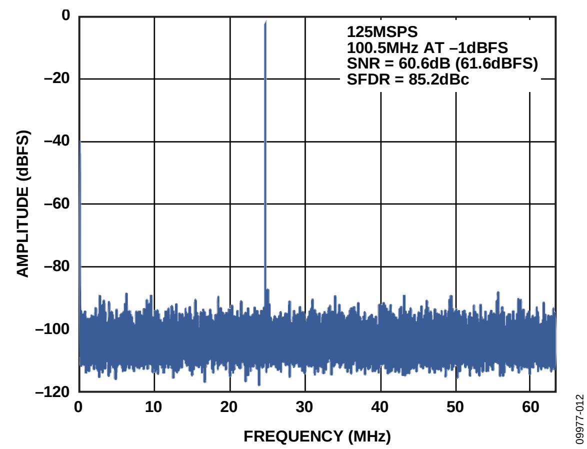

Figure 12. Single-Tone FFT with f_{IN} = 100.5 MHz

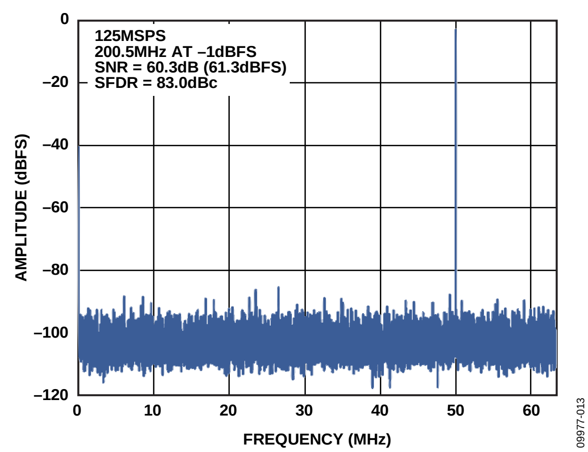

Figure 13. Single-Tone FFT with f_{IN} = 200.5 MHz

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

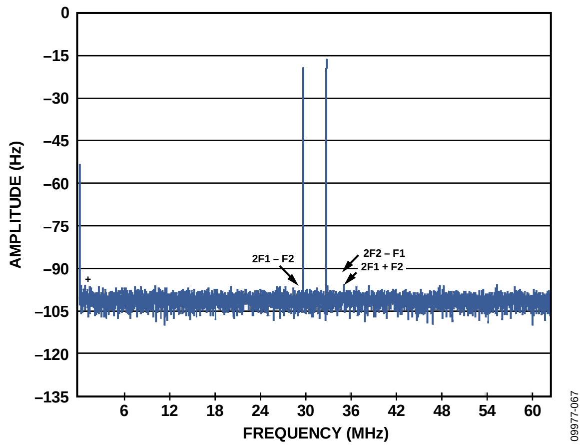

Figure 14. Two-Tone FFT with f_{IN1} = 29 MHz and f_{IN2} = 32 MHz

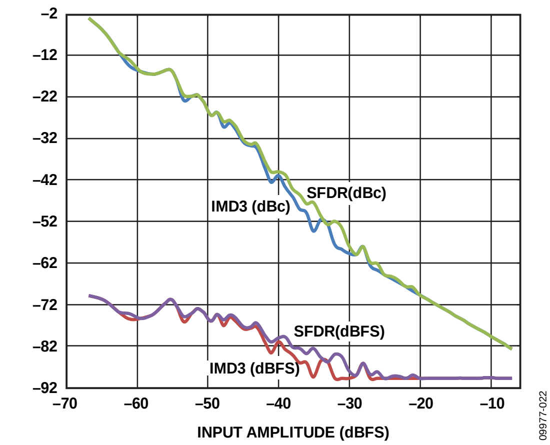

Figure 17. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with f_{IN1} = 29 MHz and f_{IN2} = 32 MHz

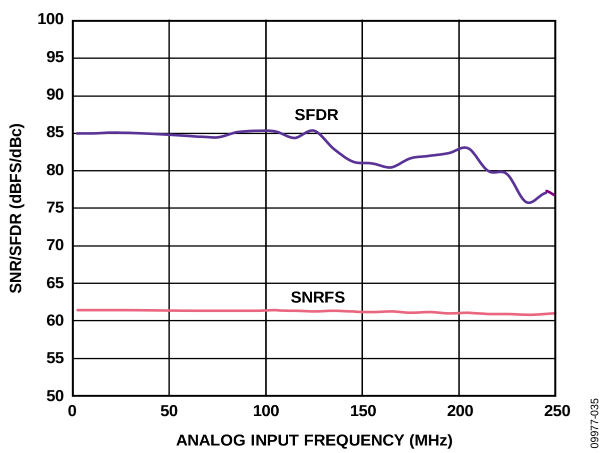

Figure 15. SNR/SFDR vs. Input Frequency (AIN) with 2 V p-p Full Scale

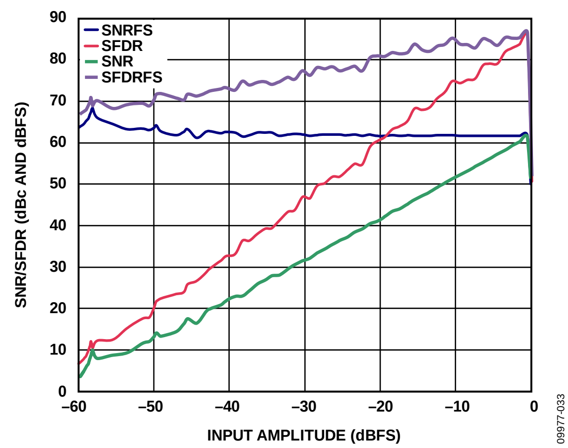

Figure 18. SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 9.7 MHz

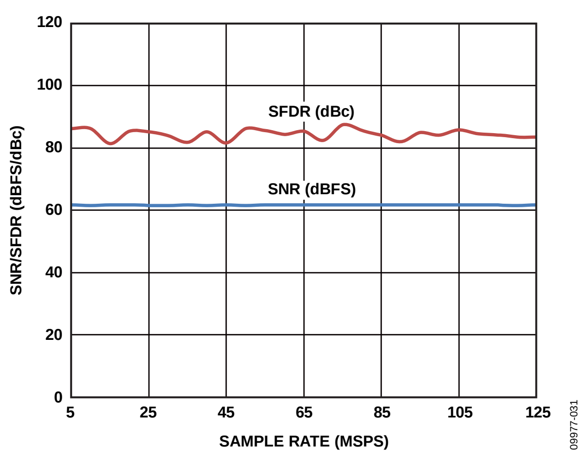

Figure 16. SNR/SFDR vs. Sample Rate with AIN = 9.7 MHz

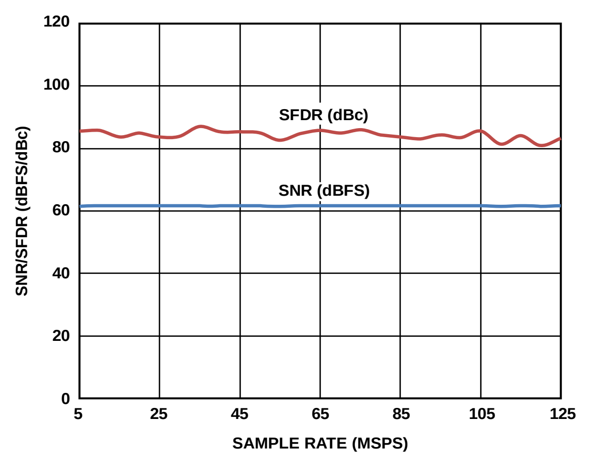

Figure 19. SNR/SFDR vs. Sample Rate with AIN = 70 MHz

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

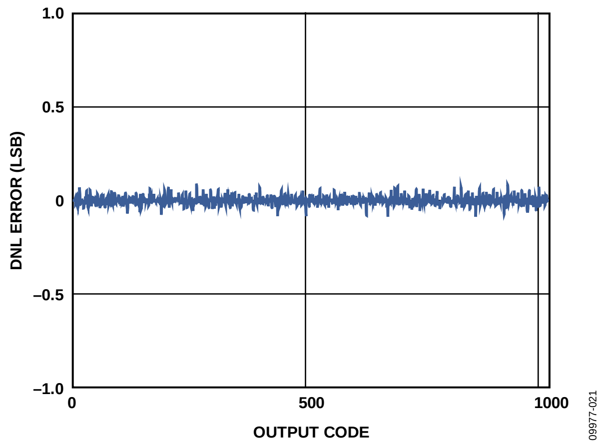

Figure 20. DNL Error with f_{IN} = 9.7 MHz

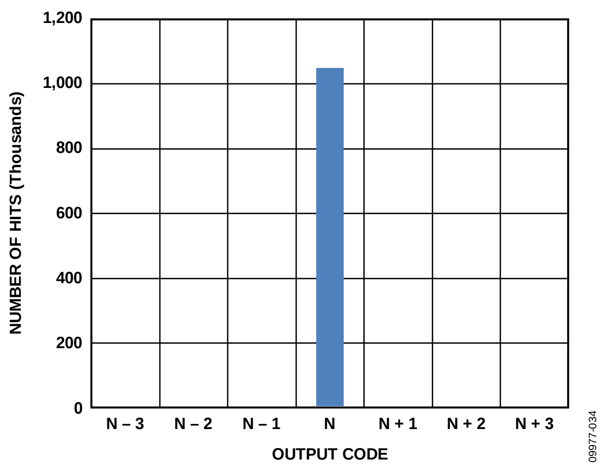

Figure 21. Shorted Input Histogram

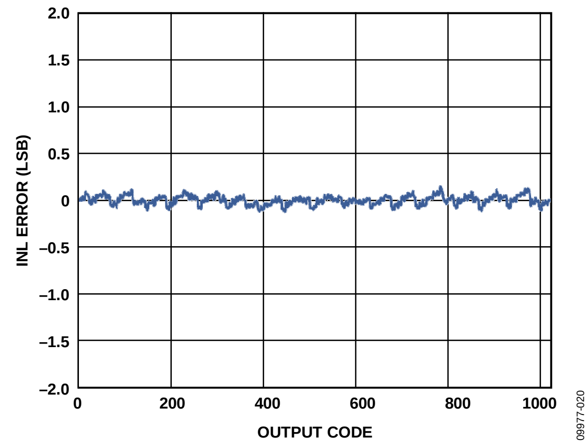

Figure 22. INL Error with f_{IN} = 9.7 MHz

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AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

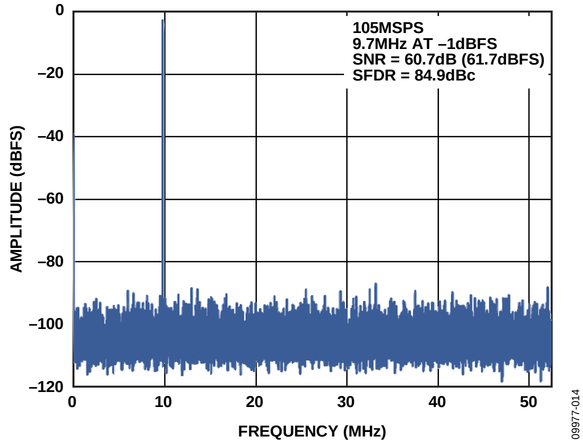

Figure 23. Single-Tone FFT with f_{IN} = 9.7 MHz

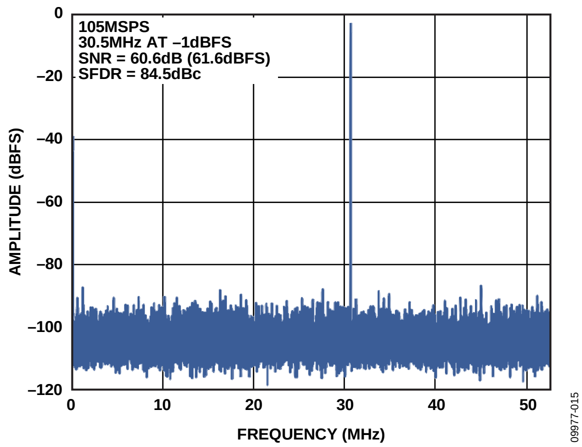

Figure 24. Single-Tone FFT with f_{IN} = 30.5 MHz

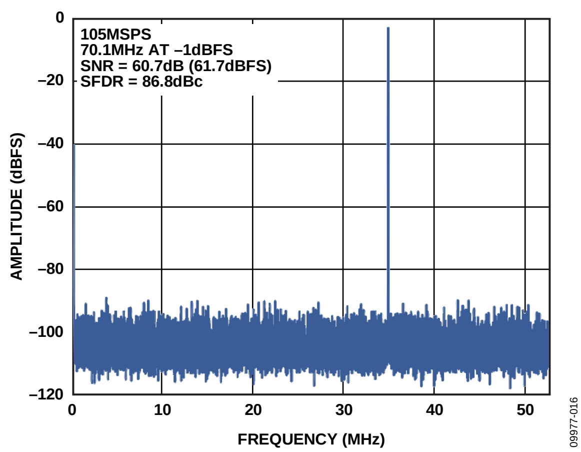

Figure 25. Single-Tone FFT with f_{IN} = 70.1 MHz

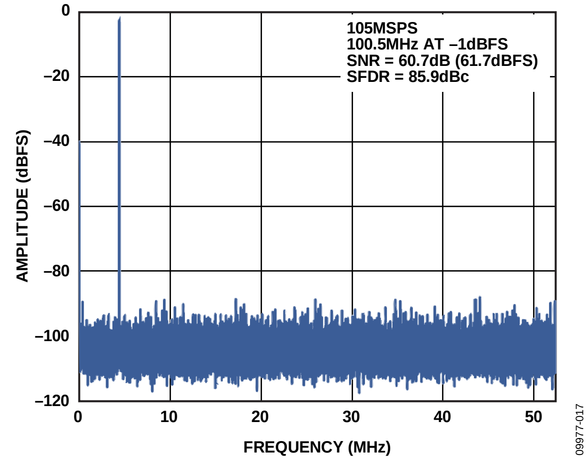

Figure 26. Single-Tone FFT with f_{IN} = 100.5 MHz

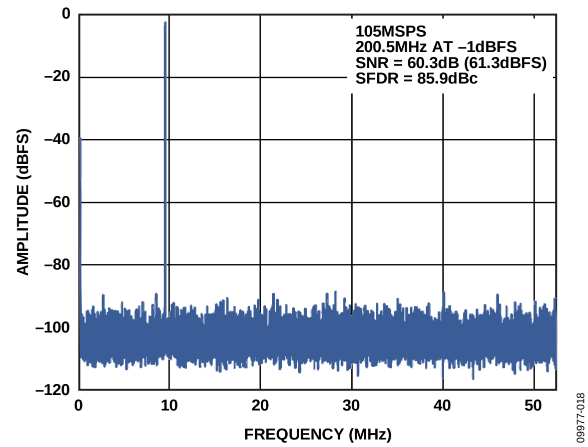

Figure 27. Single-Tone FFT with f_{IN} = 200.5 MHz

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

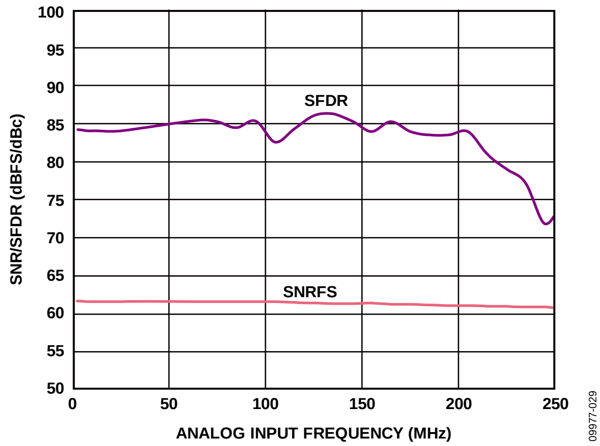

Figure 28. SNR/SFDR vs. Input Frequency (AIN) with 2 V p-p Full Scale

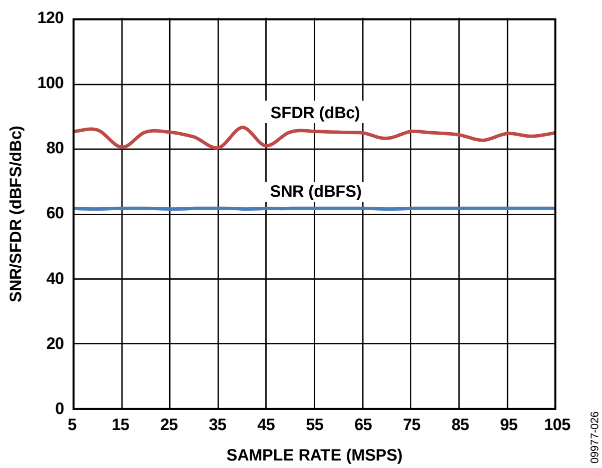

Figure 29. SNR/SFDR vs. Sample Rate with AIN = 9.7 MHz

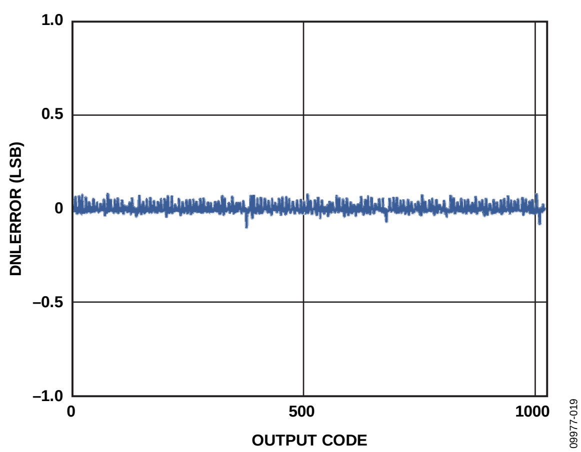

Figure 30. DNL Error with f_{IN} = 9.7 MHz

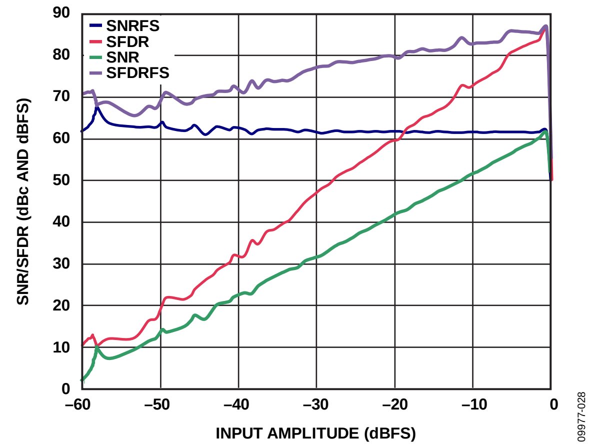

Figure 31. SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 9.7 MHz

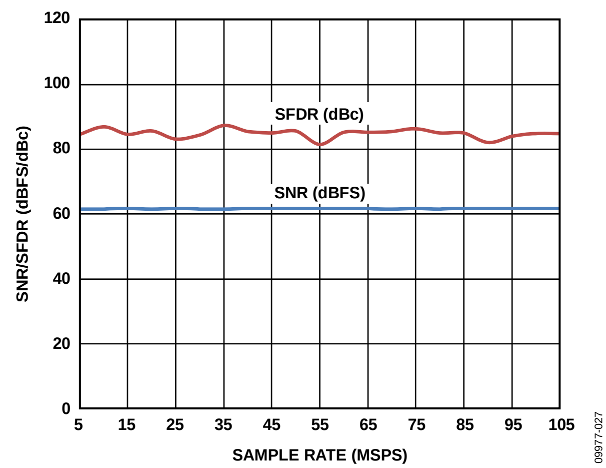

Figure 32. SNR/SFDR vs. Sample Rate with AIN = 70 MHz

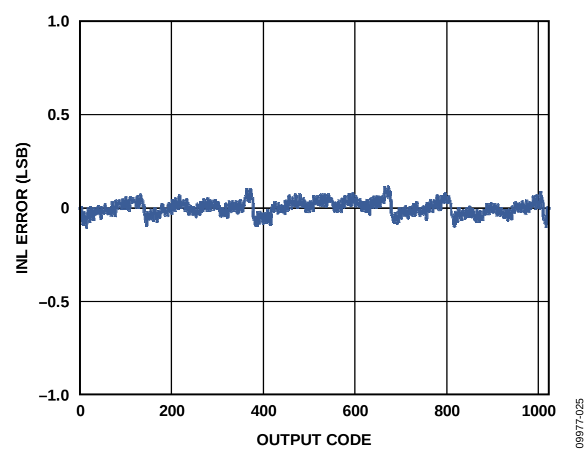

Figure 33. INL Error with f_{IN} = 9.7 MHz

EQUIVALENT CIRCUITS

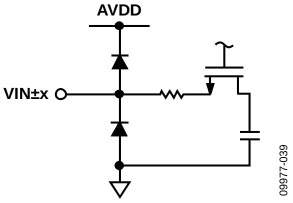

Figure 34. Equivalent Analog Input Circuit

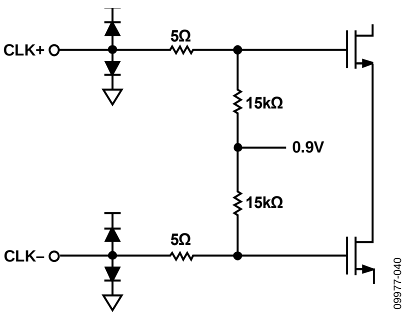

Figure 35. Equivalent Clock Input Circuit

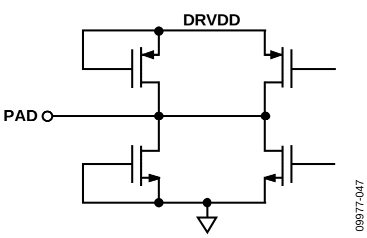

Figure 36. Equivalent Digital Output Circuit

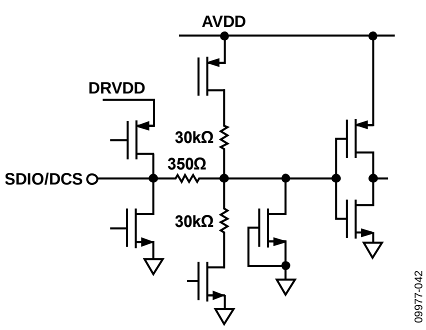

Figure 37. Equivalent SDIO/DCS Input Circuit

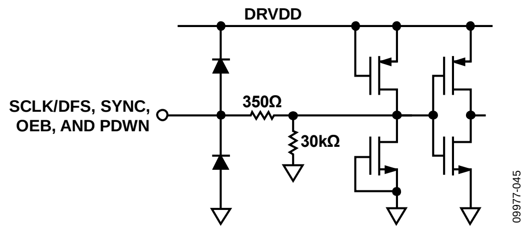

Figure 38. Equivalent SCLK/DFS, SYNC, OEB, and PDWN Input Circuit

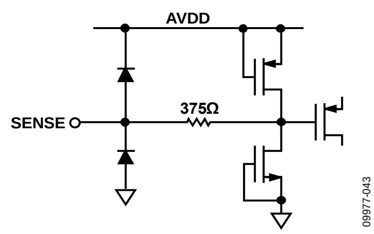

Figure 39. Equivalent SENSE Circuit

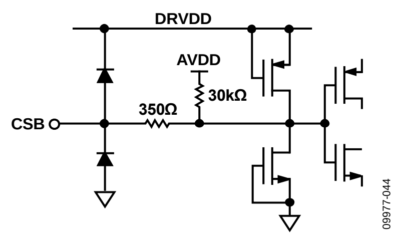

Figure 40. Equivalent CSB Input Circuit

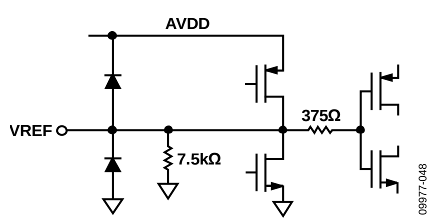

Figure 41. Equivalent VREF Circuit

THEORY OF OPERATION

The AD9608 dual ADC design can be used for diversity reception of signals, where the ADCs are operating identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample any $f_S/2$ frequency segment from dc to 200 MHz, using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. Operation to 300 MHz analog input is permitted but occurs at the expense of increased ADC noise and distortion.

In nondiversity applications, the AD9608 can be used as a baseband or direct downconversion receiver, where one ADC is used for I input data and the other is used for Q input data.

Synchronization capability is provided to allow synchronized timing between multiple channels or multiple devices.

Programming and control of the AD9608 is accomplished using a 3-bit SPI-compatible serial interface.

ADC ARCHITECTURE

The AD9608 architecture consists of a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 10-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the CMOS/LVDS output buffers. The output buffers are powered from a separate (DRVDD) supply, allowing digital output noise to be separated from the analog core. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9608 is a differential switched-capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal-dependent errors and achieve optimum performance.

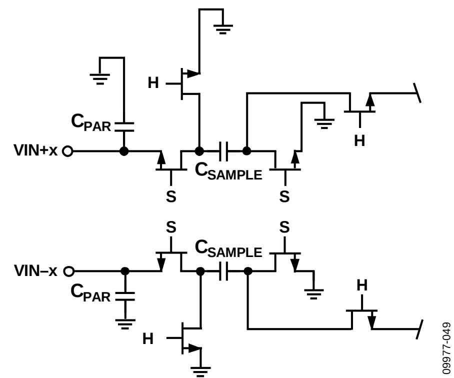

Figure 42. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample-and-hold mode (see Figure 42). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, therefore, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a shunt capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

Input Common Mode

The analog inputs of the AD9608 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide a dc bias externally. Setting the device so that VCM = AVDD/2 is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 43.

An on-board, common-mode voltage reference is included in the design and is available from the VCM pin. The VCM pin must be decoupled to ground by a 0.1 µF capacitor, as described in the Applications Information section.

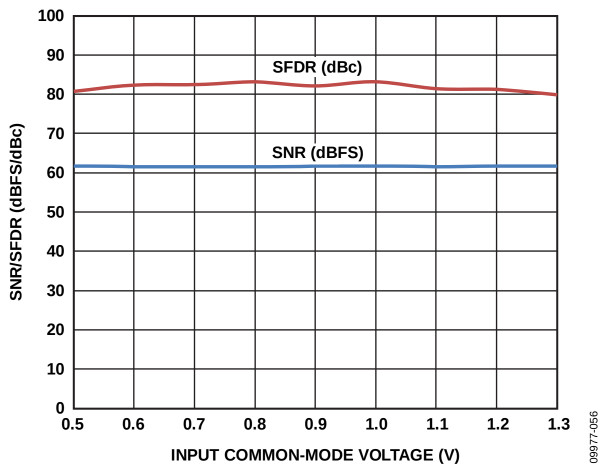

Figure 43. SNR/SFDR vs. Input Common-Mode Voltage, f_{IN} = 70 MHz, f_S = 125 MSPS

Differential Input Configurations

Optimum performance is achieved while driving the AD9608 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, and ADA4938-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4938-2 is easily set with the VCM pin of the AD9608 (see Figure 44), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

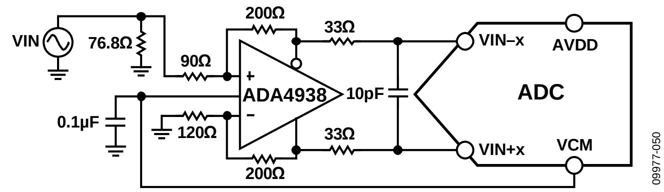

Figure 44. Differential Input Configuration Using the ADA4938-2

For baseband applications below ~10 MHz where SNR is a key parameter, differential transformer coupling is the recommended input configuration (see Figure 45). To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

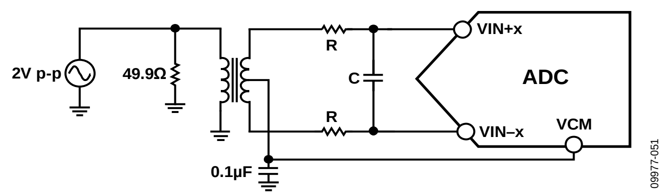

Figure 45. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies that are below a few megahertz (MHz). Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of theAD9608. For applications above ~10 MHz where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 46).

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use the AD8352 differential driver (see Figure 47). See the AD8352 data sheet for more information.

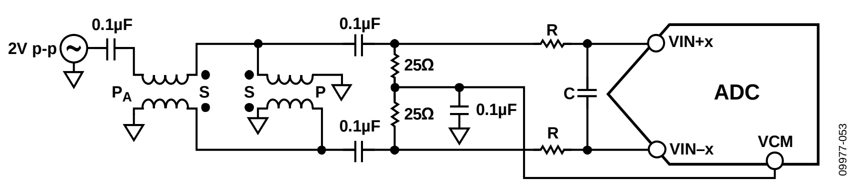

Figure 46. Differential Double Balun Input Configuration

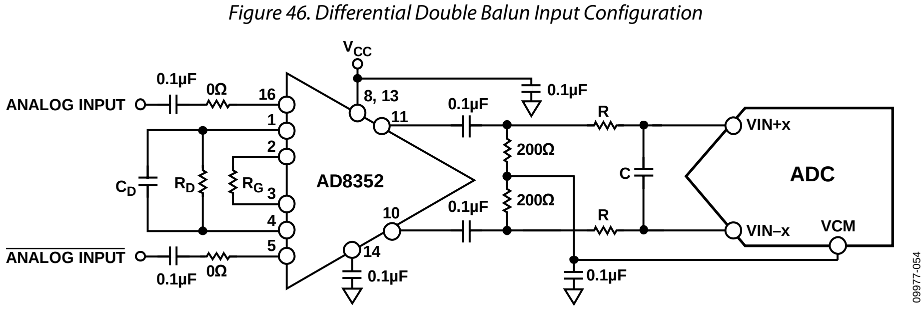

Figure 47. Differential Input Configuration Using the AD8352

In any configuration, the value of Shunt Capacitor C is dependent on the input frequency and source impedance and may need to be reduced or removed. Table 11 displays the suggested values to set the RC network. However, these values are dependent on the input signal and should be used only as a starting guide.

Table 11. Example RC Network

Frequency Range (MHz)	R Series (Ω Each)	C Differential (pF)
0 to 70	33	22
70 to 200	125	Open

It is not recommended to drive the AD9608 inputs single-ended.

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD9608. The VREF pin can be configured using either the internal 1.0 V reference or an externally applied 1.0 V reference voltage. The various reference modes are summarized in the sections that follow. The Reference Decoupling section describes the best practices PCB layout of the reference.

Internal Reference Connection

A comparator within the AD9608 detects the potential at the SENSE pin and configures the reference into two possible modes, which are summarized in Table 12. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 48), setting VREF to 1.0 V.

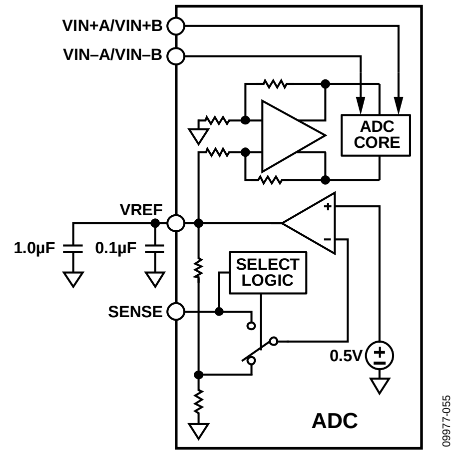

Figure 48. Internal Reference Configuration

If the internal reference of the AD9608 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 49 shows how the internal reference voltage is affected by loading.

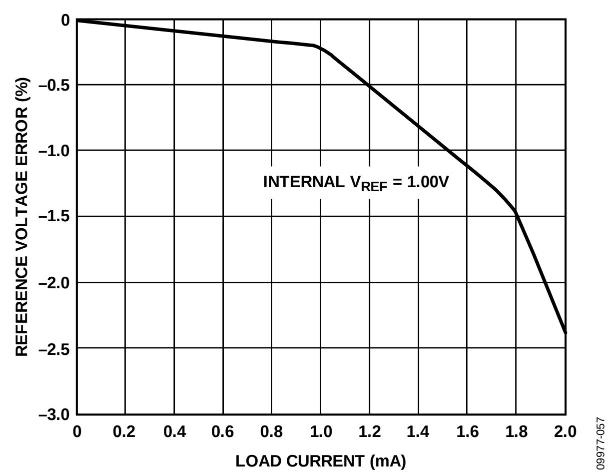

Figure 49. V_{REF} Accuracy vs. Load Current

Table 12. Reference Configuration Summary

Selected Mode	SENSE Voltage (V)	Resulting VREF (V)	Resulting Differential Span (V p-p)
Fixed Internal Reference	AGND to 0.2	1.0 internal	2.0
Fixed External Reference	AVDD	1.0 applied to external VREF pin	2.0

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 50 shows the typical drift characteristics of the internal reference in 1.0 V mode.

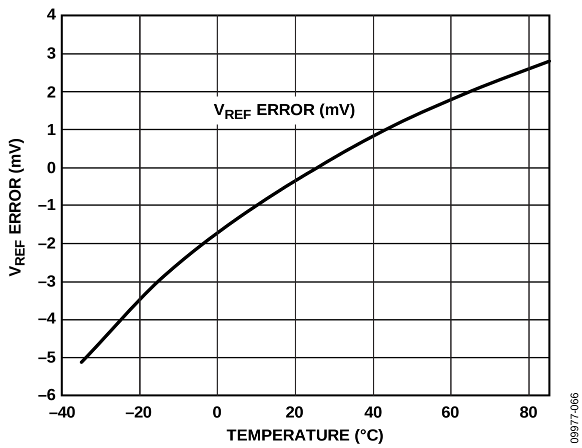

Figure 50. Typical V_{REF} Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7.5 kΩ load (see Figure 41). The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, the external reference must be limited to a maximum of 1.0 V.

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD9608 sample clock inputs, CLK+ and CLK−, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally (see Figure 51) and require no external bias.

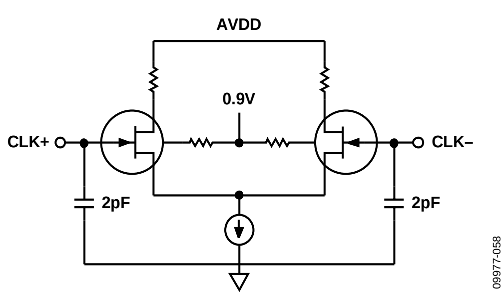

Figure 51. Equivalent Clock Input Circuit

Clock Input Options

The AD9608 has a very flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section.

Figure 52 and Figure 53 show two preferred methods for clocking the AD9608 (at clock rates up to 1 GHz prior to internal CLK divider). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 1 GHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200 MHz. The antiparallel Schottky diodes across the transformer/balun secondary limit clock excursions into the AD9608 to approximately 0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9608 while preserving the fast rise and fall times of the signal that are critical to a low jitter performance.

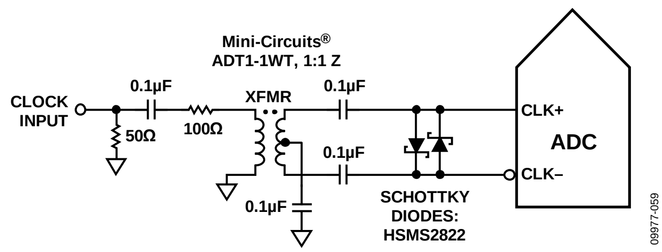

Figure 52. Transformer-Coupled Differential Clock (Up to 200 MHz)

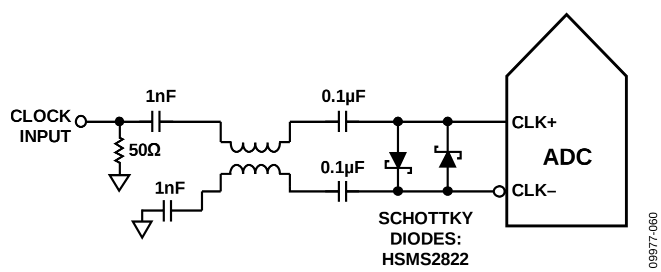

Figure 53. Balun-Coupled Differential Clock (Up to 1 GHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 54. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-0/AD9516-1/AD9516-2/AD9516-3/AD9516-4/AD9516-5/AD9517-0/AD9517-1/AD9517-2/AD9517-3/AD9517-4 clock drivers offer excellent jitter performance.

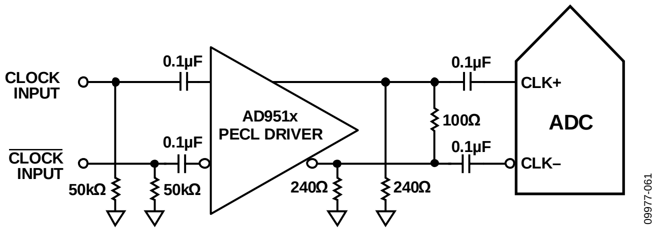

Figure 54. Differential PECL Sample Clock (Up to 1 GHz)

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 55. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-0/AD9516-1/AD9516-2/AD9516-3/AD9516-4/AD9516-5/AD9517-0/AD9517-1/AD9517-2/AD9517-3/AD9517-4 clock drivers offer excellent jitter performance.

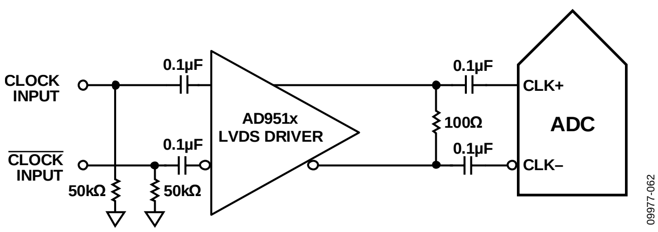

Figure 55. Differential LVDS Sample Clock (Up to 1 GHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended 1.8 V CMOS signal. In such applications, drive the CLK+ pin directly from a CMOS gate, and bypass the CLK– pin to ground with a 0.1 µF capacitor (see Figure 56).

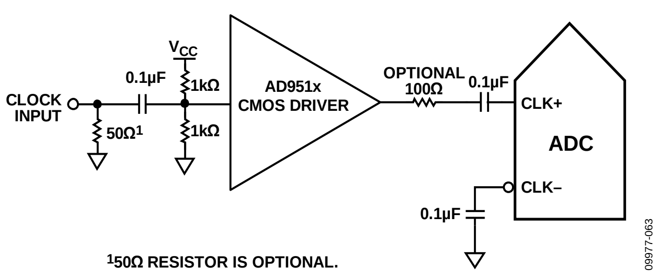

Figure 56. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

Input Clock Divider

The AD9608 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8.

The AD9608 clock divider can be synchronized using the external SYNC input. Bit 1 and Bit 2 of Register 0x3A allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. A ±5% tolerance is commonly required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9608 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9608. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS on, as shown in Figure 57.

Jitter in the rising edge of the input is still of concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates less than 20 MHz, nominally. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal.

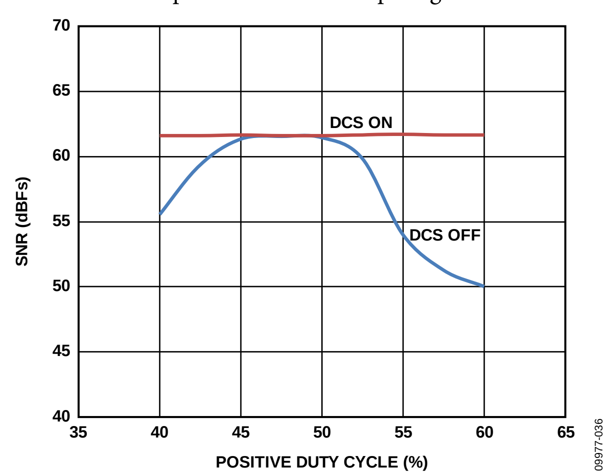

Figure 57. SNR vs. DCS On/Off

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR from the low frequency SNR (SNR_{LF}) at a given input frequency (f_{INPUT}) due to jitter (t_{JRMS}) can be calculated by

$$SNR_{HF} = -10\log[(2\pi \times f_{INPUT} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the previous equation, the rms aperture jitter represents the clock input jitter specification. IF undersampling applications are particularly sensitive to jitter, as illustrated in Figure 58.

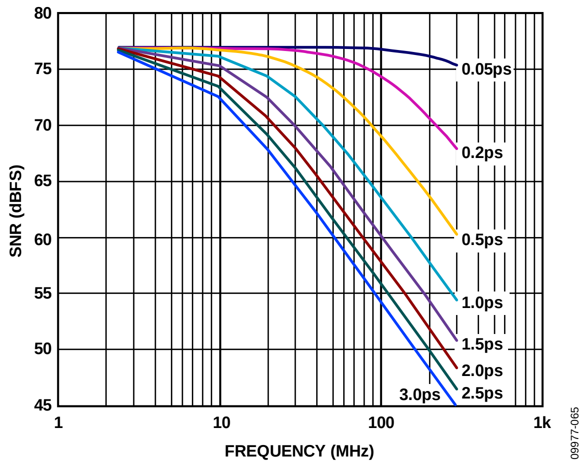

Figure 58. SNR vs. Input Frequency and Jitter

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9608. To avoid modulating the clock signal with digital noise, keep power supplies for clock drivers separate from the ADC output driver supplies. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock at the last step.

For more information, see the AN-501 Application Note and the AN-756 Application Note.

CHANNEL/CHIP SYNCHRONIZATION

The AD9608 has a SYNC input that offers the user flexible synchronization options for synchronizing sample clocks across multiple ADCs. The input clock divider can be enabled to synchronize on a single occurrence of the SYNC signal or on every occurrence. The SYNC input is internally synchronized to the sample clock; however, to ensure that there is no timing uncertainty between multiple parts, the SYNC input signal should be externally synchronized to the input clock signal, meeting the setup and hold times shown in Table 5. Drive the SYNC input using a single-ended CMOS-type signal.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 59, the analog core power dissipated by the AD9608 is proportional to its sample rate. The digital power dissipation of the CMOS outputs are determined primarily by the strength of the digital drivers and the load on each output bit.

The maximum DRVDD current (I_{DRVDD}) can be calculated as

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLK} \times N$$

where N is the number of output bits (22, in the case of the AD9608).

This maximum current occurs when every output bit switches on every clock cycle, that is, a full-scale square wave at the Nyquist frequency of $f_{CLK}/2$. In practice, the DRVDD current is established by the average number of output bits switching, which is determined by the sample rate and the characteristics of the analog input signal.

Reducing the capacitive load presented to the output drivers can minimize digital power consumption. The data in Figure 59 was taken in CMOS mode using the same operating conditions as those used for the power supplies and power consumption parameters in Table 1, with a 5 pF load on each output driver.

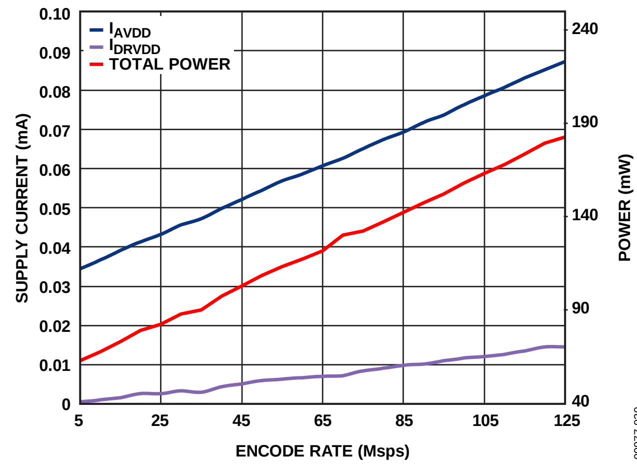

Figure 59. AD9608-125 Power and Current vs. Clock Rate (1.8 V CMOS Output Mode)

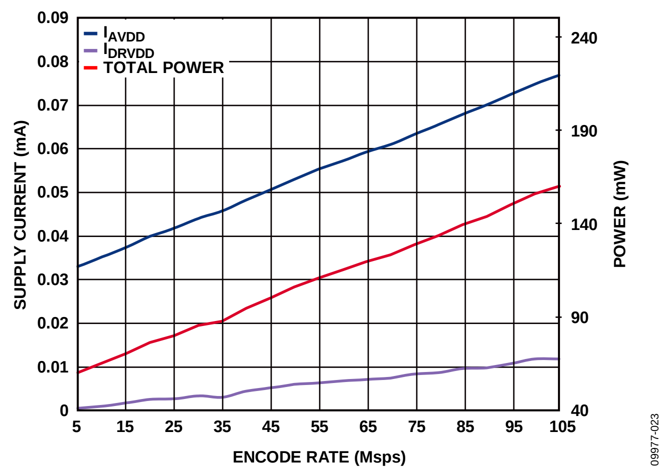

Figure 60. AD9608-105 Power and Current vs. Clock Rate (1.8 V CMOS Output Mode)

The AD9608 is placed in power-down mode either by the SPI port or by asserting the PDWN pin high. In this state, the ADC typically dissipates <2 mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD9608 to its normal operating mode. Note that PDWN is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map section for more details.

DIGITAL OUTPUTS

The AD9608 output drivers can be configured to interface with either 1.8 V CMOS or 1.8 V LVDS logic families. The default output mode is CMOS, with each channel output on separate busses as shown in Figure 2.

In CMOS output mode, the CMOS output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies and may affect converter performance.

Applications requiring the ADC to drive large capacitive loads or large fanouts may require external buffers or latches.

The CMOS output can also be configured for interleaved CMOS output mode via the SPI port. In interleaved CMOS mode, the data for both channels is output onto a single output bus to reduce the total number of traces required. The timing diagram for interleaved CMOS output mode is shown in Figure 3.

The interleaved CMOS output mode is enabled globally onto both output channels via Bit 5 in Register 0x14. The unused channel output can be disabled by selecting the appropriate bit (Bit 1 or Bit 0) in Register 0x05 and then writing a 1 to the local (channel-specific) output port disable bit (Bit 4) in Register 0x14.

The output data format can be selected to be either offset binary or twos complement by setting the SCLK/DFS pin when operating in the external pin mode (see Table 13).

As detailed in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, the data format can be selected for offset binary, twos complement, or Gray code when using the SPI control.

Table 13. SCLK/DFS Mode Selection (External Pin Mode)

Voltage at Pin	SCLK/DFS	SDIO/DCS
AGND	Offset binary (default)	DCS disabled
DRVDD	Twos complement	DCS enabled (default)

Digital Output Enable Function (OEB)

The AD9608 has a flexible three-state ability for the digital output pins. The three-state mode is enabled through the SPI interface and can subsequently be controlled using the OEB pin or through the SPI. Once enabled via the SPI (Bit 7) in Register 0x101 and the OEB pin is low, the output data drivers and DCOs are enabled. If the OEB pin is high, the output data drivers and DCOs are placed in a high impedance state. This OEB function is not intended for rapid access to the data bus. Note that OEB is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

When using the SPI interface, the data outputs and DCO of each channel can be independently three-stated by using the output port disable bit (Bit 4) in Register 0x14.

TIMING

The AD9608 provides latched data with a pipeline delay of 16 clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

Minimize the length of the output data lines and loads placed on them to reduce transients within the AD9608. These transients can degrade converter dynamic performance.

The lowest typical conversion rate of the AD9608 is 10 MSPS. At clock rates below 10 MSPS, dynamic performance can degrade.

Data Clock Output (DCO)

The AD9608 provides two data clock output (DCO) signals intended for capturing the data in an external register. In CMOS output mode, the data outputs are valid on the rising edge of DCO, unless the DCO clock polarity has been changed via the SPI. In LVDS output mode, the DCO and data output switching edges are closely aligned. Additional delay can be added to the DCO output using SPI Register 0x17 to increase the data setup time. In this case, the Channel A output data is valid on the rising edge of DCO, and the Channel B output data is valid on the falling edge of DCO. See Figure 2, Figure 3, and Figure 4 for a graphical timing description of the output modes.

Table 14. Output Data Format

Input (V)	Condition (V)	Offset Binary Output Mode	Twos Complement Mode	OR
VIN+ − VIN−	< −VREF − 0.5 LSB	00 0000 0000	10 0000 0000	1
VIN+ − VIN−	= −VREF	00 0000 0000	10 0000 0000	0
VIN+ − VIN−	= 0	10 0000 0000	00 0000 0000	0
VIN+ − VIN−	= +VREF − 1.0 LSB	11 1111 1111	01 1111 1111	0
VIN+ − VIN−	> +VREF − 0.5 LSB	11 1111 1111	01 1111 1111	1

OUTPUT TEST

The AD9608 includes various output test options to place predictable values on the outputs of theAD9608.

OUTPUT TEST MODES

The output test options are described in Table 18 at Address 0x0D. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The PN generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x0D. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock. For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

SERIAL PORT INTERFACE (SPI)

The AD9608 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, which are documented in the Memory Map section. For detailed operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK/DFS pin, the SDIO/DCS pin, and the CSB pin (see Table 15). The SCLK/DFS (a serial clock) is used to synchronize the read and write data presented from and to the ADC. The SDIO/DCS (serial data input/output) is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The CSB (chip select bar) is an active low control that enables or disables the read and write cycles.

Table 15. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input, which is used to synchronize serial interface reads and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles.

The falling edge of the CSB, in conjunction with the rising edge of the SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 61 and Table 5.

Other modes involving the CSB are available. The CSB can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in high impedance mode. This mode turns on any SPI pin secondary functions.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and W1 bits.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. The first bit of the first byte in a multibyte serial data transfer frame indicates whether a read command or a write command is issued. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

All data is composed of 8-bit words. Data can be sent in MSB-first mode or in LSB-first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

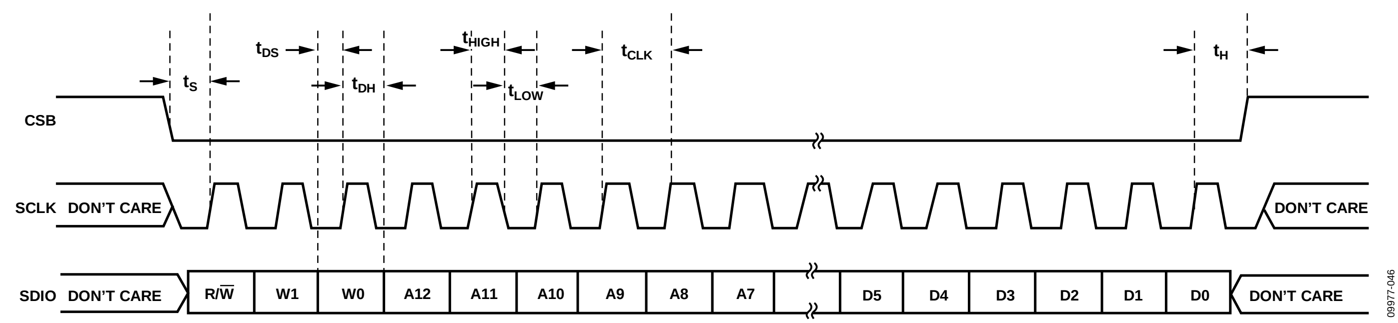

Figure 61. Serial Port Interface Timing Diagram

HARDWARE INTERFACE

The pins described in Table 15 comprise the physical interface between the user programming device and the serial port of the AD9608. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9608 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

Some pins serve a dual function when the SPI interface is not being used. When the pins are strapped to DRVDD or ground during device power-on, they are associated with a specific function. Table 16 describes the strappable functions supported on the AD9608.

CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SDIO/DCS pin, the SCLK/DFS pin, the OEB pin, and the PDWN pin serve as standalone CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the duty cycle stabilizer, output data format, and power-down feature control. In this mode, the CSB chip select bar should be connected to AVDD, which disables the serial port interface.

When the device is in SPI mode, the PDWN and OEB pins (if enabled) remain active. For SPI control of output enable and power-down, the OEB and PDWN pins should be set to their default states.

Table 16. Mode Selection

Pin	External Voltage	Configuration
SDIO/DCS	DRVDD (default)	Duty cycle stabilizer enabled
	AGND	Duty cycle stabilizer disabled
SCLK/DFS	DRVDD	Twos complement enabled
	AGND (default)	Offset binary enabled
OEB	DRVDD	Outputs in high impedance
	AGND (default)	Outputs enabled
PDWN	DRVDD	Chip in power-down or standby
	AGND (default)	Normal operation

SPI ACCESSIBLE FEATURES

Table 17 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. The AD9608 part-specific features are described in detail following Table 18, the external memory map register table (see the Memory Map Register Descriptions section).

Table 17. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows user to set either power-down mode or standby mode
Clock	Allows user to access the DCS, set the clock divider, set the clock divider phase, and enable the sync
Offset	Allows user to digitally adjust the converter offset
Test I/O	Allows user to set test modes to have known data on output bits
Output Mode	Allows user to set the output mode, including LVDS
Output Phase	Allows user to set the output clock polarity
Output Delay	Allows user to vary the DCO delay

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into three sections: the chip configuration registers (Address 0x00 to Address 0x02); the channel index and transfer registers (Address 0x05 and Address 0xFF) and the ADC functions registers, including setup, control, and test (Address 0x08 to Address 0x102).

The memory map register table (see Table 18) lists the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x05, the device index register, has a hexadecimal default value of 0x03. This means that in Address 0x05, Bits[7:2] = 0, and Bits[1:0] = 1. This setting is the default channel index setting. The default value results in both ADC channels receiving the next write command. For more information about this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. This application note details the functions controlled by Register 0x00 to Register 0xFF. The remaining registers are documented in the Memory Map Register Descriptions section.

Open Locations

All address and bit locations that are not included in Table 18 are not currently supported for this device. Unused bits of a valid address location should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x05). If the entire address location is open (for example, Address 0x13), this address location should not be written to.

Default Values

After the AD9608 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 18.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Channel-Specific Registers

Some channel setup functions can be programmed for each channel individually. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 18 as local. These local registers and bits can be accessed by setting the appropriate Channel A or Channel B bits in Register 0x05. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, only Channel A or Channel B should be set to read one of the two registers. If both bits are set during an SPI read cycle, the part returns the value for Channel A. Registers and bits designated as global in Table 18 affect the entire part or the channel features for which independent settings are not allowed between channels.

MEMORY MAP REGISTER TABLE

All address and bit locations that are not included in Table 18 are not currently supported for this device.

Table 18. Memory Map Registers

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments
Chip Configuration Registers											
0x00	SPI port config (global)	Open	LSB first	Soft reset	1	1	Soft reset	LSB first	Open	0x18	Nibbles are mirrored so LSB-first mode or MSB-first mode registers correctly, regardless of shift mode
0x01	Chip ID (global)	8-bit chip ID, Bits[7:0] AD9608 = 0x9C								Read only	Unique chip ID used to differentiate devices; read only
0x02	Chip grade (global)	Open	Speed grade ID 100 = 105 MSPS 101 = 125 MSPS			Open	Open	Open	Open	Read only	Unique speed grade ID used to differentiate devices; read only
Channel Index and Transfer Registers											
0x05	Device index (global)	Open	Open	Open	Open	Open	Open	Channel B	Channel A	0x03	Bits are set to determine which device on the chip receives the next write command; applies to local registers only
0xFF	Transfer (global)	Open	Open	Open	Open	Open	Open	Open	Transfer	0x00	Synchronous transfer of data from the master shift register to the slave
ADC Functions											
0x08	Power modes (local)	Open	Open	External power-down pin function 0 = PDWN 1 = standby	Open	Open	Open	Internal power-down mode 00 = normal operation 01 = full power-down 10 = standby 11 = digital reset		0x00	Determines various generic modes of chip operation
0x09	Global clock (global)	Open	Open	Open	Open	Open	Open	Open	Duty cycle stabilizer 0 = disabled 1 = enabled	0x01	

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments
0x0B	Clock divide (global)	Open	Open	Open	Open	Open	Clock divide ratio 000 = divide by 1 001 = divide by 2 010 = divide by 3 011 = divide by 4 100 = divide by 5 101 = divide by 6 110 = divide by 7 111 = divide by 8			0x00	The divide ratio is value plus 1
0x0C	Enhance-ment control (global)	Open	Open	Open	Open	Open	Chop mode 0 = disabled 1 = enabled	Open	Open	0x00	Chop mode enabled if Bit 2 = 1
0x0D	Test mode (local)	User test mode control 00 = single pattern mode 01 = alternate continuous/repeat pattern mode 10 = single once pattern mode 11 = alternate once pattern mode		Reset PN long gen	Reset PN short gen	Output test mode 0000 = off (default) 0001 = midscale short 0010 = positive FS 0011 = negative FS 0100 = alternating checkerboard 0101 = PN long sequence 0110 = PN short sequence 0111 = one/zero word toggle 1000 = user test mode 1111 = ramp output				0x00	When this register is set, the test data is placed on the output pins in place of normal data
0x10	Customer offset adjust (local)	Offset adjust in LSBs from +127 to −128 (twos complement format)								0x00	
0x14	Output mode	Output port logic type (global) 00 = CMOS, 1.8 V 10 = LVDS, ANSI 11 = LVDS, reduced range		Output interleave enable (global)	Output port disable (local)	Open (global)	Output invert (local)	Output format 00 = offset binary 01 = twos complement 10 = Gray code		0x00	Configures the outputs and the format of the data
0x15	Output adjust	Open	Open	CMOS 1.8 V DCO drive strength 00 = 1× 01 = 2× 10 = 3× 11 = 4×		Open	Open	CMOS 1.8 V data drive strength 00 = 1× 01 = 2× 10 = 3× 11 = 4×		0x00	Determines CMOS output drive strength properties
0x16	Clock phase control (global)	Invert DCO clock 0 = not inverted 1 = inverted	Open	Open	Open	Open	Input clock divider phase adjust relative to the encode clock 000 = no delay 001 = 1 input clock cycle 010 = 2 input clock cycles 011 = 3 input clock cycles 100 = 4 input clock cycles 101 = 5 input clock cycles 110 = 6 input clock cycles 111 = 7 input clock cycles			0x00	Allows selection of clock delays into the input clock divider
0x17	Output delay (global)	DCO clock delay 0 = disabled 1 = enabled	Open	Data delay 0 = disabled 1 = enabled	Open	Open	Delay selection 000 = 0.56 ns 001 = 1.12 ns 010 = 1.68 ns 011 = 2.24 ns 100 = 2.80 ns 101 = 3.36 ns 110 = 3.92 ns 111 = 4.48 ns			0x00	This sets the fine output delay of the output clock but does not change internal timing
0x18	VREF select (global)	Open	Open	Open	Open	Open	Internal V_{REF} digital adjustment 000 = 1.0 V p-p 001 = 1.14 V p-p 010 = 1.33 V p-p 011 = 1.6 V p-p 100 = 2.0 V p-p			0x04	Select and/or adjust V_{REF}

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments
0x19	User Pattern 1, LSB (global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-Defined Pattern 1, LSB
0x1A	User Pattern 1, MSB (global)	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-Defined Pattern 1, MSB
0x1B	User Pattern 2, LSB (global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-Defined Pattern 2, LSB
0x1C	User Pattern 2, MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-Defined Pattern 2, MSBs
0x2A	Overrange control (global)	Open	Open	Open	Open	Open	Open	Open	Overrange output 0 = disabled 1 = enabled	0x01	Overrange control settings
0x2E	Output assign (local)	Open	Open	Open	Open	Open	Open	Open	0 = ADC A 1 = ADC B (local)	0x00 = ADC A 0x01 = ADC B	Assign an ADC to an output channel
0x3A	Sync control (global)	Open	Open	Open	Open	Open	Clock divider next sync only	Clock divider sync enable	Open	0x00	Sets the global sync options
0x100	Sample rate override	Open	Sample rate override enable	Open	Open	Open	Sample rate 011 = 80 MSPS 100 = 105 MSPS 101 = 125 MSPS			0x00	
0x101	User I/O Control Register 2	Output enable bar (OEB) pin enable	Open	Open	Open	Open	Open	Open	Disable SDIO pull-down	0x80	OEB and SDIO pin controls
0x102	User I/O Control Register 3	Open	Open	Open	Open	VCM power-down	Open			0x00	

MEMORY MAP REGISTER DESCRIPTIONS

For additional information about functions controlled in Register 0x00 to Register 0xFF, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Power Modes (Register 0x08)

Bits[7:6]—Open

Bit 5—External Power-Down Pin Function

If set, the external PDWN pin initiates power-down mode. If clear, the external PDWN pin initiates standby mode.

Bits[4:2]—Open

Bits[1:0]—Internal Power-Down Mode

In normal operation (Bits[1:0] = 00), both ADC channels are active.

In power-down mode (Bits[1:0] = 01), the digital data path clocks are disabled while the digital data path is reset. Outputs are disabled.

In standby mode (Bits[1:0] = 10), the digital data path clocks and the outputs are disabled.

During a digital reset (Bits[1:0] = 11), the digital data path clocks are disabled while the digital data path is held in reset. The outputs are enabled in this state. For optimum performance, it is recommended that both ADC channels be reset simultaneously. This is accomplished by ensuring that both channels are selected via Register 0x05 prior to issuing the digital reset instruction.

Enhancement Control (Register 0x0C)

Bits[7:3]—Open

Bit 2—Chop Mode

For applications that are sensitive to offset voltages and other low frequency noise, such as homodyne or direct-conversion receivers, chopping in the first stage of the AD9628 is a feature that can be enabled by setting Bit 2. In the frequency domain, chopping translates offsets and other low frequency noise to $f_{CLK}/2$ where it can be filtered.

Bits[1:0]—Open

Output Mode (Register 0x14)

Bits[7:6]—Output Port Logic Type

00 = CMOS, 1.8 V
10 = LVDS, ANSI
11 = LVDS, reduced range

Bit 5—Output Interleave Enable

For LVDS outputs, setting Bit 5 enables interleaving. Channel A is sent coincident with a high DCO clock, and Channel B is coincident with a low DCO clock. Clearing Bit 5 disables the interleaving feature. Channel A is sent on least significant bits (LSBs), and Channel B is sent on most significant bits (MSBs). The even bits are sent coincident with a high DCO clock, and the odd bits are sent coincident with a low DCO clock.

For CMOS outputs, setting Bit 5 enables interleaving in CMOS DDR mode. On ADC Output Port A, Channel A is sent coincident with a low DCO clock, and Channel B is coincident with a high DCO clock. On ADC Output Port B, Channel B is sent coincident with a low DCO clock, and Channel A is coincident with a high DCO clock. Clearing Bit 5 disables the interleaving feature, and data is output in CMOS SDR mode. Channel A is sent to Port A, and Channel B is sent to Port B.

Bit 4—Output Port Disable

Setting Bit 4 high disables the output port for the channels selected in Bits[1:0] of the device index register (Register 0x05).

Bit 3—Open

Bit 2—Output Invert

Setting Bit 2 high inverts the output port data for the channels selected in Bits[1:0] of the device index register (Register 0x05).

Bits[1:0]—Output Format

00 = offset binary
01 = twos complement
10 = Gray code

Sync Control (Register 0x3A)

Bits[7:3]—Open

Bit 2—Clock Divider Next Sync Only

If the clock divider sync enable bit (Address 0x3A, Bit 1) is high, Bit 2 allows the clock divider to sync to the first sync pulse it receives and to ignore the rest. The clock divider sync enable bit resets after it syncs.

Bit 1—Clock Divider Sync Enable

Bit 1 gates the sync pulse to the clock divider. The sync signal is enabled when Bit 1 is high. This is continuous sync mode.

Bit 0—Open

Transfer (Register 0xFF)

All registers except Register 0x100 are updated the moment they are written. Setting Bit 0 of this transfer register high initializes the settings in the ADC sample rate override register (Address 0x100).

Sample Rate Override (Register 0x100)

This register is designed to allow the user to downgrade the device. Any attempt to upgrade the default speed grade results in a chip power-down. Settings in this register are not initialized until Bit 0 of the transfer register (Register 0xFF) is written high.

User I/O Control 2 (Register 0x101)

Bit 7—OEB Pin Enable

If the OEB pin enable bit (Bit 7) is set (default), the OEB pin is enabled. If Bit 7 is clear, the OEB pin is disabled.

Bits[6:1]—Open

Bit 0—SDIO Pull-Down

Bit 0 can be set to disable the internal 30 kΩ pull-down on the SDIO pin, which can be used to limit the loading when many devices are connected to the SPI bus.

User I/O Control 3 (Register 0x102)

Bits[7:4]—Open

Bit 3—VCM Power-Down

Bit 3 can be set high to power down the internal VCM generator. This feature is used when applying an external reference.

Bits[2:0]—Open

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting design and layout of the AD9608 as a system, it is recommended that the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements that are needed for certain pins.

Power and Ground Recommendations

When connecting power to the AD9608, it is recommended that two separate 1.8 V supplies be used. Use one supply for analog (AVDD); use a separate supply for the digital outputs (DRVDD). For both AVDD and DRVDD, several different decoupling capacitors should be used to cover both high and low frequencies. Place these capacitors close to the point of entry at the PCB level and close to the pins of the part, with minimal trace length.

A single PCB ground plane should be sufficient when using the AD9608. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

LVDS Operation

The AD9608 defaults to CMOS output mode on power-up. If LVDS operation is desired, this mode must be programmed, using the SPI configuration registers after power-up. When the AD9608 powers up in CMOS mode with LVDS termination resistors (100 Ω) on the outputs, the DRVDD current can be higher than the typical value until the part is placed in LVDS mode. This additional DRVDD current does not cause damage to the AD9608, but it should be taken into account when considering the maximum DRVDD current for the part.

To avoid this additional DRVDD current, the AD9608 outputs can be disabled at power-up by taking the PDWN pin high. After the part is placed into LVDS mode via the SPI port, the PDWN pin can be taken low to enable the outputs.

Clock Stability Considerations

When powered on, the AD9608 enters an initialization phase during which an internal state machine sets up the biases and the registers for proper operation. During the initialization process, the AD9608 needs a stable clock. If the ADC clock source is not present or not stable during ADC power-up, it disrupts the state machine and causes the ADC to start up in an unknown state. To correct this, an initialization sequence must be reinvoked after the ADC clock is stable by issuing a digital reset via Register 0x08. In the default configuration (internal V_{REF}, ac-coupled input) where V_{REF} and V_{CM} are supplied by the ADC itself, a stable clock during power-up is sufficient. In the case where V_{REF} and/or V_{CM} are supplied by an external source, these, too, must be stable at power-up; otherwise, a subsequent digital reset via Register 0x08 is needed. Interruption of the sample clock during operation and changes in sample rate also necessitate a digital reset.

The pseudo code sequence for a digital reset is as follows:

```
SPI_Write (0x08, 0x03);   # Digital Reset
SPI_Write (0x08, 0x00);   # Can be asserted
as soon as the next SPI cycle, normal
operation resumes after 2.9e6 sample clock
cycles, ADC outputs 0s until the reset is
complete.
```

Exposed Paddle Thermal Heat Slug Recommendations

It is mandatory that the exposed paddle on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance. A continuous, exposed (no solder mask) copper plane on the PCB should mate to the AD9608 exposed paddle, Pin 0.

The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be filled or plugged to prevent solder wicking through the vias, which can compromise the connection.

To maximize the coverage and adhesion between the ADC and the PCB, a silkscreen should be overlaid to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the ADC and the PCB during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and the PCB. For detailed information about packaging and PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

VCM

The VCM pin should be decoupled to ground with a 0.1 µF capacitor.

Reference Decoupling

The VREF pin should be externally decoupled to ground with a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

SPI Port

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9608 to keep these signals from transitioning at the converter inputs during critical sampling periods.

OUTLINE DIMENSIONS

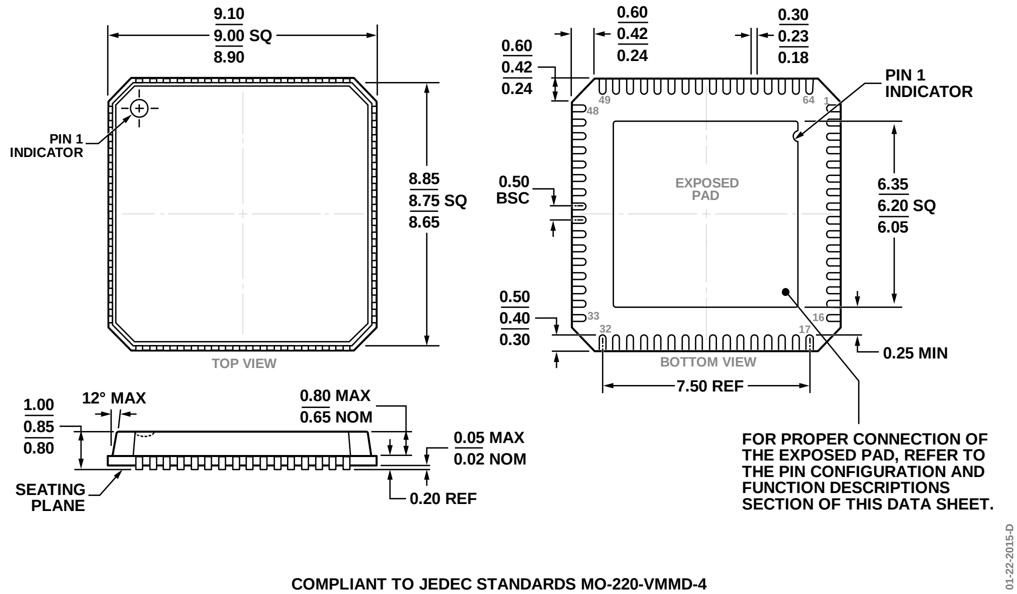

Figure 62. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9608BCPZ-105	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-4
AD9608BCPZ-125	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-4
AD9608BCPZRL7-105	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-4
AD9608BCPZRL7-125	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-4
AD9608-125EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.