

FEATURES

- Quad 14-bit 250 MSPS ADC**
SFDR = 83 dBc at 87 MHz input
- Dual 14-bit 500 MSPS DAC**
SFDR = 75 dBc at 20 MHz output
- On-chip PLL clock synthesizer**
- Low power**
1536 mW, 1 GHz master clock, on-chip synthesizer
- 500 MHz double data rate (DDR)**
- LVDS interfaces for DACs and ADCs**
- Small 12 mm × 12 mm lead-free BGA package**

APPLICATIONS

- Point to point microwave backhaul radios**
- Wireless repeaters**

GENERAL DESCRIPTION

The AD9993 is a mixed-signal front-end (MxFE®) device that integrates four 14-bit ADCs and two 14-bit DACs. Figure 1 shows the block diagram of the MxFE. The MxFE is programmable using registers accessed via a serial peripheral interface (SPI). ADC and DAC datapaths include FIFO buffers to absorb phase differences between LVDS lane clocks and the data converter sampling clocks.

The MxFE DACs are part of the Analog Devices, Inc., high speed CMOS DAC core family. These DACs are designed to be used in wide bandwidth communication system transmitter (Tx) signal chains.

The MxFE ADCs are multistage pipelined CMOS ADC cores designed for use in communications receivers.

FUNCTIONAL BLOCK DIAGRAM

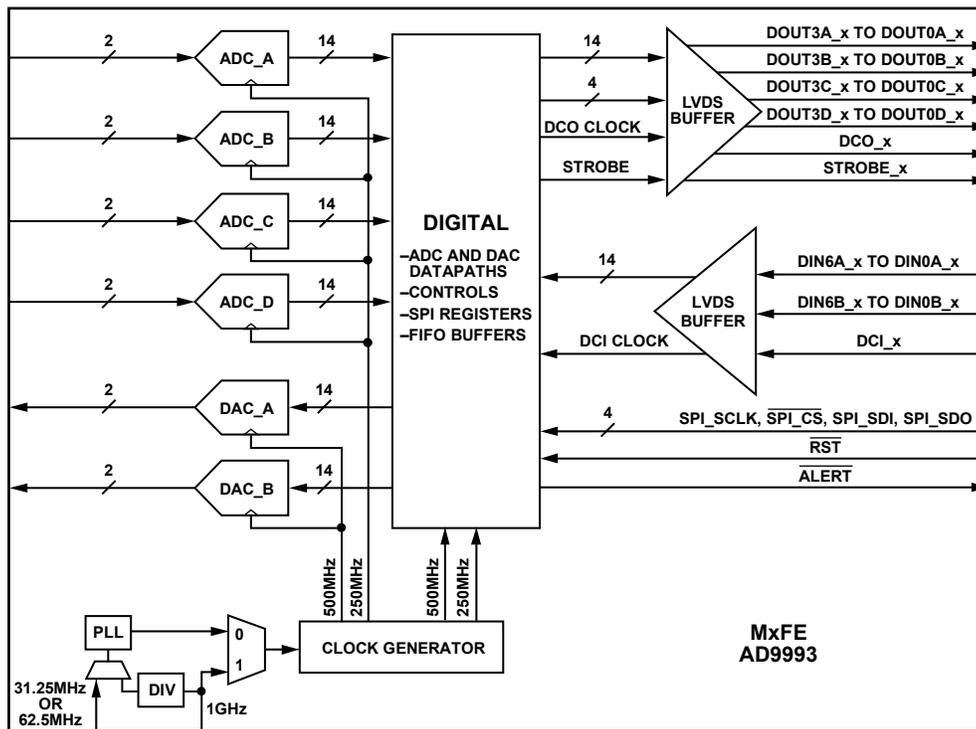


Figure 1.

AD9993* Product Page Quick Links

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REVISION HISTORY

5/14—Rev. 0 to Rev. A

Changes to Ordering Guide.....56

5/14—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX} , AVDD33 = 3.3 V, DVDD = AVDD = 1.8 V, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Tx DAC RESOLUTION			14		Bits
Tx DAC OUTPUT CHARACTERISTICS					
Offset Error			±0.5		% FSR
Gain Error			±2.0		% FSR
Full-Scale Output Current (I_{OUTFS})			20.0		mA
Output Compliance Voltage Range	CML_A, CML_B connected to AVSS, setting of DAC_VCM_VREF_BIT[2:0] following reset	-0.5		+0.5	V
Output Compliance Voltage Range	CML_A, CML_B connected to a bypass capacitor, DAC_VCM_VREF_BIT[2:0] set to 010	0.0		1.0	V
Output Resistance			10		MΩ
Tx DAC TEMPERATURE DRIFT					
Gain	Gain using on-chip VREF_DAC		±85		ppm/°C
Reference Voltage (VREF_DAC)	On-chip VREF_DAC		±215		ppm/°C
REFERENCE (VREF_DAC)					
Internal Reference Voltage		0.95	1.0	1.05	V
Rx ADC RESOLUTION			14		Bits
Rx ADC CHARACTERISTICS					
Gain Error			±1.0		% FSR
Peak-to-Peak Differential Input Voltage Range	Setting of VREF_FS_ADJ[4:0] at reset		1.75		V p-p
Input Capacitance			2.5		pF
Rx ADC FULL-SCALE V_{REF} ADJUSTMENT		1.383	1.75	2.087	V
COMMON-MODE VOLTAGE REFERENCE (A_CML, B_CML, C_CML, D_CML)					
ADC Common-Mode Voltage Output	ADC inputs are not self biased	0.84	0.9	0.96	V
ANALOG SUPPLY VOLTAGES					
AVDD33		3.14	3.3	3.47	V
AVDD		1.71	1.8	1.89	V
DIGITAL SUPPLY VOLTAGES					
DVDD		1.62	1.8	1.98	V
POWER CONSUMPTION					
Single Tone Input, Single Tone Output			1536		mW
AVDD33			55		mA
AVDD			65		mA
DVDD			210		mA
Power-Down Mode			10.0		mA
OPERATING RANGE		-40	+25	+85	°C

AC SPECIFICATIONS

T_{MIN} to T_{MAX} , AVDD33 = 3.3 V, DVDD = AVDD = 1.8 V, DAC sampling rate = 500 MSPS and ADC sampling rate = 250 MSPS, unless otherwise specified.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DAC OUTPUT					
Spurious-Free Dynamic Range (SFDR)	$f_{OUT} = 20$ MHz		75		dBc
Two Tone Intermodulation Distortion (IMD3)	$f_{OUT} = 80$ MHz		65		dBc
Noise Spectral Density (NSD), Single Tone	$f_{OUT} = 80$ MHz		-160		dBm/Hz
256-QAM Adjacent Channel Power (ACP)	$f_{CENTER} = 50$ MHz, single carrier, 3.375 MHz offset frequency		76		dBc
ADC INPUT					
Signal to Noise Ratio (SNR) $f_{IN} = 87$ MHz	Measured with -1.0 dBFS sine wave input		70		dBc
Spurious-Free Dynamic Range (SFDR) $f_{IN} = 10$ MHz	Measured with -1.0 dBFS sine wave input		86		dBc
$f_{IN} = 87$ MHz			83		dBc
Two-Tone IMD3	$f_{IN1} = 89$ MHz, $f_{IN2} = 92$ MHz, $A_{IN} = -12$ dBFS		90		dBc
Full Power Bandwidth	Bandwidth of operation in which proper ADC performance can be achieved		1000		MHz

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX} , AVDD33 = 3.3 V, DVDD = AVDD = 1.8 V, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL					
Input V_{IN} Logic High			1.8		V
Input V_{IN} Logic Low			0.0		V
CMOS OUTPUT LOGIC LEVEL					
Output V_{OUT} Logic High		1.2			V
Output V_{OUT} Logic Low				0.8	V
ADC AND DAC LVDS DATA INTERFACES					
ADC LVDS Transmitter Outputs					
DCO_P/DCO_N to Data Skew (t_{SKEW})	Data to DDR DCO_P/DCO_N transition delay	350			ps
Output Voltage High, V_{OH} , Single Ended	Applies to output voltage, positive and negative, V_{OUTP} and V_{OUTN}		1375		mV
Output Voltage Low, V_{OL} , Single Ended	Applies to V_{OUTP} and V_{OUTN}		1025		mV
Output Differential Voltage			200		mV
Output Offset Voltage			1200		mV
DAC LVDS Receiver Inputs					
Input Voltage Range, Single Ended	Specifications apply to DAC data inputs and DCI_P/DCI_N Applies to input voltage, positive and negative, V_{INP} and V_{INN}	825		1575	mV
Input Differential Threshold		-100		+100	mV
Input Differential Hysteresis			25		mV
Receiver Differential Input Impedance		85		115	Ω

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK INPUT (CLKP, CLKN) Differential Peak to Peak Voltage Common Mode Voltage Master Clock Frequency			350 1.2		mV V MHz
REFCLK Input (REFCLK) Input V _{IN} Logic High Input V _{IN} Logic Low REFCLK Frequency			1.8 0.0 31.25 or 62.5		V V MHz
SERIAL PERIPHERAL INTERFACE (SPI) SPI_SCLK Frequency SPI_SCLK Pulse Width High SPI_SCLK Pulse Width Low Setup Time, SPI_SDI to SPI_SCLK Rising Edge Hold Time, SPI_SCLK Rising Edge to SPI_SDI Setup Time, $\overline{\text{SPI_CS}}$ to SPI_SCLK Rising Edge Hold Time, SPI_SCLK Rising Edge to SPI_CS Data Valid, SPI_SCLK Falling Edge to SPI_SDO				25	MHz ns ns ns ns ns ns ns

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AVSS to DVSS	−0.3 V to +0.3 V
AVDD33 to AVSS, DVSS	−0.3 V to +3.9 V
AVDD to AVSS, DVSS	−0.3 V to +2.2 V
DVDD to DVSS, AVSS	−0.3 V to +2.2 V
CP, A_VINP, A_VINN, B_VINP, B_VINN, C_VINP, C_VINN, D_VINP, D_VINN, IBIAS_TEST to AVSS	−0.3 V to AVDD + 0.3 V
VREF_DAC, FSAJ_A, FSAJ_B, CML_A, CML_B, A_CML, B_CML, B_CML, D_CML to AVSS	−0.3 V to AVDD + 0.3 V
IOUTA_P, IOUTA_N, IOUTB_P, IOUTB_N to AVSS	−0.3 V to AVDD + 0.3 V
CLKP, CLKN, REFCLK to AVSS	−0.3 V to AVDD + 0.3 V
PDWN, ALERT, RST, MODE, SPI_SCLK, SPI_CS, SPI_SDI, SPI_SDO to DVSS	−0.3 V to DVDD + 0.3 V
LVDS Data Inputs to DVSS	−0.3 V to DVDD + 0.3 V
LVDS Data Outputs to DVSS	−0.3 V to DVDD + 0.3 V
STROBE_P, STROBE_N to DVSS	−0.3 V to DVDD + 0.3 V
DCI_N, DCI_P, DCO_N, DCO_P	−0.3 V to DVDD + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +160°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 5. Thermal Resistances and Characterization Parameters

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	ψ_{JT}	ψ_{JB}	Unit
196-Ball CSP_BGA	27.0	15.4	5.38	0.11	15.0	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	AVSS	CLKP	AVSS	D_VINP	C_CML	C_VINP	AVSS	AVSS	B_VINP	B_CML	A_VINP	AVSS	IBIAS_TEST	AVSS
B	CLKN	REFCLK	AVSS	D_VINN	D_CML	C_VINN	AVSS	AVSS	B_VINN	A_CML	A_VINN	AVSS	IOUTA_N	IOUTA_P
C	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVDD33	AVDD33
D	LDO15	CP	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	IOUTB_N	IOUTB_P
E	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
F	PDWN	$\overline{\text{ALERT}}$	$\overline{\text{RST}}$	MODE	AVDD33	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	VREF_DAC	FSAJ_B	FSAJ_A
G	SPI_SCLK	$\overline{\text{SPI_CS}}$	SPI_SDI	SPI_SDO	DVDD	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVDD	CML_B	CML_A
H	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS
J	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD
K	DIN6B_N	DIN4B_N	DIN1B_N	DOUT3D_P	DOUT3D_N	DOUT3C_P	DCO_N	DCO_P	DOUT3B_P	DOUT3A_N	DOUT3A_P	DIN1A_N	DIN4A_N	DIN6A_N
L	DIN6B_P	DIN4B_P	DIN1B_P	DOUT1D_N	DOUT2D_N	DOUT1C_N	DOUT3C_N	DOUT3B_N	DOUT1B_N	DOUT2A_N	DOUT1A_N	DIN1A_P	DIN4A_P	DIN6A_P
M	DIN5B_N	DIN3B_N	DIN3B_P	DOUT1D_P	DOUT2D_P	DOUT1C_P	STROBE_N	STROBE_P	DOUT1B_P	DOUT2A_P	DOUT1A_P	DIN3A_N	DIN3A_P	DIN5A_N
N	DIN5B_P	DIN2B_N	DIN0B_N	DOUT0D_N	DOUT0C_N	DOUT2C_N	DVSS	DVSS	DOUT2B_N	DOUT0B_N	DOUT0A_N	DIN0A_N	DIN2A_N	DIN5A_P
P	DVSS	DIN2B_P	DIN0B_P	DOUT0D_P	DOUT0C_P	DOUT2C_P	DCI_N	DCI_P	DOUT2B_P	DOUT0B_P	DOUT0A_P	DIN0A_P	DIN2A_P	DVSS

12260-002

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1, A3, A7, A8, A12, A14, B3, B7, B8, B12, C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, F6, F7, F8, F9, F10, F11, G6, G7, G8, G9, G10, G11	AVSS	Analog Ground.
A2	CLKP	External Master Clock Input Positive.
A4	D_VINP	ADC D Input Voltage Positive.
A5	C_CML	Common-Mode Level Bias Voltage Output ADC C.
A6	C_VINP	ADC C Input Voltage Positive.
A9	B_VINP	ADC B Voltage Input Positive.
A10	B_CML	Common-Mode Level Bias Voltage Output for ADC B.

Pin No.	Mnemonic	Description
A11	A_VINP	ADC A Voltage Input Positive.
A13	IBIAS_TEST	Test. Connect to ground.
B1	CLKN	External Master Clock Input Negative
B2	REFCLK	On-Chip PLL Synthesizer Reference Clock Input.
B4	D_VINN	ADC D Input Voltage Negative.
B5	D_CML	Common-Mode Level Bias Voltage Output ADC D.
B6	C_VINN	ADC C Input Voltage Negative.
B9	B_VINN	ADC B Voltage Input Negative.
B10	A_CML	Common-Mode Level Bias Voltage Output for ADC A.
B11	A_VINN	ADC A Voltage Input Negative.
B13	IOUTA_N	DAC A Output Current Negative.
B14	IOUTA_P	DAC A Output Current Positive.
C13, C14, F5	AVDD33	3.3 V Analog Power Supply.
D1	LDO15	On-Chip Regulator Output. Bypass with 4.7 μ F capacitor to ground.
D2	CP	Connection for On-Chip PLL Optional External Portion of Loop Filter.
D13	IOUTB_N	DAC B Output Current Negative.
D14	IOUTB_P	DAC B Output Current Positive.
E1, E2, E3, E4, E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, G12	AVDD	1.8 V Analog Power Supply.
F1	$\overline{\text{PDWN}}$	Power-Down. Set to 1 to place the device in low power mode.
F2	$\overline{\text{ALERT}}$	Active Low Alarm Indicator Output, Open Drain.
F3	$\overline{\text{RST}}$	Reset Input, Active Low.
F4	MODE	Connect to ground.
F12	VREF_DAC	DAC A and DAC B Reference Voltage Input/Output.
F13	FSAJ_B	DAC B Full-Scale Current Output Adjust.
F14	FSAJ_A	DAC A Full-Scale Current Output Adjust.
G1	SPI_SCLK	SPI Clock.
G2	$\overline{\text{SPI_CS}}$	SPI Chip Select, Active Low.
G3	SPI_SDI	SPI Serial Data Input.
G4	SPI_SDO	SPI Serial Data Output.
G5, J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14	DVDD	1.8 V Digital Supply.
G13	CML_B	DAC B Common-Mode Control. Connect to ground for DAC bias < 0.5 V. Connect a 0.1 μ F capacitor between CML_B and ground for other DAC bias values \geq 0.5 V.
G14	CML_A	DAC A Common-Mode Control. Connect to ground for DAC bias < 0.5 V. Connect a 0.1 μ F capacitor between CML_A and ground for other DAC bias values \geq 0.5 V.
H1, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, H12, H13, H14, N7, N8, P1, P14	DVSS	Digital Ground.
K1	DIN6B_N	DAC B Data Input Lane 6 Negative.
K2	DIN4B_N	DAC B Data Input Lane 4 Negative.
K3	DIN1B_N	DAC B Data Input Lane 1 Negative.
K4	DOU3D_P	ADC D Data Output Lane 3 Positive.
K5	DOU3D_N	ADC D Data Output Lane 3 Negative.
K6	DOU3C_P	ADC C Data Output Lane 3 Positive.
K7	DCO_N	LVDS Data Clock Output Negative.
K8	DCO_P	LVDS Data Clock Output Positive.
K9	DOU3B_P	ADC B Data Output Lane 3 Positive.
K10	DOU3A_N	ADC A Data Output Lane 3 Negative.
K11	DOU3A_P	ADC A Data Output Lane 3 Positive.
K12	DIN1A_N	DAC A Data Input Lane 1 Negative.
K13	DIN4A_N	DAC A Data Input Lane 4 Negative.
K14	DIN6A_N	DAC A Data Input Lane 6 Negative.

Pin No.	Mnemonic	Description
L1	DIN6B_P	DAC B Data Input Lane 6 Positive.
L2	DIN4B_P	DAC B Data Input Lane 4 Positive.
L3	DIN1B_P	DAC B Data Input Lane 1 Positive.
L4	DOU1D_N	ADC D Data Output Lane 1 Negative.
L5	DOU2D_N	ADC D Data Output Lane 2 Negative.
L6	DOU1C_N	ADC C Data Output Lane 1 Negative.
L7	DOU3C_N	ADC C Data Output Lane 3 Negative.
L8	DOU3B_N	ADC B Data Output Lane 3 Negative.
L9	DOU1B_N	ADC B Data Output Lane 1 Negative.
L10	DOU2A_N	ADC A Data Output Lane 2 Negative.
L11	DOU1A_N	ADC A Data Output Lane 1 Negative.
L12	DIN1A_P	DAC A Data Input Lane 1 Positive.
L13	DIN4A_P	DAC A Data Input Lane 4 Positive.
L14	DIN6A_P	DAC A Data Input Lane 6 Positive.
M1	DIN5B_N	DAC B Data Input Lane 5 Negative.
M2	DIN3B_N	DAC B Data Input Lane 3 Negative.
M3	DIN3B_P	DAC B Data Input Lane 3 Positive.
M4	DOU1D_P	ADC D Data Output Lane 1 Positive.
M5	DOU2D_P	ADC D Data Output Lane 2 Positive.
M6	DOU1C_P	ADC C Data Output Lane 1 Positive.
M7	STROBE_N	LVDS Data Output Strobe Negative.
M8	STROBE_P	LVDS Data Output Strobe Positive.
M9	DOU1B_P	ADC B Data Output Lane 1 Positive.
M10	DOU2A_P	ADC A Data Output Lane 2 Positive.
M11	DOU1A_P	ADC A Data Output Lane 1 Positive.
M12	DIN3A_N	DAC A Data Input Lane 3 Negative.
M13	DIN3A_P	DAC A Data Input Lane 3 Positive.
M14	DIN5A_N	DAC A Data Input Lane 5 Negative.
N1	DIN5B_P	DAC B Data Input Lane 5 Positive.
N2	DIN2B_N	DAC B Data Input Lane 2 Negative.
N3	DIN0B_N	DAC B Data Input Lane 0 Negative.
N4	DOU0D_N	ADC D Data Output Lane 0 Negative.
N5	DOU0C_N	ADC C Data Output Lane 0 Negative.
N6	DOU2C_N	ADC C Data Output Lane 2 Negative.
N9	DOU2B_N	ADC B Data Output Lane 2 Negative.
N10	DOU0B_N	ADC B Data Output Lane 0 Negative.
N11	DOU0A_N	ADC A Data Output Lane 0 Negative.
N12	DIN0A_N	DAC A Data Input Lane 0 Negative.
N13	DIN2A_N	DAC A Data Input Lane 2 Negative.
N14	DIN5A_P	DAC A Data Input Lane 5 Positive.
P2	DIN2B_P	DAC B Data Input Lane 2 Positive.
P3	DIN0B_P	DAC B Data Input Lane 0 Positive.
P4	DOU0D_P	ADC D Data Output Lane 0 Positive.
P5	DOU0C_P	ADC C Data Output Lane 0 Positive.
P6	DOU2C_P	ADC C Data Output Lane 2 Positive.
P7	DCI_N	LVDS Data Clock Input Negative.
P8	DCI_P	LVDS Data Clock Input Positive.
P9	DOU2B_P	ADC B Data Output Lane 2 Positive.
P10	DOU0B_P	ADC B Data Output Lane 0 Positive.
P11	DOU0A_P	ADC A Data Output Lane 0 Positive.
P12	DIN0A_P	DAC A Data Input Lane 0 Positive.
P13	DIN2A_P	DAC A Data Input Lane 2 Positive.

TYPICAL PERFORMANCE CHARACTERISTICS

RECEIVER ADC PERFORMANCE

$f_{ADC} = 250$ MHz, unless otherwise specified.

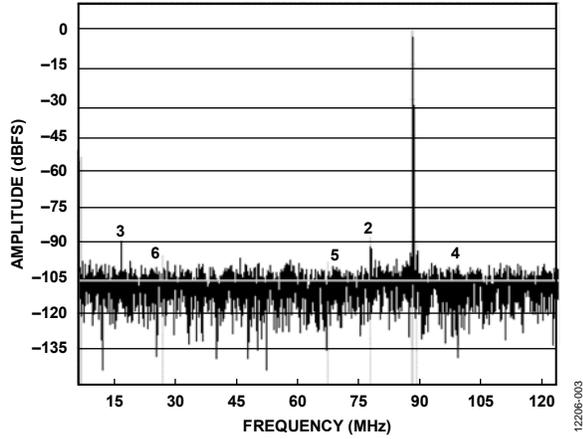


Figure 3. Single Tone FFT, $f_{IN} = 87$ MHz

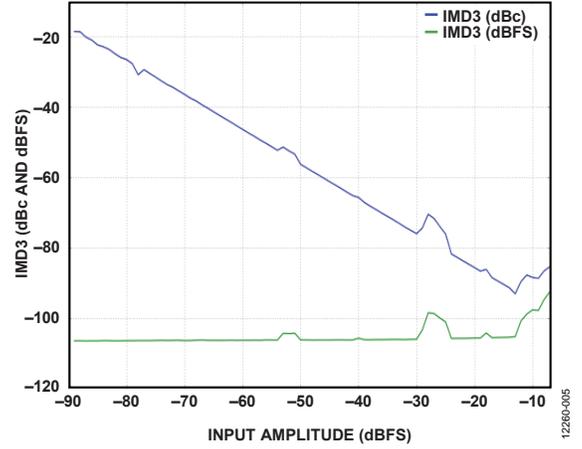


Figure 6. Two Tone IMD3 vs. Input Amplitude (A_{IN}), $f_{IN1} = 89.12$ MHz, $f_{IN2} = 92.12$ MHz

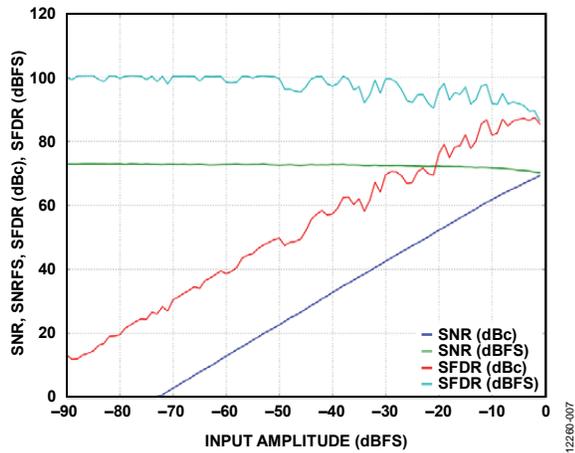


Figure 4. Single Tone SNR and SFDR vs. Input Amplitude (A_{IN}), $f_{IN} = 87$ MHz

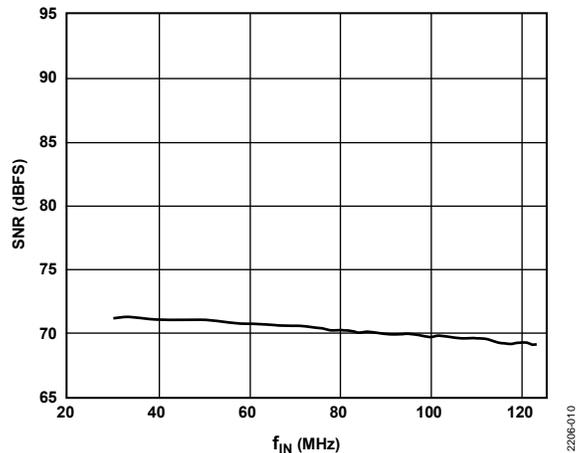


Figure 7. Single Tone SNR vs. Input Frequency (f_{IN})

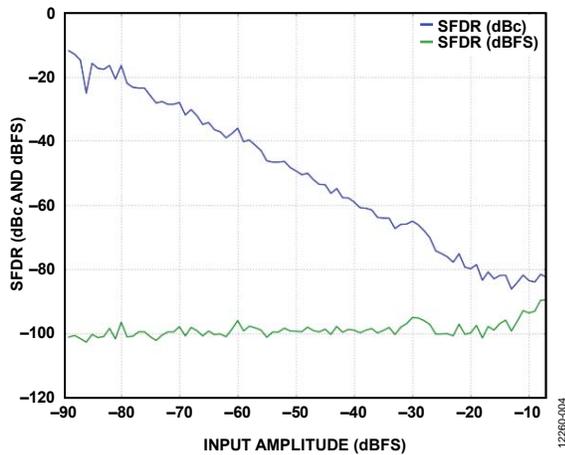


Figure 5. Two Tone SFDR vs. Input Amplitude (A_{IN}), $f_{IN1} = 89.12$ MHz, $f_{IN2} = 92.12$ MHz

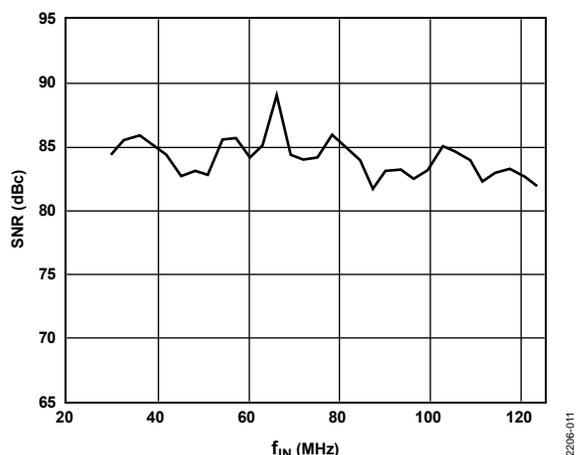


Figure 8. Single Tone SNR vs. Input Frequency (f_{IN})

$f_{ADC} = 250$ MHz, unless otherwise specified.

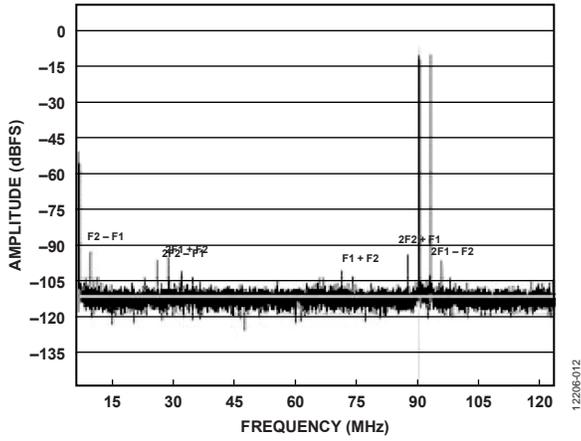


Figure 9. Two Tone FFT, $f_{IN1} = 89.12$ MHz, $f_{IN2} = 92.12$ MHz

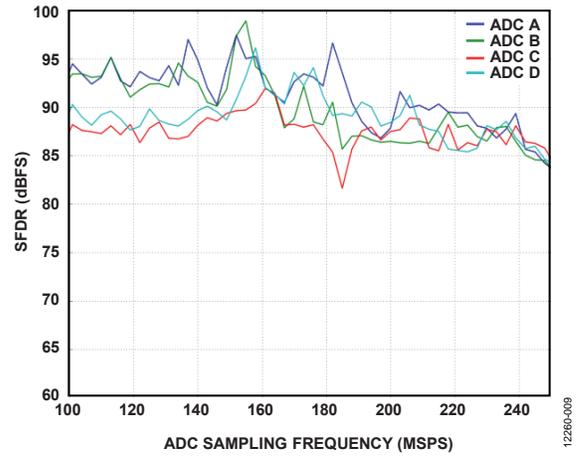


Figure 11. Single Tone SFDR vs. ADC Sampling Frequency (f_{ADC}), $f_{IN} = 90.0$ MHz, All Four ADCs

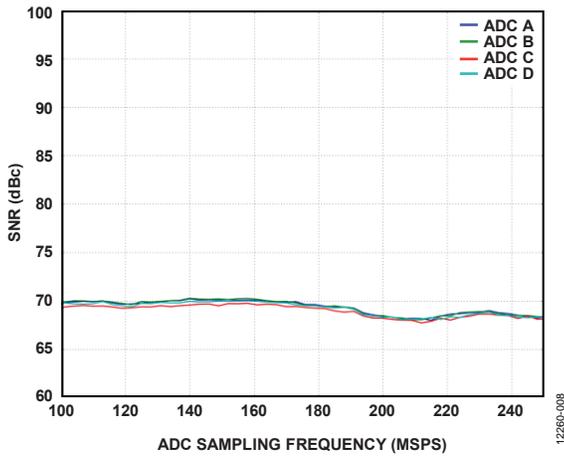


Figure 10. Single Tone SNR vs. ADC Sampling Frequency (f_{ADC}), $f_{IN} = 90.0$ MHz, All Four ADCs

TRANSMITTER DAC PERFORMANCE

$f_{DAC} = 500$ MHz, unless otherwise specified.

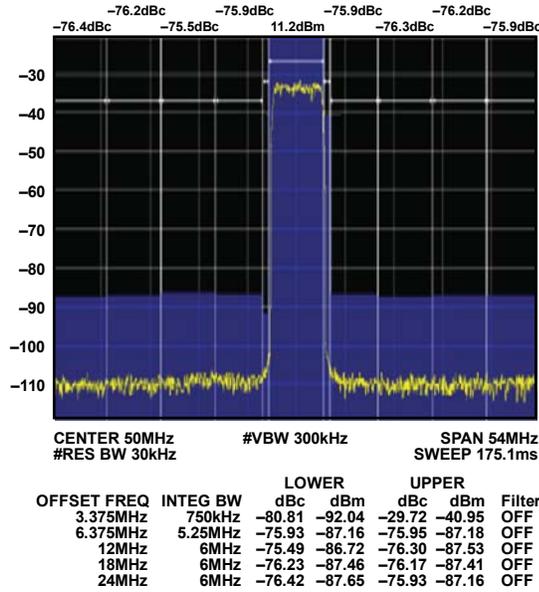


Figure 12. 5 MHz Bandwidth 256-QAM Adjacent Channel Power

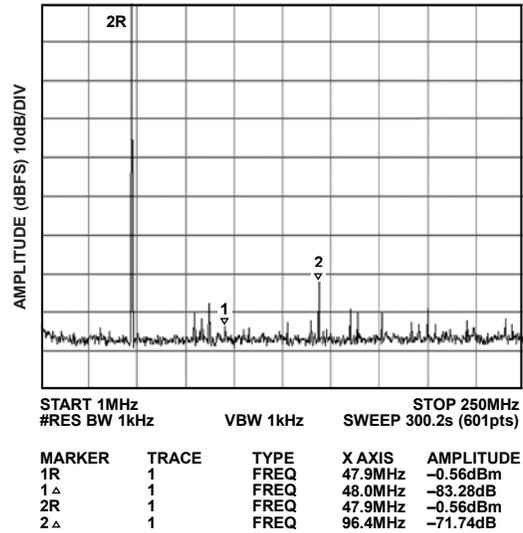


Figure 15. 1st Nyquist Zone Output Spectrum, $f_{OUT} = 48$ MHz

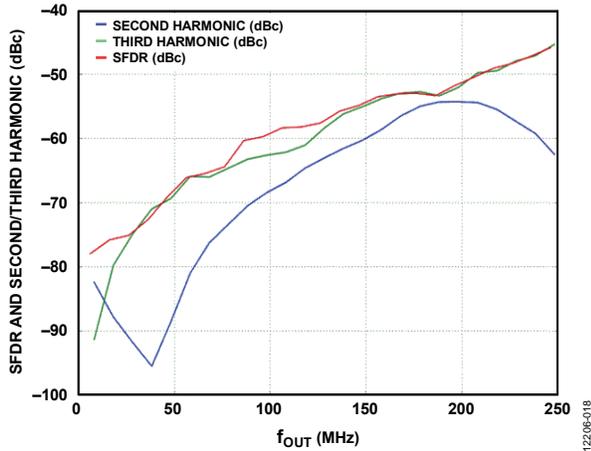


Figure 13. SFDR, 2nd and 3rd Harmonics vs. f_{OUT} , Maximum I_{OUTFS} (DAC Gain)

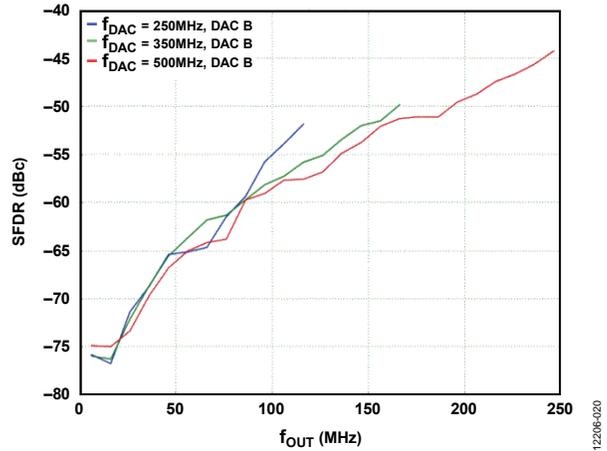


Figure 16. SFDR at Three DAC Sampling Frequencies (f_{DAC}) vs. f_{OUT}

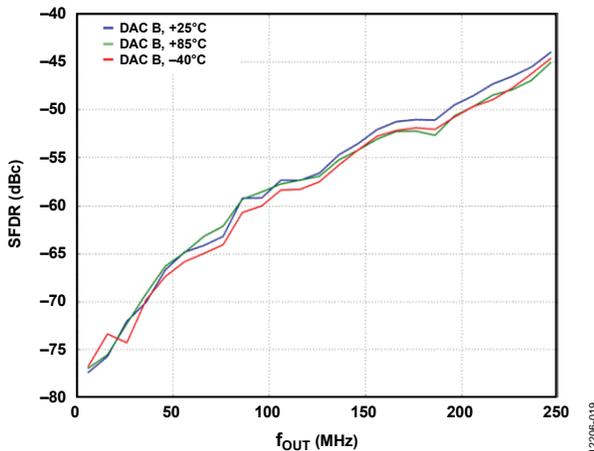


Figure 14. SFDR at Three Temperatures vs. f_{OUT}

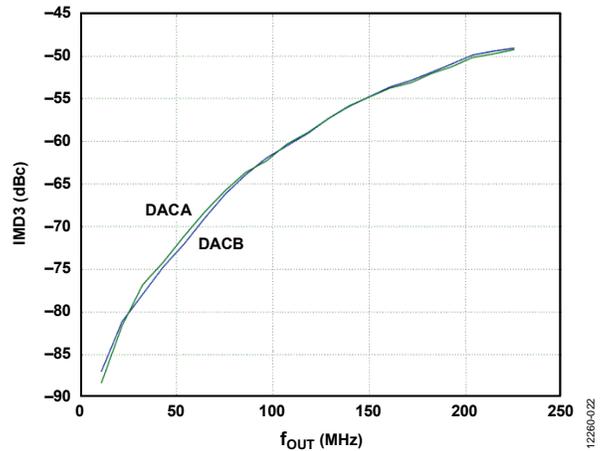


Figure 17. IMD3 vs. f_{OUT} , Both DACs

$f_{DAC} = 500$ MHz, unless otherwise specified.

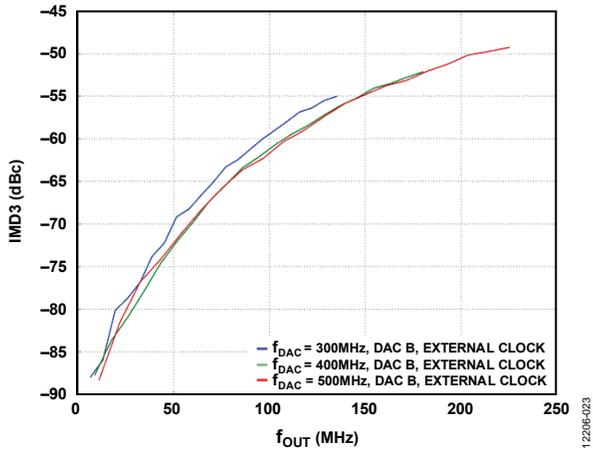


Figure 18. IMD3 at Three DAC Sampling Frequencies (f_{DAC}) vs. f_{OUT}

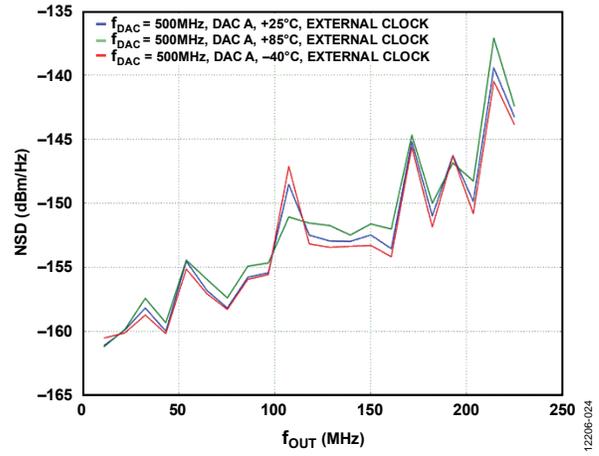


Figure 19. NSD at Three Temperatures vs. f_{OUT}

TERMINOLOGY

Linearity Error (Integral Nonlinearity or INL)

INL is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)

DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity

A digital-to-analog converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error

Offset error is the deviation of the output current from the ideal of zero. For IOU_{Tx_P}, 0 mA output is expected when the inputs are all 0s. For IOU_{Tx_N}, 0 mA output is expected when all inputs are set to 1.

Gain Error

Gain error is the difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1, minus the output when all inputs are set to 0. The ideal gain is calculated using the measured VREF. Therefore, the gain error does not include effects of the reference.

Output Compliance Voltage

Output compliance voltage is the range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift

Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Settling Time

Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Noise Spectral Density (NSD)

Noise spectral density is the average noise power normalized to a 1 Hz bandwidth, with the DAC converting and producing an output tone.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Signal to Noise and Distortion (SINAD)

The ratio of the total signal power level (wanted signal + noise + distortion or SND) to unwanted signal power (noise + distortion or ND).

THEORY OF OPERATION

PRODUCT DESCRIPTION

Figure 1 shows a block diagram of the MxFE. This product integrates four 14-bit ADCs and two 14-bit DACs. The DAC data interface consists of six DDR LVDS data lanes for each DAC and a shared DCI_P/DCI_N clock (hereafter referred to as DCI). The ADC data interface consists of four DDR LVDS data lanes for each ADC with a shared DCO_P/DCO_N clock (hereafter referred to as DCO) and a shared STROBE output. The MxFE control and status registers are written/read via an SPI interface. ADC and DAC datapaths include FIFO buffers to absorb phase differences between LVDS lane timing and the data converter sampling clocks. Internal AD9993 clock signals can be developed from an external clock signal or from the output of an on-chip PLL frequency multiplier driven by an external reference oscillator.

SPI PORT

The AD9993 provides a 4-wire synchronous serial communications SPI port that allows easy interfacing to ASICs, FPGAs, and industry-standard microcontrollers. The interface facilitates read/write access to all registers that configure the AD9993. Its data rate can be up to 25 MHz.

SPI Port Signals

SPI_SCLK (serial clock) is the serial shift clock. The serial clock pin synchronizes data to and from the device and runs the internal state machines. All address and input data bits are sampled on the rising edge of SPI_SCLK. All output data is driven out on the falling edge of SPI_SCLK.

$\overline{\text{SPI_CS}}$ (chip select) is an active low control signal used by the SPI master to select the AD9993 SPI port. When $\overline{\text{SPI_CS}}$ is high, SPI_SDO is in a high impedance state. During the communication cycle, chip select must remain low.

SPI_SDI (serial data input) is the address and data input, sampled on the rising edge of SPI_SCLK.

SPI_SDO (serial data output) is the data output pin. Data is shifted out on the falling edge of SCLK.

Figure 20 shows a timing diagram for a single byte MSB first AD9993 SPI write operation. Each AD9993 register address is an 8-bit value. During the first SPI_SCLK cycle, SPI_SDI = 0, indicating that the operation is a data write. SPI_SDI is always held low for the next two clock cycles. The next 13 clock cycles are the first register address. The next eight clock cycles contain data to be written. The write operation ends when $\overline{\text{SPI_CS}}$ goes high. In this example, data for one 8-bit register is written. Multiple registers can be written in a single write operation by keeping $\overline{\text{SPI_CS}}$ low for multiple byte periods. The register address is automatically updated using an address counter as bytes are written while $\overline{\text{SPI_CS}}$ remains low.

Figure 21 depicts an MSB first register read operation. Register data from the AD9993 appears on SPI_SDO starting on the SPI_SCLK cycle following the last bit of the 16-bit instruction header on SPI_SDI. Multiple registers can be read in a single read operation by keeping $\overline{\text{SPI_CS}}$ low for multiple byte periods.

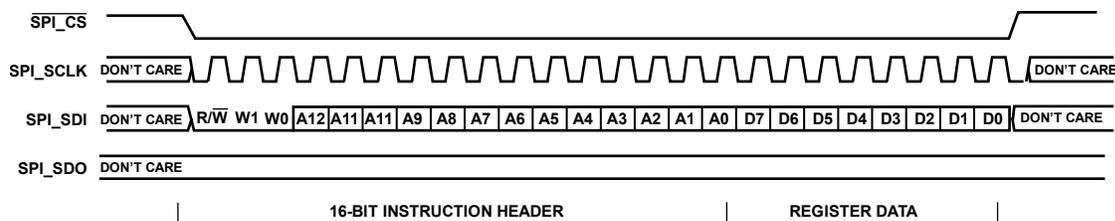


Figure 20. 4-Wire SPI Interface Timing, MSB First Write

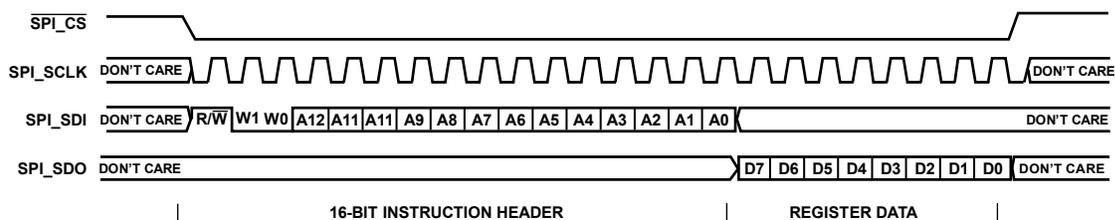


Figure 21. 4-Wire SPI Interface Timing, MSB First Read

SPI CONFIGURATION PROGRAMMING

The SPI_CONFIG register controls AD9993 SPI interface operation. By default, the SPI bus operates MSB first. In MSB first mode, the register address counter decrements automatically during multiple byte reads or writes. The SPI bus can be configured to run LSB first by setting the SPI_LSB_FIRSTx bits to 1. During LSB first multiple register read or write operations, the register address counter is incremented automatically. SPI registers can be reset to their Reset values by setting the self-clearing SPI_SOFT_RESETx bits to 1.

REGISTER UPDATE TRANSFER METHOD

Changes to the writeable SPI registers labeled transfer in Table 10 do not take effect immediately when written to the device via the SPI. Values are held in a shadow register set until the self-clearing CHIP_REGMAP_TRANSFER bit in the DEVICE_UPDATE register is set. All changes to transfer register values then take effect simultaneously.

ADC REGISTER UPDATE INDEXING

In addition to the register transfer mechanism, the POWER_MODES and FLEX_OUTPUT_MODE registers have an indexing mechanism. Each of the four ADC cores has its own page containing these registers. These pages can be programmed independently or simultaneously in any combination. ADC core register sets are addressed for a particular register map master/slave transfer by setting the SPI_ADC_x_INDEX bits in the DEVICE_INDEX register. Register data is transferred to the ADC core pages that have these bits set when the next transfer occurs.

ADCs

The MxFE ADCs are multistage pipelined CMOS ADC cores designed for use in communications receivers.

ADC ARCHITECTURE

The AD9993 architecture consists of a dual front-end sample-and-hold circuit, followed by a pipelined switched capacitor ADC. The quantized outputs from each stage are combined into a final 14-bit result.

The input stage of each ADC core contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes.

Input Common-Mode Voltage (V_{CM}) References

The analog inputs of the AD9993 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that $V_{CM} = 0.5 \times AVDD$ (or 0.9 V) is recommended for optimum performance. Four on-board common-mode voltage references are included in the design, one for each AD9993 ADC, and are available from the

A_CML, B_CML, C_CML, and D_CML pins. Using these common-mode voltage outputs to set the input common mode of each ADC is recommended. Optimum performance is achieved when the common-mode voltage of the analog input is set by the on-chip common mode references. The A_CML, B_CML, C_CML, and D_CML pins must be decoupled to ground by a 0.1 μ F capacitor.

ADC SECTION PROGRAMMING

Each of the four ADCs has its power mode programmed by the indexed ADC_PDWN_MODE bit field of the POWER_MODES register (see the ADC Register Update Indexing section). At reset, all four ADC cores are in power-down mode.

ADC digital data output modes are programmed by the indexed FLEX_OUTPUT_MODE register (see the ADC Register Update Indexing section). Setting the DP_OUT_DATA_EN_N bit to 0 enables the data output of each ADC selected in the DEVICE_INDEX register. At reset, ADC output data is disabled. Setting the DP_OUT_DATA_INV bit to 1 inverts the data output from selected ADCs. The DP_OUT_DFS bit field selects the output code for each selected ADC, offset binary (twos complement with the sine bit inverted), twos complement (reset value), or gray code.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9993 is a differential switched capacitor circuit that has been designed for optimum performance while processing a differential input signal.

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 22. To bias the analog input, the V_{CM} voltage can be connected to the center tap of the secondary winding of the transformer.

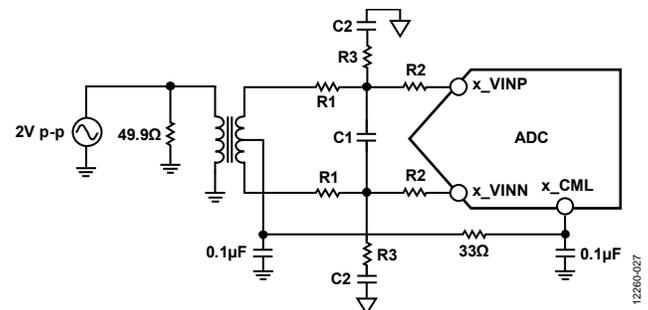


Figure 22. Differential Transformer-Coupled Configuration

Differential double balun coupling is used as the input configuration for AD9993 ADC performance characterization (see Figure 23). In this configuration, the input is ac-coupled and the V_{CM} voltage is provided to each input through a 33 Ω resistor. These resistors compensate for losses in the input baluns to provide a 50 Ω impedance to the driver.

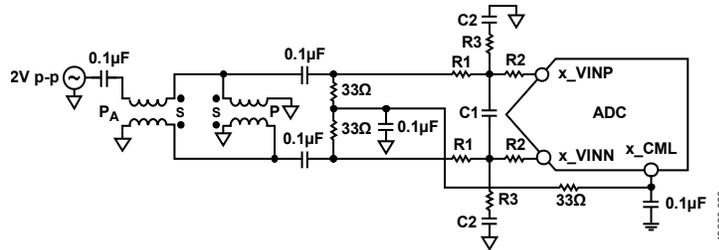


Figure 23. Differential Double Balun Input Configuration

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance. Based on these parameters, the value of the input resistors and capacitors may need to be adjusted or some components may need to be removed. Table 7 displays recommended values to set the RC network for the 0 MHz to 100 MHz frequency range:

Table 7. Example RC Network

Component	Value
R1 Series	33 Ω
C1 Differential	8.2 pF
R2 Series	0 Ω
C2 Shunt	15 pF
R3 Shunt	49.9 Ω

The values given in Table 7 are for each R1, R2, C1, C2, and R3 component shown in Figure 22 and Figure 23.

ADRF6518 as ADC Driver

The ADRF6518 is a variable gain amplifier and low-pass filter that is designed to drive the analog inputs of analog-to-digital converters like the ones included in the AD9993. A principle application of the ADRF6518 is as part of the signal chain in a wideband radio receiver. Figure 32 shows a block diagram for a wideband microwave radio that includes the ADRF6518 and the AD9993.

The low impedance (<math><10\ \Omega</math>) output buffers of the ADRF6518 are designed to drive ADC inputs. They are capable of delivering up to 4 V p-p composite two-tone signals into 400 Ω differential loads with >60 dBc IMD3. The output common-mode voltage can be adjusted to 900 mV (the AD9993 input common-mode voltage) without loss of drive capability by presenting the ADRF6518 VOCM pin with the desired common-mode voltage. The high input impedance of VOCM allows the AD9993 reference output (A_CML, B_CML, C_CML or D_CML) to be connected directly.

DACs

The MxFE DACs are part of the Analog Devices high speed CMOS DAC core family. These DACs are designed to be used as part of wide bandwidth communication system transmitter signal chains.

DAC TRANSFER FUNCTION

The AD9993 DACs provide two differential current outputs: IOUTA_P/IOUTA_N, and IOUTB_P/IOUTB_N.

The DAC output current equations are as follows:

$$IOUT_{x_P} = IOUT_{FS} \times DACx \text{ input code} / 2^{14}$$

$$IOUT_{x_N} = IOUT_{FS} \times ((2^{14} - 1) - DACx \text{ input code}) / 2^{14}$$

where:

$$DACx \text{ input code} = 0 \text{ to } 2^{14} - 1.$$

$IOUT_{FS}$ is the full-scale output current or DAC gain specified in Table 1.

$$IOUT_{FS} = 32 \times I_{REFx}$$

where $I_{REFx} = V_{REFDAC} / R_{FSADJ_x}$.

Each DAC has its own I_{REFx} set resistor, R_{FSADJ_x} . R_{FSADJ_x} resistors can be on or off chip at the discretion of the users. The nominal value of R_{FSADJ_x} is 1.6 kΩ. The nominal value of V_{REFDAC} is 1.0 V. V_{REFDAC} can be selected as the on-chip band gap reference or as an external user supplied reference.

DAC outputs have a $\sin(\pi f_{OUT} / f_{DAC}) / (\pi f_{OUT} / f_{DAC})$ envelope response as a function frequency. This response is also referred to as a sinc envelope.

DAC OUTPUT COMPLIANCE VOLTAGE RANGE AND AC PERFORMANCE

Each DAC has a pair of differential current outputs. The compliance voltage range for each of these two outputs is specified in Table 1. Optimal DAC ac performance is achieved when the output common-mode voltage is between 0.0 V and 0.5 V. and the signal swing falls within the compliance range.

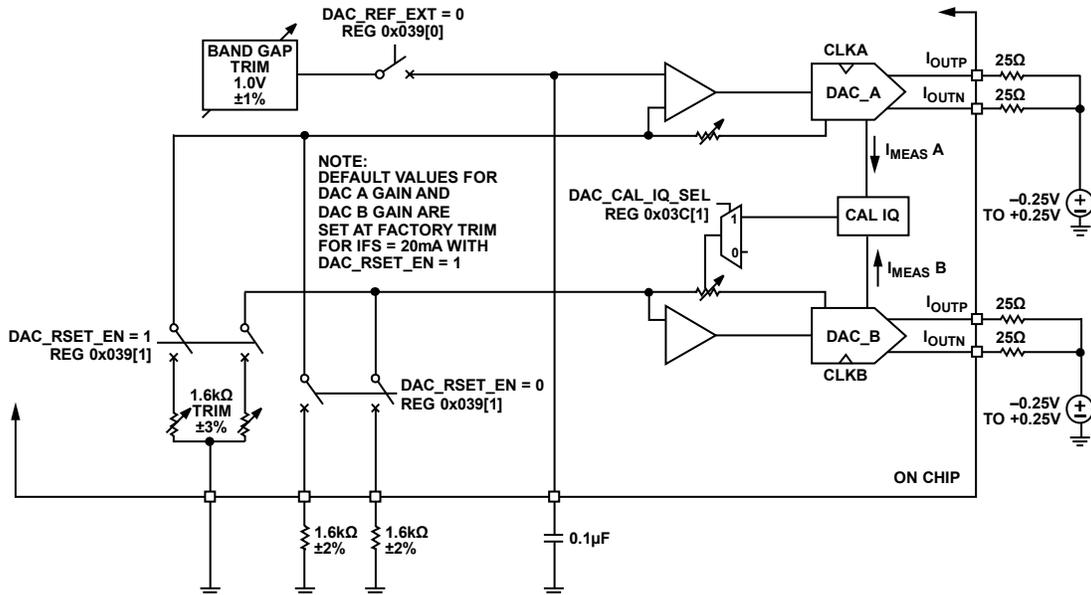


Figure 24. DACs, Band Gap Reference, On-Chip and Off-Chip R_{FSADJ_x} DAC Gain Setting, and IQ Calibration

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Selecting DAC Output Common-Mode Voltage

Two steps are required to select the common-mode output voltages for the two DACs. For a common-mode voltage less than 0.5 V, the CML_A and CML_B pins are grounded. For common-mode voltages that are greater than or equal to 0.5 V, connect a 0.1 μ F capacitor between CML_A or CML_B and ground. The second step is to program the DAC_VCM_VREF_BIT bit field. There are three common-mode level settings to choose from. This common-mode setting applies to both DACs.

DAC VOLTAGE REFERENCE

The DACs use a single common voltage reference. An on-chip band gap reference is provided. Optionally, an off-chip voltage reference can be used. If an off-chip DAC reference is used, set the DAC_REF_EXT bit in the DAC_CTRL register to 1. After reset, the on-chip reference is selected.

DAC GAIN SETTING

Figure 24 is a diagram of the AD9993 DACs gain setting section. It shows the two transmit DACs, the bypassable built-in 1.0 V band gap reference, and the selectable internal and board level R_{FSADJ_x} resistors. By default, the on-chip band gap reference is selected. If using a board level DAC reference voltage, write 1 to the DAC_REF_EXT bit of the DAC_CTRL register.

Each DAC has its own R_{FSADJ_x} set resistor. These resistors can be on or off chip at the discretion of the user. When the on-chip resistors are in use, their gain accuracy is factory calibrated. When the off-chip R_{FSADJ_x} resistors are used, an on-chip IQ calibration scheme can be employed to maintain accuracy between DAC pairs. By default, the on-chip R_{FSADJ_x} is selected. If using a board level R_{FSADJ_x} , write 0 to the DAC_RSET_EN bit of the DAC_CTRL register.

DAC IQ Gain Calibration

When board level R_{FSADJ_x} resistors are used, the gains of the two DACs can be better matched by running the automatic DAC IQ gain calibration procedure. This is done by programming the DAC_CAL_IQ_CTRL register and observing the DAC_CAL_IQ_STAT register as follows:

1. Write 0x23 to DAC_CAL_IQ_CTRL (power up the DAC clock, enable IQ calibration, and start IQ calibration).
2. Read the DAC_CAL_IQ_DONE bit of the DAC_CAL_IQ_STAT register until it goes high.
3. Write 0x4 to DAC_CAL_IQ_CTRL.

DAC DATAPATH FORMAT SELECTION

At reset, the DAC_BINARY bit in the DAC_DP_FMT register is set to 0, selecting twos complement as the data input format for both DACs. To select binary offset, set the DAC_BINARY bit to 1.

DAC TEST TONE GENERATOR DDS

The AD9993 includes a tunable direct digital synthesizer for DAC output tone generation. When the DDS_EN bit of the DDS_CTRL register is set to 1, the DDS becomes the digital signal source for the two DACs. The DDS_CTRL register also has a clock inversion control and amplitude attenuation controls. At reset, the 32-bit DDS tuning word in the DDS_TW1_3, DDS_TW1_2, DDS_TW1_1, and DDS_TW1_0 registers is set to 0x19A00000. This value programs the DDS to produce a 50 MHz tone at both DAC outputs if the master clock frequency is 1 GHz (DAC sampling rate = 500 MSPS). The equation for DDS output frequency is

$$f_{DDS} = (DDS_TW1/2^{32}) \times f_{DAC}$$

CLOCKING

The clock signals for the LVDS lanes, the DACs, and the ADCs are developed from a single master clock signal. This signal is either input directly on the CLKP/CLKN pins or synthesized by an on-chip PLL multiplier using the REFCLK input signal as a reference. The ADC output and DAC input LVDS lanes run at the master clock frequency divided by 2 and are DDR. Data is clocked on both edges. The sampling rate of the ADCs is $\frac{1}{4}$ the master clock rate. The sampling rate of the DACs is $\frac{1}{2}$ the master clock frequency. A 1 GHz master clock is shown in Figure 1.

At a 1 GHz master clock frequency, the other on-chip clock frequencies are as follows:

- DCO (ADC DDR LVDS output lane clock): 500 MHz
- DCI (DAC DDR LVDS input lane clock): 500 MHz
- DAC sampling rate: 500 MSPS
- ADC sampling rate: 250 MSPS

ON-CHIP PLL CLOCK MULTIPLIER

Figure 25 shows a block diagram of the MxFE on-chip PLL clock multiplier. If the PLL clock multiplier is used to generate

the master clock, the buffered VCO output signal is divided by 4 to produce the synthesized master clock signal.

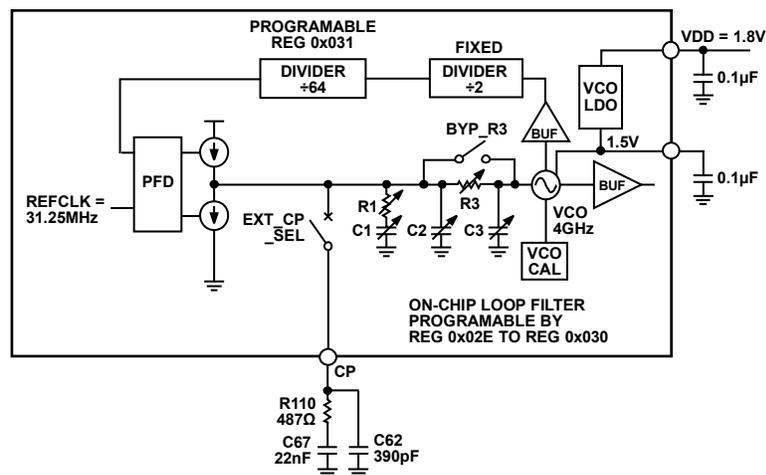
The reference clock of the on-chip PLL can be either 31.25 MHz or 62.5 MHz. When using a 62.5 MHz clock, a divide by 2 option is provided, as shown in Figure 25, such that the internal PLL reference clock can be set to 31.25 MHz.

A programmable loop filter is integrated on chip. At reset, the on-chip loop filter bandwidth is set to 500 kHz. Lower loop bandwidth can be achieved using an external loop filter connected to the CP pin, as shown in Figure 25.

An on-chip LDO provides the supply voltage for the VCO.

PLL Synthesizer Control and Status Registers

At reset, the SYNTH_INT register contains the reset default value for the VCO output divider of 64 (shown in Figure 25). The PLL multiplier lock status can be read back on Bit 1 of the SYNTH_STAT register. Calibration status is also read from this register. Bits in the SYNTH_CTRL register are used to enable charge pump calibration and to start synthesizer calibration. Synthesizer calibration is required as part of the process of acquiring lock. Charge pump calibration and synthesizer calibration are steps described in the Power-Up Routine When Using the On-Chip Clock Synthesizer section.



NOTES
1. WHEN USING EXTERNAL LOOP FILTER SET C1, C2, C3, R1, AND R3 TO MIN OR MAX VALUES AS DEFINED IN REGISTER DESCRIPTION, AS DESIRED.

Figure 25. On-Chip PLL Clock Multiplier Block Diagram

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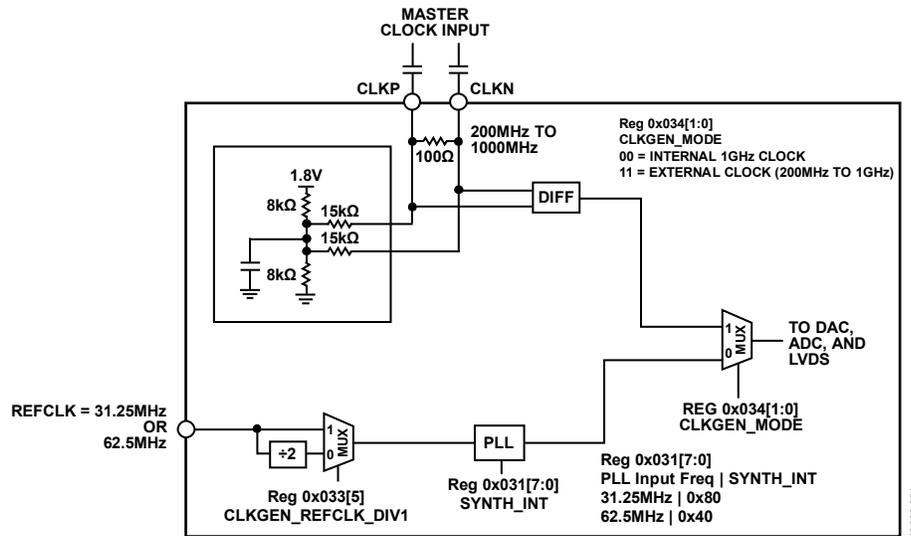


Figure 26. MxFE Clock Control

SELECTING CLOCKING OPTIONS

Figure 26 is a block diagram of the MxFE clocking system and its controls. Options of using either an external master clock or a master clock generated from the on-chip PLL are provided. CLKGEN_MODE[1:0] in the CLKGEN_CTRL2 register selects the PLL multiplier or CLKP/CLKN as the master clock source.

ADC DATAPATH AND DAC DATAPATH FIFOS

In the AD9993, data FIFOs are placed between the ADC core outputs and the LVDS buffers and drivers. Similarly, on the DAC side, data FIFOs are placed between the LVDS input buffers and the DAC cores. These FIFOs absorb the phase difference between DCI and the DAC sampling clock and between the ADC sampling clock and DCO. DAC sampling clock and DCI are locked in frequency but have an unknown phase relationship. The ADC sampling clock and DCO have the same characteristics.

FIFOs are eight samples deep. During a start-up register sequence, both the DAC input datapath FIFOs and the ADC output data path FIFOs have their read and write pointers initialized (see the Start-Up Register Sequences section). This occurs after all clocks in the AD9993 are running and settled. The pointers are set four data samples apart. The ADC datapath FIFO depth can be read in the RXFIFO_WR_OFFSET bit field in the align register. The DAC datapath FIFO depth can be read

as the RXFIFO_THERM[7:0] value in the DAC_FIFO_STS1 register. This value is a thermometer code. FIFO depths remain constant after initialization when all clocks are running properly.

LVDS INTERFACES

Each DAC has seven DDR LVDS input data lanes. Each DAC sample input requires the user to input two 7-bit words to the interface with appropriate zero stuffing. Each ADC has four DDR LVDS output data lanes. For each ADC output sample, four 4-bit words are output.

LVDS ADC Data Link

There are two LVDS ADC buses for the two ADCs. Each LVDS ADC Data bus has four lanes for 14-bit data output in two full DDR cycles. A strobe lane is shared by the four ADC LVDS links to identify the MSB of the 14-bit data. Figure 27 shows one LVDS ADC output data link with four lanes. Lane 0 to Lane 2 output the 12 MSBs of the 14-bit ADC data. Lane 3 carries the two LSBs of the 14-bit ADC data and an overrange bit.

LVDS DAC Data Link

There are two LVDS DAC data links for the dual DAC. Each LVDS DAC data link has seven lanes capable of transmitting 14-bit data in one DDR full cycle. Figure 28 shows one LVDS DAC input data link with seven lanes.

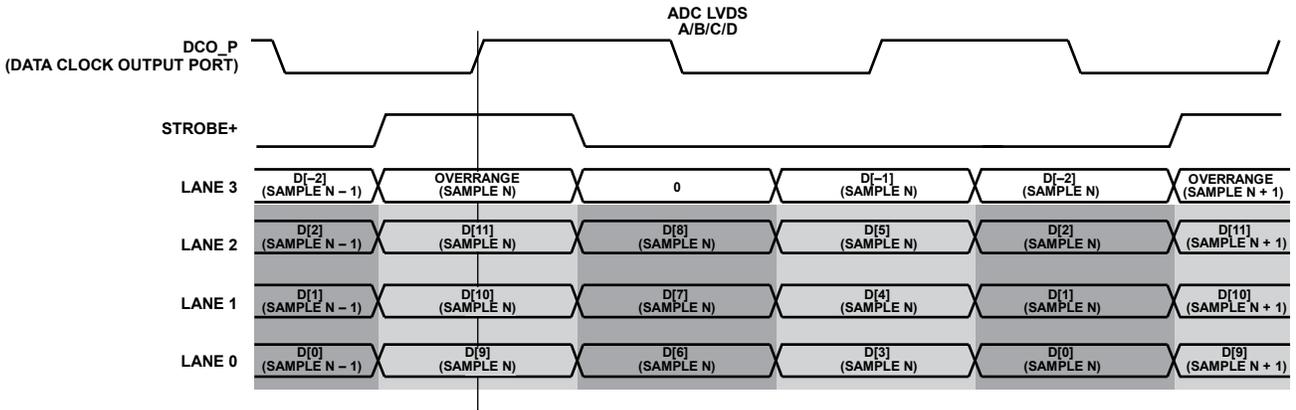


Figure 27. Output Sample Data Format

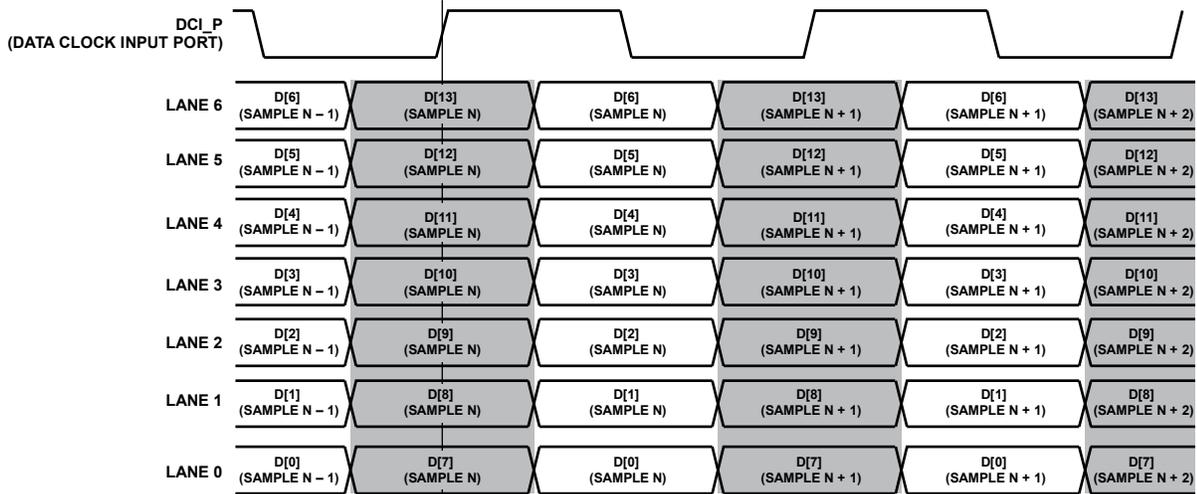


Figure 28. DAC Input Sample Data Format

LVDS INTERFACE TIMING

DAC Input Interface

Table 8 specifies the setup and hold time requirements for DAC LVDS data lane inputs relative to DCI. Figure 29 shows a timing diagram for this interface. DDR DCI edges occur at the position within the data eye (the white region in Figure 29) listed in Table 8.

Table 8. DAC DDR LVDS Input Setup and Hold Times Relative to DCI (Guaranteed)

Parameter	Minimum	Unit
$ t_{SU} $	150	ps
$ t_{HOLD} $	200	ps
Data Period	1000	Ps

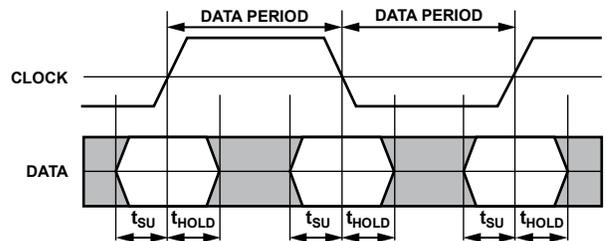


Figure 29. DAC Input LVDS Lane Timing

ADC Output Interface

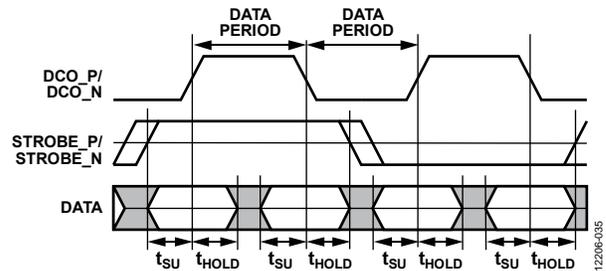


Figure 30. ADC Output LVDS Lane Timing

Table 9 specifies the time between the ADC LVDS data lane output transitions and the DDR DCO clock edge 50% transition point.

Table 9. ADC DDR LVDS Data and Strobe Output Setup and Hold Times Relative to DCO (Guaranteed)

Parameter	Minimum	Unit
t _{SU}	400	ps
t _{HOLD}	430	ps
Data Period	1000	ps

LVDS LANE TESTING USING PRBS

One pseudorandom binary sequence (PRBS) generator is included for each ADC LVDS lane and one PRBS detector on each DAC LVDS lane. The designs for the generator and detector are implemented as a 23rd-order pseudorandom noise (PN23) sequence defined by the generator polynomial $x^{23} + x^{18} + 1$. The initial seed of the generator is programmable so that each lane can output different values if started simultaneously. The four seed registers are indexed as described in the ADC Register Update Indexing section.

DAC PRBS test results are read back on the DAC_A_PRBS_ERRx and DAC_B_PRBS_ERRx error counter registers. The DAC input PRBS error counters are enabled and the error counters cleared by the bits in the DAC_PRBS_CTRL register. ADC output lane PRBS generation is controlled by the bits in the PRBS_GEN_CTRL register.

POWER MODE PROGRAMMING

The AD9993 has a POWER_MODES register that allows the user to place sections of the chip into different power modes. The PDWN_PIN_FUNC bit programs the function of the PDWN pin. By default, assertion of PDWN causes the AD9993 to go into full power-down. The clock generator, indexed ADCs, DACs, and PLL synthesizer are all powered down at reset. The indexed ADCs have four power modes. See the ADC Register Update Indexing section for a definition of indexing.

INTERRUPT REQUEST OPERATION

The AD9993 provides an interrupt request signal, ALERT. It is used to notify the user system of significant on-chip events. The ALERT pin is an open-drain, active low output.

Eight different event flags provide visibility into the device. These raw events are located in the INT_RAW register. These raw events are always latched in the INT register. If the event is left unmasked, the latched event triggers an external interrupt on ALERT. INTEN is the interrupt enable register. When an event is masked, the INT register captures the event in latched form. A masked event does not cause ALERT to go true.

The eight events that trigger an interrupt (if enabled) are

- PLL lock lost
- PLL locked
- FIFO Warning 1
- FIFO Warning 2
- ADC A overrange
- ADC B overrange
- ADC C overrange
- ADC D overrange

Interrupt Service Routine

For the interrupt service routine, interrupt request management starts by selecting the set of events that require host intervention or monitoring using the bits in the INTEN register. For events requiring host intervention, upon ALERT activation, run the following routine to clear an interrupt request:

1. Read the status of the latched bits in the INT register that are being monitored.
2. Monitor the unlatched status bits in the INT_RAW register directly if needed.
3. Perform any actions that may be required to clear the interrupt(s).
4. Read the INT_RAW bits to verify that the actions taken have cleared the event.
5. Clear the interrupt by writing 1 to the event flag bit in the INT register.

TEMPERATURE SENSOR

The AD9993 has a diode-based temperature sensor for measuring the temperature of the die. The temperature reading is accessed using the TS_RD_LSB and TS_RD_MSB registers. The temperature of the die can be calculated as

$$T_{DIE} = \frac{Die\ Temp[15:0] - 41,237}{106}$$

where:

T_{DIE} is the die temperature in degrees Celsius.

$Die\ Temp$ is the concatenated 16-bit contents of the TD_RD_LSB and TD_RD_MSB registers. The temperature accuracy is $\pm 7^{\circ}\text{C}$ typical over the -40°C to $+85^{\circ}\text{C}$ range with one point temperature calibration against a known temperature. A typical plot of the die temperature code readback vs. die temperature is shown in Figure 31.

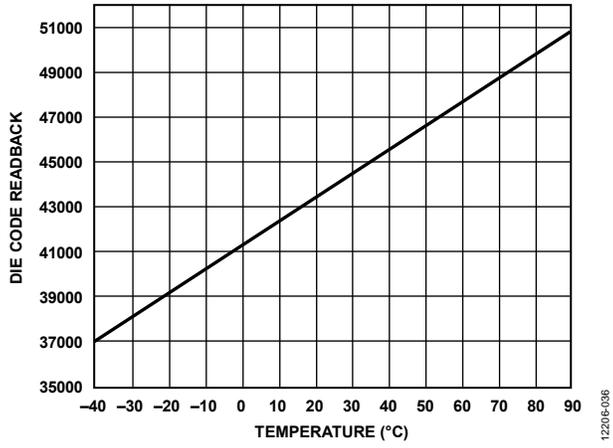


Figure 31. Die Temperature Code Readback vs. Die Temperature

Estimates of the ambient temperature can be made if the power dissipation of the device is known.

START-UP REGISTER SEQUENCES

POWER-UP ROUTINE WHEN USING THE ON-CHIP CLOCK SYNTHESIZER

To power up the device, set the register settings as described in the following sections.

Chip Power-Up

```
SPI.Write(0x008, 0x00); power up all blocks
```

DAC Setup

```
SPI.Write(0x03A, 0x02); DAC data format offset binary
```

or

```
SPI.Write(0x03A, 0x00); DAC data format twos complement
```

ADC Setup

```
SPI.Write(0x013, 0x00); enable ADC LVDS output and offset binary
```

or

```
SPI.Write(0x013, 0x01); enable ADC LVDS output and twos complement
```

```
SPI.Write(0x014, 0x01); set LVDS to 2 mA (optional: 1 mA is default)
```

```
SPI.Write(0x0FF, 0x01); transfer
```

Synthesizer Setup (62.5 MHz Reference Clock Input)

```
SPI.Write(0x032, 0x01); SYNTH_CP_CAL_EN
```

```
SPI.Write(0x0FF, 0x01); transfer
```

```
SPI.Write(0x032, 0x11); start synthesizer calibration
```

```
SPI.Write(0x0FF, 0x01); transfer
```

```
SPI.Read(0x02D); synthesizer status
```

```
0x01; calibration in progress
```

```
0x04; calibration done, synthesizer no lock
```

```
0x06; calibration done, synthesizer locked
```

Synthesizer Setup (31.25 MHz Reference Clock Input)

```
SPI.Write(0x033, 0x20); CLKGEN_REFCLK_DIV1
```

```
SPI.Write(0x032, 0x01); synthesizer CP_CAL_EN
```

```
SPI.Write(0x0FF, 0x01); transfer
```

```
SPI.Write(0x032, 0x11); start synth calibration
```

```
SPI.Write(0x0FF, 0x01); transfer
```

```
SPI.Read(0x02D); synthesizer status
```

```
0x01; calibration in progress
```

```
0x04; calibration done, synthesizer no lock
```

```
0x06; calibration done, synthesizer locked
```

Synchronize LVDS Interface

```
SPI.Write(0x00A, 0x82); synchronize ADC data with DCO clock, self cleared but needs following SPI clock
```

```
SPI.Write(0x00A, 0x81); realign Tx FIFO read and write pointers, self cleared but need following SPI clock
```

```
SPI.Write(0x00A, 0x90); realign Rx FIFO read and write pointers, DCI clock must be present, self cleared but need following SPI clock
```

Miscellaneous

Clear Interrupt

```
SPI.Write(0x0F0, 0xFF)
```

Enable Interrupt

```
SPI.Write(0x0F1, 0xFF)
```

```
SPI.Write(0x055, 0x01); ALERT_PULLUP_EN (optional)
```

```
SPI.Write(0x0FF, 0x01); transfer
```

```
SPI.Write(0x039, 0x12); set DAC CML based on compliance range of 0.7 V and on-chip RFSADJ_x resistors
```

Set this bit if using DAC compliance range > 0.7 V.

```
SPI.Write(0x0ff, 0x001); data transfer
```

POWER-UP ROUTINE WHEN USING EXTERNAL CLOCK

Chip Power-Up

```
SPI.Write(0x008, 0x00); power up all blocks
```

DAC Setup

```
SPI.Write(0x03A, 0x02); DAC data format offset binary
```

or

```
SPI.Write(0x03A, 0x00); DAC data format twos complement
```

ADC Setup

```
SPI.Write(0x013, 0x00); enable ADC LVDS output and offset binary
```

or

```
SPI.Write(0x013, 0x01); enable ADC LVDS output and twos complement
```

```
SPI.Write(0x014, 0x01); set LVDS to 2 mA (optional: 1 mA is default)
```

```
SPI.Write(0x0FF, 0x01); transfer
```

External Clock Setup

```
SPI.Write(0x034, 0x07); set external clock mode
```

```
SPI.Write(0x0FF, 0x01); transfer
```

Synchronize LVDS Interface

SPI.Write(0x00A, 0x82); synchronize ADC data with DCO clock, self cleared but needs following SPI clock

SPI.Write(0x00A, 0x81); realign Tx FIFO read and write pointers, self cleared but need following SPI clock

SPI.Write(0x00A, 0x90); realign Rx FIFO read and write pointers, DCI clock must be present, self cleared but need following SPI clock.

Miscellaneous**Clear Interrupt**

SPI.Write(0x0F0, 0xFF)

Enable Interrupt

SPI.Write(0x0F1, 0xFF)

SPI.Write(0x055, 0x01); ALERT_PULLUP_EN (optional)

SPI.Write(0x0FF, 0x01); transfer

SPI.Write(0x039, 0x12); set DAC CML based on compliance range of 0.7 V and on-chip R_{FSADJ_X} resistors,

Set this bit if using DAC compliance range > 0.7 V

SPI.Write(0x0FF, 0x001); data transfer

APPLICATIONS INFORMATION

DIRECT CONVERSION RADIO APPLICATION

A direct conversion radio application of the MxFE is shown in Figure 32. The DAC output signals, IOUTA_P/IOUTA_N and IOUTB_P/IOUTB_N, are differential currents. At 500 MSPS, DAC output signals fall within the 1st Nyquist zone (dc to 250 MHz). DAC current outputs are converted to a voltage and then processed by passive low-pass filters (LPF). The low-pass filters reject out of band signal harmonics and their sampling images. The filter outputs feed the baseband inputs of a quadrature modulator. Quadrature modulator baseband inputs

must fall within an allowable voltage range, which gives rise to a common-mode voltage requirement at the outputs of the DACs.

The MxFE receive signal chain consists of a VGA followed by a quadrature demodulator, then by a programmable LPF, and another VGA. The ADRF6518 is an LPF and VGA specifically designed to drive the analog inputs of high speed ADCs like the ones on the MxFE. The LPF is an antialiasing filter. At 250 MSPS, the ADC signal bandwidth is 125 MHz.

See the ADRF6518 as ADC Driver section for further information about this interface.

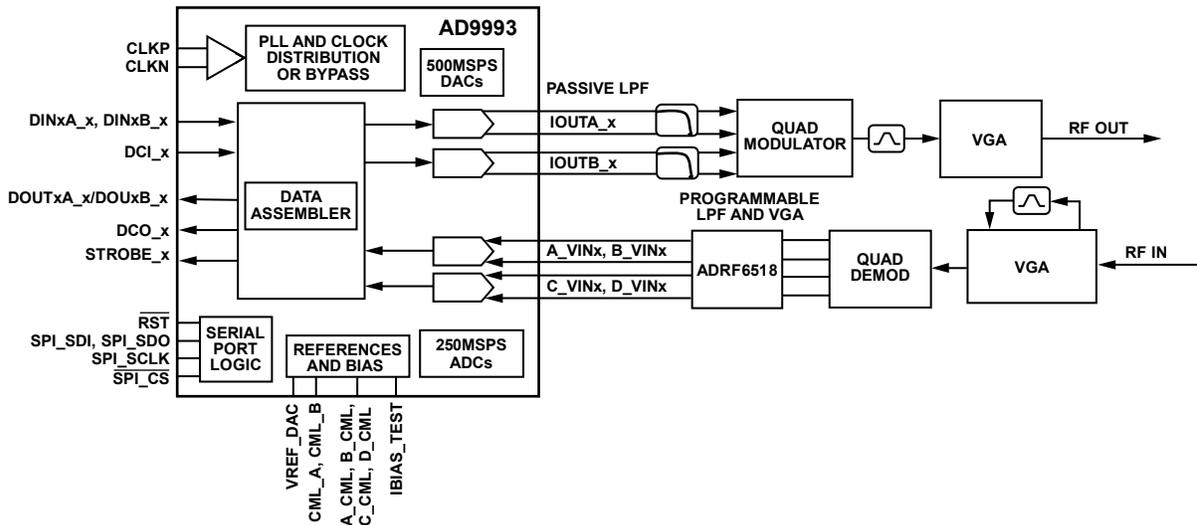


Figure 32. Radio Signal Chain Example

12206-037

REGISTER MAP

Table 10. SPI Accessible Register Summary

Address	Name	Description	Reset Value	RW
0x000	SPI_CONFIG	SPI configuration	0x18	RW
0x001	CHIP_ID	Chip ID	0xB2	R
0x002	CHIP_GRADE	CHIP_GRADE	0x01	R
0x005	DEVICE_INDEX	Device index	0x0F	RW
0x008	POWER_MODES	Power mode control (indexed)	0x55	RW
0x00A	ALIGN	Align ADC LVDS clocks, ADC FIFO, DAC FIFO	0x80	RW
0x00C	Reserved	Reserved	0x01	R
0x010	Reserved	Reserved	0x00	R
0x011	Reserved	Reserved	0x00	R
0x012	STROBE_CTRL	Strobe lane control (transfer)	0x00	RW
0x013	FLEX_OUTPUT_MODE	Output mode (transfer, indexed)	0x11	RW
0x014	FLEX_OUTPUT_ADJUST	LVDS Tx control (transfer)	0x00	RW
0x016	FLEX_VREF	V _{REF} control (transfer)	0x00	RW
0x017	PRBS_GEN_CTRL	PRBS generator control (transfer, indexed)	0x00	RW
0x020	PRBS0_SEED_MSB	8-bit seed MSB of PRBS generator for Lane0 (transfer, indexed)	0x01	RW
0x021	PRBS1_SEED_MSB	8-bit seed MSB of PRBS generator for Lane1 (transfer, indexed)	0x02	RW
0x022	PRBS2_SEED_MSB	8-bit seed MSB of PRBS generator for Lane2 (transfer, indexed)	0x03	RW
0x023	PRBS3_SEED_MSB	8-bit seed MSB of PRBS generator for Lane3 (transfer, indexed)	0x04	RW
0x02D	SYNTH_STAT	Synthesizer status	0x00	R
0x02E	LF_CTRL1	Loop filter control signals (transfer)	0x77	RW
0x02F	LF_CTRL2	Loop filter control signals (transfer)	0xF7	RW
0x030	LF_CTRL3	Loop filter control signals (transfer)	0x00	RW
0x031	SYNTH_INT	Integer value of synthesize divider (transfer)	0x40	RW
0x032	SYNTH_CTRL	Synthesizer control (transfer)	0x00	RW
0x033	CLKGEN_CTRL1	Clock generator control (transfer)	0x00	RW
0x034	CLKGEN_CTRL2	CLKGEN control (transfer)	0x04	RW
0x035	DAC_LVDS_CTRL	DAC LVDS Rx control (transfer)	0x4D	RW
0x036	DAC_LVDS_BIAS	DAC LVDS current bias control (transfer)	0x00	RW
0x037	Reserved	Reserved	0x00	RW
0x038	Reserved	Reserved	0x00	RW
0x039	DAC_CTRL	DAC cores control (transfer)	0x02	RW
0x03A	DAC_DP_FMT	DAC datapath format control (transfer)	0x00	RW
0x03C	DAC_CAL_IQ_CTRL	DAC IQ calibration control (transfer)	0x04	RW
0x03D	DAC_CAL_IQ_STAT	DAC IQ calibration status	0x00	R
0x03F	DAC_FIFO_STS1	DAC Rx FIFO Status 1	0x55	R
0x040	DAC_PRBS_CTRL	PRBS detector control (transfer)	0x00	RW
0x041	DAC_A_PRBS_ERR0	PRBS Detector Error Count 0 for DAC A	0x00	R
0x042	DAC_A_PRBS_ERR1	PRBS Detector Error Count 1 for DAC A	0x00	R
0x043	DAC_A_PRBS_ERR2	PRBS Detector Error Count 2 for DAC A	0x00	R
0x044	DAC_A_PRBS_ERR3	PRBS Detector Error Count 3 for DAC A	0x00	R
0x045	DAC_A_PRBS_ERR4	PRBS Detector Error Count 4 for DAC A	0x00	R
0x046	DAC_A_PRBS_ERR5	PRBS Detector Error Count 5 for DAC A	0x00	R
0x047	DAC_A_PRBS_ERR6	PRBS Detector Error Count 6 for DAC A	0x00	R
0x048	DAC_B_PRBS_ERR0	PRBS Detector Error Count 0 for DAC B	0x00	R
0x049	DAC_B_PRBS_ERR1	PRBS Detector Error Count 1 for DAC B	0x00	R
0x04A	DAC_B_PRBS_ERR2	PRBS Detector Error Count 2 for DAC B	0x00	R
0x04B	DAC_B_PRBS_ERR3	PRBS Detector Error Count 3 for DAC B	0x00	R
0x04C	DAC_B_PRBS_ERR4	PRBS Detector Error Count 4 for DAC B	0x00	R
0x04D	DAC_B_PRBS_ERR5	PRBS Detector Error Count 5 for DAC B	0x00	R
0x04E	DAC_B_PRBS_ERR6	PRBS Detector Error Count 6 for DAC B	0x00	R

Address	Name	Description	Reset Value	RW
0x050	TS_RD_LSB	Bits[7:0] of Temperature sensor data readback	0x00	R
0x051	TS_RD_MSB	Bits[15:8] of Temperature sensor data readback	0x00	R
0x052	Reserved	Reserved	0x00	R
0x053	Reserved	Reserved	0x00	R
0x054	TS_CTRL	Temperature sensor control signals	0x01	RW
0x055	IRQ_CTRL	Interrupt pin control	0x00	RW
0x060	DDS_CTRL	DDS control	0x00	RW
0x061	DDS_TW1_0	DDS tuning word for Tone 1	0x00	RW
0x062	DDS_TW1_1	DDS tuning word for Tone 1	0x00	RW
0x063	DDS_TW1_2	DDS tuning word for Tone 1	0xA0	RW
0x064	DDS_TW1_3	DDS tuning word for Tone 1	0x19	RW
0x0F0	INT	Interrupt status	0x00	R
0x0F1	INTEN	Interrupt enable (transfer)	0x00	RW
0x0F2	INT_RAW	Interrupt source status	0x00	R
0x0FF	DEVICE_UPDATE	Global device update register	0x00	RW

REGISTER DESCRIPTIONS

SPI CONFIGURATION REGISTER

Address: 0x000, Reset: 0x18, Name: SPI_CONFIG

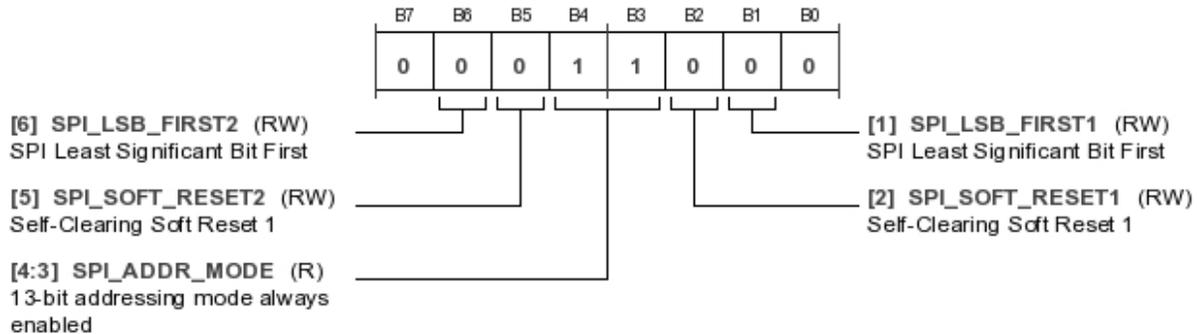


Table 11. Bit Descriptions for SPI_CONFIG

Bits	Bit Name	Description	Reset	Access
6	SPI_LSB_FIRST2	SPI least significant bit first. 1 = least significant bit shifted first for all SPI operations. On multibyte SPI operations, addressing increments automatically. 0 = most significant bit shifted first for all SPI operations. On multibyte SPI operations, addressing decrements automatically. This bit must be accessed with all devices enabled and is not reset by setting the SPI_SOFT_RESET1 or SPI_SOFT_RESET2 bit.	0x0	RW
5	SPI_SOFT_RESET2	Self Clearing Soft Reset 1. Reset the SPI registers (self clearing). This bit must be accessed with all devices enabled.	0x0	RW
[4:3]	SPI_ADDR_MODE	13-bit addressing mode always enabled.	0x3	R
2	SPI_SOFT_RESET1	Self Clearing Soft Reset 1. Reset the SPI registers (self clearing). This bit must be accessed with all devices enabled.	0x0	RW
1	SPI_LSB_FIRST1	SPI least significant bit first. 1 = least significant bit shifted first for all SPI operations. On multibyte SPI operations, addressing increments automatically. 0 = most significant bit shifted first for all SPI operations. On multibyte SPI operations, addressing decrements automatically. This bit must be accessed with all devices enabled and is not reset by setting the SPI_SOFT_RESET1 or SPI_SOFT_RESET2 bit.	0x0	RW

CHIP ID REGISTER

Address: 0x001, Reset: 0xB2, Name: CHIP_ID

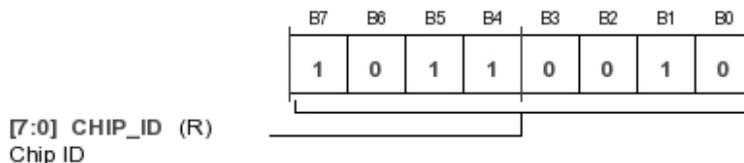


Table 12. Bit Descriptions for CHIP_ID

Bits	Bit Name	Description	Reset	Access
[7:0]	CHIP_ID	Chip ID.	0xB2	R

CHIP GRADE REGISTER

Address: 0x002, Reset: 0x01, Name: CHIP_GRADE

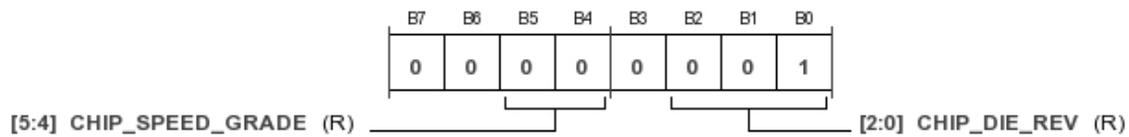


Table 13. Bit Descriptions for CHIP_GRADE

Bits	Bit Name	Description	Reset	Access
[5:4]	CHIP_SPEED_GRADE	Chip ID/speed grade.	0x0	R
[2:0]	CHIP_DIE_REV	Chip die revision.	0x1	R

DEVICE INDEX REGISTER

Address: 0x005, Reset: 0x0F, Name: DEVICE_INDEX

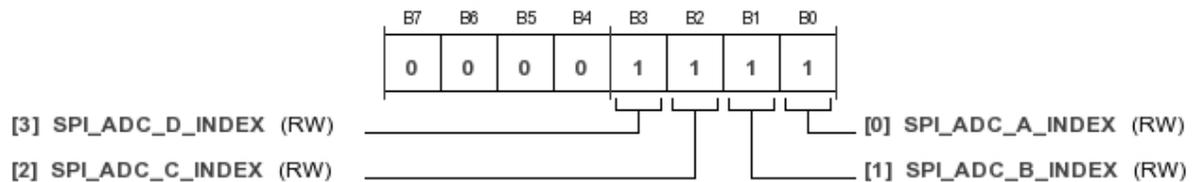


Table 14. Bit Descriptions for DEVICE_INDEX

Bits	Bit Name	Description	Reset	Access
3	SPI_ADC_D_INDEX	ADC Core D access enable. 1 = ADC Core D receives the next read/write access from the SPI interface. 0 = ADC Core D does not receive the next read/write access from the SPI interface.	0x1	RW
2	SPI_ADC_C_INDEX	ADC Core C access enable. 1 = ADC Core C receives the next read/write access from the SPI interface. 0 = ADC Core C does not receive the next read/write access from the SPI interface.	0x1	RW
1	SPI_ADC_B_INDEX	ADC Core B access enable. 1 = ADC Core B receives the next read/write access from the SPI interface. 0 = ADC Core B does not receive the next read/write access from the SPI interface.	0x1	RW
0	SPI_ADC_A_INDEX	ADC Core A access enable. 1 = ADC Core A receives the next read/write access from the SPI interface. 0 = ADC Core A does not receive the next read/write access from the SPI interface.	0x1	RW

POWER MODE CONTROL REGISTER

Address: 0x008, Reset: 0x55, Name: POWER_MODES

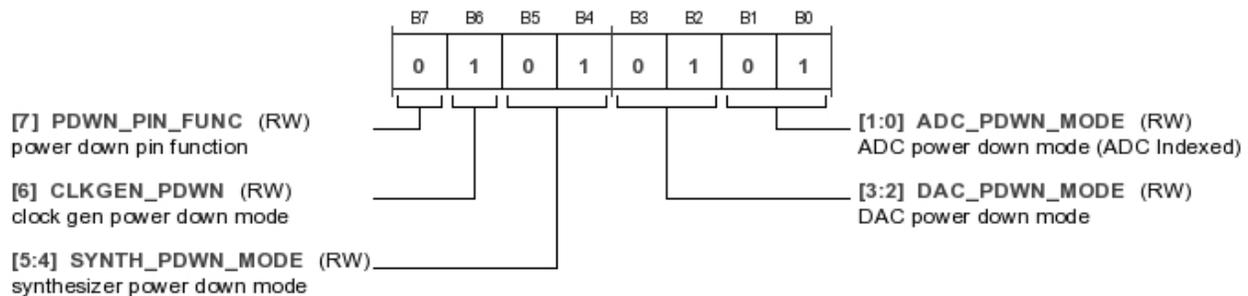


Table 15. Bit Descriptions for POWER_MODES

Bits	Bit Name	Description	Reset	Access
7	PDWN_PIN_FUNC	Power-down pin function. External power-down pin mode. 0 = assertion of external power-down pin (PDWN) causes chip to enter full power-down mode. 1 = assertion of external power-down pin (PDWN) causes chip to enter standby mode.	0x0	RW
6	CLKGEN_PDWN	Clock generation power-down mode.	0x1	RW
[5:4]	SYNTH_PDWN_MODE	Synthesizer power-down mode.	0x1	RW
[3:2]	DAC_PDWN_MODE	DAC power-down mode.	0x1	RW
[1:0]	ADC_PDWN_MODE	ADC power-down mode. (ADC indexed) 00 = normal mode (power up). 01 = power-down mode; digital datapath clocks disabled; digital datapath held in reset; outputs disabled. 10 = standby mode; digital datapath clocks disabled; outputs disabled. 11 = reserved.	0x1	RW

ALIGN ADC LVDS CLOCKS, ADC FIFO, DAC FIFO REGISTER

Address: 0x00A, Reset: 0x80, Name: ALIGN

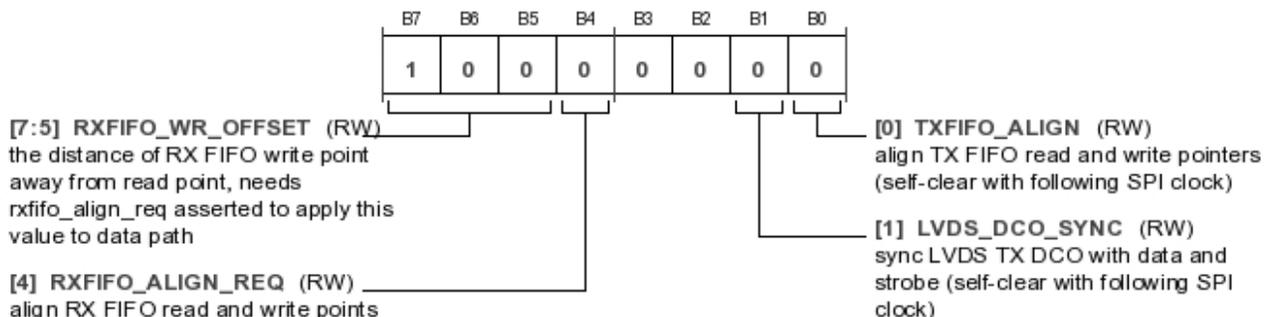


Table 16. Bit Descriptions for ALIGN

Bits	Bit Name	Description	Reset	Access
[7:5]	RXFIFO_WR_OFFSET	The distance of Rx FIFO write pointer away from read pointer; needs RXFIFO_ALIGN_REQ asserted to apply this value to datapath.	0x4	RW
4	RXFIFO_ALIGN_REQ	Align Rx FIFO read and write pointers.	0x0	RW
1	LVDS_DCO_SYNC	Sync LVDS Tx DCO with data and strobe (self clear with following SPI clock).	0x0	RW
0	TXFIFO_ALIGN	Align Tx FIFO read and write pointers (self clear with following SPI clock).	0x0	RW

STROBE LANE CONTROL REGISTER

Address: 0x012, Reset: 0x00, Name: STROBE_CTRL

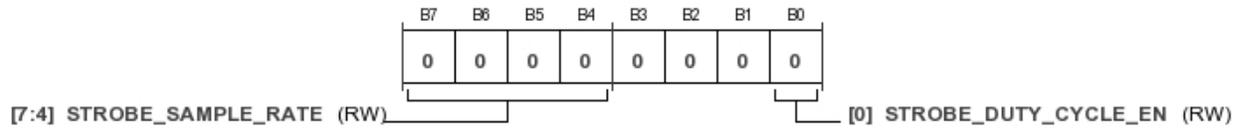


Table 17. Bit Descriptions for STROBE_CTRL

Bits	Bit Name	Description	Reset	Access
[7:4]	STROBE_SAMPLE_RATE	Sample rate of strobe output. 0 = 1/1 of data sample rate. 1 = 1/2 of data sample rate. 2 = 1/4 of data sample rate. 3 = 1/8 of data sample rate. 4 = 1/16 of data sample rate. 5 = 1/32 of data sample rate. 6 = 1/64 of data sample rate. 7 = 1/128 of data sample rate. 8 = 1/256 of data sample rate. Needs at least one ADC channel working.	0x0	RW
0	STROBE_DUTY_CYCLE_EN	Enable 50% duty cycle of strobe lane. Needs at least one ADC channel working.	0x0	RW

OUTPUT MODE REGISTER

Address: 0x013, Reset: 0x11, Name: FLEX_OUTPUT_MODE

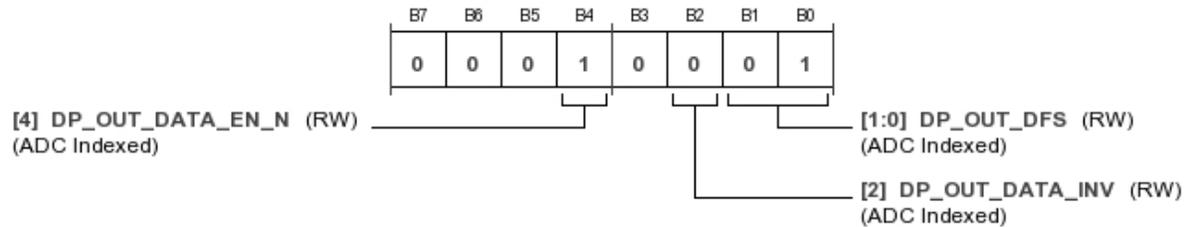


Table 18. Bit Descriptions for FLEX_OUTPUT_MODE

Bits	Bit Name	Description	Reset	Access
4	DP_OUT_DATA_EN_N	Digital datapath output enable (active low) (ADC indexed). 0 = digital output from ADC is enabled. 1 = digital output from ADC is disabled.	0x1	RW
2	DP_OUT_DATA_INV	Digital datapath output invert (ADC indexed). 0 = output from ADC is not inverted. 1 = output from ADC is inverted.	0x0	RW
[1:0]	DP_OUT_DFS	Digital datapath output data format select (DFS) (ADC indexed). 00 = offset binary. 01 = twos complement. 10 = gray code. 11 = reserved.	0x1	RW

LVDS TX CONTROL REGISTER

Address: 0x014, Reset: 0x00, Name: FLEX_OUTPUT_ADJUST

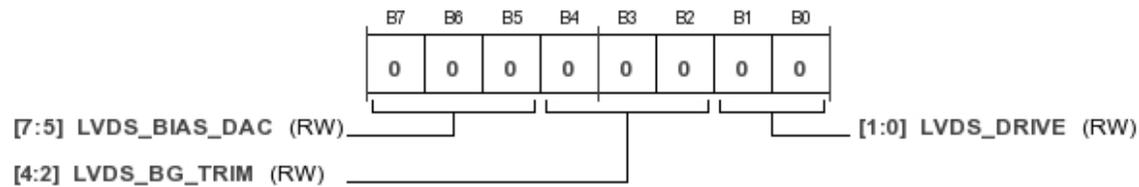


Table 19. Bit Descriptions for FLEX_OUTPUT_ADJUST

Bits	Bit Name	Description	Reset	Access
[7:5]	LVDS_BIAS_DAC	Sets LVDS output swing. 000 = 200 mV. 001 = 227 mV. 010 = 257 mV. 011 = 282 mV. 100 = 296 mV. 101 = 330 mV. 110 = 350 mV. 111 = 372 mV.	0x0	RW
[4:2]	LVDS_BG_TRIM	Band gap trim for LVDS Tx DOUTxx_P and DOUTxx_N pins.	0x0	RW
[1:0]	LVDS_DRIVE	Output LVDS drive current. 00 = 1 mA output drive current (default). 01 = 2 mA output drive current. 10 = 3 mA output drive current. 11 = 4 mA output drive current.	0x0	RW

V_{REF} CONTROL REGISTER

Address: 0x016, Reset: 0x00, Name: FLEX_VREF

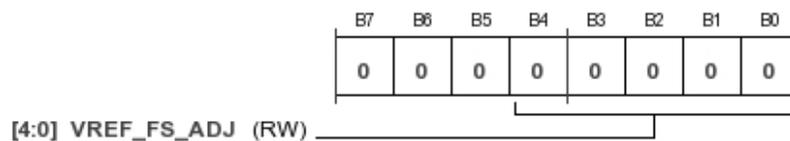


Table 20. Bit Descriptions for FLEX_VREF

Bits	Bit Name	Description	Reset	Access
[4:0]	VREF_FS_ADJ	Main reference full-scale V _{REF} adjustment. 01111 = internal 2.087 V p-p. ... 00001 = internal 1.772 V p-p. 00000 = internal 1.75 V p-p. 11111 = internal 1.727 V p-p. ... 10000 = internal 1.383 V p-p.	0x0	RW

PRBS GENERATOR CONTROL REGISTER

Address: 0x017, Reset: 0x00, Name: PRBS_GEN_CTRL

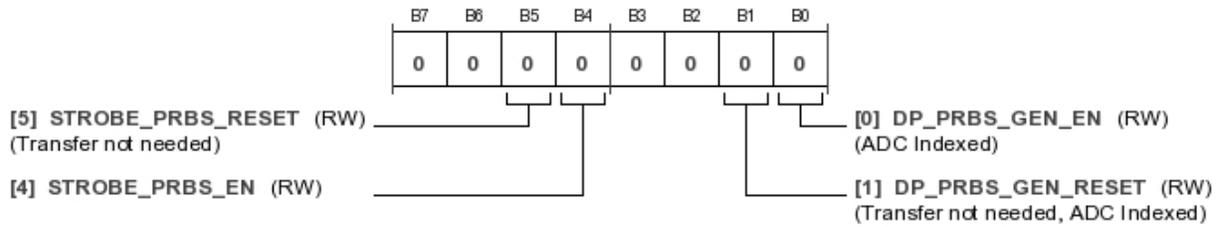


Table 21. Bit Descriptions for PRBS_GEN_CTRL

Bits	Bit Name	Description	Reset	Access
5	STROBE_PRBS_RESET	Reset PRBS generator on strobe lane (transfer not needed). 0 = normal working if PRBS enabled. 1 = reset the PRBS on strobe lane.	0x0	RW
4	STROBE_PRBS_EN	Enable PRBS testing on strobe lane. 0 = normal mode working with STROBE_DUTY_CYCLE_EN and STROBE_SAMPLE_RATE. 1 = test mode only. Note: needs at least one ADC channel working.	0x0	RW
1	DP_PRBS_GEN_RESET	Pseudorandom binary sequence generator reset (transfer not needed, ADC indexed). 0 = PRBS generator enabled. 1 = PRBS generator held in reset.	0x0	RW
0	DP_PRBS_GEN_EN	Enable PRBS generating on ADC data lanes (ADC indexed).	0x0	RW

8-BIT SEED MSB OF PRBS GENERATOR FOR LANE 0 REGISTER

Address: 0x020, Reset: 0x01, Name: PRBS0_SEED_MSB

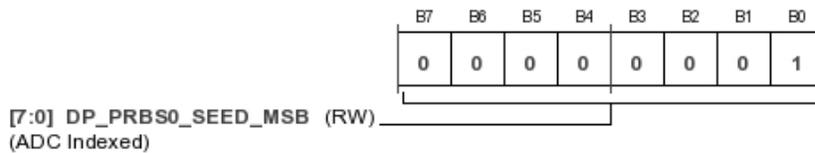


Table 22. Bit Descriptions for PRBS0_SEED_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	DP_PRBS0_SEED_MSB	8-bit MSB seed of PRBS generator in Lane 0 (ADC indexed). The 15-bit LSB is always 0x3AFF.	0x1	RW

8-BIT SEED MSB OF PRBS GENERATOR FOR LANE 1 REGISTER

Address: 0x021, Reset: 0x02, Name: PRBS1_SEED_MSB

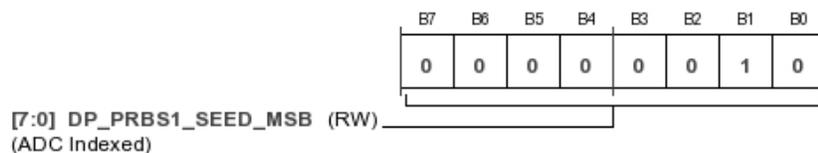


Table 23. Bit Descriptions for PRBS1_SEED_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	DP_PRBS1_SEED_MSB	8-bit MSB seed of PRBS generator in Lane 1 (ADC indexed). The 15-bit LSB is always 0x3AFF.	0x2	RW

8-BIT SEED MSB OF PRBS GENERATOR FOR LANE 2 REGISTER

Address: 0x022, Reset: 0x03, Name: PRBS2_SEED_MSB

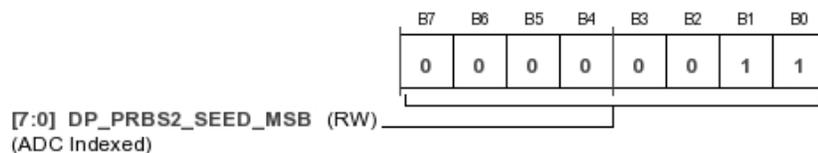


Table 24. Bit Descriptions for PRBS2_SEED_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	DP_PRBS2_SEED_MSB	8-bit MSB seed of PRBS generator in Lane 2 (ADC indexed). The 15-bit LSB is always 0x3AFF.	0x3	RW

8-BIT SEED MSB OF PRBS GENERATOR FOR LANE 3 REGISTER

Address: 0x023, Reset: 0x04, Name: PRBS3_SEED_MSB

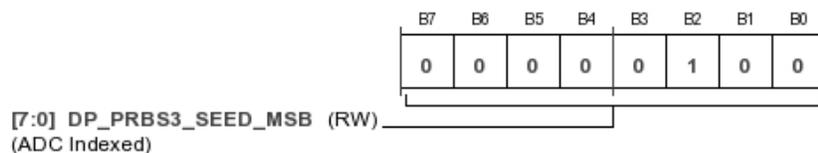


Table 25. Bit Descriptions for PRBS3_SEED_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	DP_PRBS3_SEED_MSB	8-bit MSB seed of PRBS generator in Lane 3 (ADC indexed). The 15-bit LSB is always 0x3AFF.	0x4	RW

SYNTHESIZER STATUS REGISTER

Address: 0x02D, Reset: 0x00, Name: SYNTH_STAT

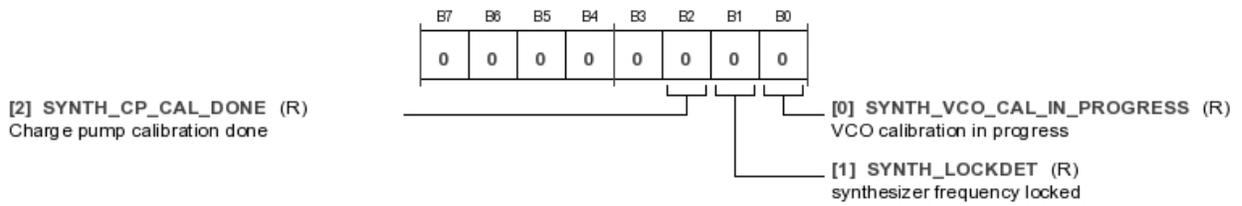


Table 26. Bit Descriptions for SYNTH_STAT

Bits	Bit Name	Description	Reset	Access
2	SYNTH_CP_CAL_DONE	Charge pump calibration done.	0x0	R
1	SYNTH_LOCKDET	Synthesizer frequency locked.	0x0	R
0	SYNTH_VCO_CAL_IN_PROGRESS	VCO calibration in progress.	0x0	R

LOOP FILTER CONTROL SIGNALS REGISTER

Address: 0x02E, Reset: 0x77, Name: LF_CTRL1

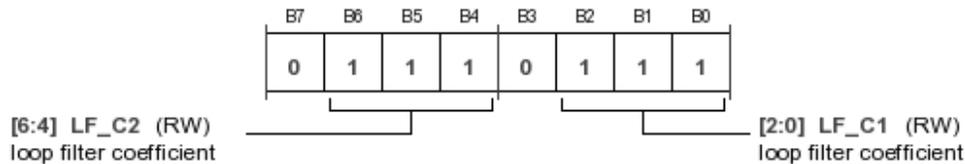


Table 27. Bit Descriptions for LF_CTRL1

Bits	Bit Name	Description	Reset	Access
[6:4]	LF_C2	Loop filter coefficient. 000 = 3.13 pF. 001 = 2.26 pF. 010 = 9.39 pF. 011 = 12.52 pF. 100 = 15.65 pF. 101 = 18.78 pF. 110 = 21.91 pF. 111 = 25.04 pF.	0x7	RW
[2:0]	LF_C1	Loop filter coefficient. 000 = 46.584 pF. 001 = 93.168 pF. 010 = 139.752 pF. 011 = 186.336 pF. 100 = 232.920 pF. 101 = 279.504 pF. 110 = 326.088 pF. 111 = 372.672 pF.	0x7	RW

LOOP FILTER CONTROL SIGNALS REGISTER

Address: 0x02F, Reset: 0xF7, Name: LF_CTRL2

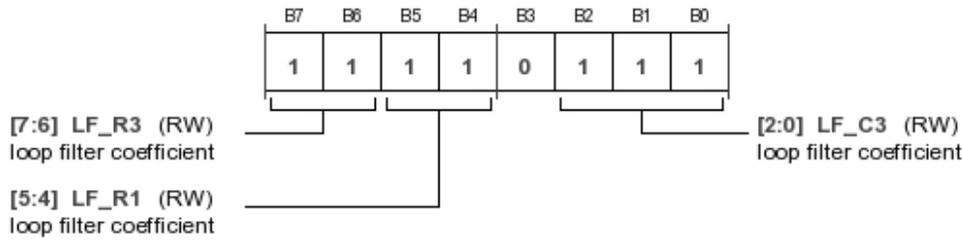


Table 28. Bit Descriptions for LF_CTRL2

Bits	Bit Name	Description	Reset	Access
[7:6]	LF_R3	Loop filter coefficient. 00 = 4.63 kΩ. 01 = 2.315 kΩ. 10 = 1.543 kΩ. 11 = 1.157 kΩ	0x3	RW
[5:4]	LF_R1	Loop filter coefficient. 00 = 12.04 kΩ. 01 = 6.02 kΩ. 10 = 4.01 kΩ. 11 = 3.01 kΩ.	0x3	RW
[2:0]	LF_C3	Loop filter coefficient. 000 = 0.6325 pF. 001 = 1.265 pF. 010 = 1.8975 pF. 011 = 2.530 pF. 100 = 3.1625 pF. 101 = 3.795 pF. 110 = 4.4275 pF. 111 = 5.06 pF.	0x7	RW

LOOP FILTER CONTROL SIGNALS REGISTER

Address: 0x030, Reset: 0x00, Name: LF_CTRL3

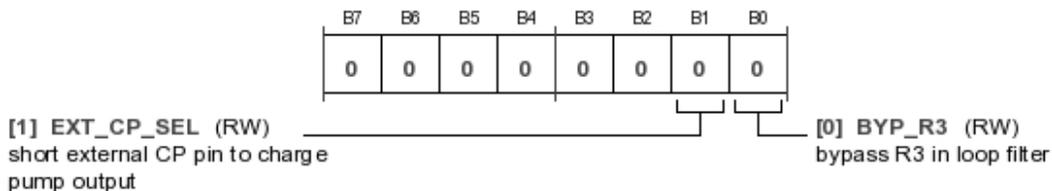


Table 29. Bit Descriptions for LF_CTRL3

Bits	Bit Name	Description	Reset	Access
1	EXT_CP_SEL	Short external CP pin to charge pump output.	0x0	RW
0	BYP_R3	Bypass R3 in loop filter.	0x0	RW

INTEGER VALUE OF SYNTHESIZER DIVIDER REGISTER

Address: 0x031, Reset: 0x40, Name: SYNTH_INT

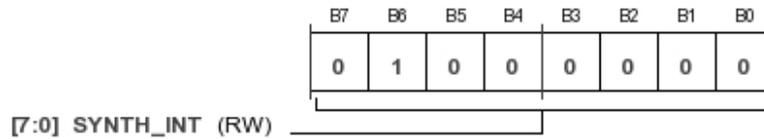


Table 30. Bit Descriptions for SYNTH_INT

Bits	Bit Name	Description	Reset	Access
[7:0]	SYNTH_INT	Integer part on the synthesizer divider (N). $N = freq (MHz)/31.25$.	0x40	RW

SYNTHESIZER CONTROL REGISTER

Address: 0x032, Reset: 0x00, Name: SYNTH_CTRL

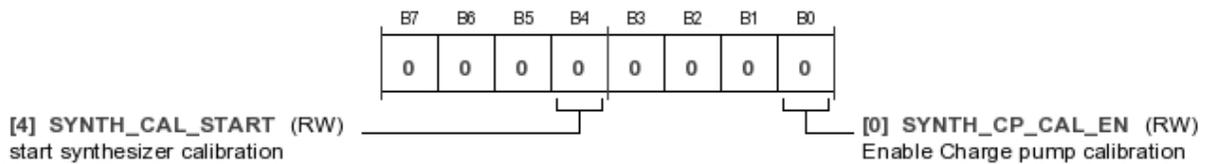


Table 31. Bit Descriptions for SYNTH_CTRL

Bits	Bit Name	Description	Reset	Access
4	SYNTH_CAL_START	Start synthesizer calibration.	0x0	RW
0	SYNTH_CP_CAL_EN	Enable charge pump calibration.	0x0	RW

CLOCK GENERATOR CONTROL REGISTER

Address: 0x033, Reset: 0x00, Name: CLKGEN_CTRL1

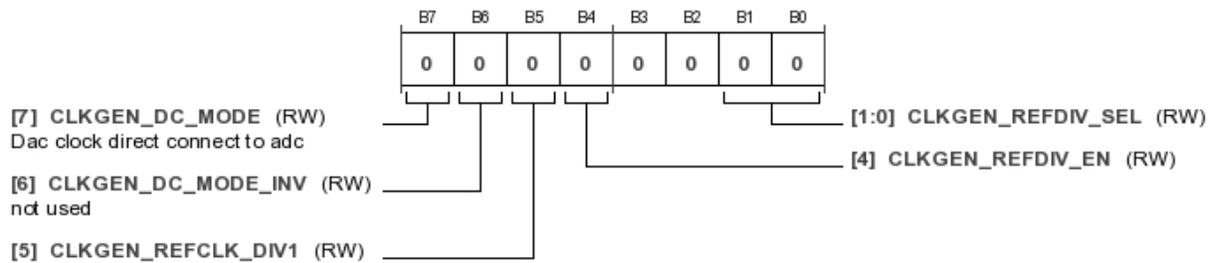


Table 32. Bit Descriptions for CLKGEN_CTRL1

Bits	Bit Name	Description	Reset	Access
7	CLKGEN_DC_MODE	DAC clock direct connect to ADC. 0 = ADC clock from 1 GHz. 1 = ADC clock from DAC.	0x0	RW
6	CLKGEN_DC_MODE_INV	Not used.	0x0	RW
5	CLKGEN_REFCLK_DIV1	0 = select REFCLK as PLL reference. 1 = select REFCLK/2 as PLL reference.	0x0	RW
4	CLKGEN_REFDIV_EN	Selects the output of the on-chip reference clock divider to the PLL.	0x0	RW
[1:0]	CLKGEN_REFDIV_SEL	Sets the divider ratio for the on-chip reference clock divider.	0x0	RW

CLKGEN CONTROL REGISTER

Address: 0x034, Reset: 0x04, Name: CLKGEN_CTRL2

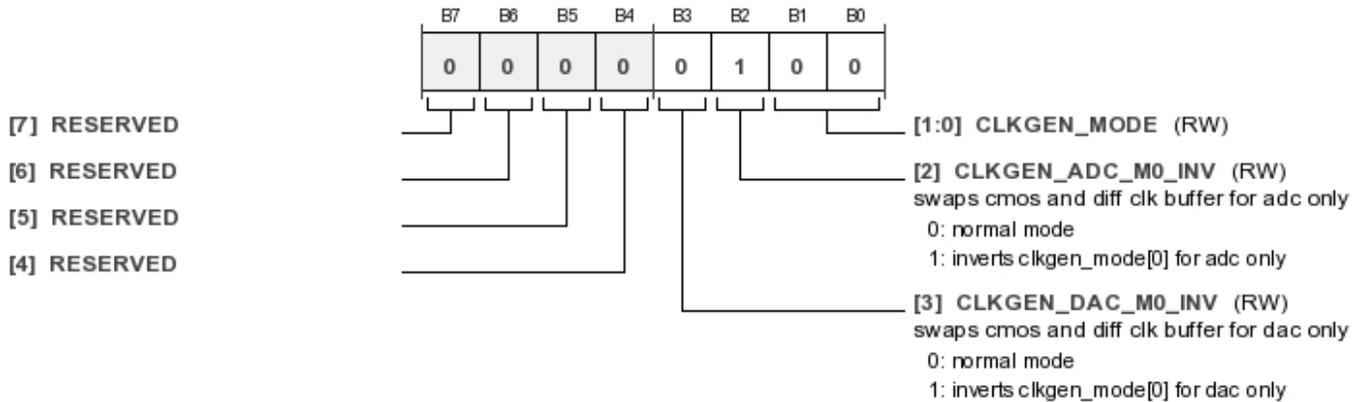


Table 33. Bit Descriptions for CLKGEN_CTRL2

Bits	Bit Name	Description	Reset	Access
3	CLKGEN_DAC_M0_INV	Swaps CMOS and differential clock buffer for DAC only. 0 = normal mode. 1 = inverts CLKGEN_MODE[0] for DAC only.	0x0	RW
2	CLKGEN_ADC_M0_INV	Swaps CMOS and differential clock buffer for ADC only. 0 = normal mode. 1 = inverts CLKGEN_MODE[0] for ADC only.	0x1	RW
[1:0]	CLKGEN_MODE	Configures the IC for external or internal clock. 00 = selects on-chip synthesizer to drive LVDS at 1 GHz, ADC at 250 MHz, and DAC at 500 MHz. 01 = same as 00 except uses differential clock buffer for DAC and ADC. 10 = selects external clock source to drive LVDS at clock rate, ADC at clock rate divide by 4, and DAC at clock rate divide by 2. Minimum clock rate = 200 MHz. 11 = same as 10 except uses differential clock buffer for DAC and ADC.	0x0	RW

DAC LVDS RX CONTROL REGISTER

Address: 0x035, Reset: 0x4D, Name: DAC_LVDS_CTRL

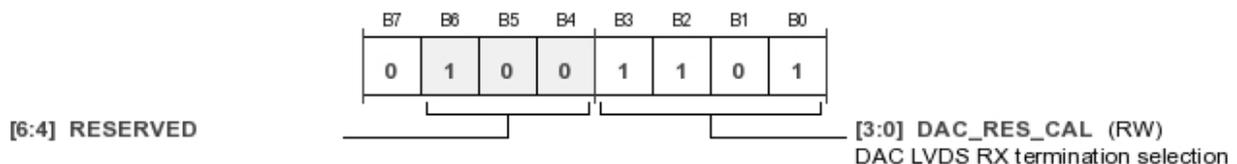


Table 34. Bit Descriptions for DAC_LVDS_CTRL

Bits	Bit Name	Description	Reset	Access
[3:0]	DAC_RES_CAL	DAC LVDS Rx termination selection. 0001 = 977 Ω. 0010 = 497 Ω. 0011 = 341 Ω. 0100 = 267 Ω. 0101 = 215 Ω. 0110 = 184 Ω. 0111 = 160 Ω. 1000 = 145Ω. 1001 = 131 Ω. 1010 = 121 Ω. 1011 = 112 . 1100 = 105 Ω. 1101 = 99 Ω. 1110 = 93Ω. 1111 = 89 Ω.	0xD	RW

DAC LVDS CURRENT BIAS CONTROL REGISTER

Address: 0x036, Reset: 0x00, Name: DAC_LVDS_BIAS

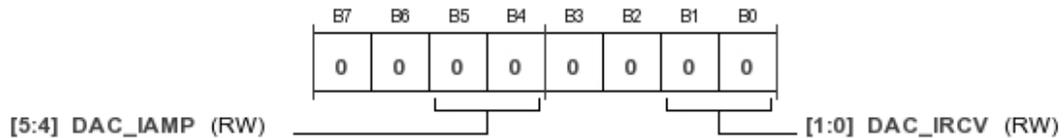


Table 35. Bit Descriptions for DAC_LVDS_BIAS

Bits	Bit Name	Description	Reset	Access
[5:4]	DAC_IAMP	Adjust bias current for LVDS DAC receiver. 00 = nominal. 01 = 25%. 10 = 50%. 11 = 75%.	0x0	RW
[1:0]	DAC_IRCV	Adjust the bias current to cascade voltage for LVDS DAC receiver. 00 = nominal. 01 = 25%. 10 = 50%. 11 = 75%.	0x0	RW

DAC CORES CONTROL REGISTER

Address: 0x039, Reset: 0x02, Name: DAC_CTRL

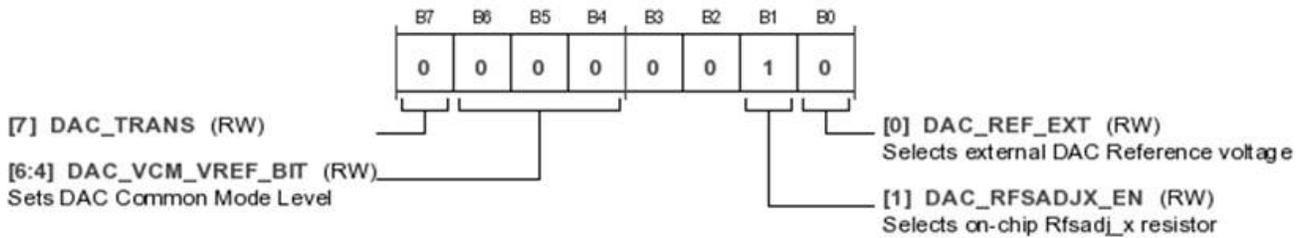


Table 36. Bit Descriptions for DAC_CTRL

Bits	Bit Name	Description	Reset	Access
7	DAC_TRANS	DAC input latch data transfer method select. 0 = edge triggered. 1 = level triggered.	0x0	RW
[6:4]	DAC_VCM_VREF_BIT	Sets DAC common-mode level. 000 = 0.0 V. 001 = 0.2 V. 010 = 0.3 V. 011 = 0.4 V 100 = 0.5 V 101 = 0.6 V 110 = 0.7 V. 111 = 0.8 V.	0x0	RW
1	DAC_RSET_EN	Selects on-chip R _{FSDJ_x} resistor.	0x1	RW
0	DAC_REF_EXT	Selects external DAC Reference voltage. Set to 1 to use an off-chip DAC reference.	0x0	RW

DAC DATAPATH FORMAT CONTROL REGISTER

Address: 0x03A, Reset: 0x00, Name: DAC_DP_FMT

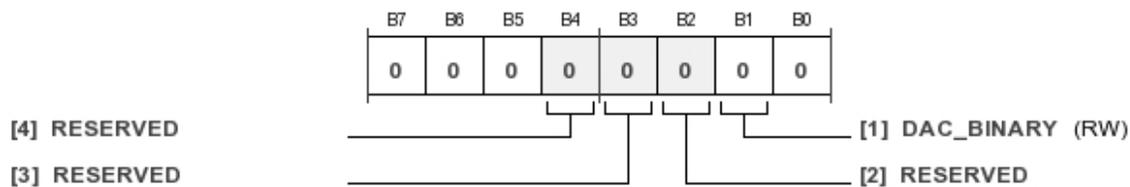


Table 37. Bit Descriptions for DAC_DP_FMT

Bits	Bit Name	Description	Reset	Access
1	DAC_BINARY	Enable binary offset data format (default is twos complement). 0 = twos complement. 1 = binary offset.	0x0	RW

DAC IQ CALIBRATION CONTROL REGISTER

Address: 0x03C, Reset: 0x04, Name: DAC_CAL_IQ_CTRL

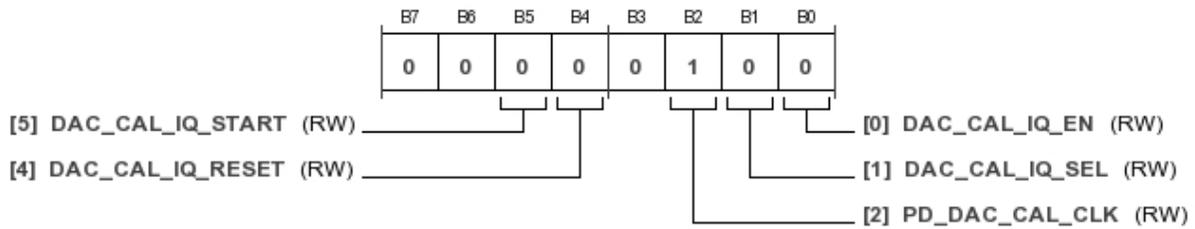


Table 38. Bit Descriptions for DAC_CAL_IQ_CTRL

Bits	Bit Name	Description	Reset	Access
5	DAC_CAL_IQ_START	Starts DAC IQ calibration.	0x0	RW
4	DAC_CAL_IQ_RESET	Resets DAC IQ calibration.	0x0	RW
2	PD_DAC_CAL_CLK	0 = DAC IQ calibration clock enabled. Must be 0 to run IQ calibration. 1 = DAC IQ calibration clock disabled.	0x1	RW
1	DAC_CAL_IQ_SEL	Selects output of IQ calibration. Must be 1 to run IQ calibration.	0x0	RW
0	DAC_CAL_IQ_EN	Enables DAC I to Q calibration. Must stay high until DAC_CAL_IQ_DONE = 1.	0x0	RW

DAC IQ CALIBRATION STATUS REGISTER

Address: 0x03D, Reset: 0x00, Name: DAC_CAL_IQ_STAT

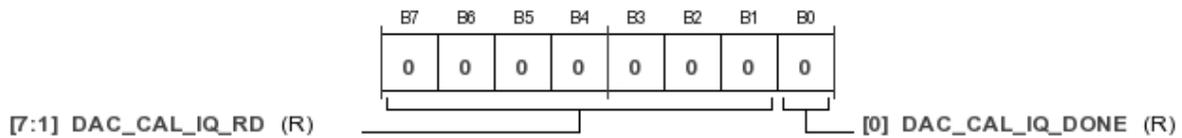


Table 39. Bit Descriptions for DAC_CAL_IQ_STAT

Bits	Bit Name	Description	Reset	Access
[7:1]	DAC_CAL_IQ_RD	Value of DAC IQ calibration, valid when DAC_CAL_IQ_DONE = 1.	0x0	R
0	DAC_CAL_IQ_DONE	Indicates when DAC IQ calibration is done.	0x0	R

DAC RX FIFO STATUS 1 REGISTER

Address: 0x03E, Reset: 0x55, Name: DAC_FIFO_STS1

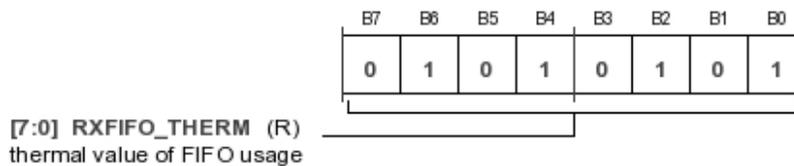
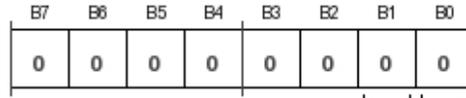


Table 40. Bit Descriptions for DAC_FIFO_STS1

Bits	Bit Name	Description	Reset	Access
[7:0]	RXFIFO_THERM	Thermal value of FIFO usage.	0x55	R

PRBS DETECTOR CONTROL REGISTER

Address: 0x040, Reset: 0x00, Name: DAC_PRBS_CTRL



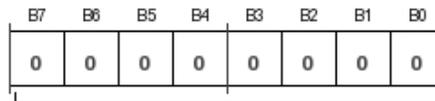
[1] PRBS_DET_ERRCLR (RW) clear the error count of PRBS Detector (Transfer not required)
 [0] PRBS_DET_EN (RW) enable the PRBS Detector

Table 41. Bit Descriptions for DAC_PRBS_CTRL

Bits	Bit Name	Description	Reset	Access
1	PRBS_DET_ERRCLR	Clear the error count of PRBS detector (transfer not required).	0x0	RW
0	PRBS_DET_EN	Enable the PRBS detector.	0x0	RW

PRBS DETECTOR ERROR COUNT 0 FOR DAC A REGISTER

Address: 0x041, Reset: 0x00, Name: DAC_A_PRBS_ERR0



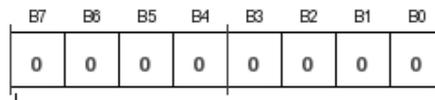
[7:0] PRBS_DET_ERRCNT_A0 (R) Error Count of Lane 0 of DAC A

Table 42. Bit Descriptions for DAC_A_PRBS_ERR0

Bits	Bit Name	Description	Reset	Access
[7:0]	PRBS_DET_ERRCNT_A0	Error count of Lane 0 of DAC A.	0x0	R

PRBS DETECTOR ERROR COUNT 1 FOR DAC A REGISTER

Address: 0x042, Reset: 0x00, Name: DAC_A_PRBS_ERR1



[7:0] PRBS_DET_ERRCNT_A1 (R) Error Count of Lane 1 of DAC A

Table 43. Bit Descriptions for DAC_A_PRBS_ERR1

Bits	Bit Name	Description	Reset	Access
[7:0]	PRBS_DET_ERRCNT_A1	Error count of Lane 1 of DAC A.	0x0	R

PRBS DETECTOR ERROR COUNT 2 FOR DAC A REGISTER

Address: 0x043, Reset: 0x00, Name: DAC_A_PRBS_ERR2

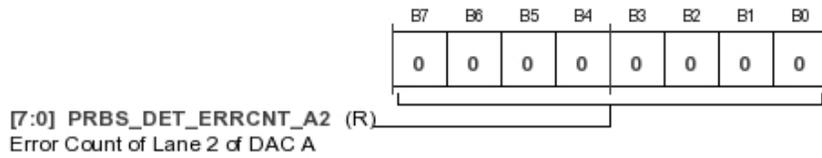


Table 44. Bit Descriptions for DAC_A_PRBS_ERR2

Bits	Bit Name	Description	Reset	Access
[7:0]	PRBS_DET_ERRCNT_A2	Error count of Lane 2 of DAC A.	0x0	R

PRBS DETECTOR ERROR COUNT 3 FOR DAC A REGISTER

Address: 0x044, Reset: 0x00, Name: DAC_A_PRBS_ERR3

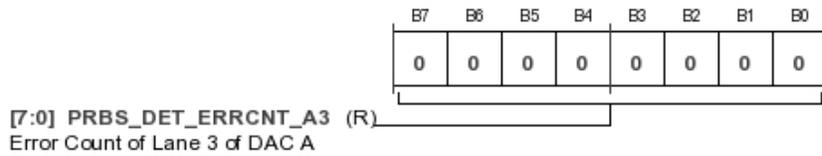


Table 45. Bit Descriptions for DAC_A_PRBS_ERR3

Bits	Bit Name	Description	Reset	Access
[7:0]	PRBS_DET_ERRCNT_A3	Error count of Lane 3 of DAC A.	0x0	R

PRBS DETECTOR ERROR COUNT 4 FOR DAC A REGISTER

Address: 0x045, Reset: 0x00, Name: DAC_A_PRBS_ERR4

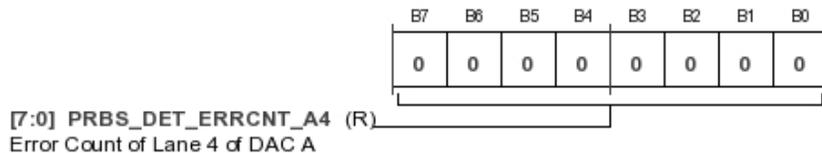


Table 46. Bit Descriptions for DAC_A_PRBS_ERR4

Bits	Bit Name	Description	Reset	Access
[7:0]	PRBS_DET_ERRCNT_A4	Error count of Lane 4 of DAC A.	0x0	R

PRBS DETECTOR ERROR COUNT 5 FOR DAC A REGISTER

Address: 0x046, Reset: 0x00, Name: DAC_A_PRBS_ERR5

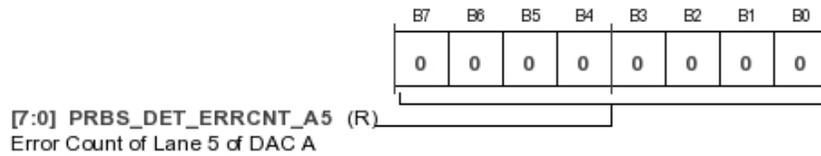


Table 47. Bit Descriptions for DAC_A_PRBS_ERR5

Bits	Bit Name	Description	Reset	Access
[7:0]	PRBS_DET_ERRCNT_A5	Error count of Lane 5 of DAC A.	0x0	R

PRBS DETECTOR ERROR COUNT 6 FOR DAC A REGISTER

Address: 0x047, Reset: 0x00, Name: DAC_A_PRBS_ERR6

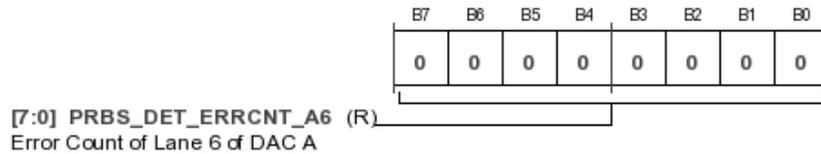


Table 48. Bit Descriptions for DAC_A_PRBS_ERR6

Bits	Bit Name	Description	Reset	Access
[7:0]	PRBS_DET_ERRCNT_A6	Error count of Lane 6 of DAC A.	0x0	R

PRBS DETECTOR ERROR COUNT 0 FOR DAC B REGISTER

Address: 0x048, Reset: 0x00, Name: DAC_B_PRBS_ERR0

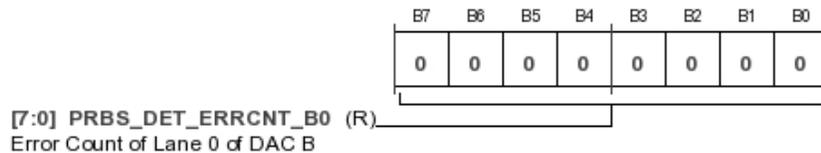


Table 49. Bit Descriptions for DAC_B_PRBS_ERR0

Bits	Bit Name	Description	Reset	Access
[7:0]	PRBS_DET_ERRCNT_B0	Error count of Lane 0 of DAC B.	0x0	R

PRBS DETECTOR ERROR COUNT 1 FOR DAC B REGISTER

Address: 0x049, Reset: 0x00, Name: DAC_B_PRBS_ERR1

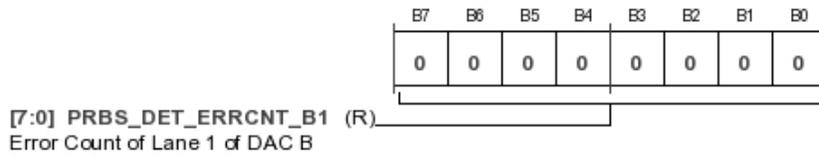


Table 50. Bit Descriptions for DAC_B_PRBS_ERR1

Bits	Bit Name	Description	Reset	Access
[7:0]	PRBS_DET_ERRCNT_B1	Error count of Lane 1 of DAC B.	0x0	R

PRBS DETECTOR ERROR COUNT 2 FOR DAC B REGISTER

Address: 0x04A, Reset: 0x00, Name: DAC_B_PRBS_ERR2

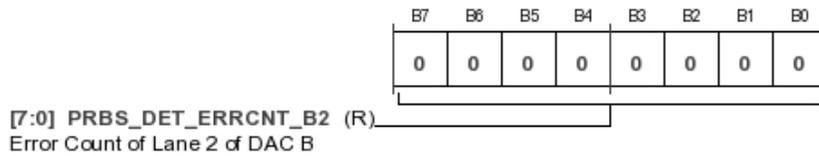


Table 51. Bit Descriptions for DAC_B_PRBS_ERR2

Bits	Bit Name	Description	Reset	Access
[7:0]	PRBS_DET_ERRCNT_B2	Error count of Lane 2 of DAC B.	0x0	R

PRBS DETECTOR ERROR COUNT 3 FOR DAC B REGISTER

Address: 0x04B, Reset: 0x00, Name: DAC_B_PRBS_ERR3

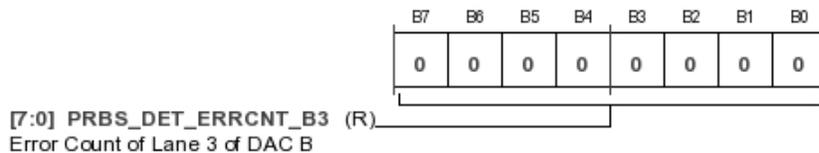


Table 52. Bit Descriptions for DAC_B_PRBS_ERR3

Bits	Bit Name	Description	Reset	Access
[7:0]	PRBS_DET_ERRCNT_B3	Error count of Lane 3 of DAC B.	0x0	R

PRBS DETECTOR ERROR COUNT 4 FOR DAC B REGISTER

Address: 0x04C, Reset: 0x00, Name: DAC_B_PRBS_ERR4

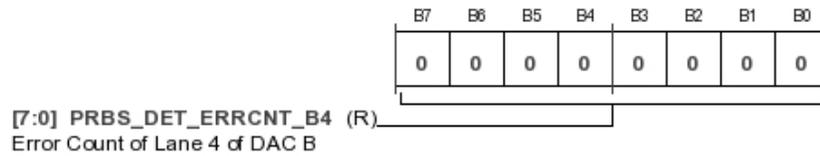


Table 53. Bit Descriptions for DAC_B_PRBS_ERR4

Bits	Bit Name	Description	Reset	Access
[7:0]	PRBS_DET_ERRCNT_B4	Error count of Lane 4 of DAC B.	0x0	R

PRBS DETECTOR ERROR COUNT 5 FOR DAC B REGISTER

Address: 0x04D, Reset: 0x00, Name: DAC_B_PRBS_ERR5

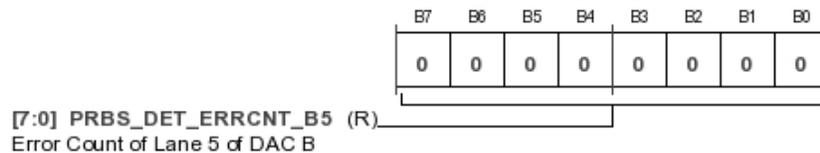


Table 54. Bit Descriptions for DAC_B_PRBS_ERR5

Bits	Bit Name	Description	Reset	Access
[7:0]	PRBS_DET_ERRCNT_B5	Error count of Lane 5 of DAC B.	0x0	R

PRBS DETECTOR ERROR COUNT 6 FOR DAC B REGISTER

Address: 0x04E, Reset: 0x00, Name: DAC_B_PRBS_ERR6

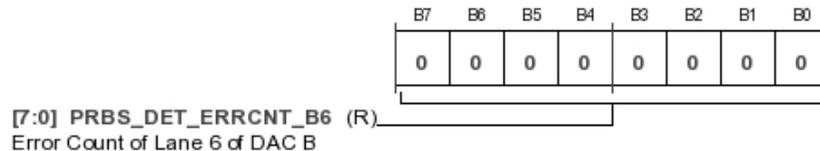


Table 55. Bit Descriptions for DAC_B_PRBS_ERR6

Bits	Bit Name	Description	Reset	Access
[7:0]	PRBS_DET_ERRCNT_B6	Error count of Lane 6 of DAC B.	0x0	R

BITS[7:0] OF TEMPERATURE SENSOR DATA READBACK REGISTER

Address: 0x050, Reset: 0x00, Name: TS_RD_LSB

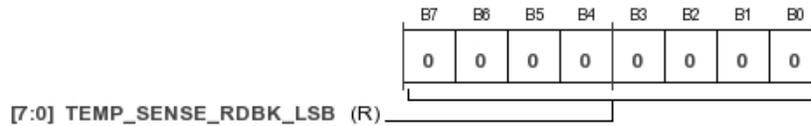


Table 56. Bit Descriptions for TS_RD_LSB

Bits	Bit Name	Description	Reset	Access
[7:0]	TEMP_SENSE_RDBK_LSB	Temperature sensor measurement MSB.	0x0	R

BITS[15:8] OF TEMPERATURE SENSOR DATA READBACK REGISTER

Address: 0x051, Reset: 0x00, Name: TS_RD_MSB

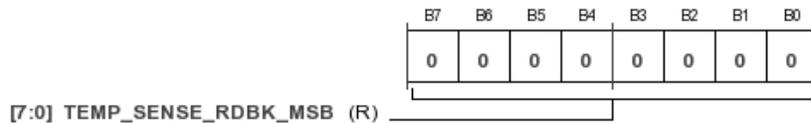


Table 57. Bit Descriptions for TS_RD_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	TEMP_SENSE_RDBK_MSB	Temperature sensor measurement LSB.	0x0	R

TEMPERATURE SENSOR CONTROL SIGNALS REGISTER

Address: 0x054, Reset: 0x01, Name: TS_CTRL

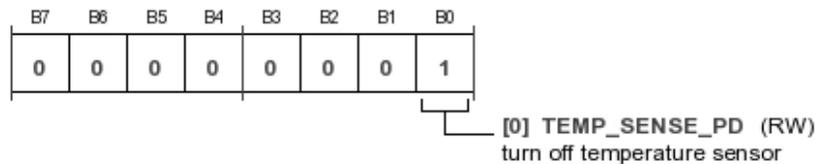


Table 58. Bit Descriptions for TS_CTRL

Bits	Bit Name	Description	Reset	Access
0	TEMP_SENSE_PD	Turn off temperature sensor.	0x1	RW

INTERRUPT PIN CONTROL REGISTER

Address: 0x055, Reset: 0x00, Name: IRQ_CTRL

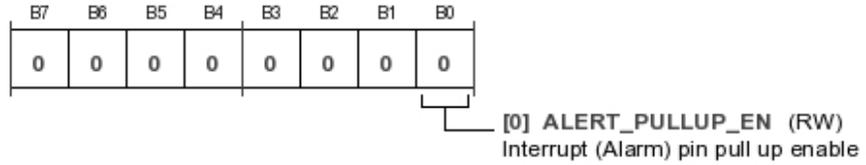


Table 59. Bit Descriptions for IRQ_CTRL

Bits	Bit Name	Description	Reset	Access
0	ALERT_PULLUP_EN	Interrupt (alarm) pin pull-up enable.	0x0	RW

DDS CONTROL REGISTER

Address: 0x060, Reset: 0x00, Name: DDS_CTRL

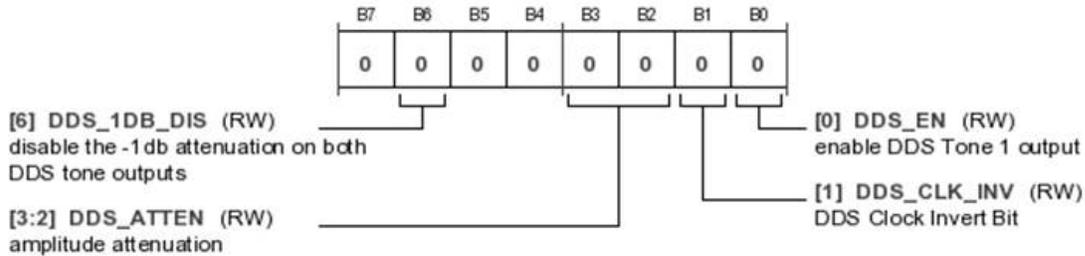
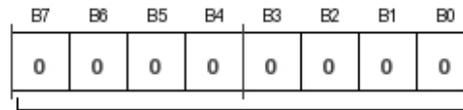


Table 60. Bit Descriptions for DDS_CTRL

Bits	Bit Name	Description	Reset	Access
6	DDS_1DB_DIS	Disable the -1 db attenuation on both DDS tone outputs.	0x0	RW
[3:2]	DDS_ATTEN	Amplitude attenuation. 00 = $\times 1/1$ amplitude. 01 = $\times 1/2$ amplitude. 10 = $\times 1/4$ amplitude. 11 = $\times 1/8$ amplitude.	0x0	RW
1	DDS_CLK_INV	DDS clock invert bit. 0 = normal. DDS clock not inverted. 1 = DDS clock inverted.	0x0	RW
0	DDS_EN	Enable DDS Tone 1 output.	0x0	RW

DDS TUNING WORD FOR TONE 1 REGISTER

Address: 0x061, Reset: 0x00, Name: DDS_TW1_0



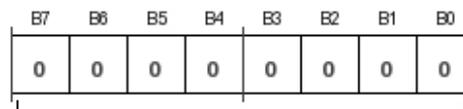
[7:0] DDS_TW1_0 (RW)
 32-bit tuning word for Tone 1 combined by {dds_tw1_3, dds_tw1_2, dds_tw1_1, dds_tw1_0}. The default configuration is for 50MHz when working with 500MHz DAC clock.

Table 61. Bit Descriptions for DDS_TW1_0

Bits	Bit Name	Description	Reset	Access
[7:0]	DDS_TW1_0	32-bit tuning word for Tone 1 combined by DDS_TW1_3, DDS_TW1_2, DDS_TW1_1, and DDS_TW1_0. The default configuration is for 50 MHz when working with 500 MHz DAC clock.	0x0	RW

DDS TUNING WORD FOR TONE 1 REGISTER

Address: 0x062, Reset: 0x00, Name: DDS_TW1_1



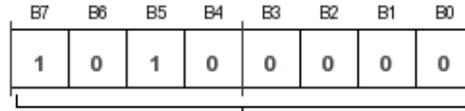
[7:0] DDS_TW1_1 (RW)
 32-bit tuning word for Tone 1 combined by {dds_tw1_3, dds_tw1_2, dds_tw1_1, dds_tw1_0}. The default configuration is for 50MHz when working with 500MHz DAC clock.

Table 62. Bit Descriptions for DDS_TW1_1

Bits	Bit Name	Description	Reset	Access
[7:0]	DDS_TW1_1	32-bit tuning word for Tone 1 combined by DDS_TW1_3, DDS_TW1_2, DDS_TW1_1, and DDS_TW1_0. The default configuration is for 50 MHz when working with 500 MHz DAC clock.	0x0	RW

DDS TUNING WORD FOR TONE 1 REGISTER

Address: 0x063, Reset: 0xA0, Name: DDS_TW1_2



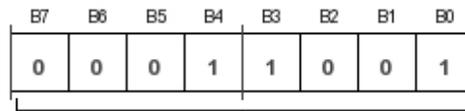
[7:0] DDS_TW1_2 (RW)
 32-bit tuning word for Tone 1 combined by {dds_tw1_3, dds_tw1_2, dds_tw1_1, dds_tw1_0}. The default configuration is for 50MHz when working with 500MHz DAC clock.

Table 63. Bit Descriptions for DDS_TW1_2

Bits	Bit Name	Description	Reset	Access
[7:0]	DDS_TW1_2	32-bit tuning word for Tone 1 combined by DDS_TW1_3, DDS_TW1_2, DDS_TW1_1, and DDS_TW1_0. The default configuration is for 50 MHz when working with 500 MHz DAC clock.	0xA0	RW

DDS TUNING WORD FOR TONE 1 REGISTER

Address: 0x064, Reset: 0x19, Name: DDS_TW1_3



[7:0] DDS_TW1_3 (RW)
 32-bit tuning word for Tone 1 combined by {dds_tw1_3, dds_tw1_2, dds_tw1_1, dds_tw1_0}. The default configuration is for 50MHz when working with 500MHz DAC clock.

Table 64. Bit Descriptions for DDS_TW1_3

Bits	Bit Name	Description	Reset	Access
[7:0]	DDS_TW1_3	32-bit tuning word for Tone 1 combined by DDS_TW1_3, DDS_TW1_2, DDS_TW1_1, and DDS_TW1_0. The default configuration is for 50 MHz when working with 500 MHz DAC clock.	0x19	RW

INTERRUPT STATUS REGISTER

Address: 0x0F0, Reset: 0x00, Name: INT

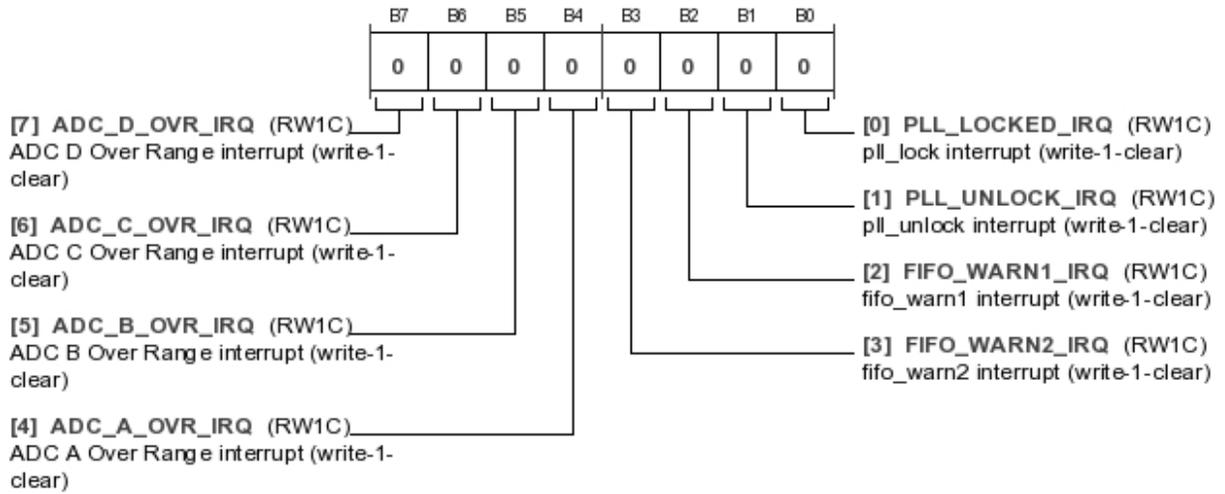


Table 65. Bit Descriptions for INT

Bits	Bit Name	Description	Reset	Access
7	ADC_D_OVR_IRQ	ADC D overrange interrupt (write 1 to clear).	0x0	RW1C
6	ADC_C_OVR_IRQ	ADC C overrange interrupt (write 1 to clear).	0x0	RW1C
5	ADC_B_OVR_IRQ	ADC B overrange interrupt(write 1 to clear).	0x0	RW1C
4	ADC_A_OVR_IRQ	ADC A overrange interrupt (write 1 to clear).	0x0	RW1C
3	FIFO_WARN2_IRQ	FIFO Warning 2 interrupt (write 1 to clear).	0x0	RW1C
2	FIFO_WARN1_IRQ	FIFO Warning 1 interrupt (write 1 to clear).	0x0	RW1C
1	PLL_UNLOCK_IRQ	PLL unlock interrupt (write 1 to clear).	0x0	RW1C
0	PLL_LOCKED_IRQ	PLL lock interrupt (write 1 to clear).	0x0	RW1C

INTERRUPT ENABLE REGISTER

Address: 0x0F1, Reset: 0x00, Name: INTEN

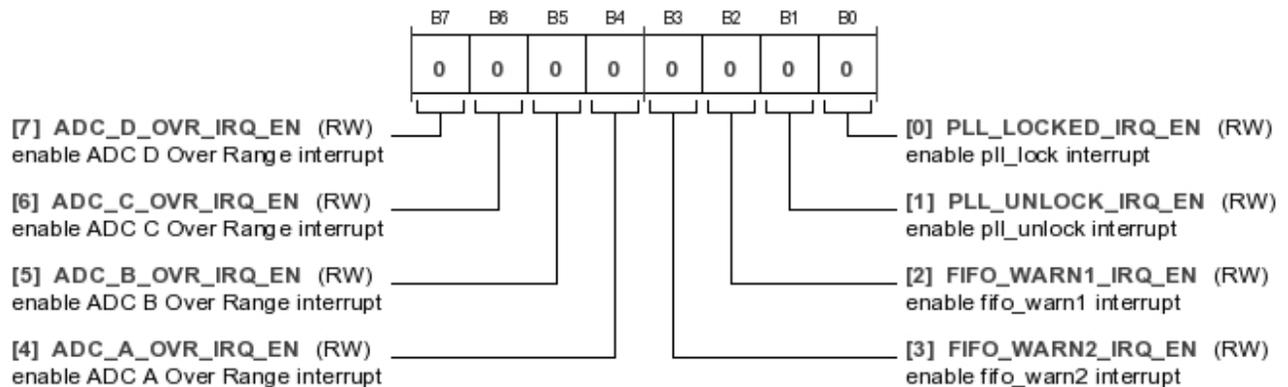


Table 66. Bit Descriptions for INTEN

Bits	Bit Name	Description	Reset	Access
7	ADC_D_OVR_IRQ_EN	Enable ADC D Overrange interrupt.	0x0	RW
6	ADC_C_OVR_IRQ_EN	Enable ADC C Overrange interrupt.	0x0	RW
5	ADC_B_OVR_IRQ_EN	Enable ADC B Overrange interrupt.	0x0	RW
4	ADC_A_OVR_IRQ_EN	Enable ADC A Overrange interrupt.	0x0	RW
3	FIFO_WARN2_IRQ_EN	Enable FIFO Warning 2 interrupt.	0x0	RW
2	FIFO_WARN1_IRQ_EN	Enable FIFO Warning 1 interrupt.	0x0	RW
1	PLL_UNLOCK_IRQ_EN	Enable PLL unlock interrupt.	0x0	RW
0	PLL_LOCKED_IRQ_EN	Enable PLL lock interrupt.	0x0	RW

INTERRUPT SOURCE STATUS REGISTER

Address: 0x0F2, Reset: 0x00, Name: INT_RAW

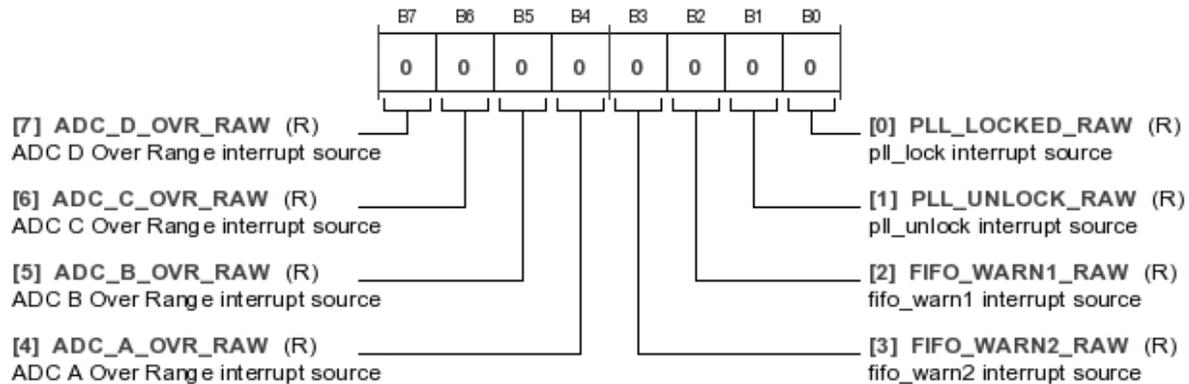


Table 67. Bit Descriptions for INT_RAW

Bits	Bit Name	Description	Reset	Access
7	ADC_D_OVR_RAW	ADC D overrange interrupt source.	0x0	R
6	ADC_C_OVR_RAW	ADC C overrange interrupt source.	0x0	R
5	ADC_B_OVR_RAW	ADC B overrange interrupt source.	0x0	R
4	ADC_A_OVR_RAW	ADC A overrange interrupt source.	0x0	R
3	FIFO_WARN2_RAW	FIFO Warning 2 interrupt source.	0x0	R
2	FIFO_WARN1_RAW	FIFO Warning 1 interrupt source.	0x0	R
1	PLL_UNLOCK_RAW	PLL unlock interrupt source.	0x0	R
0	PLL_LOCKED_RAW	PLL lock interrupt source.	0x0	R

GLOBAL DEVICE UPDATE REGISTER

Address: 0x0FF, Reset: 0x00, Name: DEVICE_UPDATE

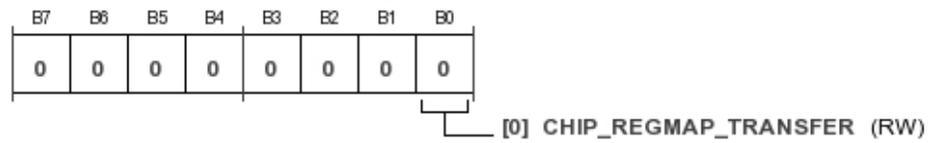
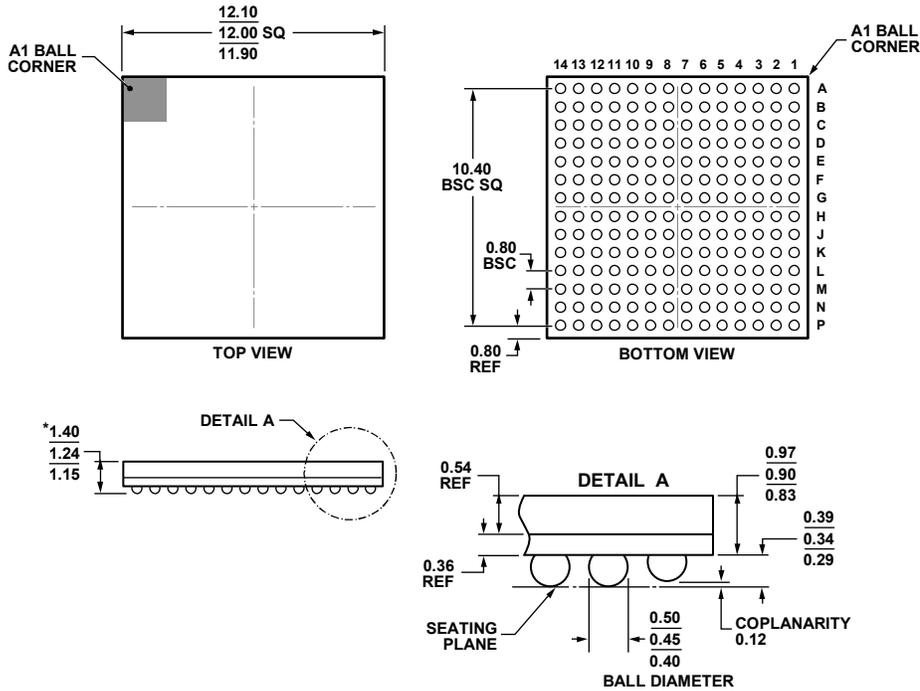


Table 68. Bit Descriptions for DEVICE_UPDATE

Bits	Bit Name	Description	Reset	Access
0	CHIP_REGMAP_TRANSFER	Register map master/slave transfer bit. Self clearing bit used to synchronize the transfer of data from the master to the slave registers. 0 = no effect 1 = transfer data from the master registers written by the register maps to the slave registers seen by the datapath.	0x0	RW

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-219 WITH EXCEPTION TO PACKAGE HEIGHT.

Figure 33. 196-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-196-9)

Dimensions shown in millimeters

05-09-2011-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
AD9993BBCZ	-40°C to +85°C	196-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-196-9
AD9993BBCZRL	-40°C to +85°C	196-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-196-9
AD9993-EBZ		Evaluation Board	

¹ Z = RoHS Compliant Part.