ANALOG DEVICES

12 × 12-Bit CMOS Multiplier

ADSP-1012A

FEATURES

- **12 × 12-Bit Parallel Multiplication**
- **20MHz Multiplication Rate (Worst Case)**
- **300mW Power Dissipation with TTL-Compatible CMOS Technology**
- **Twos-Complement, Unsigned-Magnitude, and Mixed-Mode Data Formats**
- **Available in Hermetically-Sealed 64-Pin DIP, Hermetically-Sealed 68-Pin PGA, Plastic 64-Pin DIP, or 68-Contact LCC**
- **Available Specified to MIL-STD-883, Class B**
- **Pin-Compatible with ADSP-1012 and MPY012HJ1**

APPLICATIONS

- **Digital Signal Processing**
  - **Digital Filtering**
  - **Fourier Transformations**
  - **Correlations**
- **Image Processing**

GENERAL DESCRIPTION

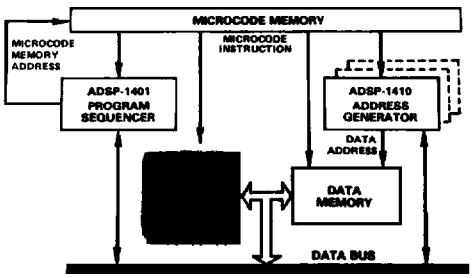
The ADSP-1012A is a high-speed, low-power 12 × 12-bit parallel multiplier fabricated in 1.5 micron CMOS.

The ADSP-1012A has two 12-bit input ports, a 12-bit Most Significant Product (MSP) port, and a 12-bit Least Significant Product (LSP) port. Input data is interpreted in twos-complement, unsigned-magnitude, or mixed-mode formats. The ADSP-1012A produces a 24-bit result whose MSP can be rounded with a control which causes a 1 to be added to the Most Significant Bit (MSB) of the LSP.

All input pins are ESD-protected. The input and output registers are all D-type positive-edge-triggered flip-flops. The input registers are controlled by independent clock lines. Both of the product registers have their own independent clock lines and their own independent three-state output controls. Three-state outputs and independently clocked inputs allow the ADSP-1012A to be connected directly to a single 12-bit bus.

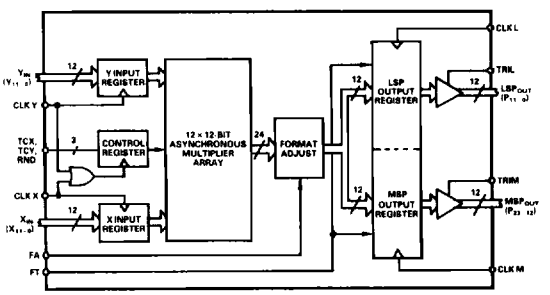
The ADSP-1012A is a pin-for-pin replacement for Analog Devices' ADSP-1012 and is also pin-for-pin compatible in a DIP package with TRW's MPY012HJ1. The ADSP-1012A's multiply time is over twice as fast as the TRW device.

The power consumption of the ADSP-1012A is 300mW maximum, 10% of the power required by equivalent bipolar devices. The differential between the ADSP-1012A's junction temperature and the ambient temperature stays small because of this low power dissipation. Thus, the ADSP-1012A can be safely specified for operation at environmental temperatures over its extended temperature range (−55°C to +125°C ambient).



WORD-SLICE® MICROCODED SYSTEM WITH ADSP-1012A

The ADSP-1012A is available for both commercial and military temperature ranges. MIL-grade parts are available processed fully to MIL-STD-883, Class B. Additionally, the ADSP-1012A is available in either a 64-pin hermetically sealed ceramic DIP, a hermetically sealed ceramic 68-pin grid array, a plastic 64-pin DIP, or a 68-contact LCC.



Functional Block Diagram

SPECIFICATIONS[1]

RECOMMENDED OPERATING CONDITIONS

Parameter		ADSP-1012A J and K Grades Min	ADSP-1012A J and K Grades Max	ADSP-1012A S and T Grades[2] Min	ADSP-1012A S and T Grades[2] Max	Unit
V_{DD}	Supply Voltage	4.75	5.25	4.5	5.5	V
T_{AMB}	Operating Temperature (ambient)	0	+70	−55	+125	°C

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	ADSP-1012A J and K Grades Min	ADSP-1012A J and K Grades Max	ADSP-1012A S and T Grades[2] Min	ADSP-1012A S and T Grades[2] Max	Unit
V_{IH}	High-Level Input Voltage	@ V_{DD} = max	2.0		2.2		V
V_{IL}	Low-Level Input Voltage	@ V_{DD} = min		0.8		0.8	V
V_{OH}	High-Level Output Voltage	@ V_{DD} = min & I_{OH} = −1.0mA	2.4		2.4		V
V_{OL}	Low-Level Output Voltage	@ V_{DD} = min & I_{OL} = 4.0mA		0.4		0.5	V
I_{IH}	High-Level Input Current, All Inputs	@ V_{DD} = max & V_{IN} = 5V		10		10	μA
I_{IL}	Low-Level Input Current, All Inputs	@ V_{DD} = max & V_{IN} = 0V		10		10	μA
I_{OZ}	Three-State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = 0V or max		50		50	μA
I_{DD}	Supply Current	@ max clock rate; TTL inputs		60		70	mA
I_{DD}	Supply Current – Quiescent	All V_{IN} = 2.4V		30		35	mA

SWITCHING CHARACTERISTICS[3]

Parameter		ADSP-1012A J Grade 0 to +70° Min	J Grade Max	K Grade Min	K Grade Max	S Grade[2] −55°C to +125°C Min	S Grade[2] Max	T Grade[2] Min	T Grade[2] Max	Unit
t_D	Output Delay		30		30		35		35	ns
t_{ENA}	Three-State Enable Delay		30		30		35		35	ns
t_{DIS}	Three-State Disable Delay		30		30		35		35	ns
t_{PW}	Clock Pulse Width	20		20		20		20		ns
t_S	Input Setup Time	20		20		20		20		ns
t_H	Input Hold Time	2		2		2		2		ns
t_{MC}	Clocked Multiply Time		75		50		90		60	ns
t_{MUC}	Unclocked Multiply Time		105		80		125		95	ns

NOTES
[1]All min and max specifications are over power supply and temperature range indicated.
[2]S and T grade parts are available processed and tested in accordance with MIL-STD-883, Class B. The processing and test methods used for S/883B and T/883B versions of the ADSP-1012A can be found in Analog Devices' Military Databook.
[3]Input levels are GND and 3.0V. Rise times are 5ns. Input timing reference levels and output reference levels are 1.5V, except for t_{ENA} and t_{DIS} which are indicated in Figure 2.

Specifications subject to change without notice.

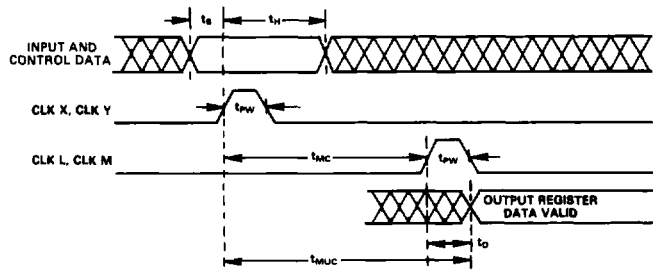


Figure 1. ADSP-1012A Timing Diagram

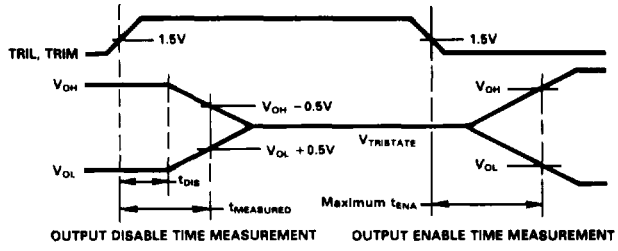


Figure 2. Three-State Disable and Enable Timing

Output disable time, t_{DIS}, is measured from the time the output enable control signal reaches 1.5V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5V toward +1.5V. From the tester capacitive loading, C_L, and the measured current, i_L, the decay time, t_{DECAY}, can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA}, is also measured from output enable control signal at 1.5V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

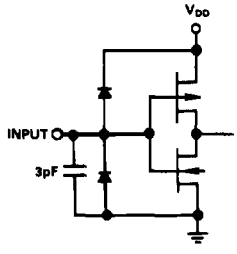


Figure 3. Equivalent Input Circuit

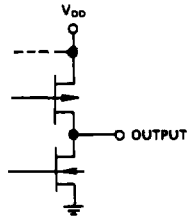


Figure 4. Equivalent Output Circuit

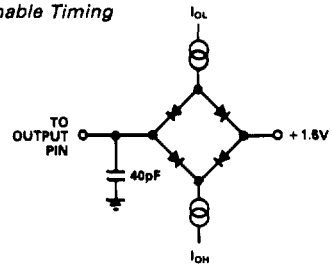


Figure 5. Normal Load for ac Measurements

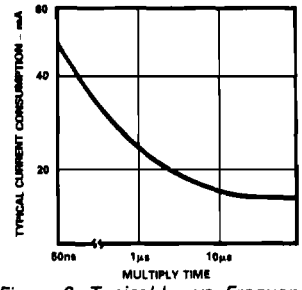


Figure 6. Typical I_{DD} vs. Frequency

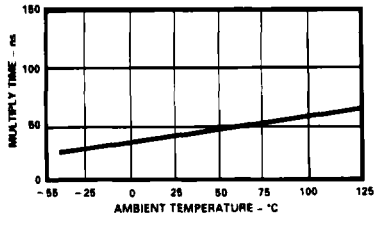


Figure 7. Approximate Worst Case Multiply Time vs. Temperature

METHOD OF OPERATION

The X and Y input registers are positive-edge-triggered D-type flip-flops. Input data is loaded to the X and Y registers by the rising edges of CLK X and CLK Y, respectively.

The X and Y input data can be either in twos-complement, unsigned-magnitude, or mixed-mode formats (Table I.) Twos-complement input data is indicated by HI (logic 1) levels on the TCX line for X input data and by HI levels on the TCY line for Y input data. Unsigned-magnitude X and Y inputs are indicated by LO (logic 0) levels on the TCX and TCY lines, respectively. Outputs will be in the same format as inputs unless the input formats are mixed, in which case the outputs will be in twos-complement representation.

The ADSP-1012A's output is fielded into an 12-bit MSP and an 12-bit LSP. When RND is HI, the MSP will be rounded by adding a binary 1 with carry to the MSB of the LSP, consistently rounding toward positive infinity. Truncating the MSP (RND LO) introduces a large-sample statistical bias $-(2^{12}-1)/2$ LSBs of the LSP, while rounding (RND HI) reduces the bias to only $+1/2$ LSBs of the LSP.

TCX, TCY, and RND are registered input controls. TCX and TCY are latched by the rising edges of CLK X and CLK Y, respectively. RND is latched by the rising edge of the logical OR of CLK X and CLK Y. Be sure that CLK X and CLK Y are both LO before attempting to clock in RND.

The asynchronous FA control format-adjusts the output from the multiplier array (Table II). FA must be HI to get a product for unsigned-magnitude or mixed-mode multiplications in a standard format. In a mixed-mode product, the sign bit will be product Bit 23 (P23). For twos-complement multiplications, FA can be LO. If FA is at a LO level, the MSP and the MSB of the LSP are left-shifted one bit and the sign bit is duplicated in the MSB of the LSP.

Format-adjusting a twos-complement product increases the number of significant bits in the MSP by eliminating one of the two normally redundant MSBs in the MSP. However, an overflow on format-adjust will occur when full-scale negative is multiplied by itself, yielding full-scale negative instead of the correct positive product (which is not representable in format-adjusted twos-complement format). To avoid this overflow, disallow X and Y inputs that are both full-scale negative.

The output latches can be bypassed for asynchronous operation by setting the feed-through (FT) line HI. Data previously latched in the output registers is unaffected by FT going HI. If FT is later restored to LO, the output registers will drive the three-state outputs with the product most recently clocked to those registers (even if clocked while FT was HI).

Products are clocked into the MSP and LSP output registers with the rising edges of CLK M and CLK L, respectively. Each of these registers has its own three-state control. A HI on the asynchronous TRIL or TRIM line disables the corresponding LSP or MSP output driver to a high-impedance state. Conversely, a LO on TRIL or TRIM enables the corresponding output driver, driving the output bus.

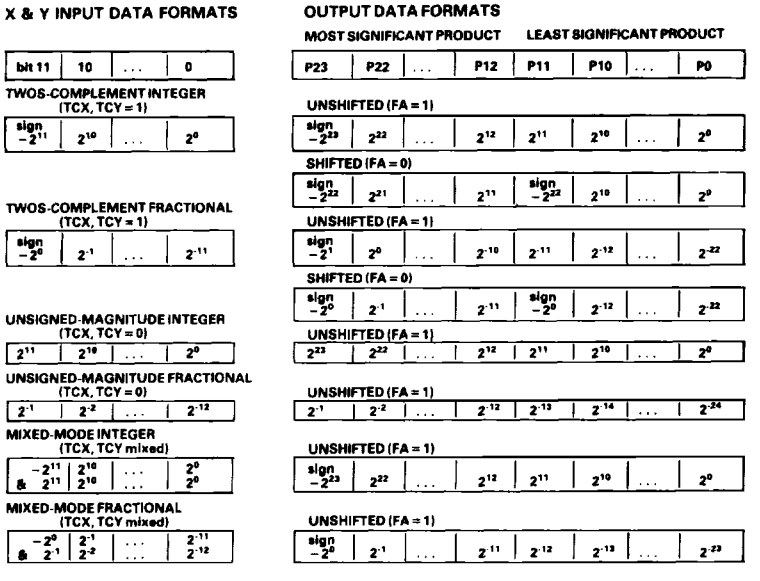


Table I. ADSP 1012A Data Formats

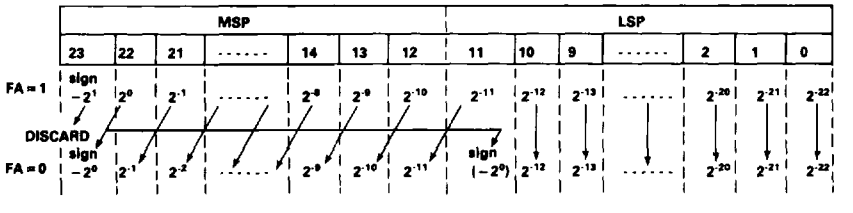


Table II. ADSP-1012A Format Adjust

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.3V to 7V	Operating Temperature Range (Ambient)	−55°C to +125°C
Input Voltage	−0.3V to V_{DD}	Storage Temperature Range	−65°C to +150°C
Output Voltage Swing	−0.3V to V_{DD}	Lead Temperature (10 Seconds)	300°C

ORDERING INFORMATION

Part Number	Temperature Range	Package	Package Outline
ADSP-1012AJN	0 to +70°C	64-Pin Plastic DIP	N-64A
ADSP-1012AKN	0 to +70°C	64-Pin Plastic DIP	N-64A
ADSP-1012AJD	0 to +70°C	64-Pin Ceramic DIP	D-64A
ADSP-1012AKD	0 to +70°C	64-Pin Ceramic DIP	D-64A
ADSP-1012AJG	0 to +70°C	68-Lead Pin Grid Array	G-68A
ADSP-1012AKG	0 to +70°C	68-Lead Pin Grid Array	G-68A
ADSP-1012ASD	−55°C to +125°C	64-Pin Ceramic DIP	D-64A
ADSP-1012ATD	−55°C to +125°C	64-Pin Ceramic DIP	D-64A
ADSP-1012ASD/883B	−55°C to +125°C	64-Pin Ceramic DIP	D-64A
ADSP-1012ATD/883B	−55°C to +125°C	64-Pin Ceramic DIP	D-64A
ADSP-1012ASG	−55°C to +125°C	68-Lead Pin Grid Array	G-68A
ADSP-1012ATG	−55°C to +125°C	68-Lead Pin Grid Array	G-68A
ADSP-1012ASG/883B	−55°C to +125°C	68-Lead Pin Grid Array	G-68A
ADSP-1012ATG/883B	−55°C to +125°C	68-Lead Pin Grid Array	G-68A
ADSP-1012ASE/883B	−55°C to +125°C	68-Contact LCC	E-68A
ADSP-1012ATE/883B	−55°C to +125°C	68-Contact LCC	E-68A

Contact DSP Marketing in Norwood concerning the availability of other package types.

ESD SENSITIVITY

The ADSP-1012A features proprietary input protection circuitry to dissipate high energy discharges (Human Body Model). Per Method 3015 of MIL-STD-883, the ADSP-1012A has been classified as a Class 1 device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

ADSP-1012A PIN CONFIGURATIONS

DIP
D-64A
N-64A

PIN	FUNCTION	PIN	FUNCTION
1	X7	33	P16
2	X6	34	P17
3	X5	35	P18
4	X4	36	P19
5	X3	37	P20
6	X2	38	P21
7	X1	39	P22
8	X0	40	P23
9	P0	41	TCY
10	P1	42	Y11
11	P2	43	Y10
12	P3	44	Y9
13	P4	45	Y8
14	P5	46	Y7
15	P6	47	Y6
16	P7	48	$+V_{DD}$
17	P8	49	$+V_{DD}$
18	P9	50	$+V_{DD}$
19	P10	51	Y5
20	P11	52	Y4
21	TRIL	53	Y3
22	TRIM	54	Y2
23	GND	55	Y1
24	GND	56	Y0
25	FT	57	TCX
26	FA	58	RND
27	CLKL	59	CLKY
28	CLKM	60	CLKX
29	P12	61	X11
30	P13	62	X10
31	P14	63	X9
32	P15	64	X8

PIN GRID ARRAY
G-68A

PIN	FUNCTION	PIN	FUNCTION
1	P0	35	TCY
2	P1	36	Y11
3	P2	37	Y10
4	P3	38	Y9
5	P4	39	Y8
6	P5	40	Y7
7	P6	41	Y6
8	P7	42	V_{DD}
9	P8	43	V_{DD}
10	P9	44	V_{DD}
11	P10	45	Y5
12	P11	46	Y4
13	TRIL	47	Y3
14	TRIM	48	Y2
15	GND	49	Y1
16	GND	50	Y0
17	N/C	51	N/C
18	FT	52	TCX
19	FA	53	RND
20	CLKL	54	CLKY
21	CLKM	55	CLKX
22	P12	56	X11
23	P13	57	X10
24	P14	58	X9
25	P15	59	X8
26	P16	60	X7
27	P17	61	X6
28	P18	62	X5
29	P19	63	X4
30	P20	64	X3
31	P21	65	X2
32	P22	66	X1
33	P23	67	X0
34	N/C	68	N/C

LCC
E-68A

PIN	FUNCTION	PIN	FUNCTION
1	X7	35	P16
2	X6	36	P17
3	X5	37	P18
4	X4	38	P19
5	X3	39	P20
6	X2	40	P21
7	X1	41	P22
8	X0	42	P23
9	N/C	43	N/C
10	P0	44	TCY
11	P1	45	Y11
12	P2	46	Y10
13	P3	47	Y9
14	P4	48	Y8
15	P5	49	Y7
16	P6	50	Y6
17	P7	51	$+V_{DD}$
18	P8	52	$+V_{DD}$
19	P9	53	$+V_{DD}$
20	P10	54	Y5
21	P11	55	Y4
22	TRIL	56	Y3
23	TRIM	57	Y2
24	GND	58	Y1
25	GND	59	Y0
26	N/C	60	N/C
27	FT	61	TCX
28	FA	62	RND
29	CLKL	63	CLKY
30	CLKM	64	CLKX
31	P12	65	X11
32	P13	66	X10
33	P14	67	X9
34	P15	68	X8