

AEIC-7273-S16

Quad Differential Line Driver LC

With Open-Collector Outputs And Enable Function



Data Sheet

Description

These line drivers are similar in function to the AEIC-7272-S16, only in an open-collector format. The VCC pin powers the internal logic only. Output voltage is dependent on the customer supplied voltage, up to a maximum of 30 V. There is essentially no difference in output swing or performance with VCC (LOGIC) values from 3.5-30 V. Internal clamp diodes allow trouble-free operation when driving cable lengths exceeding 100 meters. The outputs are protected by initiating shutdown when junction temperatures exceed safe limits. This feature assures highly reliable operation in harsh environments. Heat sinking is aided by having pin 8 directly connected to the ASIC substrate inside the package.

This part is available in 16L SOIC (Pb-free) package.

Applications

- Encoders
- Industrial controls

Features

- Supply (Bias) Voltage Range 3.5 V to 30 V
- Operation to 800KHz
- CMOS and TTL Compatible Inputs
- Support RS422A
- High Impedance Buffered Inputs with hysteresis
- NPN Open-Collector outputs
- 80 mA peak SINK/SOURCE current
- Outputs Protected by Thermal Shut-Down

Pin Assignment

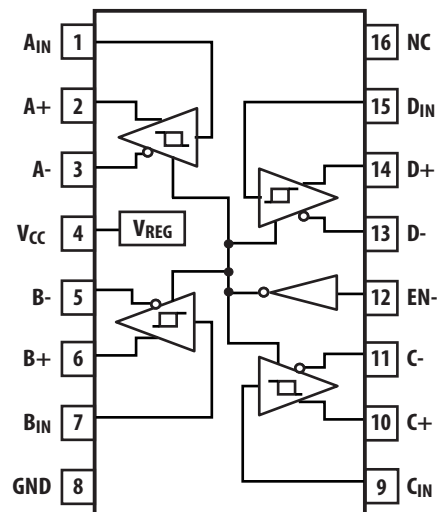


Table 1. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Units	Notes
Operating Temperature Range	T _A	-55	125	°C	
Supply (Driver) Voltage Range	V _{CCD}	3.5	30	V	

Table 2. Electrical Characteristics

Unless otherwise specified, T_A = 25° C and EN- < 0.8 V.

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Overtmp Operate Point (junction)	T _{JOP}	–	172	–	°C	Note 1
Overtmp Release Point (junction)	T _{JRP}	–	136	–	°C	Note 1
V _{CC} Voltage Range	V _{CC}	3.5	5	30	V	
Supply Current V _{CC1}	I _{CC1}	–	11.9	16.0	mA	V _{CC} = 5 V
Supply Current V _{CC2}	I _{CC2}	–	2.5	3.4	mA	V _{CC} = 5 V, EN- > 2 V
Supply Current V _{CC3}	I _{CC3}	–	12.1	18.5	mA	V _{CC} = 30 V
Supply Current V _{CC4}	I _{CC2}	–	2.6	3.5	mA	V _{CC} = 30 V, EN- > 2 V
Enable Input Threshold	V _{THE}	0.8	1.5	2	V	
Enable Low Level Input Current	I _{I LE}	-10	0	10	μA	V _{IN} = 0 V, V _{CC} = 5 V
Enable High Level Input Current	I _{I HE}	–	108	150	μA	V _{IN} = 5 V, V _{CC} = 5 V
High Impedance Output Leakage	I _{OZ}	-4.0	0.0	4.0	μA	V _{CC} = 5 V, EN- > 2 V, Output at 15 V
Input Positive-Going Threshold	V _{T+}	1.05	1.25	1.45	V	
Input Negative-Going Threshold	V _{T-}	0.75	0.95	1.15	V	
Input Hysteresis	V _H	–	0.3	–	V	
Low Level Input Current	I _{IL}	-4.0	-0.1	–	μA	V _{IN} = 0 V, V _{CC} = 5 V
High Level Input Current	I _{I H}	–	0	4.0	μA	V _{IN} = 5 V, V _{CC} = 5 V
Low Level Output1	V _{OL1}	–	375	500	mV	I _{OL} = 20 mA, V _{CC} = 5 V, V _{OC} = 30 V
Low Level Output2	V _{OL2}	–	370	500	mV	I _{OL} = 20 mA, V _{CC} = 30 V, V _{OC} = 30 V
High Level Output Current1	I _{OH1}	–	0	10	μA	V _{CC} = 5 V, V _{OC} = 30 V
High Level Output Current2	I _{OH2}	–	0	10	μA	V _{CC} = 30 V, V _{OC} = 30 V

Notes :

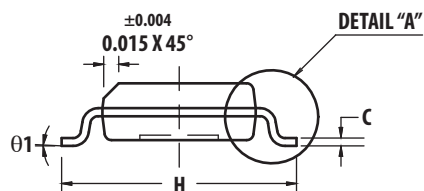
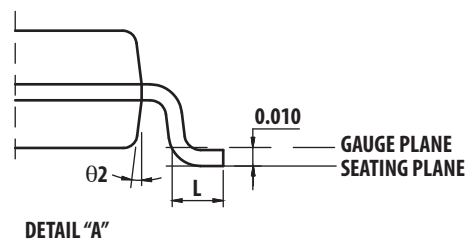
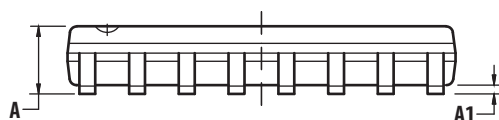
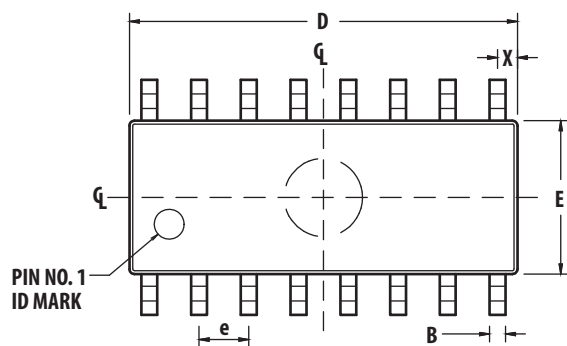
1. This is not a test parameter, but for information only.
2. Unused inputs should be connected to ground.
3. Do not leave pin 12 open. In applications which do not use the enable function, this pin should be tied to ground.

Table 3. AC Switching Characteristics

Load is 470 ohms and 1000 pF, output to its compliment and 470 ohms each output to Voc.

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Propagation delay, rising input 50% point to zero crossing of differential outputs	T _{PLH}	–	232	325	ns	See above.
Propagation delay, falling input 50% point to zero crossing of differential outputs	T _{PHL}	–	236	330	ns	See above.
Output Rise Time	T _R	–	516	722	ns	See above.
Output Fall Time	T _F	–	516	722	ns	See above.

Package Drawings (Dimensions in Inches)



Symbol	16 SOIC	
	Min	Max
A	0.054	0.068
A1	0.004	0.0098
B	0.014	0.019
D	0.386	0.393
E	0.150	0.157
H	0.229	0.244
e	0.050 BSC	
C	0.0075	0.0098
L	0.016	0.034
X	0.020 REF	
theta 1	0°	8°
theta 2	7° BSC	

Notes:

1. Lead coplanarity should be 0 to 0.004" max.
2. Package surface finishing: VD1 24~27 (Dual).
Package surface finishing: VD1 13~15 (16L Soic(NB) Matrix).
3. All dimension excluding mold flashes.
4. The lead width, B to be determined at 0.0075" from the lead tip.

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