Document Number: AFT20P140-4WN
Rev. 1, 1/2014

RoHS

RF Power LDMOS Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

This 24 W symmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 1880 to 2025 MHz.

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.6 Vdc, P_{out} = 24 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

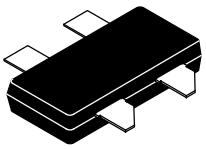
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
1880 MHz	17.8	41.7	7.7	-31.0
1960 MHz	17.8	41.7	7.7	-33.7
2025 MHz	17.6	41.2	7.8	-34.0

Features

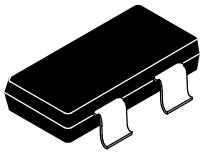
- Designed for Wide Instantaneous Bandwidth Applications
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Able to Withstand Extremely High Output VSWR and Broadband Operating Conditions
- Designed for Digital Predistortion Error Correction Systems
- In Tape and Reel. R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel.

AFT20P140-4WNR3
AFT20P140-4WGNR3

1880-2025 MHz, 24 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTORS



OM-780-4L
PLASTIC
AFT20P140-4WNR3



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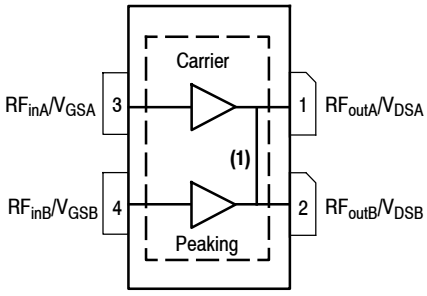


(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 1. Pin Connections

1. Pin connections 1 and 2 are DC coupled and RF independent.

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +125	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 74°C, 24 W 2-Carrier W-CDMA, 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.6 Vdc, f1 = 1880 MHz, f2 = 1910 MHz Case Temperature 88°C, 118 W 2-Carrier W-CDMA, 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.6 Vdc, f1 = 1880 MHz, f2 = 1910 MHz	$R_{\theta JC}$	 0.60 0.42	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics (5)					
Gate Threshold Voltage (6) (V_{DS} = 10 Vdc, I_D = 150 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DA} = 500 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	1.3	1.9	2.3	Vdc
Drain-Source On-Voltage (4) (V_{GS} = 10 Vdc, I_D = 2.0 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

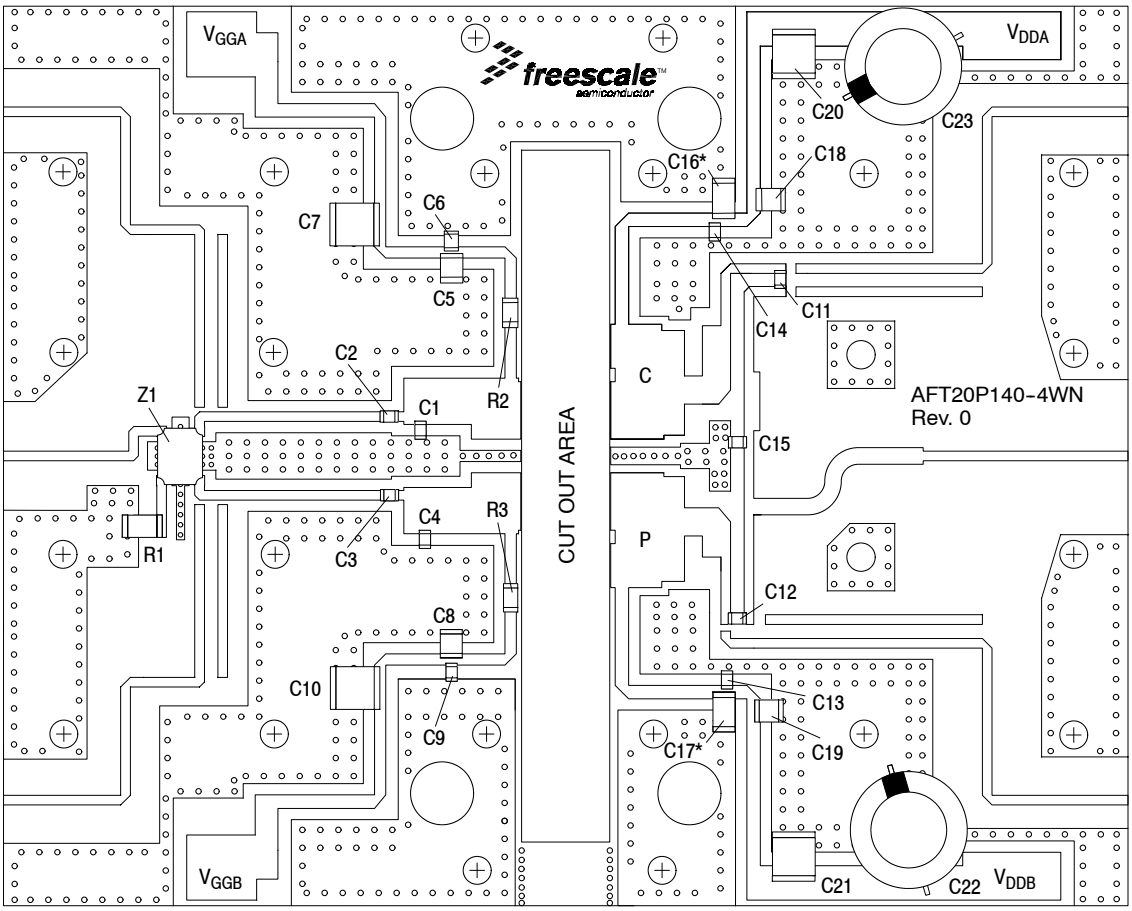
1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. Side A and Side B are tied together for these measurements.
5. V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.
6. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests — 1900 MHz (1,2,3,4) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.6 Vdc, P_{out} = 24 W Avg., f1 = 1880 MHz, f2 = 1910 MHz, 2-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±20 MHz Offset.					
Power Gain	G_{ps}	17.0	17.8	20.0	dB
Drain Efficiency	η_D	38.0	41.4	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.1	7.7	—	dB
Adjacent Channel Power Ratio	ACPR	—	-33.1	-31.0	dBc
Functional Tests — 2025 MHz (1,2,3,4) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.6 Vdc, P_{out} = 24 W Avg., f1 = 1995 MHz, f2 = 2025 MHz, 2-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±20 MHz Offset.					
Power Gain	G_{ps}	16.6	17.8	19.6	dB
Drain Efficiency	η_D	38.0	40.7	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.1	7.8	—	dB
Adjacent Channel Power Ratio	ACPR	—	-33.5	-31.0	dBc
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQA} = 500 mA, f = 1960 MHz					
VSWR 10:1 at 32 Vdc, 170 W CW Output Power (3 dB Input Overdrive from 130 W CW Rated Power)	No Device Degradation				
Typical Performance (3) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.6 Vdc, 1880-2025 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	130	—	W
P_{out} @ 3 dB Compression Point (5)	P3dB	—	170	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1880-2025 MHz bandwidth)	Φ	—	-22.7	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	160	—	MHz
Gain Flatness in 145 MHz Bandwidth @ P_{out} = 24 W Avg.	G_F	—	0.25	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.001	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.003	—	dB/°C

1. V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.
2. Part internally matched both on input and output.
3. Measurement made with device in a symmetrical Doherty configuration.
4. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.
5. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



*C16 and C17 are mounted vertically.

Figure 2. AFT20P140-4WNR3 Test Circuit Component Layout

Table 6. AFT20P140-4WNR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	0.6 pF Chip Capacitor	ATC600F0R6BT250XT	ATC
C2, C3, C6, C9, C11, C12, C13, C14	12 pF Chip Capacitors	ATC600F120JT250XT	ATC
C4	0.3 pF Chip Capacitor	ATC600F0R3BT250XT	ATC
C5, C8, C18, C19	2.2 μF, 100 V Chip Capacitors	C3225X7R2A225KT	TDK
C7, C10, C20, C21	10 μF, 100 V Chip Capacitors	C5750X7S2A106KT	TDK
C15	0.5 pF Chip Capacitor	ATC600F0R5BT250XT	ATC
C16, C17	6.8 μF, 50 V Chip Capacitors	C4532X7R1H685KT	TDK
C22, C23	100 μF, 63 V Electrolytic Capacitors	SK063M0100B5S-1012	Yageo
R1	50 Ω, 10 W Chip Resistor	CW12010T0050GBK	ATC
R2, R3	3 Ω, 1/4 W Chip Resistors	CRCW12063R00FKEA	Vishay
Z1	1700–2000 MHz Band, 90°, 3 dB Hybrid Couplers	1P503S	Anaren
PCB	0.020″, ε_r = 3.5	RO4350B	Rogers

TYPICAL CHARACTERISTICS

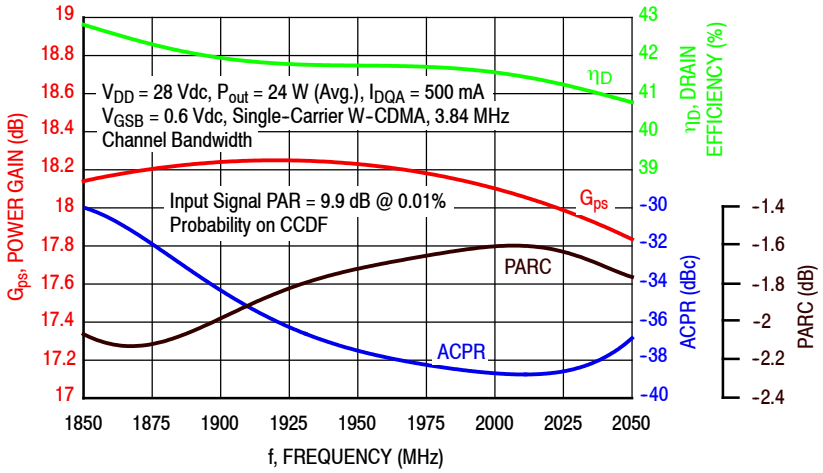


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 24 Watts Avg.

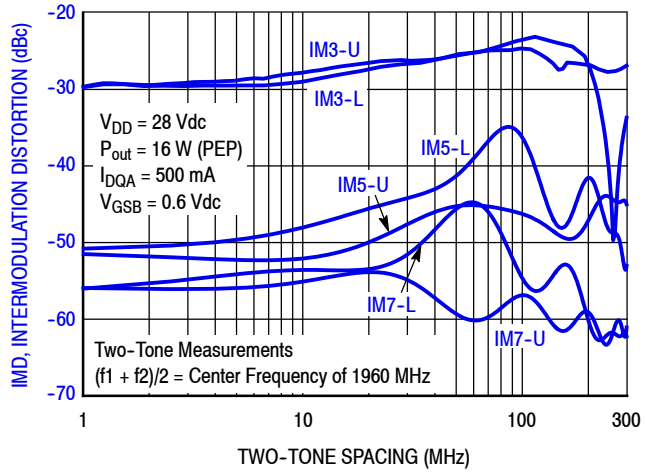


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

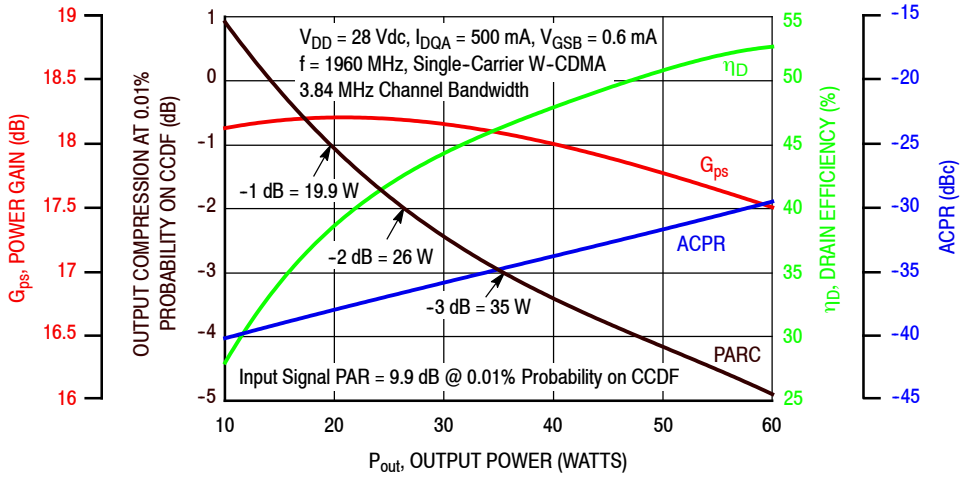


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

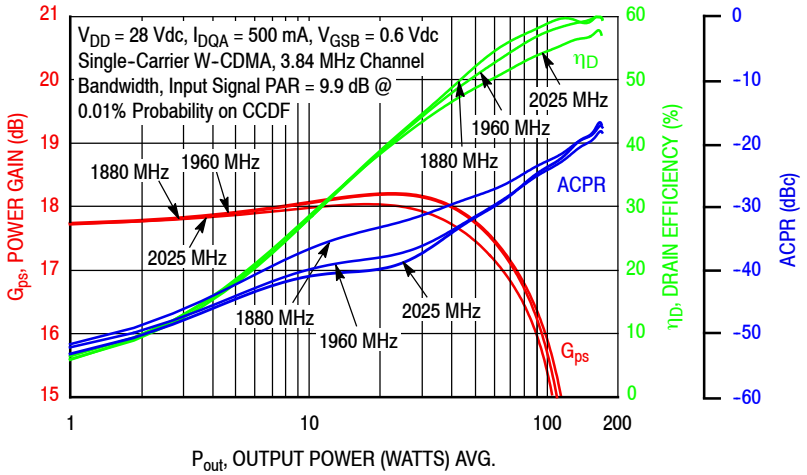


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

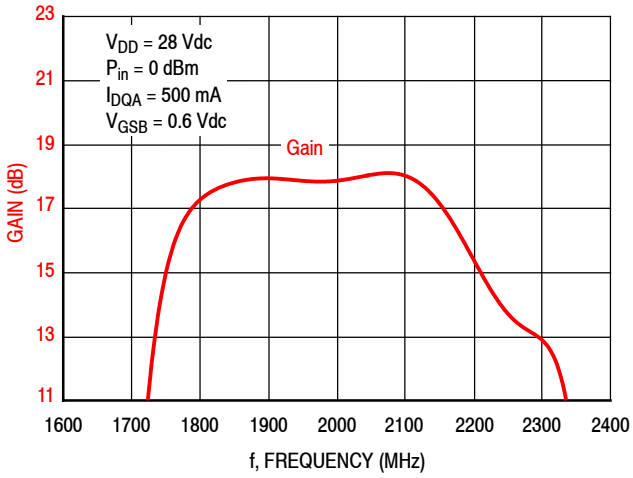


Figure 7. Broadband Frequency Response

V_{DD} = 28 Vdc, I_{DQA} = 511 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	6.86 - j8.74	6.24 + j8.58	2.15 - j5.34	19.2	50.0	101	54.0	-13
1960	10.2 - j5.77	8.98 + j6.06	2.20 - j5.78	19.1	49.9	98	53.3	-14
2025	8.51 - j1.35	8.23 + j2.78	2.14 - j6.19	18.9	50.1	102	52.6	-15

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	6.86 - j8.74	6.77 + j9.00	2.02 - j5.66	16.9	50.8	121	55.1	-17
1960	10.2 - j5.77	10.0 + j5.72	2.08 - j6.06	16.7	50.7	118	53.6	-18
2025	8.51 - j1.35	8.44 + j1.79	2.08 - j6.50	16.5	50.8	121	53.0	-19

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 8. Single Side Load Pull Performance — Maximum Power Tuning

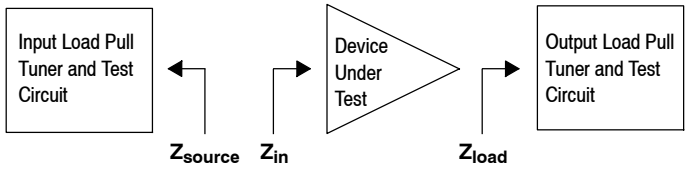
V_{DD} = 28 Vdc, I_{DQA} = 511 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	6.86 - j8.74	6.66 + j8.74	4.65 - j4.23	21.6	48.4	69	64.6	-21
1960	10.2 - j5.77	9.17 + j5.67	4.26 - j3.66	21.6	48.0	63	64.1	-22
2025	8.51 - j1.35	7.90 + j2.75	3.73 - j4.44	21.2	48.5	70	62.7	-21

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	6.86 - j8.74	7.01 + j9.10	4.65 - j4.32	19.5	49.0	79	65.6	-27
1960	10.2 - j5.77	9.95 + j5.36	4.09 - j3.61	19.6	48.6	73	65.0	-30
2025	8.51 - j1.35	8.11 + j2.05	3.50 - j4.62	19.0	49.3	86	63.7	-28

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 9. Single Side Load Pull Performance — Maximum Drain Efficiency Tuning



P1dB - TYPICAL LOAD PULL CONTOURS — 1960 MHz

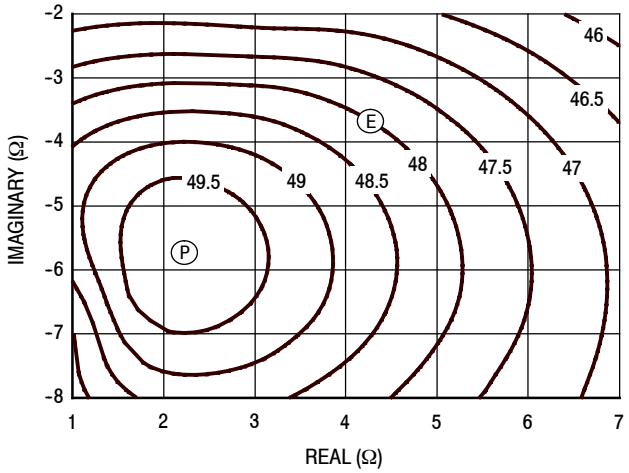


Figure 10. P1dB Load Pull Output Power Contours (dBm)

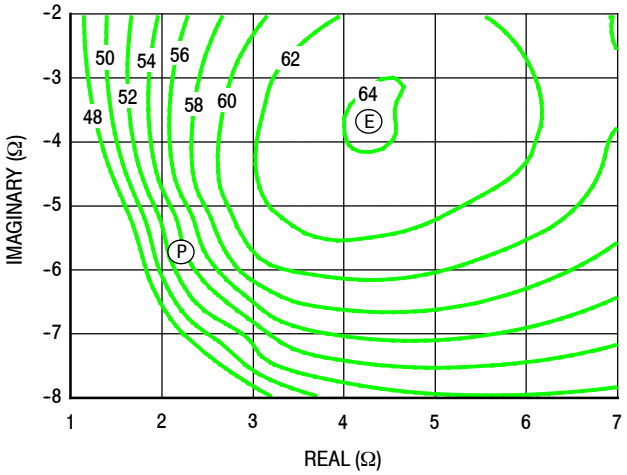


Figure 11. P1dB Load Pull Efficiency Contours (%)

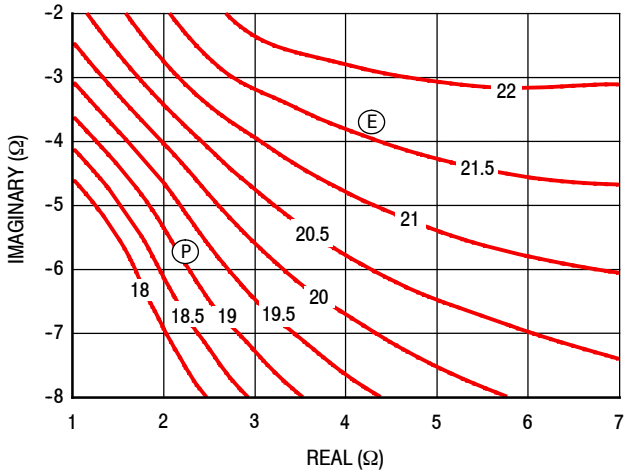


Figure 12. P1dB Load Pull Gain Contours (dB)

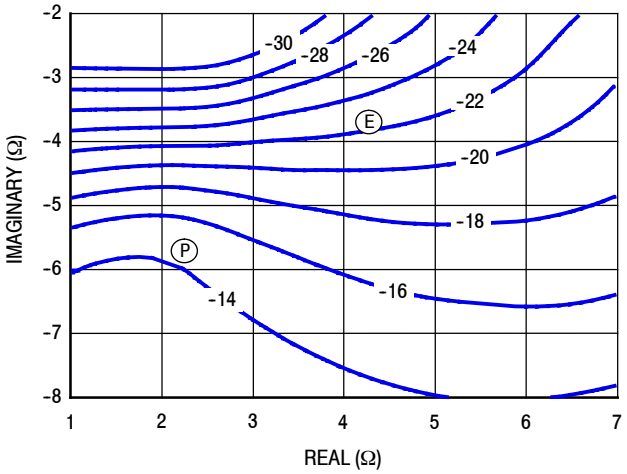


Figure 13. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL LOAD PULL CONTOURS — 1960 MHz

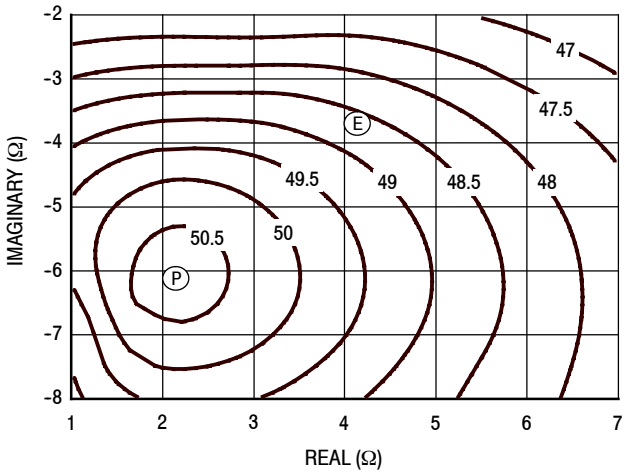


Figure 14. P3dB Load Pull Output Power Contours (dBm)

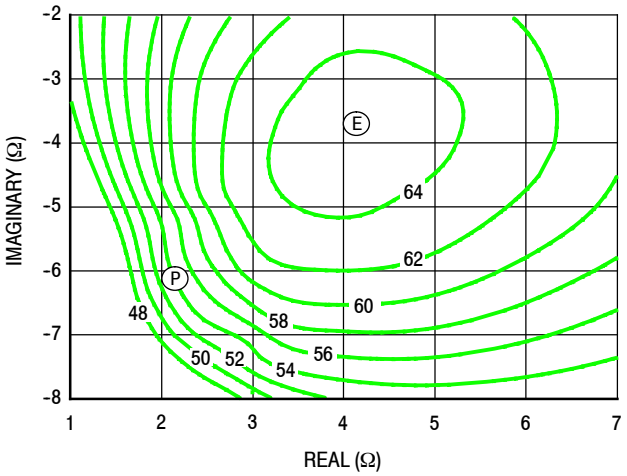


Figure 15. P3dB Load Pull Efficiency Contours (%)

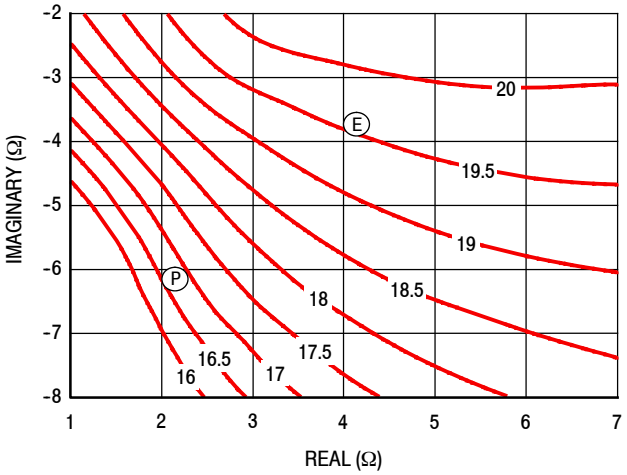


Figure 16. P3dB Load Pull Gain Contours (dB)

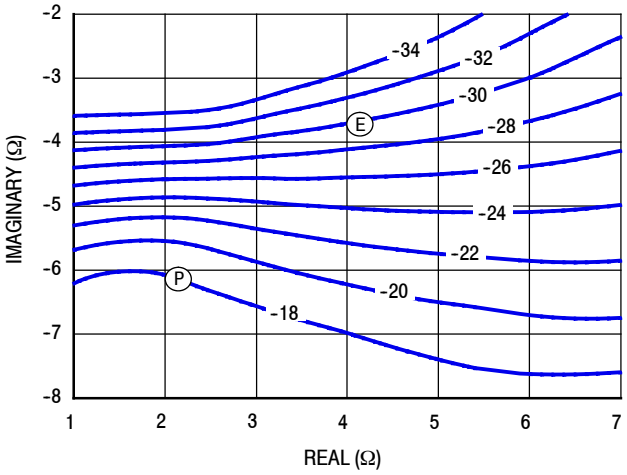


Figure 17. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

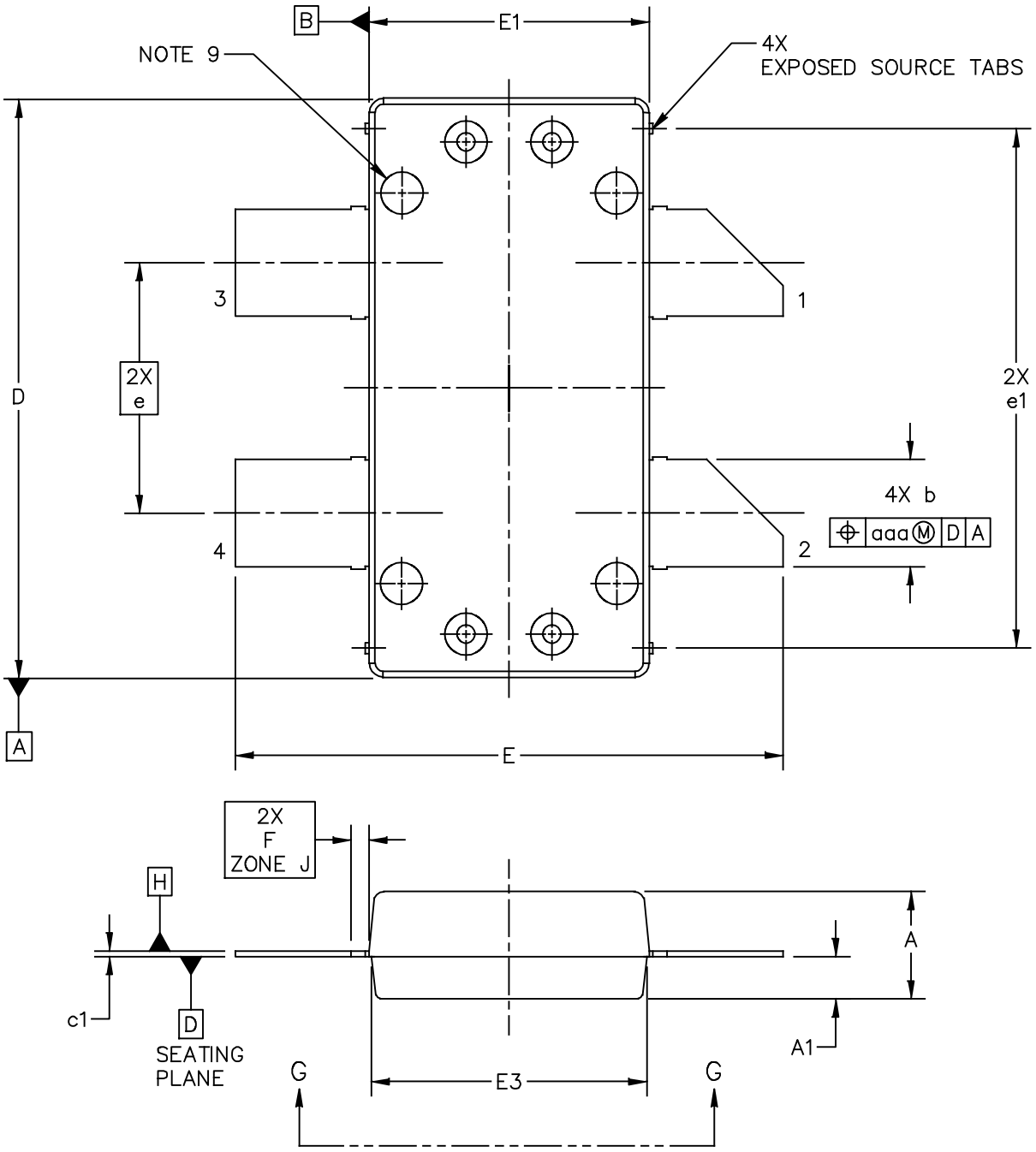
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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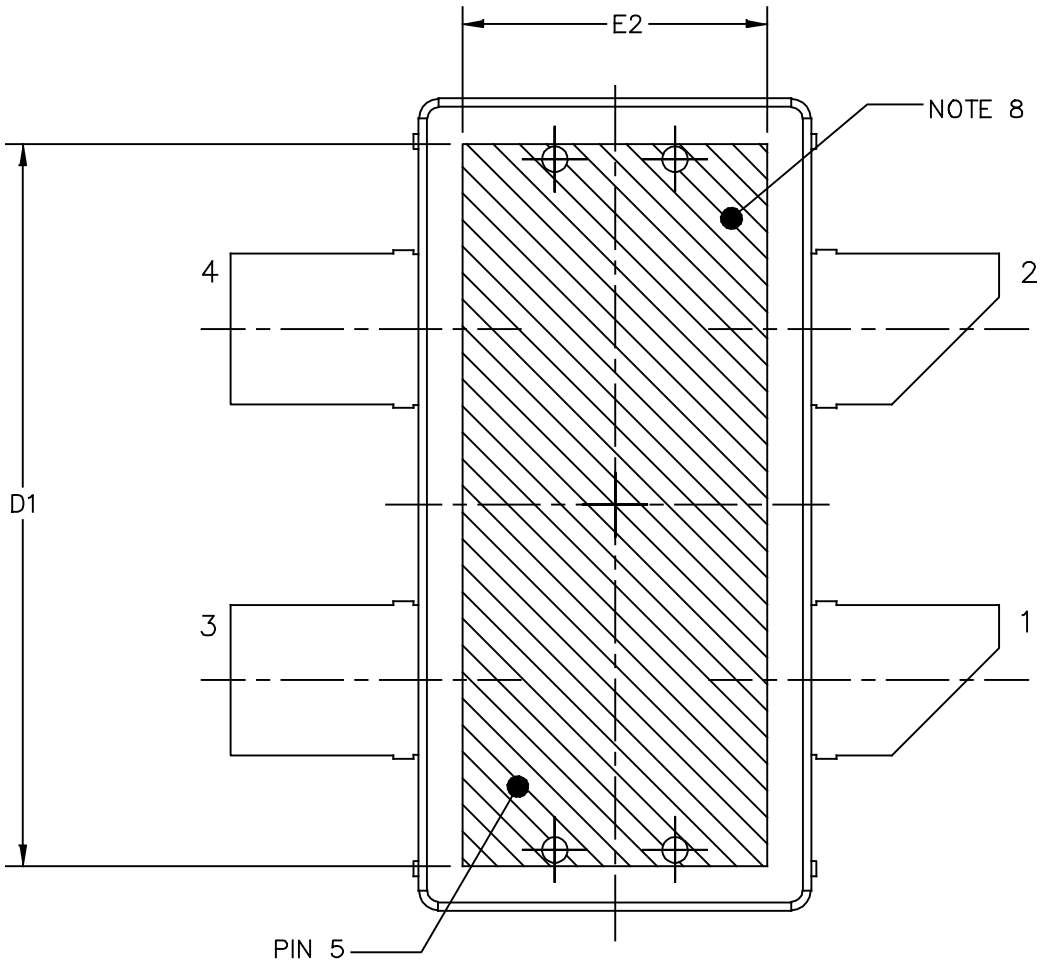
	CASE NUMBER: 2023–02	10 FEB 2010
	STANDARD: NON–JEDEC	



BOTTOM VIEW
VIEW G–G

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	CASE NUMBER: 2023–02	10 FEB 2010
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION A1 APPLIES WITHIN ZONE "J" ONLY.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

9. DIMPLED HOLE REPRESENTS INPUT SIDE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	0.148	.152	3.76	3.86	b	.147	.153	3.73	3.89
A1	.059	.065	1.50	1.65	c1	.007	.011	0.18	0.28
D	.808	.812	20.52	20.62	e	.350 BSC		8.89 BSC	
D1	.720	----	18.29	----	e1	.721	.729	18.31	18.52
E	.762	.770	19.36	19.56					
E1	.390	.394	9.91	10.01	aaa	.004		0.10	
E2	.306	----	7.77	----					
E3	.383	.387	9.72	9.83					
F	.025 BSC		0.635 BSC						

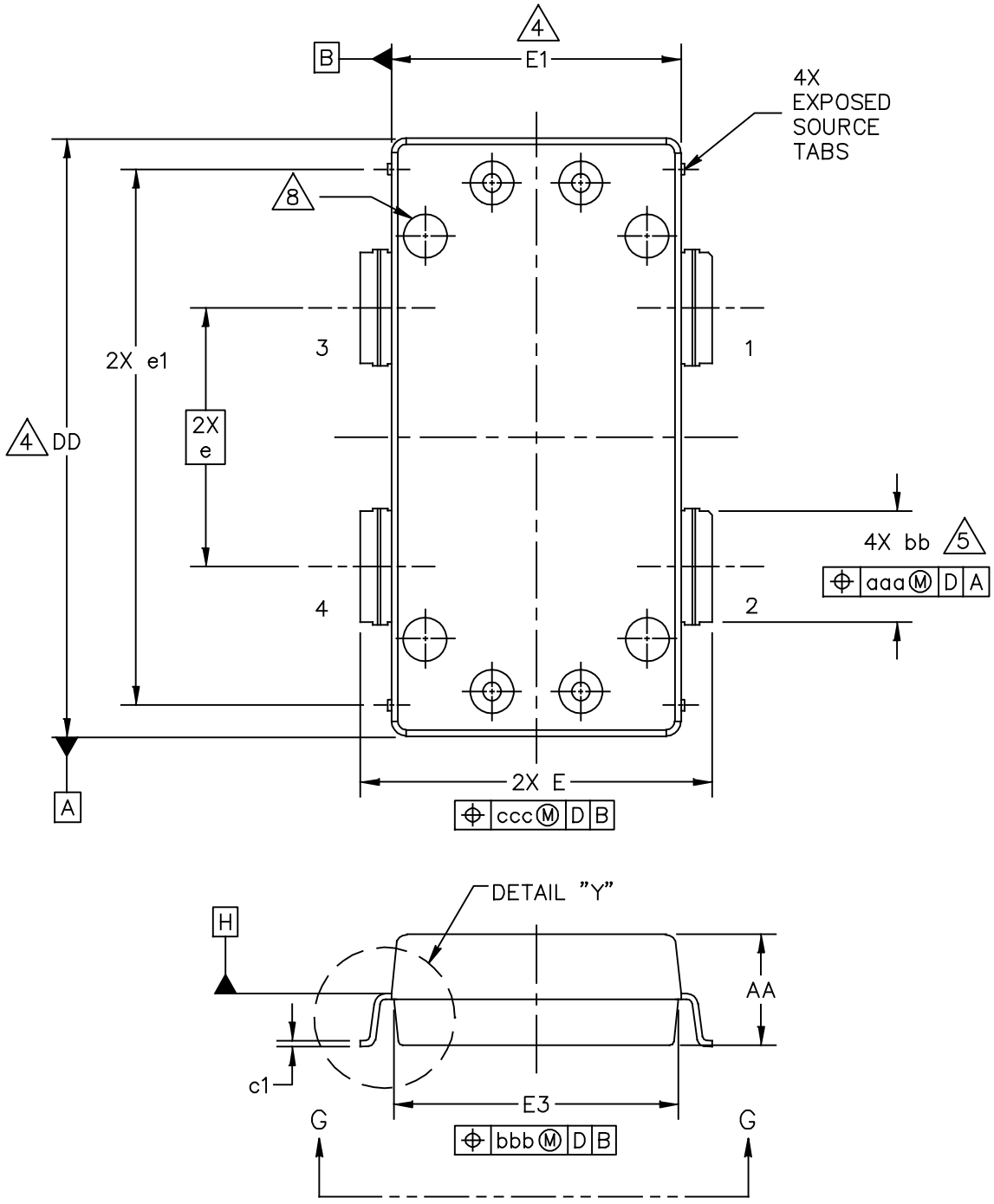
MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE: OM780–4
STRAIGHT LEAD

DOCUMENT NO: 98ASA10833D | REV: A

CASE NUMBER: 2023–02 | 10 FEB 2010

STANDARD: NON–JEDEC



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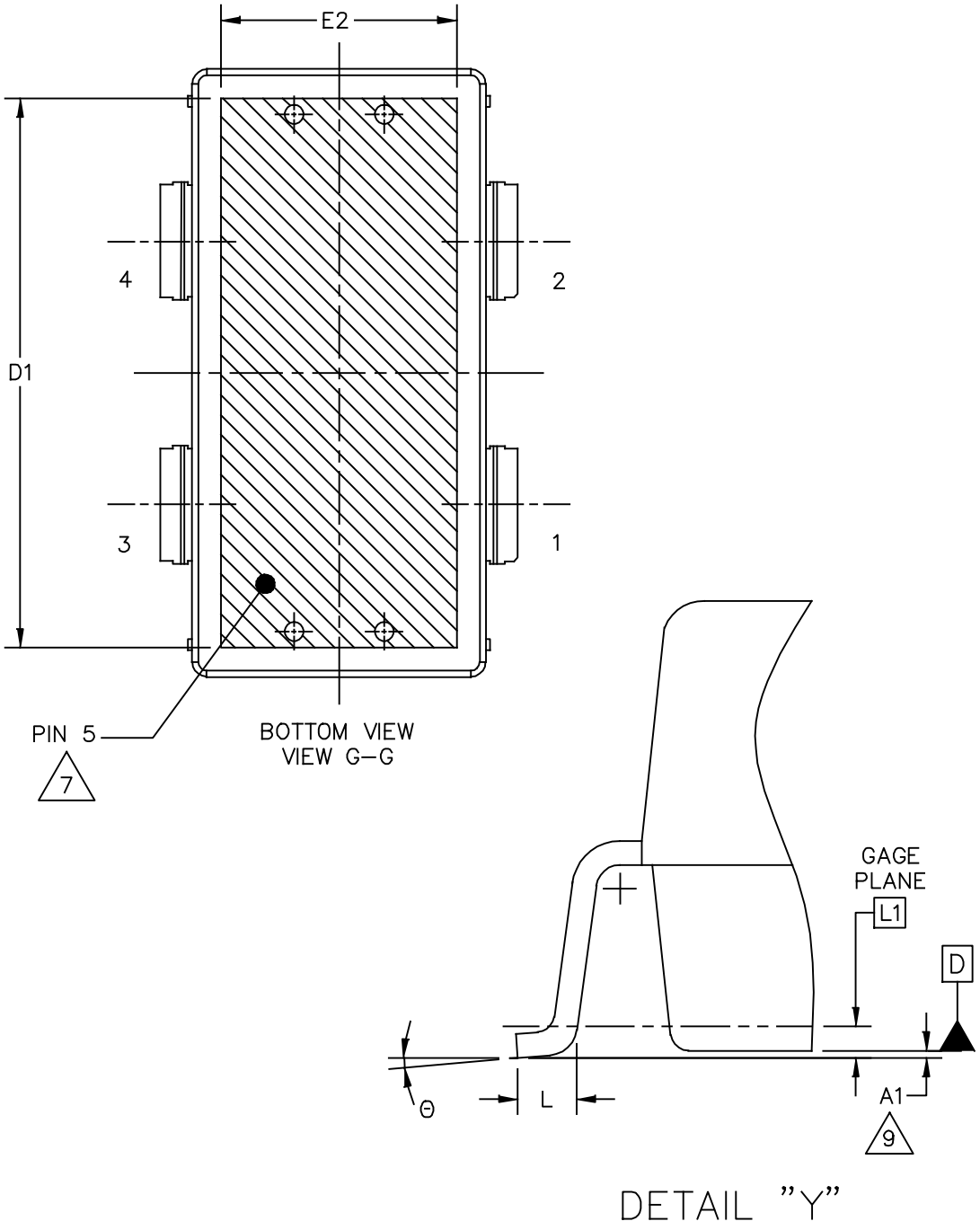

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NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

8. DIMPLED HOLE REPRESENTS INPUT SIDE.

9. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM D. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.148	.152	3.76	3.86	bb	.147	.153	3.73	3.89
A1	–.002	.002	–0.05	0.05	c1	.007	.011	0.18	0.28
DD	.808	.812	20.52	20.62	e	0.350 BSC		8.89 BSC	
D1	.720	----	18.29	----	e1	.721	.729	18.31	18.52
E	.470	.482	11.94	12.24	Θ	0°	8°	0°	8°
E1	.390	.394	9.91	10.01	aaa	.004		0.10	
E2	.306	----	7.77	----	bbb	.006		0.15	
E3	.383	.387	9.73	9.83	ccc	.010		0.25	
L	.018	.024	0.46	0.61					
L1	.010 BSC		0.25 BSC						

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2013	• Initial Release of Data Sheet
1	Jan. 2014	• Added part number AFT20P140–4WGNR3, p. 1 • Added OM780G–4L isometric, p. 1, and Mechanical Outline, pp. 13–15

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