AIF12W300

600 Watts

Full Brick DC-DC Converter

Total Power: 600 Watts
Input Voltage: 250-420 Vdc
# of Outputs: Single

RoHS 6/6 COMPLIANT

Special Features

- 600W continuous power at 100°C baseplate temperature
- 108W/in³ (6.6W/cm³)
- High efficiency – 90% typical
- Low output ripple and noise
- Positive and Negative Enable Function
- Excellent transient response
- OVP, OCP, V Adj control with ALP™ analog mode linear control, or through I²C bus for digital mode control.
- Paralleable with accurate current sharing
- Two years warranty

Safety

UL cUL	60950 Recognized
TUV	EN60950 Licensed

Product Descriptions

The AIF12W300 is an isolated, single output DC to DC converter module, providing up to 600W output with a maximum baseplate operating temperature of 100°C with no derating. The AIF features full safety isolated low voltage secondary side control and Artesyn Linear Programming (ALP™) or through I²C bus for convenient adjustment of the module's parameters.

ARTESYN™
EMBEDDED TECHNOLOGIES

Model Numbers

Standard	Output Voltage	Minimum Load	Maximum Load Current	Maximum Load Power
AIF12W300-L	48.0Vdc	0A	12.5A	600W
AIF12W300N-L	48.0Vdc	0A	12.5A	600W
AIF12W300-NTL	48.0Vdc	0A	12.5A	600W
AIF12W300N-NTL	48.0Vdc	0A	12.5A	600W

Part Number Scheme

AIF	Output Current	Output Voltage	Vin	Enable	-	Suffix	Suffix
	12	W	300	N or No suffix		NT	-L or L
"AIF" = Artesyn Integrated Full Brick Series	12 = 12.5A	W = 48Vdc	300Vdc	"N" = Negative Logic Enable; No suffix = Positive Logic Enable		"-NT" = Non-thread mounting hole	"-L" or "L" = RoHS Compliance

Options

None

Electrical Specifications

Absolute Maximum Ratings

Stress in excess of those listed in the "Absolute Maximum Ratings" can cause permanent damage to the power supply. These are stress ratings only and functional operation of the unit is not implied at these or any other conditions above those given in the operational sections of this TRN. Exposure to any absolute maximum rated condition for extended periods can adversely affect the power supply's reliability.

Table 1. Absolute Maximum Ratings:

Parameter	Model	Symbol	Min	Typ	Max	Unit
Input Voltage: DC Continuous operation DC Transient (100ms)	 All models All models	 $V_{IN,DC}$ $V_{IN,trans}$	 250 -	 300 -	 420 500	 Vdc Vdc
Maximum Output Power	All models	$P_{O,max}$	-	-	600	W
Isolation Voltage Input to output	 All models		 2700	 -	 -	 Vdc
Operating Baseplate Temperature	All models	TC	-20	-	+100	^{O}C
Start up Baseplate Temperature	All models		-40	-	+100	^{O}C
Storage Temperature	All models	T_{STG}	-55	-	+125	^{O}C
Operating Humidity (non-condensing)	All models		15	-	95	%
MTBF	All models		0.3	-	-	10^6 Hr
Altitude Operating Storage	 All models All models		 - -	 - -	 10,000 30,000	 feet feet

Input Specifications

Table 2. Input Specifications:

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Continuous Operating Input Voltage	All	$V_{IN,DC}$	250	300	420	Vdc
Transient (100ms) Input Voltage	All	$V_{IN, trans}$	-	-	500	Vdc
Input under Voltage Power On Power Off	 I_O = 10% $I_{O,max}$ I_O = 10% $I_{O,max}$	 $V_{IN,DC}$ $V_{IN,DC}$	 205 175	 - -	 245 215	 Vdc Vdc
Input Current [1]	$V_{IN} = V_{IN,min}$, $I_O = I_{O,max}$ $V_O = V_{O,nom}$	$I_{IN,max}$	-	-	2.8	A
	V_{IN} = 0 to $V_{IN,max}$, I_O = $I_{O,max}$, $V_O = V_{O,nom}$	$I_{IN,max}$	-	-	3.4	A
Input Reflected Ripple Current [2]	5Hz to 20MHz; 12uH source impedance; T_{amb} = 25°C	I_{IN}	-	30	-	mA_{PK-PK}
Inrush Transient [3]	All	I^2t	-	-	2.8	A^2s
Break Regulation	All		-	215	245	V
CLK IN Frequency Voltage Level	 All Internal ac coupled		 720 3.3	 800 -	 880 5.5	 KHz V_{PK-PK}
Enable Positive Logic Low Logic - Module Off High Logic - Module On	 All Enable pin opened	 V_{EN} V_{EN}	 0 2	 - -	 0.7 10	 V V
Enable Low Sourced Current	V_{enable} = 0.7V		-	-	150	uA
Enable Turn-On Delay	All		-	-	380	mS
No load input power	All		-	-	5	W
Turn-On Time	$I_O = I_{O,max}$; V_O within 1%; No external output capacitance		-	-	650	mS
Efficiency	$V_I = V_{IN,nom}$, $I_O = I_{O,max}$ T_{amb} = 25°C		90	91.8	-	%
Input Capacitance	All		-	0.6	0.8	uF
No Load Input Power	V_O=48V, I_O= 0A	I_{IN,no_load}	-	-	5.0	W
Isolation – Input to Output	All		2700	-	-	Vdc

Note 1 - An input line fuse is recommended for use (e.g. Littelfuse type, 10A 250V FB).
Note 2 - External input capacitance required. See Figure 12 for the Input Reflected-Ripple Current Test Setup. Measure input reflected- ripple current with a simulated source inductance of 12uH.
Note 3 - See Figure 13 for the Inrush Current Test Setup. Measure input inrush current with a simulated source inductance of 12uH and input bulk capacitor of 68uF/450Vmin must always be added.

Output Specifications

Table 3. Output Specifications:

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Output Voltage Setpoint	$V_{IN,min}$ to $V_{IN,max}$: I_O = $I_{O,max}$; T_{amb} = 25^{O}C	$V_{O,set}$	47.52	48	48.48	V
Output Line Regulation:	All		-	-	0.2	%
Output Load Regulation:	All		-	-	0.2	%
Output Voltage Adjust [1, 2] V_ADJ = 0V V_ADJ = 2V	 All All		 78 118	 80 120	 82 122	 %V_O %V_O
Output Ripple and Noise (Peak-to-Peak)	5 Hz to 20MHz		-	110	480	mV_{PK-PK}
External Load Capacitance	All		-	-	2000	uF
Switching Frequency	All		360	400	440	KHz
Output Power	All	Po	-	-	600	W
Output Current	All	Io	0	-	12.5	A
Output Current-limit Inception (Hiccup)	V_O = 97% V_{O,set_nom}	Io	105	-	120	%$I_{O,max}$
Output Current Limit Adjust [2]	All		20	-	100	%$I_{O,max}$
Output Current Monitor I_{mon} at $I_{O,max}$ Monitored I_O Range I_{mon} Compliance Voltage	 All All All		 0.9 20 -	 1.0 - -	 1.1 100 5.0	 mA %$I_{O,max}$ V
Current Share Accuracy [3]	Cshare connected together, $I_O \geq 80\%I_{O,max}$		-	±3	±5	%I_{avg}
Number of Parallel Unit	All		-	-	10	pcs
Internal Temperature Monitor Temperature Coefficient Source Impedance	 All All		 9.8 -	 10.0 1.0	 10.2 -	 mV/^{O}C Kohm
Temperature Coefficient	T_C = -40^{O}C to 100^{O}C		-	-	0.02	%V_O/^{O}C

Note 1 - The combination of remote sense and trim do not exceed a total of 0.5V.
Note 2 - Refer to Basic Operation and Features section.
Note 3 - See Figure 10 for modules in parallel connection.

Output Specifications

Table 3. Output Specifications, con't:

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Step-load Excursion Output Overshoot Output Undershoot	25% to 75% load change @ 1A/uS, recovery to 1%V_O; V_{IN} = $V_{IN,nom}$; T_{amb} = 25^{O}C		 - -	 - -	 2.4 2.4	 V V
Step Load Response	25% to 75% load change @ 1A/uS, recovery to 1%V_O; V_I = $V_{IN,nom}$; T_{amb} = 25^{O}C; measure from end of transition		-	-	250	uS
Turn-on Output Voltage Overshoot	I_O = $I_{O,max}$; T_{amb} = 25^{O}C; no external output capacitor		-	3	5	%V_O
Short Circuit Current (Hiccup Mode)	All		-	-	150	%$I_{O,max}$
CLK OUT Frequency Voltage Level No. of Fan Out Unit	 All Internal ac coupled All		 720 3.3 -	 800 - -	 880 5.5 2	 KHz V_{PK-PK} pcs
Turn-Off Negative Voltage	Resistive loading, wire length of 10cm		-	-	-0.7	V
AUX Output Voltage	All		10.5	12	13.5	V
AUX Output Current [4]	All		-	-	10	mA
AUX Output Voltage Ripple and Noise	All		-	-	600	mV
Power Good Monitor / Identification PG/ID Low	 Power Fault, $I_{sink} \leq$ 10mA		 -	 -	 0.2	 V
PG/ID Internal Pull-up Resistance to V_O	All		46	47	48	Kohm

Note 4 - The AUX output pin does not allow for any short circuit and OCP testing.

AIF12W300 Performance Curves

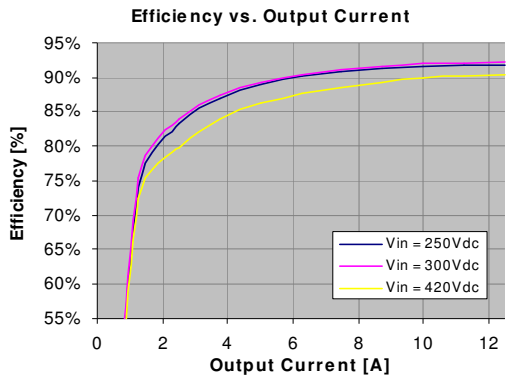


Figure 1: AIF12W300 Efficiency Curves
Full Load: Io = 12.5A, Ambient Temperature (T_{amb}) = 25°C

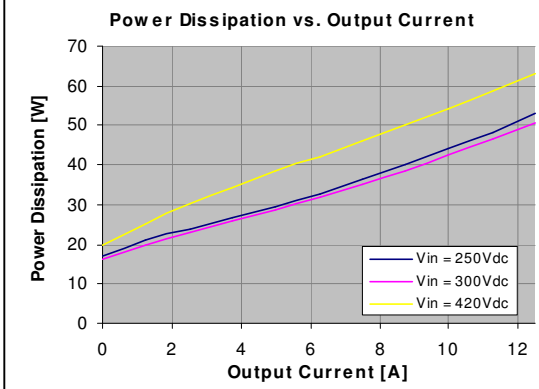


Figure 2: AIF12W300 Power Dissipation Curves
Full Load: Io = 12.5A, Ambient Temperature (T_{amb}) = 25°C

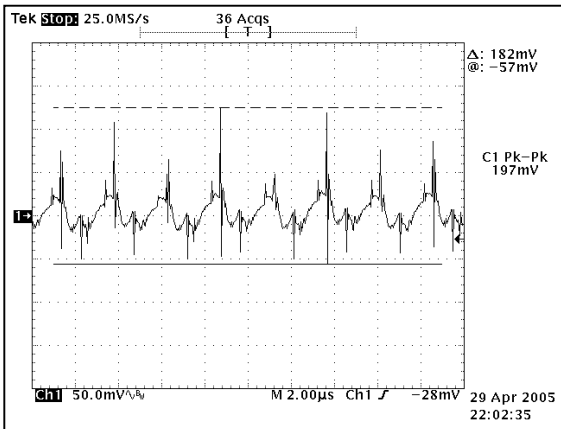


Figure 3: AIF12W300 Output Ripple Waveform - Vin = 300Vdc
Full Load: Io = 12.5A, Ambient Temperature (T_{amb}) = 25°C
Ch 1: Vo

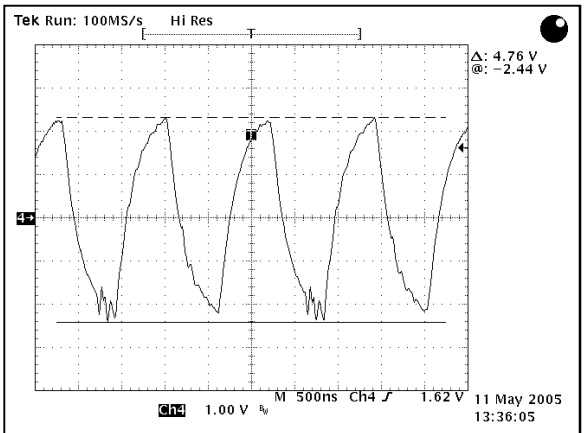


Figure 4: AIF12W300 Clock Out Waveform - Vin = 300Vdc
Full Load: Io = 12.5A, Ambient Temperature (T_{amb}) = 25°C
Ch 4: CLK OUT

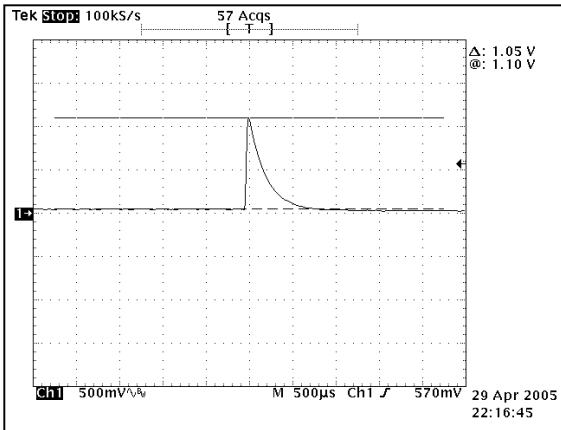


Figure 5: AIF12W300 Transient Response - Vo Deviation (high to low)
75%-50% load change, 0.1A/uS slew rate, Vin = 390Vdc
Ch 1: Vo

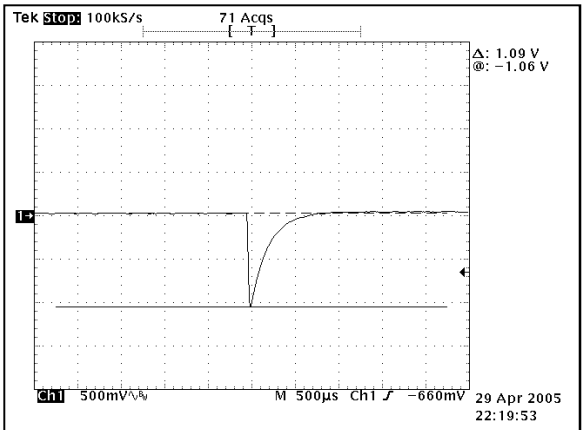


Figure 6: AIF12W300 Transient Response - Vo Deviation (low to high)
50%-75% load change, 0.1A/uS slew rate, Vin = 390Vdc
Ch 1: Vo

AIF12W300 Performance Curves

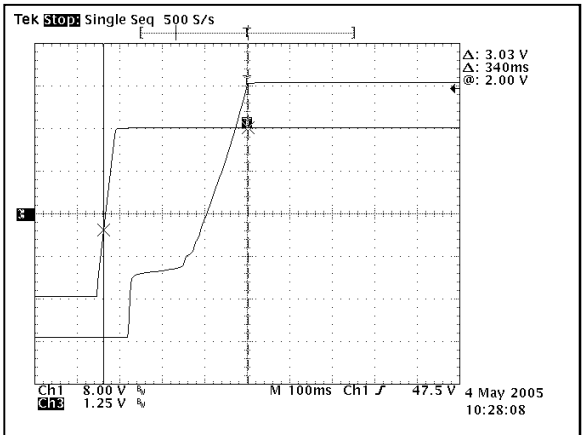


Figure 7: AIF12W300 Turn-on Time (Enable to Output)
Full Load: Io = 12.5A, Ambient Temperature (T_{amb}) = 25°C
Ch 1: V_enable Ch 2: Vo

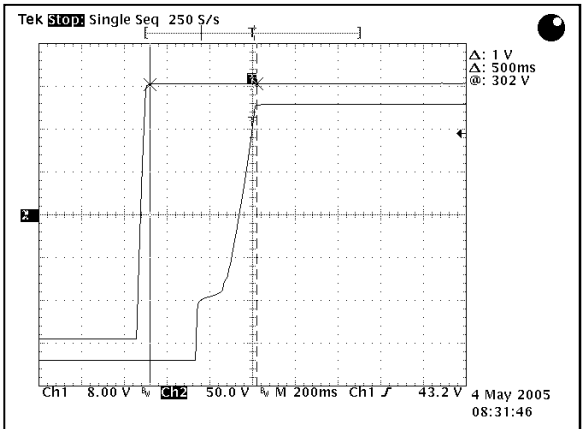


Figure 8: AIF12W300 Turn-on Time (Input to Output)
Full Load: Io = 12.5A, Ambient Temperature (T_{amb}) = 25°C
Ch 1: Vin Ch 2: Vo

Protection Function Specification

Input Fusing

AIF12W300 has no internal fuse, so input live / neutral fuses must always be used. 10A / 250Vdc rated fuses are recommended be fitted at the module's input to achieve safety regulations.

Over Voltage Protection (OVP)

The AIF12W300 power supply latches off during output overvoltage with the DC line recycled to reset the latch.

Parameter	Min	Nom	Max	Unit
V_O Output Over Voltage Protection Level	120	125	130	%Vo
V_O Output Over Voltage Protection Adjust	120	/	150	%Vo

Over Current Protection (OCP)

The AIF12W300 power supply includes internal current limit circuitry to prevent damage in the event of overload. In the event of overloads, the output voltage can deviate from the regulation band but recovery is automatic when the load is reduced to within specified limits.

Parameter	Min	Nom	Max	Unit
Over Current Protection Level (V_O dropped to 97% of $V_{O,nom}$)	105	110	115	$\%I_{O,max}$

Over Temperature Protection (OTP)

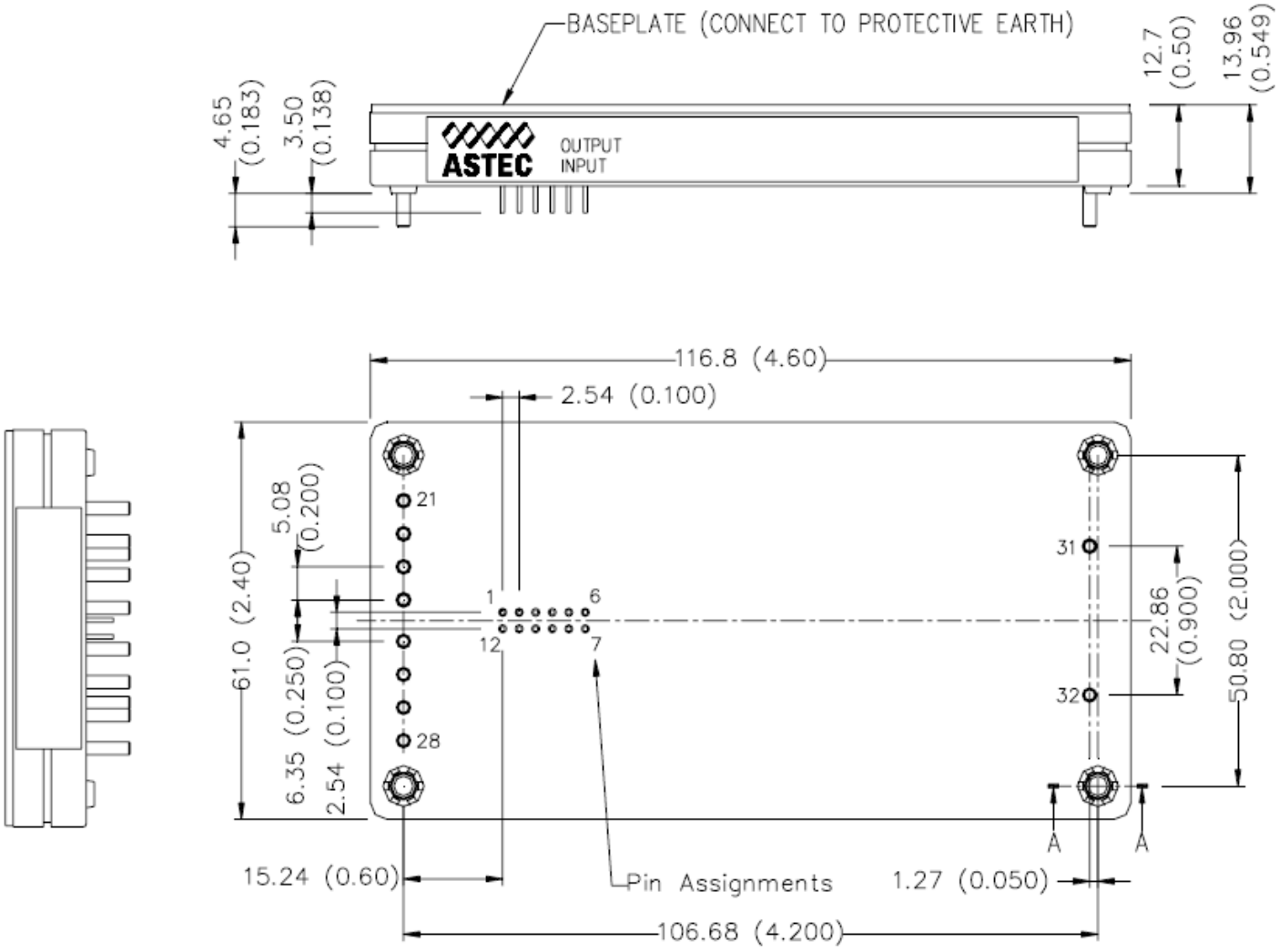
The power supply is internally protected against over temperature conditions. When the OTP circuit is activated, the power supply will latch off, requiring DC power or recycling to restart the power supply.

Parameter	Min	Nom	Max	Unit
Over Temperature Protection Trip Point (Baseplate temperature)	105	/	120	^{O}C

Mechanical Specifications

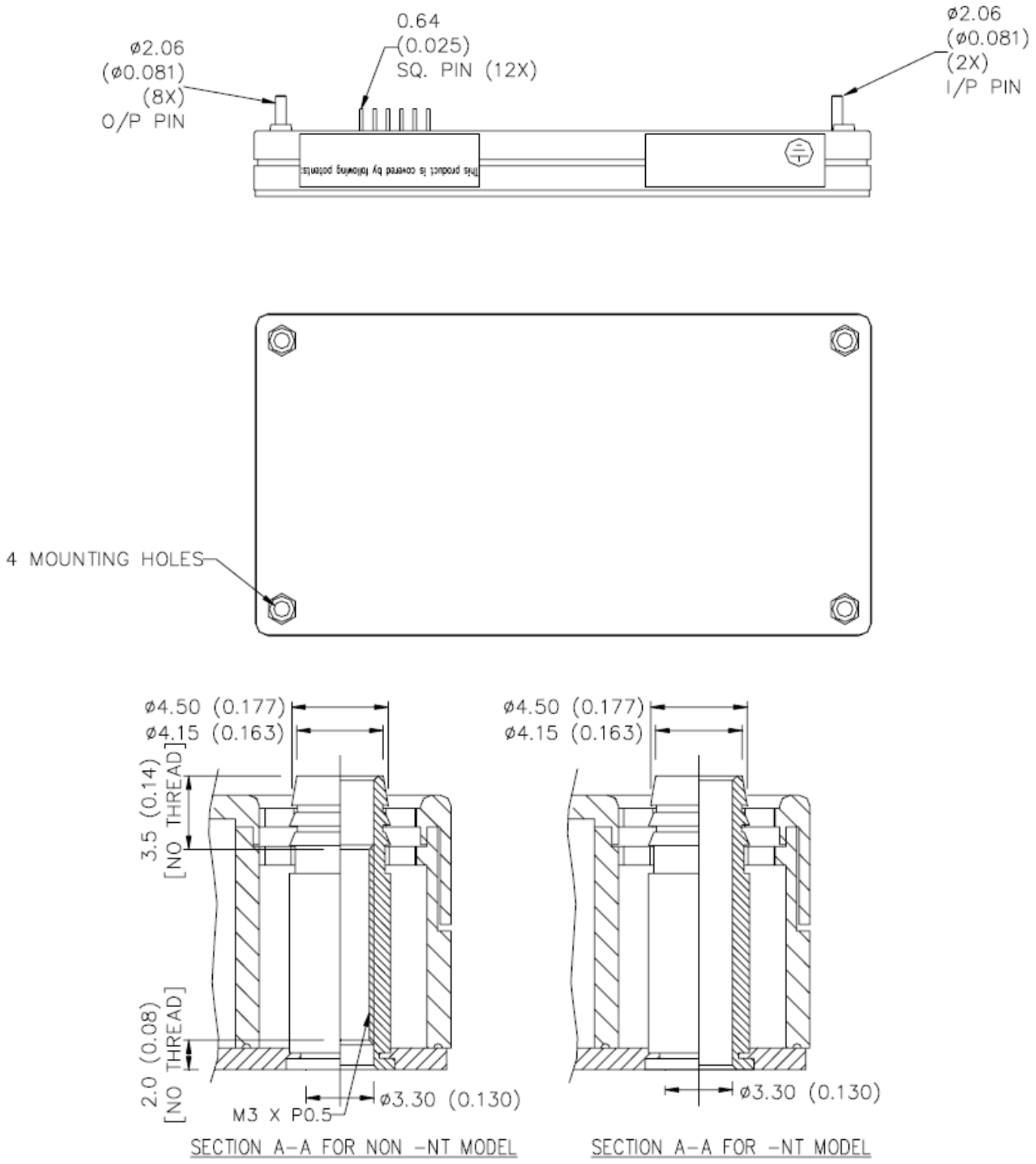
Unit: mm (inch)

Mechanical Outlines



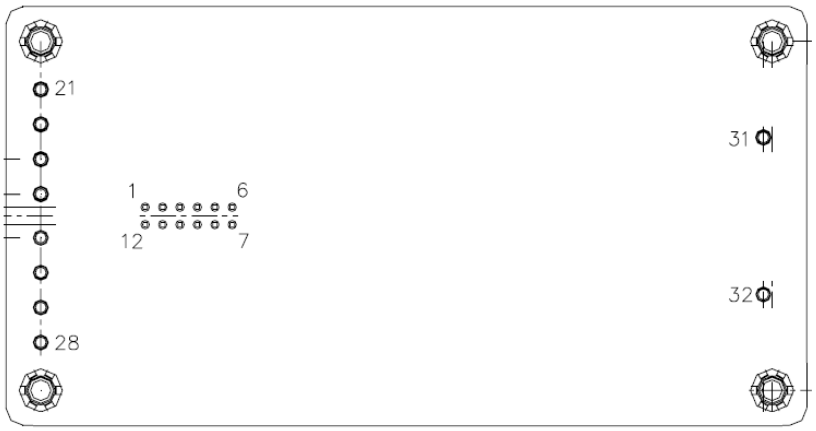
Mechanical Outlines

Unit: mm (inch)



Connector Definitions

Parameter	Device	Symbol	Min	Typ	Max	Unit
Dimension	All	L	-	4.60 [116.8]	-	in [mm]
		W	-	2.40 [61.0]	-	in [mm]
		H	-	0.50 [12.7]	-	in [mm]



Pin Assignments		
Input	**Output**	**Control Pins**
31. Positive	21. Positive	1. AUX
32. Negative	22. Positive	2. TEMP MON
	23. Positive	3. C MON
	24. Positive	4. C SHARE
	25. Negative	5. CLK OUT
	26. Negative	6. CLK IN
	27. Negative	7. PG / ID
	28. Negative	8. CLIM ADJ / I^2C CLK
		9. OVP ADJ / DCS
		10. V ADJ / I^2C DATA
		11. ENABLE
		12. -SENSE

Weight

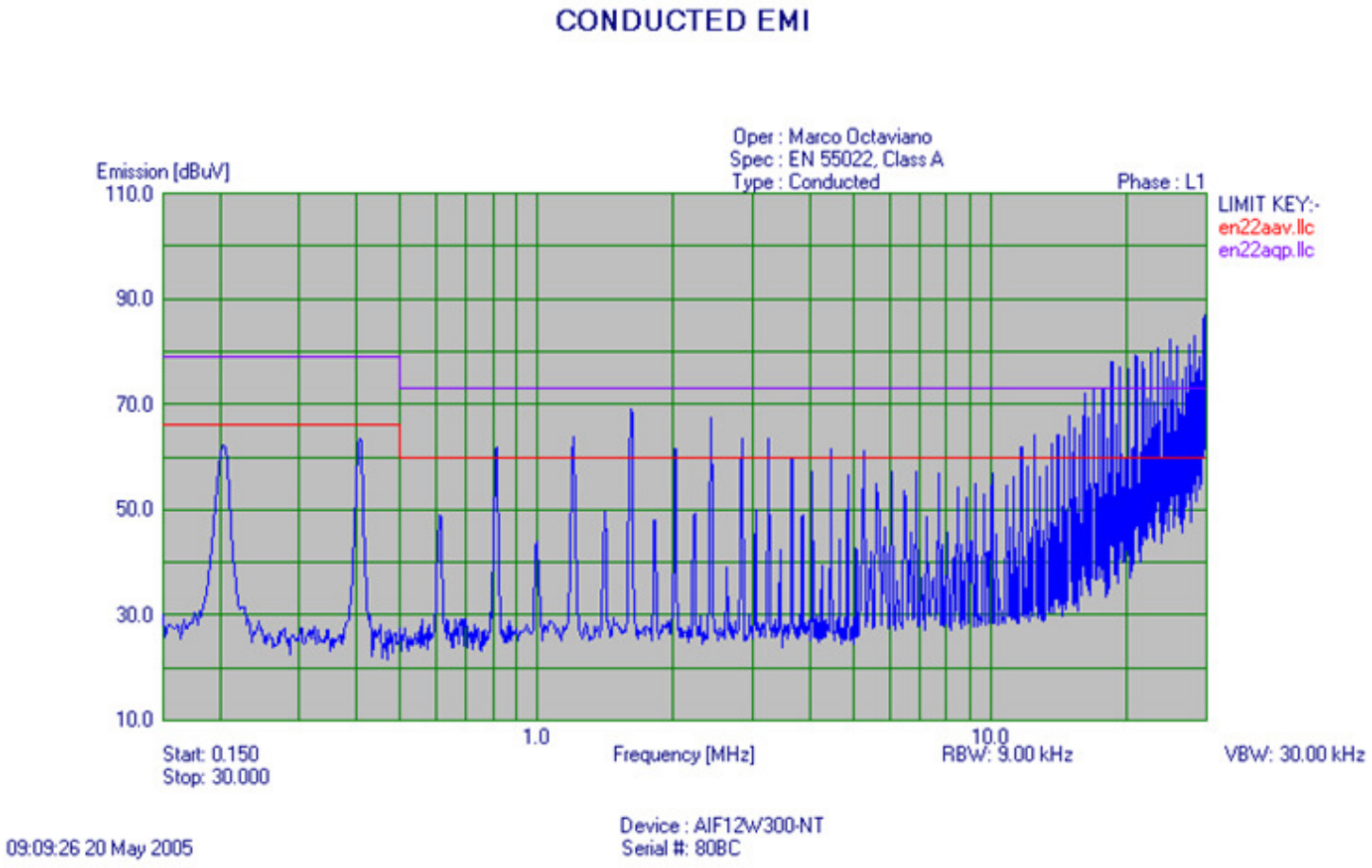
The AIF12W300 series weight is 0.55lbs/250g typically.

Environmental Specifications

EMI Emissions

The AIF12W300 has been designed to comply with the Class A limits of EMI requirements of EN55022 (FCC Part 15) and CISPR 22 for emissions and relevant sections of EN61000 (IEC 61000) for immunity. This is a system test and not a component level test. An additional input filter is needed in order to pass this test. Also the unit is enclosed inside a metal box, tested at 600W using resistive load with cooling fan.

Conducted Emissions



Vibration

Endurance random vibration (non-operating)

The AIF12W300 power supply will pass the following random vibration test at the following non-operating condition:

Frequency range	10 – 200Hz; 200 – 2000Hz
PSD	$0.01g^2$ / Hz; $0.003g^2$ / Hz
Acceleration	2.5g RMS (typical level)
Duration	20 mins per axis

Endurance random vibration (operating)

The AIF12W300 power supply will pass the following random vibration test with the unit at operating mode at nominal lines and full load condition, with POK monitored:

Frequency range	10 – 500Hz
PSD	$0.002g^2$/ Hz flat
Acceleration	1g RMS
Duration	20 mins per axis

Shock

Shock (non-operating)

The AIF12W300 power supply will pass the following shock specifications at non-operating test condition:

Acceleration	30	g
Duration	6	ms minimum
Pulse	Half-Sine	
Directions	All 6 faces, 3 times in each positive and negative directions	

Shock (operating)

The AIF12W300 power supply will pass the following shock specifications at operating test condition:

Acceleration	4	g
Duration	22	ms minimum
Pulse	Half-Sine	
Directions	All 6 faces, 3 times in each positive and negative directions	

Isolation Specifications

Parameter	Device	Symbol	Min	Typ	Max	Unit
Isolation Capacitance	All		-	300	-	PF
Isolation Resistance	All		10^6	-	-	Ohm

ESD

The AIF12W300 power supply is designed to meet the following Electrostatic Discharge (ESD) test specifications:

Contact discharge	6KV
Air discharge	8KV

The unit will pass performance criteria B as per IEC1000-4-X standards.

Safety Certifications

The AIF12W300 power supply is intended for inclusion in other equipment and the installer must ensure that it is in compliance with all the requirements of the end application. This product is only for inclusion by professional installers within other equipment and must not be operated as a stand alone product.

Safety Certifications for AIF12W300 power supply system:

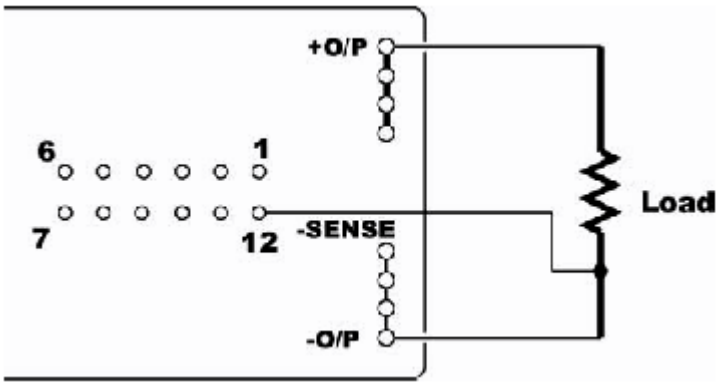
Parameter	Device	Agency	Standard	Cert. No.
Safety Approval	All	CE (LVD+RoHS)	EN 60950-1/A12:2011	14425
		TUV-SUD	EN 60950-1/A12:2011	B 12 10 51485 01153
		UL+CUL	UL60950-1 2nd Ed; CSA C22.2 No. 60950-1-07, 2nd Ed	E186249 V1 S173

Power and Control Signal Descriptions

Remote Sense (-SENSE) - (pin 12)

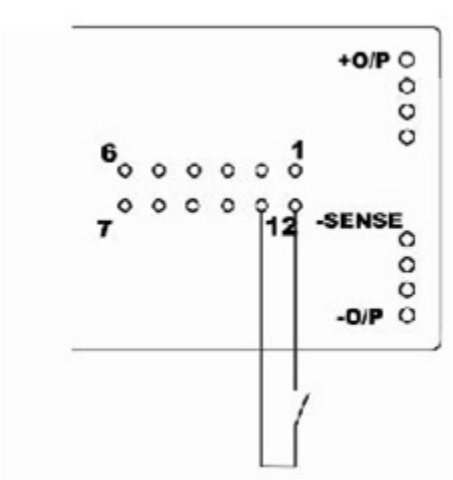
Connect the –SENSE pin 12 of the module directly to the load to allow the module to compensate for the voltage drop across the conductors carrying the load current. If remote sensing is not required (for example if the load is close to the module) the should be connected directly to the module's output pins to ensure accurate regulation.

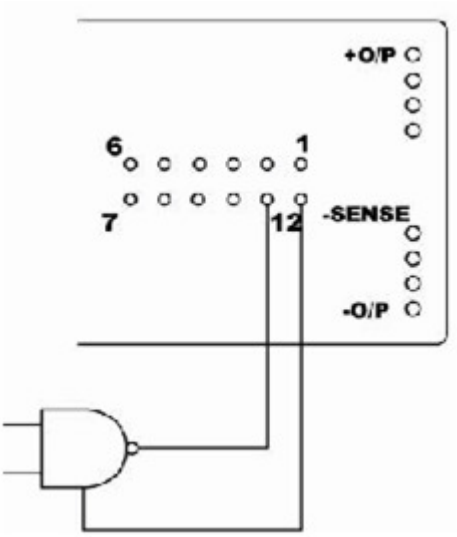
Note: If the sense leads fail open circuit, the module will revert to local sense at the output pins. Incorrect connection of sense leads can damage the module. Remote Sense compensation at nominal V_O only.



Enable Control (ENABLE) - (pin 11)

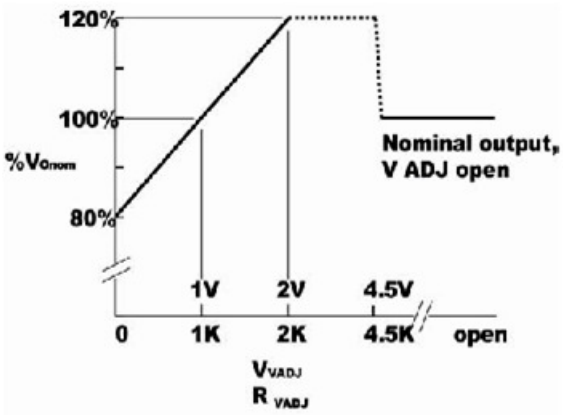
The enable pin is a TTL compatible input used to turn the output of the module on or off. The output is enabled when the ENABLE pin open or driven to a logic high, and disabled when the ENABLE pin is connected to –SENSE or driven to a logic low.

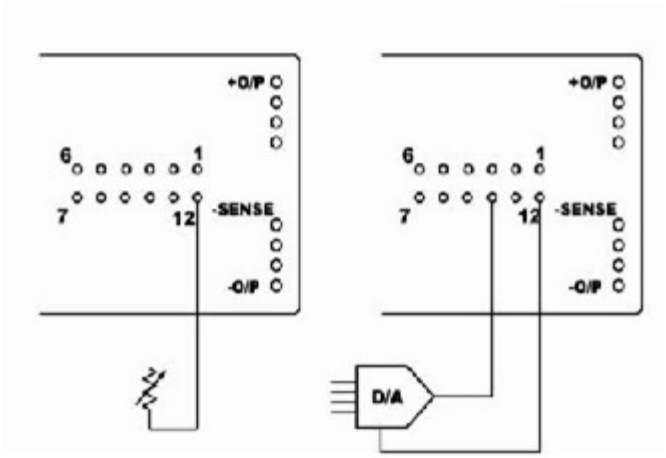




Output Voltage Adjustment (V ADJ) - (pin 10)

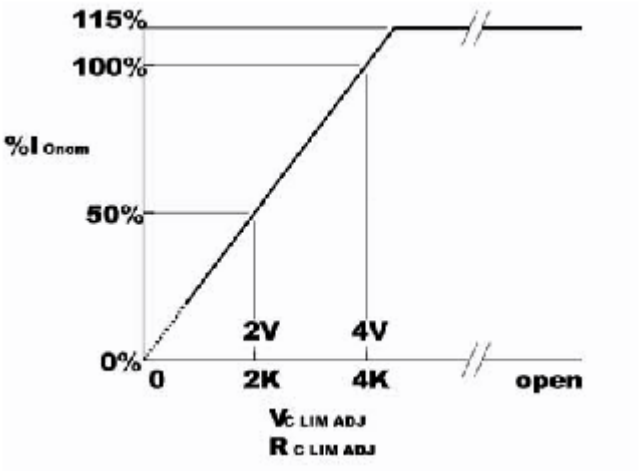
The output voltage of the module can be accurately adjusted from 80% to 120% of the nominal factory set output. Adjustment is carried out using either an external voltage source (0 to 2V, capable of sinking 1mA) or resistor (0 to 2 Kohm) connected between V ADJ and –SENSE.

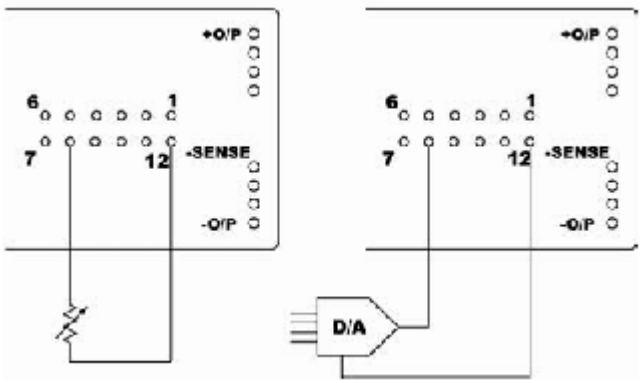




Current Limit Adjustment (CLIM ADJ) - (pin 8)

A constant current limiting circuit protects the module under overload or short circuit conditions. With the CLIM ADJ pin left unconnected, the current limit is factory set to 115% of the module's rated output. Current limit can be adjusted across the range from 20% to 100% using an external voltage source (0.8V to 4V, capable of sinking 1mA) or a resistor (800 Ohm to 4K Ohm) connected between CLIM ADJ and –SENSE.



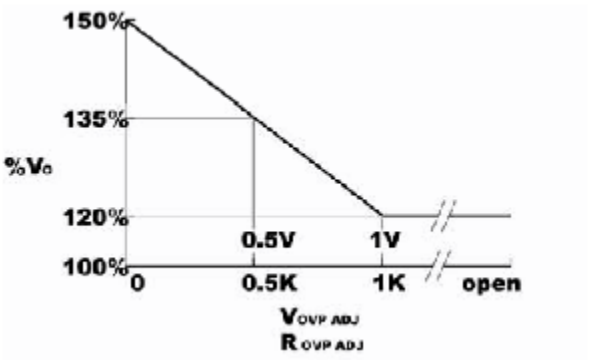


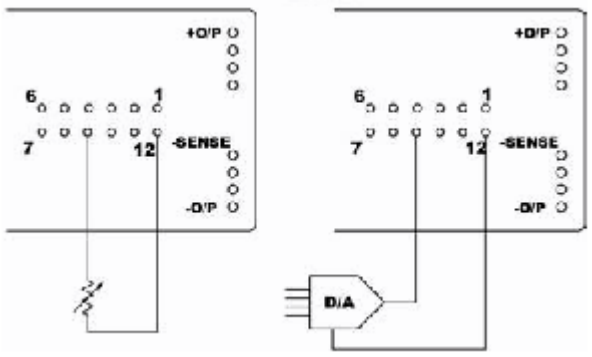
Overvoltage Protection Adjustment (OVP ADJ) - (pin 9)

An independent overvoltage circuit monitors the module's output pins and will shut the module down in the event of an internal or external fault which causes the output voltage to rise above the preset limit. The module is reset by removing and re-applying the input power or toggle the ENABLE OFF/ON.

The overvoltage set point can be adjusted between 20% and 50% above the output voltage (V_O), and automatically track adjustments made to the output voltage using V ADJ.

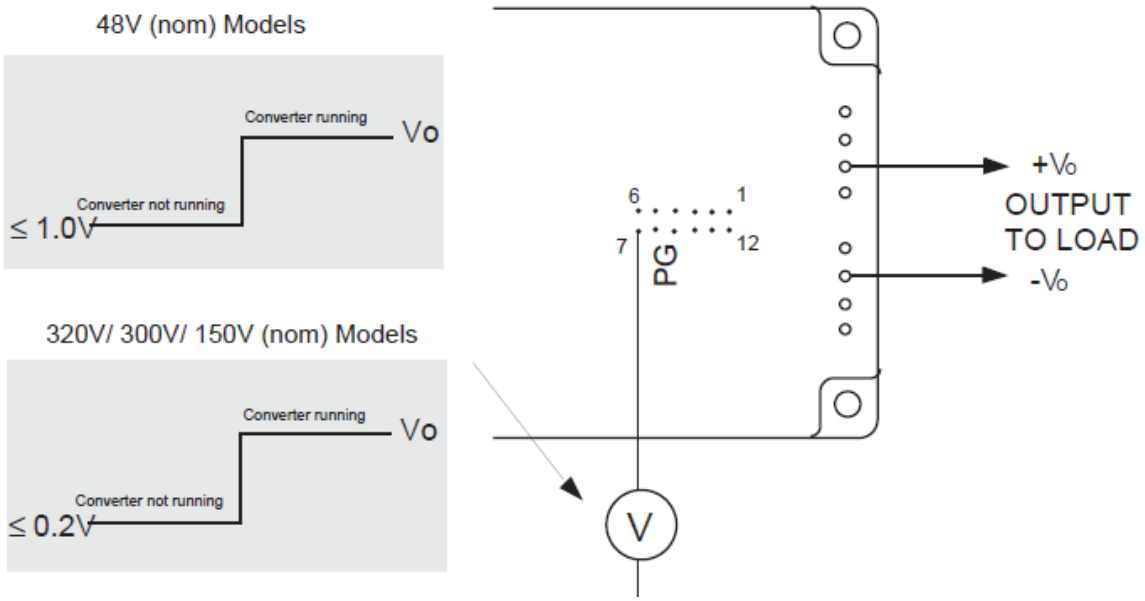
OVP ADJ should be used to increase the OVP margin when the voltage drop between power output pins and remote sense is more than 0.2V.





Power Good / Identification (PG/ID) - (pin 7)

This pin provides an indication that the module's converters are working, and can also be used to identify the factory set output voltage of the module. The PG/ID pin goes high to the level of the output voltage (V_O) to indicate that the module is operating and delivering power. The output goes low if the converters stop operating due to a fault such as an over temperature or over voltage condition. The PG/ID pin will also go low if the module is disabled via the ENABLE pin or under light load condition.

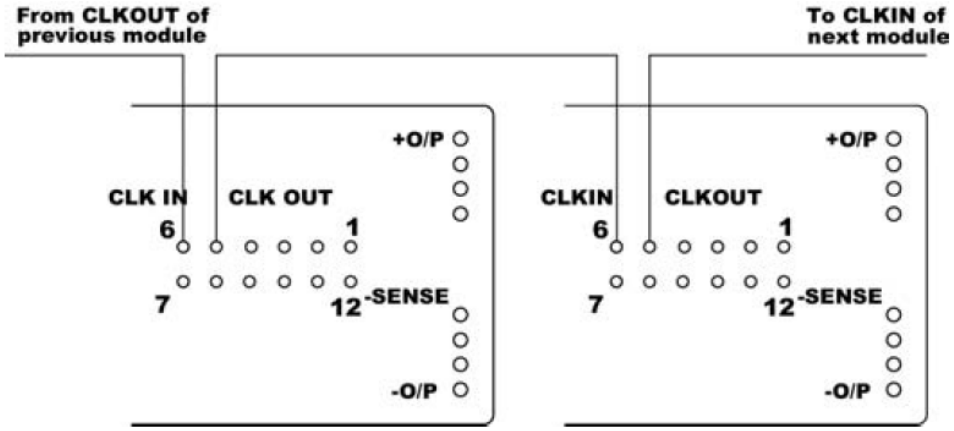


The resistance between the PG/ID pin and the +Vo output of the module can be used to identify the module with no power applied according to the table:

Model Number	Resistance (Kohm)
AIF12W300-L	47
AIF12W300N-L	47
AIF12W300-NTL	47
AIF12W300N-NTL	47

Clock Signals (CLK IN, CLK OUT) - (pin 5)

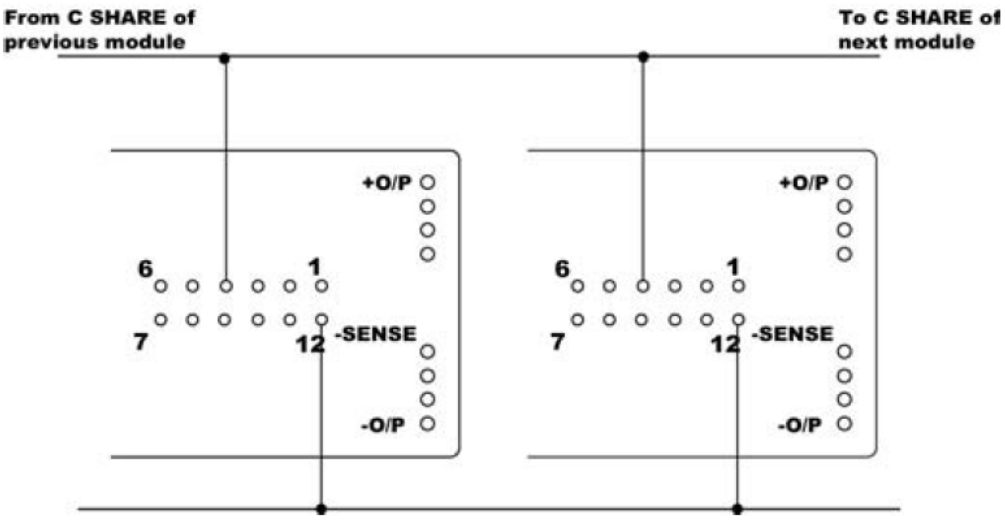
The module's internal clock is accurate and stable over its full operating range and synchronization is not normally required, but it can reduce noise in paralleled systems.
Clock signals can be wired in series (the CLK OUT pin of one module to the CLK IN pin of the next etc) in which case all the modules will be synchronized with the first module in the chain. Alternatively, an external clock signal of $5V_{PK-PK}$ at 800KHz ±10% can be connected to the CLK IN pins of all the modules.
If the clock input to any module fails, the module will automatically switch back to its internal clock and will continue to operate normally. The CLK IN and CLK OUT signals are AC coupled, so any module can clock another module regardless of polarity.



Current Share (C SHARE) - (pin 4)

To ensure that all modules in a parallel system accurately share current, the C SHARE pins on each module should be connected together.
The voltage on the C SHARE pins represents the average load current per module. Each module compares this average with its own current and adjusts its output voltage to correct the error. In this way the module maintains accurate current sharing.

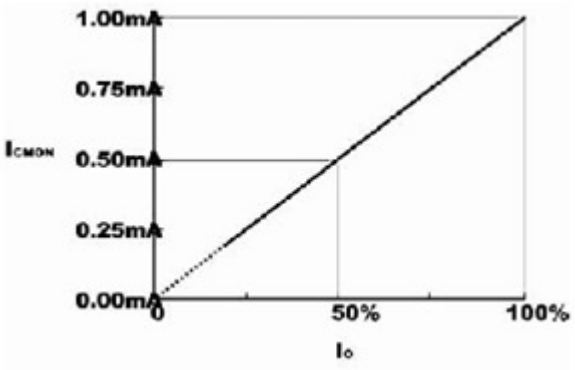
Note: The –SENSE pins of each module must also be connected together to ensure accurate current sharing.

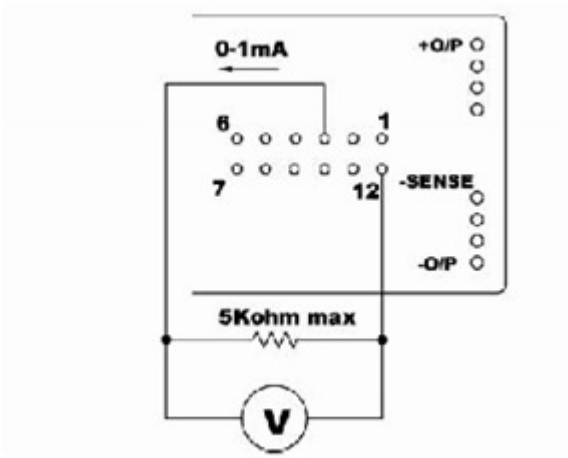


Current Monitoring (C MON) - (pin 3)

The C MON pin provides an indication of the amount of current supplied by the module. The output of the C MON pin is a current source proportional to the output current of the module, where 0.2 mA to 1 mA is 20% to 100% $I_{o,rated}$.

The C MON output can be paralleled with C MON outputs from other modules to indicate the total current supplied in a paralleled system.



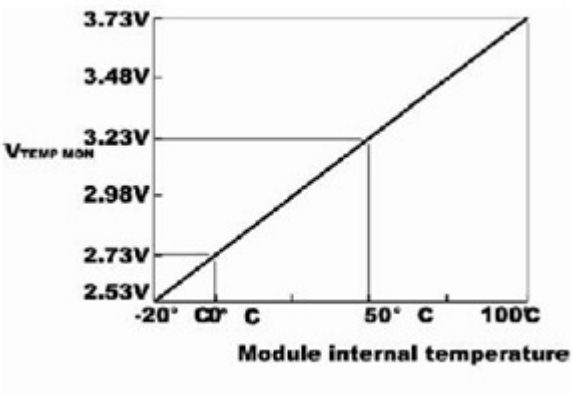


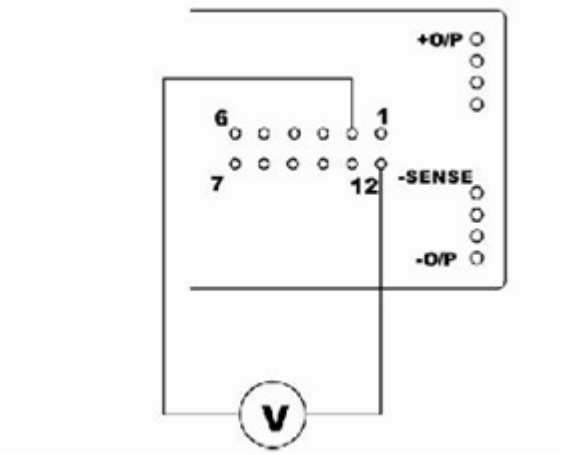
Temperature Monitoring (TEMP MON) - (pin 2)

The TEMP MON pin provides an indication of the module's internal temperature. The voltage at the TEMP MON pin is proportional to the temperature of the module baseplate at 10mV per ^{O}C, where:

Module temperature (^{O}C) = ($V_{temp,mon}$ X 100) – 273

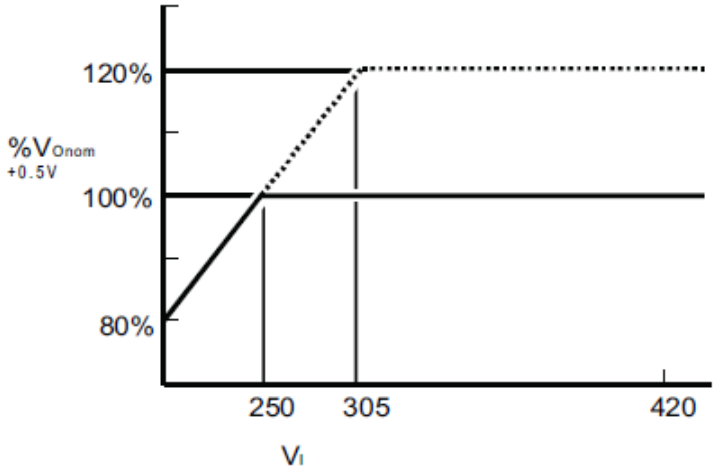
The temperature monitor signal can be used by thermal management systems (e.g. to control a variable speed fan). It can also be used for over temperature warning circuits and for thermal design verification of prototype power supplies and heatsink.





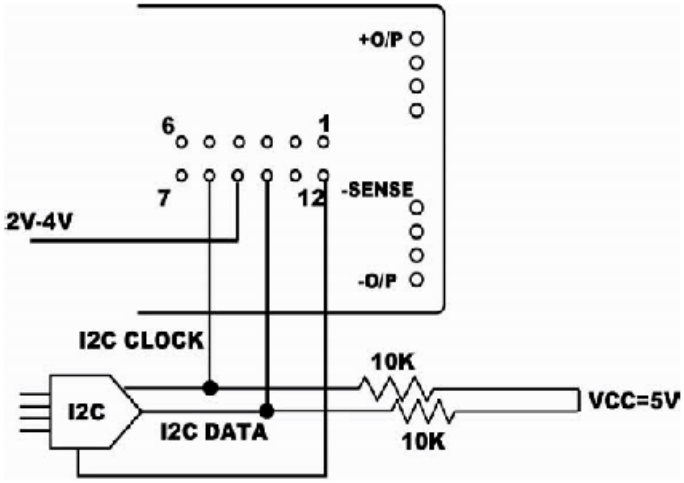
Break Regulation

AIF12W300 Series modules are designed to deliver full rate output current at up to 0.5V above $V_{O,nom}$ at the minimum specified input voltage.



I²C Digital Control (DCS, I²C CLK, I²C DATA)

The module shall be capable to be controlled by I²C interface, which is SMBus compatible, via I²C CLK and I²C DATA pins. These two pins share the same pin location of CLIM ADJ and V ADJ pins respectively. Digital control is selected when Digital Control Select (DCS) pin voltage is between 2V to 4V. When digital control is selected, analog adjust pin function is disabled. DCS signal shall only be applied when the module is powered off or disabled. An external 10 Kohm pull-up resistor is necessary for each I²C CLK, and I²C DATA pin, for 100 KHz I²C bus frequency.



I²C Communication Protocol

Command word

Command word is sent by master system to inform slave device that what kind of operation the master like to do. It is a 16-bit data. Bit 0 to bit 9 indicate the data need to transfer (e.g. the value of OV_ADJ). As there are two different lengths of data, one is 8-bit and the other is 10-bit. So, if 10-bit data is transmitting/receiving, whole 10 bits (DATA9 – DATA0) will be used. In 8 bits case, only the least significant 8 bits (DATA7 – DATA0) will be used. The two bits (DATA9 and DATA8) will be cleared. The 5 bits (REG4 – REG0) indicate which command needs to. When the master requests data from the slave, the DATA9-DATA0 bits should be cleared. And during setting the four information items (Model Name, Serial No., Firmware Version, Model Revision), DATA9-DATA8 should be cleared and is followed by the actual data.

The format of the 16-bits command word is as follow:

Bit 15							Bit 8
DSR	REG4	REG3	REG2	REG1	REG0	DATA9	DATA8
Bit 7							Bit 0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

The DSR (Data Set Read) bit controls read/write of data. If the master send a 0 (write operation) for this bit, the slave device will get the command register and data. And then set the value of the corresponding command register. If the master sends a 1 (read operation) for this bit, the slave device will get the current value of the corresponding command register and send it to the master.

The table below shows the register mapping:

Command Register	Coding (REG4 – REG0)
MODEL_NO (read/write*)	00000
SERIAL_NO (read/write*)	00001
FIRMWARE_VER (read/write*)	00010
MODEL_REV (read/write*)	00011
SLAVE_ADDRESS (read/write)	00100
OVP_ADJ (read/write)	00101
V_ADJ (read/write)	00110
CLIM ADJ (read/write)	00111
TMON (read only)	01000
VOUT (read only)	01001
CMON (read only)	01010
RESET (write only)	01111
LOCK (write only*)	10000
UNLOCK (write only*)	10001

* Remark: write functions only used to production.

Data Transfer Structure on I²C Bus

Terms	Description	No. of bits
Stt	Start bit	1
Sadd	Slave address	8
Ack	Acknowledge	1
Bt-H	Higher byte	8
Bt-L	Lower byte	8
StD(1st, 2nd,…nth)	String of bytes(1st byte, 2nd byte,……nth byte)	8
Stp	Stop Bit	1

In the block diagram below, gray boxes indicate master-send signal; white boxes indicate slave-send signal.

Set data to slave

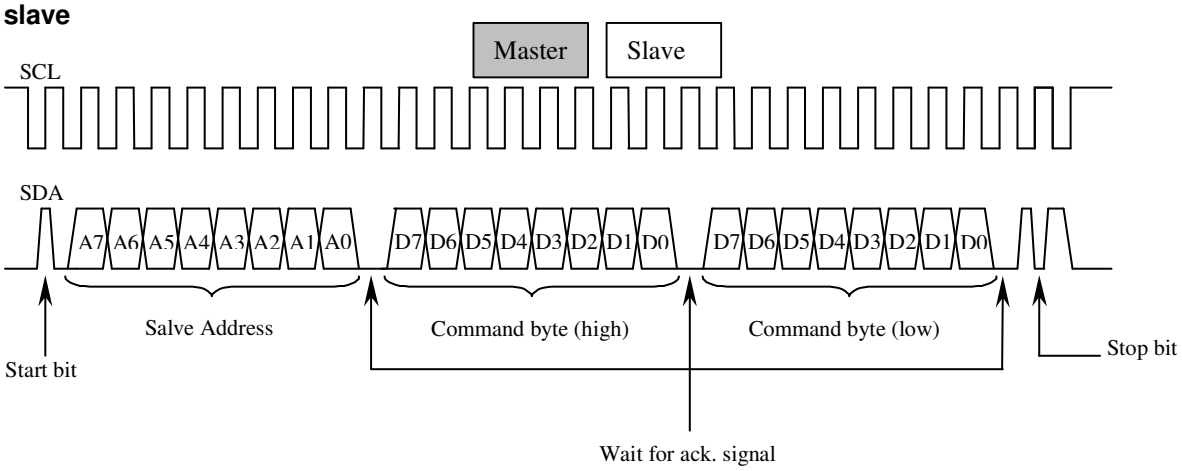


Fig 1.1 SCL and SDA signal in write mode.

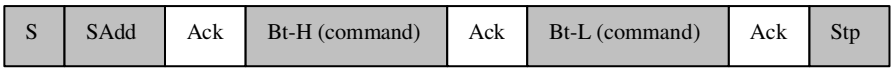


Fig 1.2 Block diagram of write mode.

Procedures:
1. The master device gives a Start condition via SDA.
2. Master sends the 8-bit slave address in which bit 0 of it should be 0 (0 indicate a write condition to slave) via SDA.
3. The addressed slave device give out acknowledge via SDA.
4. The master sends the high byte of command code via SDA.
5. The slave give out acknowledge via SDA.
6. The master sends the low byte of command code via SDA.
7. Slave gives out acknowledge after receiving the last byte.
8. Master gives a STOP condition via SDA to stop the transaction.

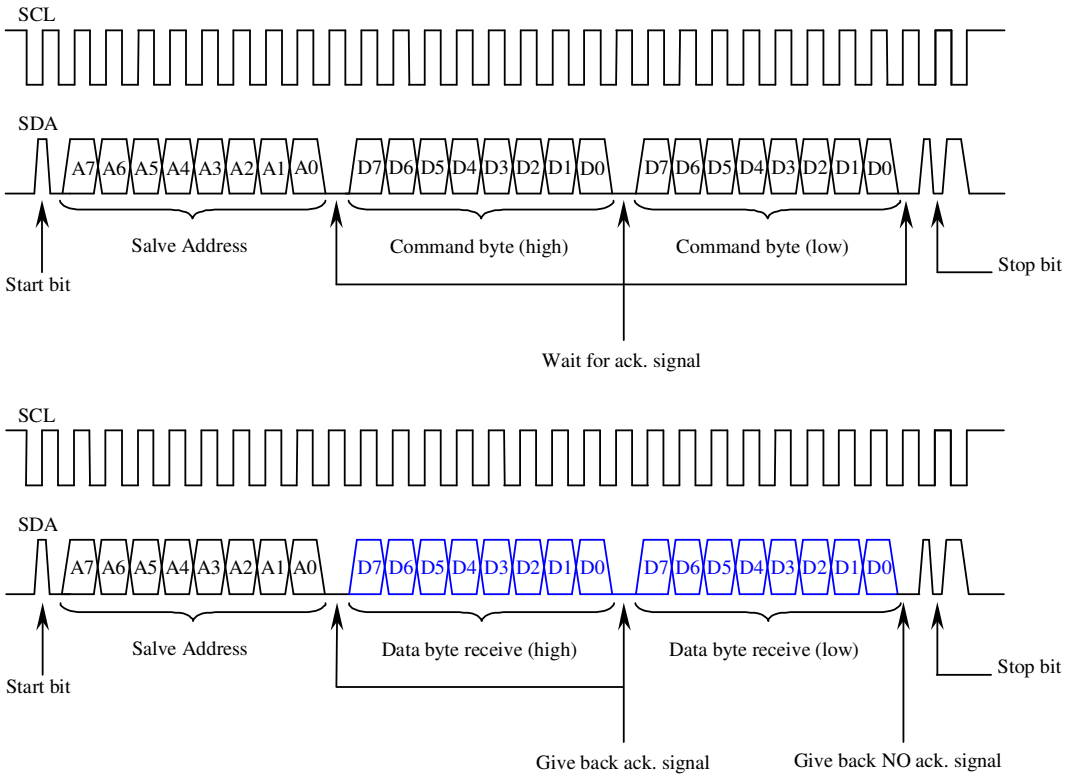


Fig. 2.1 SCL and SDA signal of read mode (2 bytes of data read).

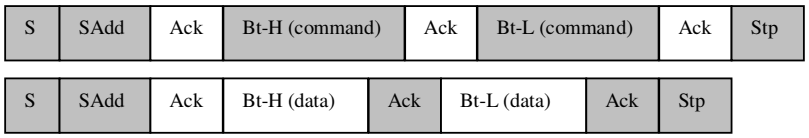


Fig. 2.2 Block diagram of read mode (2 bytes of data read).

Read data from slave (2-byte data)

Procedures:

1. The master device gives out a start condition on SDA.
2. Master sends the 8 bits slave address which bit 0 of it should be 0 (0 indicates write mode for slave) via SDA.
3. The addressed slave device gives back acknowledge via SDA.
4. Master sends out the high byte of the 2-bytes command word.
5. Slave device gives back acknowledge again.
6. Master sends out the low byte of the 2-bytes command word.
7. Slave device gives back acknowledge again.
8. Master sends out a stop condition to prepare for the next transaction.
9. Master gives out a start condition again for the next transaction.
10. Master sends the 8 bits slave address which bit 0 of it should be 1(1 indicates read mode for slave) via SDA.
11. Slave give back an acknowledge.
12. Slave then sends out the high byte of desired data.
13. Master gives back acknowledge to slave.
14. Slave sends the low byte of the desired data.

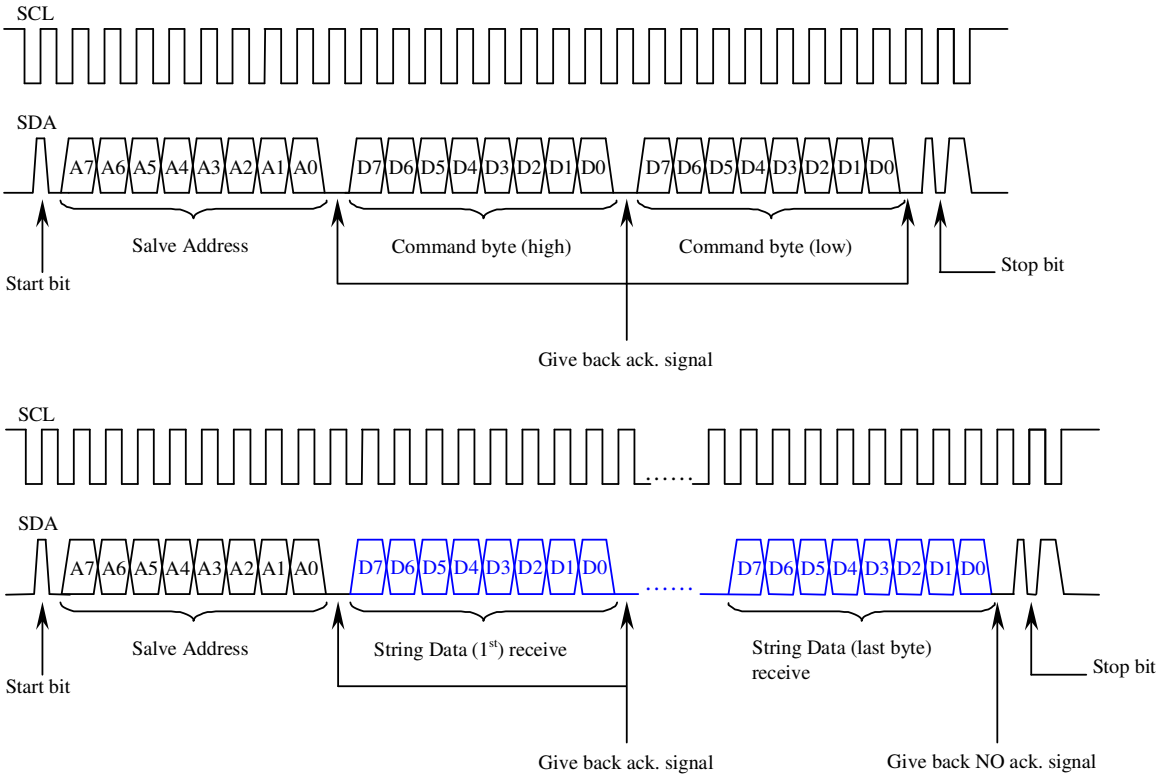


Fig 3.1 SCL and SDA signal of read mode (String of data).

Fig 3.1 Block diagram of read mode (String of data).

15. Master gives back acknowledge and sends out a stop condition to close the transaction.

Read data from slave (string of data)

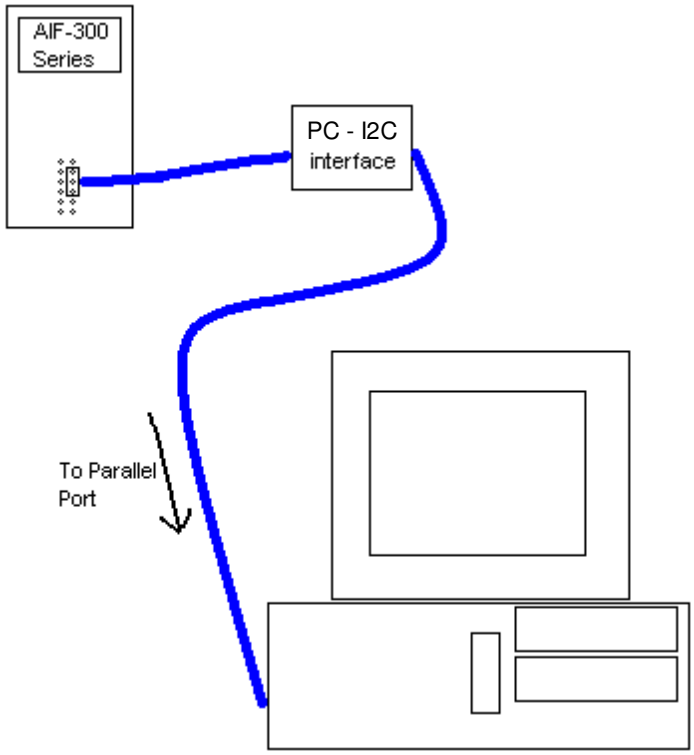
Procedures:
1. The master device gives out a start condition on SDA.
2. Master sends the 8 bits slave address which bit 0 of it should be 0 (0 indicates write mode for slave) via SDA.
3. The addressed slave device gives back acknowledge via SDA.
4. Master sends out the high byte of the 2-bytes command word.
5. Slave device gives back acknowledge again.
6. Master sends out the low byte of the 2-bytes command word.
7. Slave device gives back acknowledge again.
8. Master sends out a stop condition to prepare for the next transaction.
9. Master gives out a start condition again for the next transaction.
10. Master sends the 8 bits slave address which bit 0 of it should be 1(1 indicates read mode for slave) via SDA.
11. Slave give back an acknowledge.
12. Slave then sends out the first byte of desired data.
13. Master gives back acknowledge to slave.
14. Repeat 12 and 13 until the end of bytes.
15. Master gives back acknowledge and sends out a stop condition to close the transaction.

Digital Control Demo User Guide

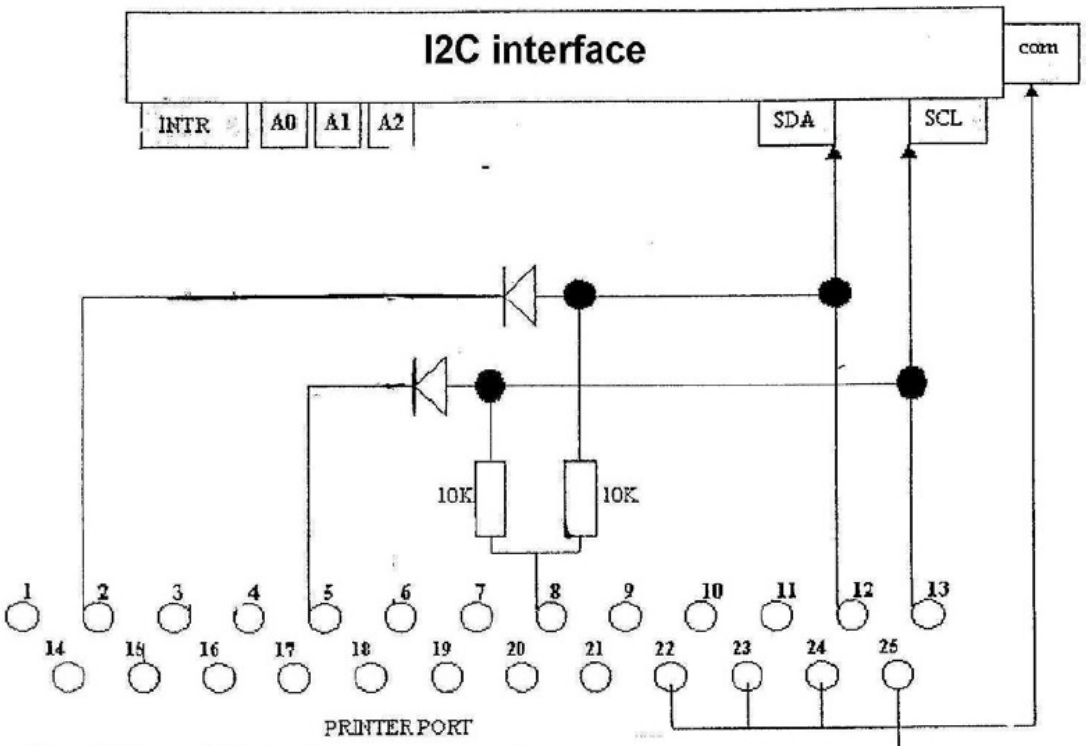
This Demo program is developed to test and evaluate I²C control features of AIF-300 DC/DC modules.

Equipment required:
1. One or more modules of AIF-300 series.
2. PC – Module interface hardware.
3. PC (with windows 98 / Me inside)

Hardware setup:
The picture shown below is the setup of the hardware.



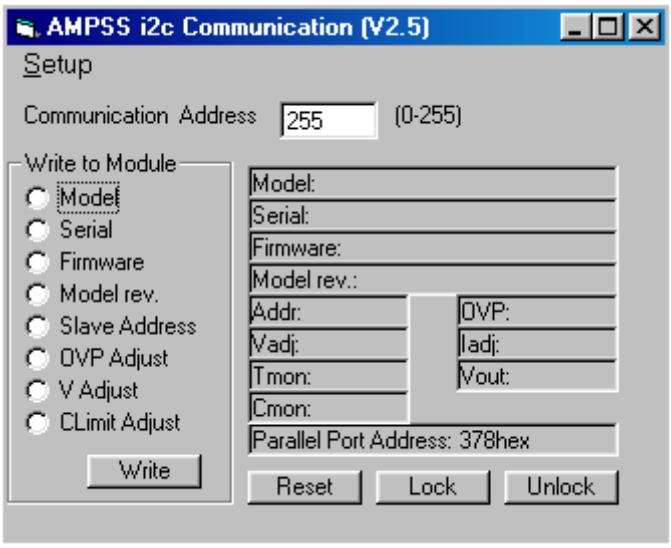
PC-I2C Interface Circuit Diagram



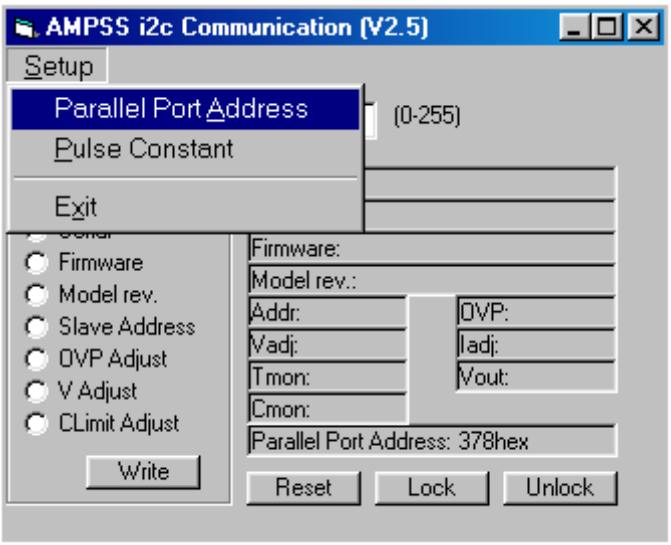
Base Address: (data port)
Pin2 = D0, Pin 5= D3, Pin 8=D6
Base Address+1 (status register)
Pin12 = Bit 5: Paper End, Pin 13= Bit 4: Select, Pin 15 = Bit 3: Fault
Ground Pin (Pin 18 to 25)

Software Setup

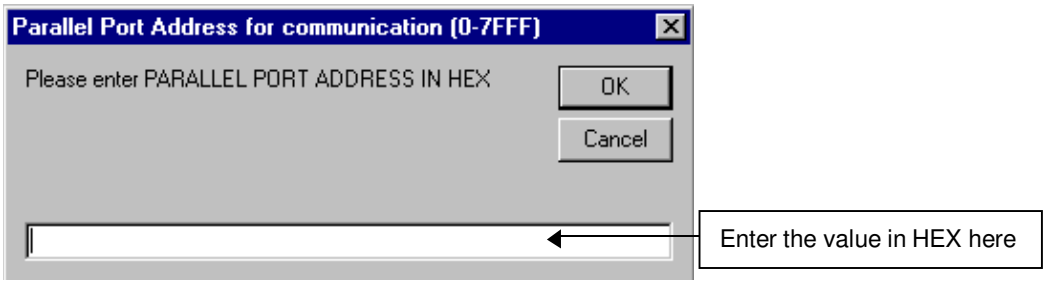
Click on the program “Ampss68.exe”. Then following dialog box shows:



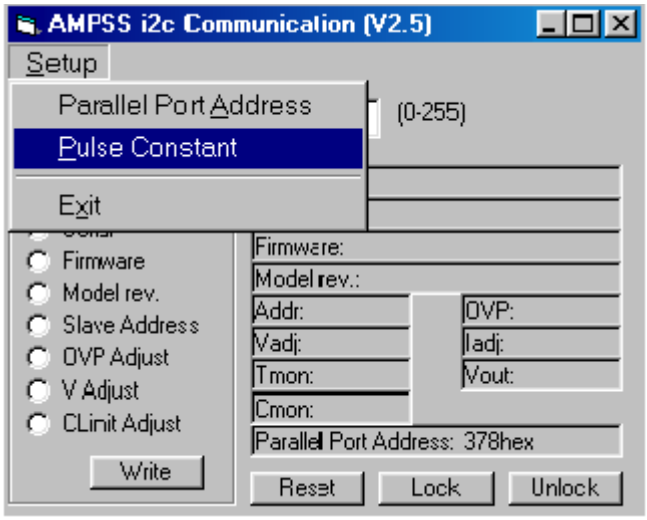
Click on “Setup” and choose “Parallel Port Address”.



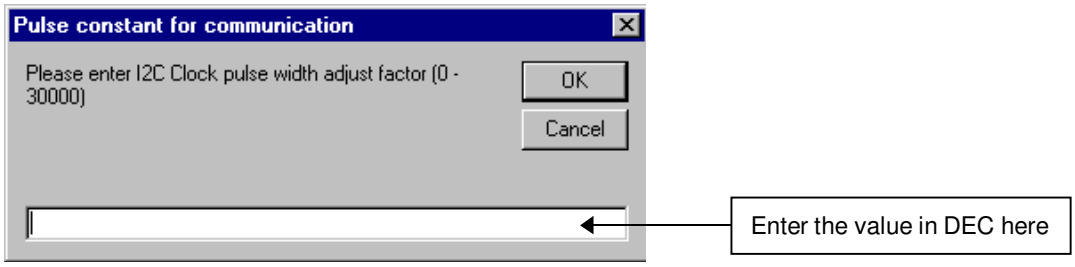
Then a new dialog box shows and enter the right value into it and click “OK”:



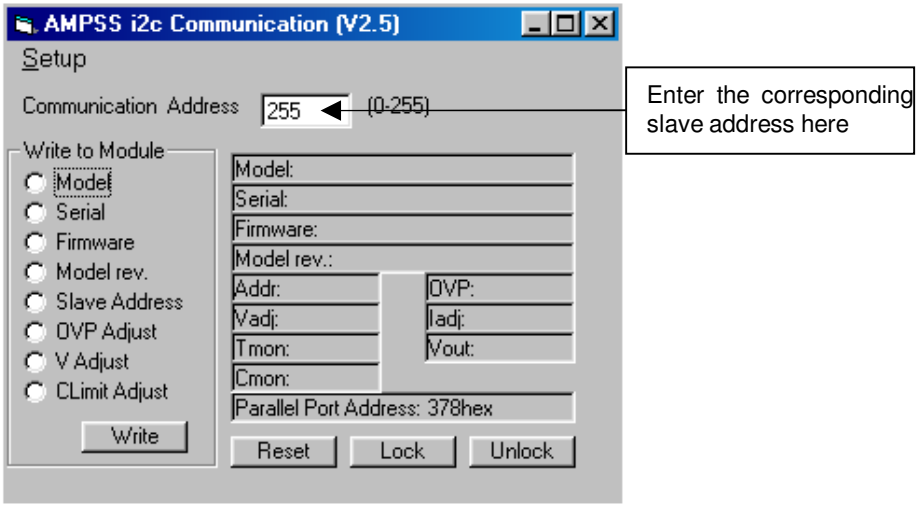
Then click on “Setup” and choose “Pulse Constant”.



Also set the desired pulse constant value into the dialog box below and click “OK”:

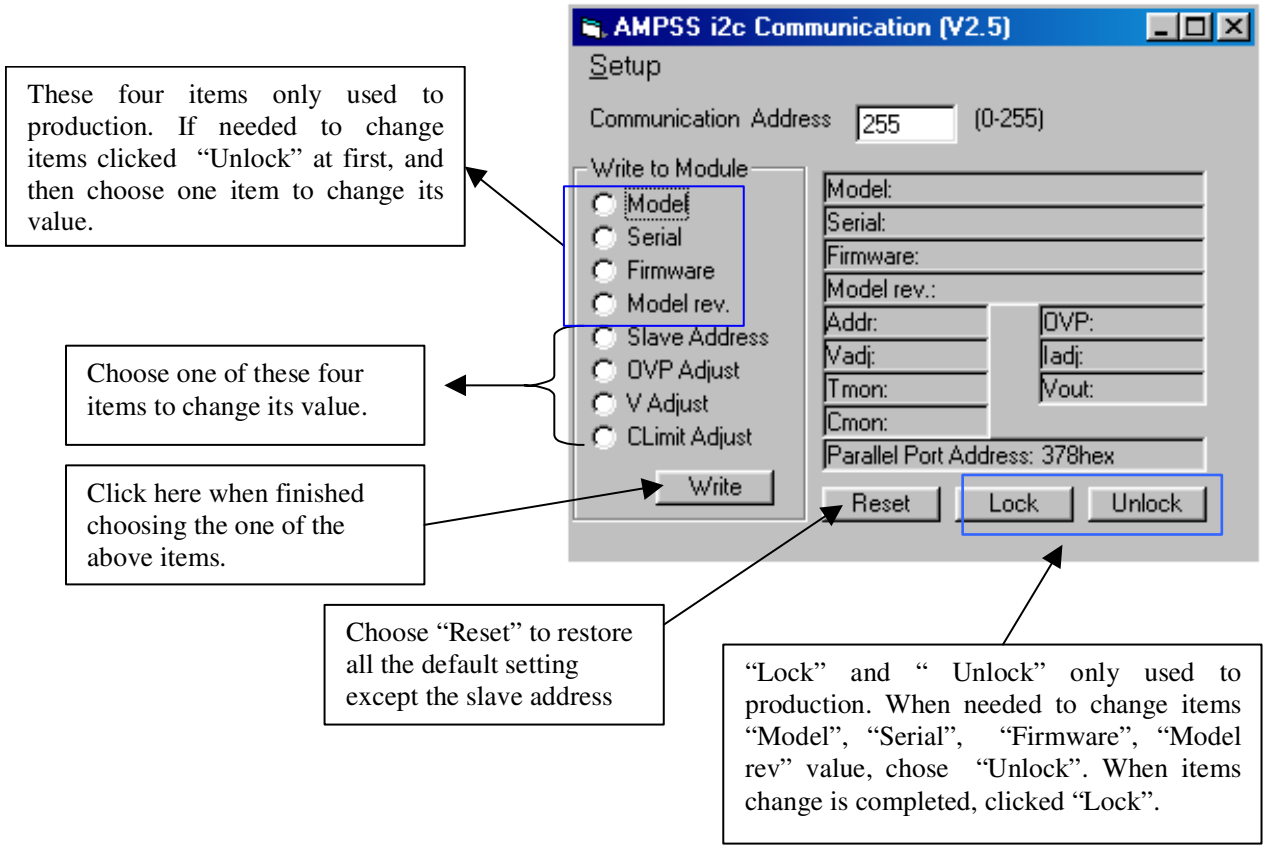


Select Module:
Enter the slave address of the module that you want to control:



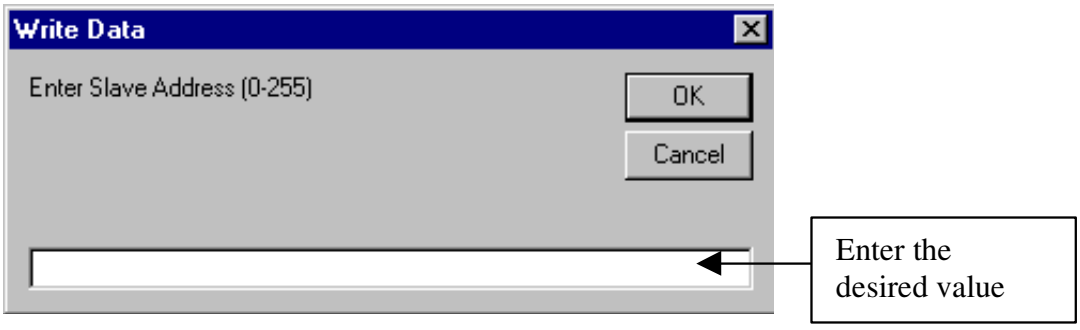
Note: “0” and “1” are the globe address of MMIIC. So, it can only perform “write” function when the UUT address is set to 0 or 1.

Write Value:



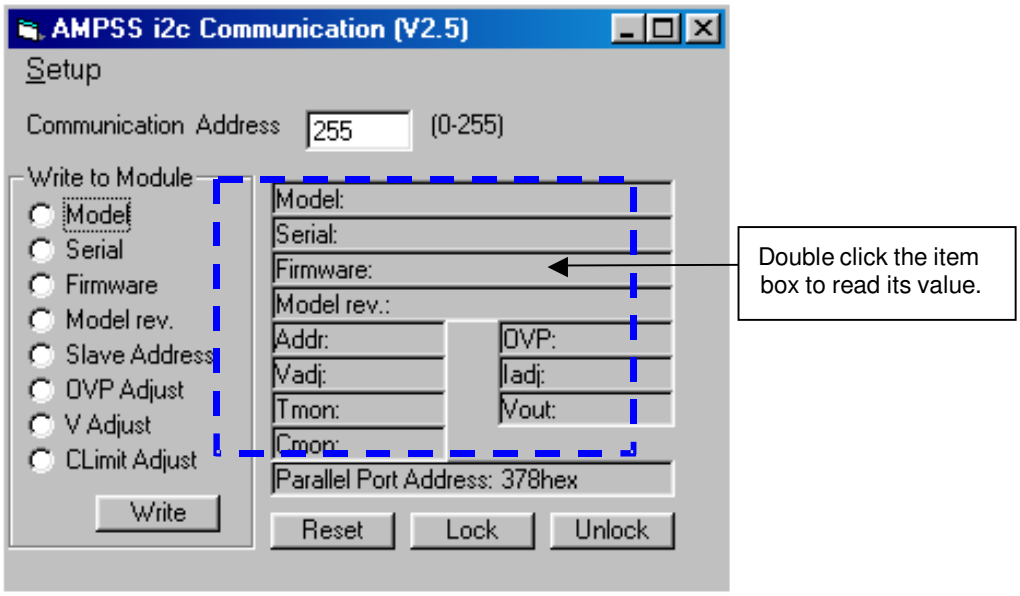
Click on the circle beside the desired item that needs to be changed its value.

After choosing the desired item, click on "Write" below the items. Then a new dialog box shows (except "Reset" option).

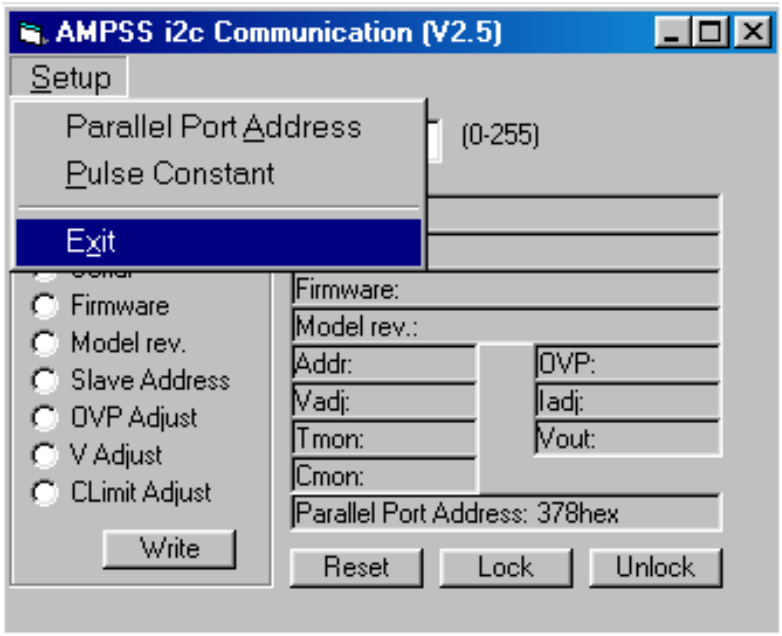


Fill the box with the new value and click "OK". Or click "Cancel " to cancel this operation.

Read Value:
Double click on the item box to read the corresponding value:



Exit Program:
Click on "Setup" and choose "Exit" to exit the program.



Application Notes

Typical Application

Below is the typical application of the AIF12W300 series power supply.

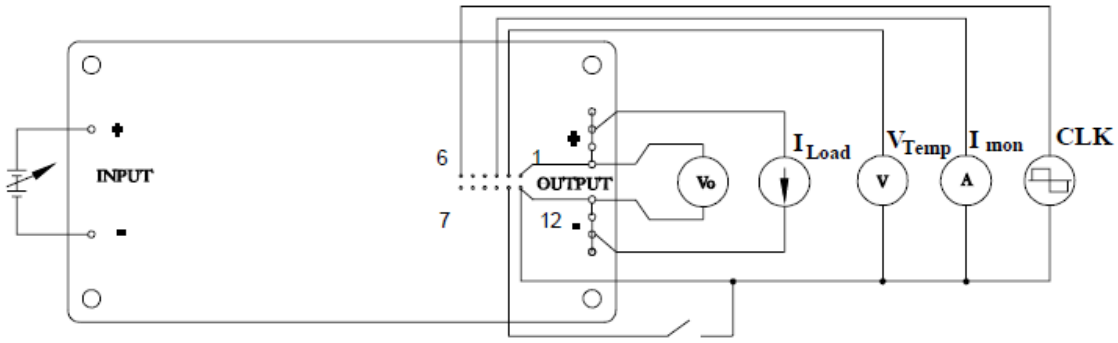


Figure 9. Single Module Operation

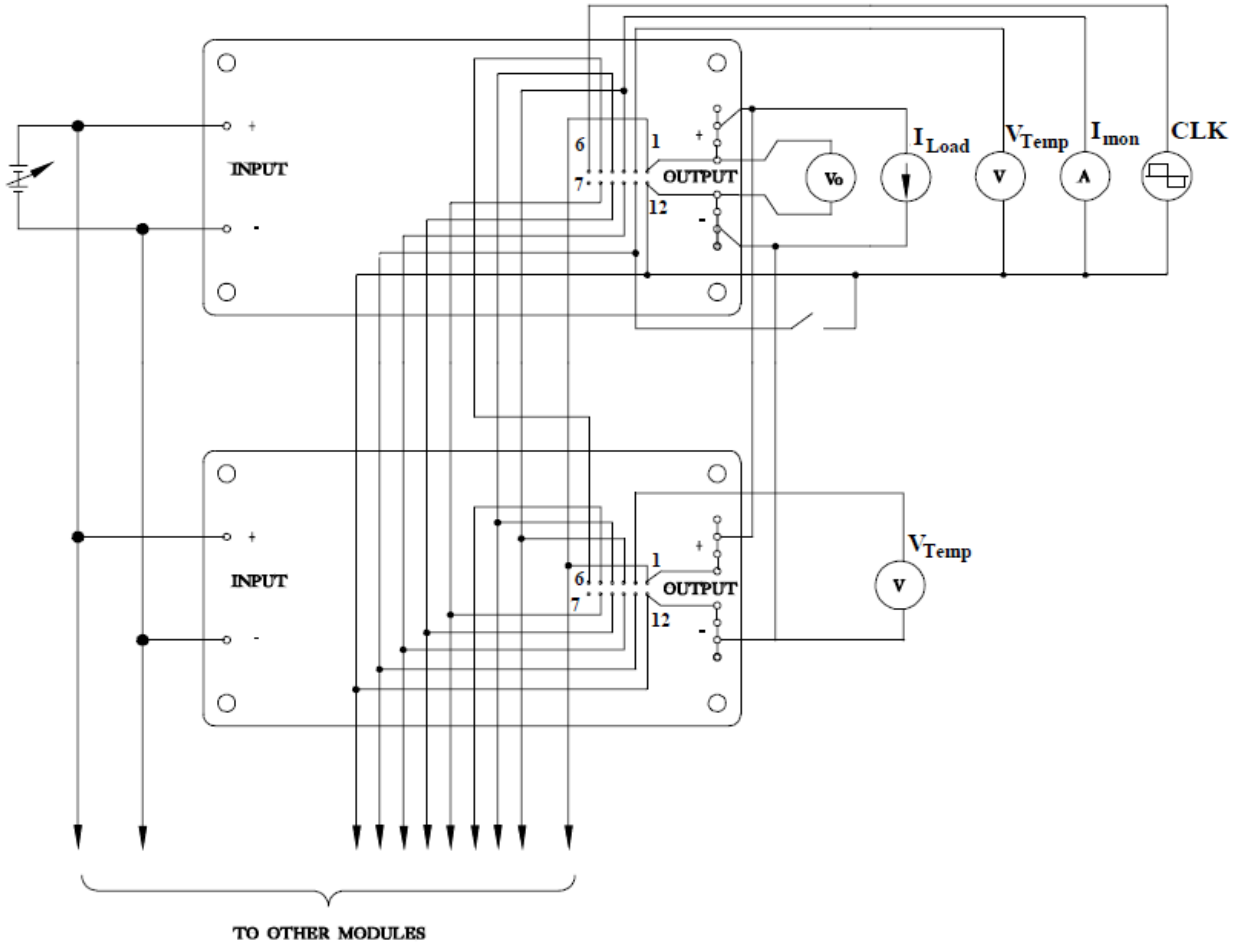


Figure 10. Parallel Module Operation

Recommend external EMI Filter Schematic

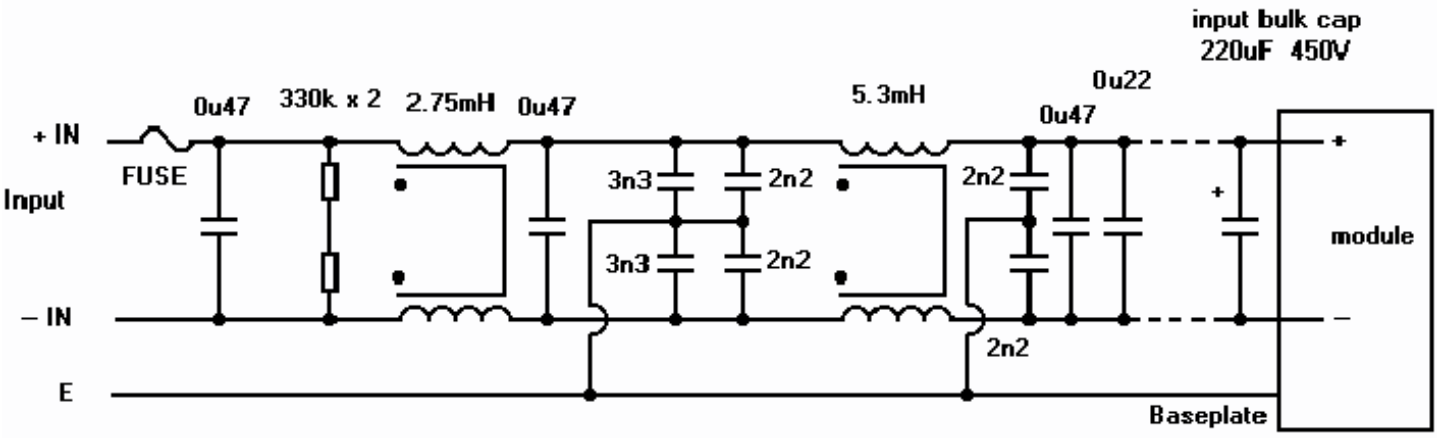


Figure 11. EMI Filter Schematic for AIF Series

Input Reflected-Ripple Current Test Configuration

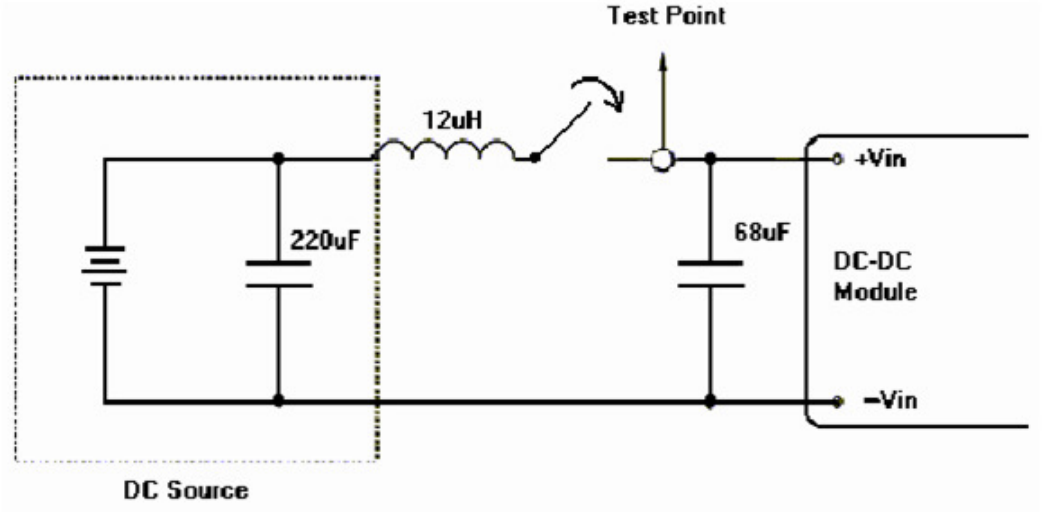


Figure 12. Input Reflected-Ripple Current Test Setup

Inrush Current Test Setup

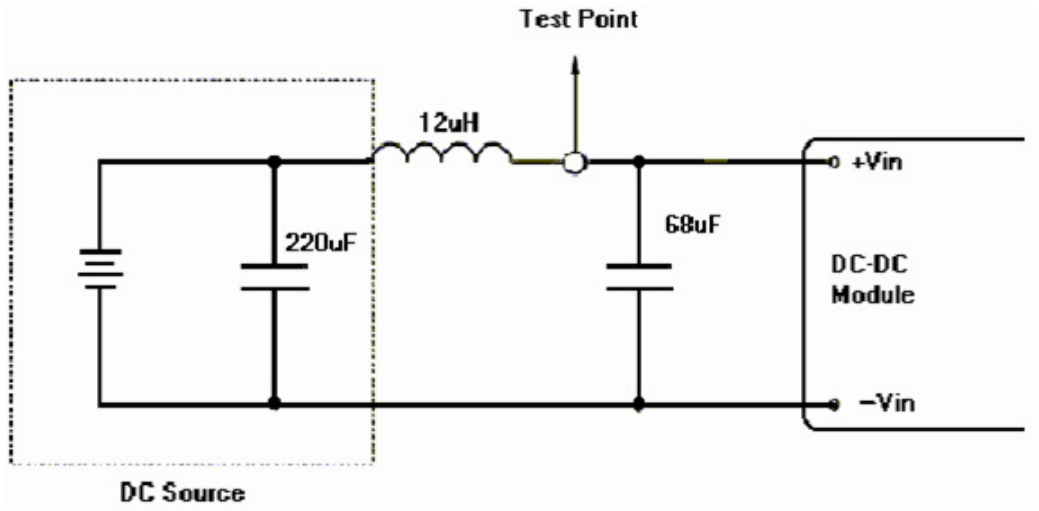


Figure 13. Inrush Current Test Setup

Output Ripple & Noise Test Configuration

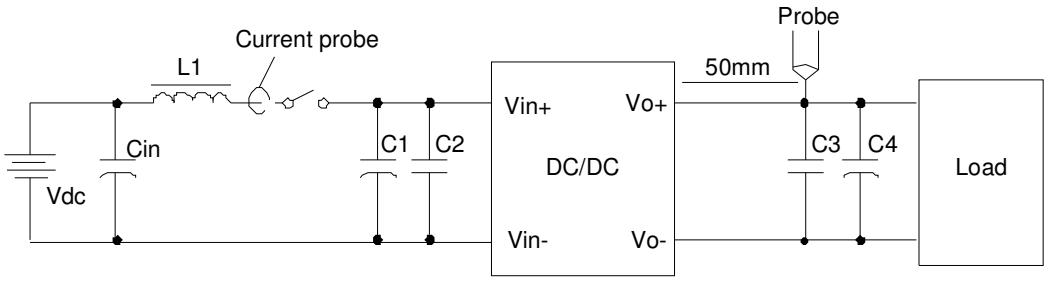


Figure 14. Output ripple & noise test configuration

Vdc: DC power supply

L1: 12uH

Cin: 100uF/450V typical

C1,C2 : 47nF/630V ceramic capacitor

C3: 1uF/63V ceramic capacitor

C4: 10uF/63V tantalum capacitor

Note - Using a coaxial cable with series 50 ohm resistor and 0.68uF ceramic capacitor or a ground ring of probe to test output ripple & noise is recommended.

Recommended OPTO Isolation Circuit

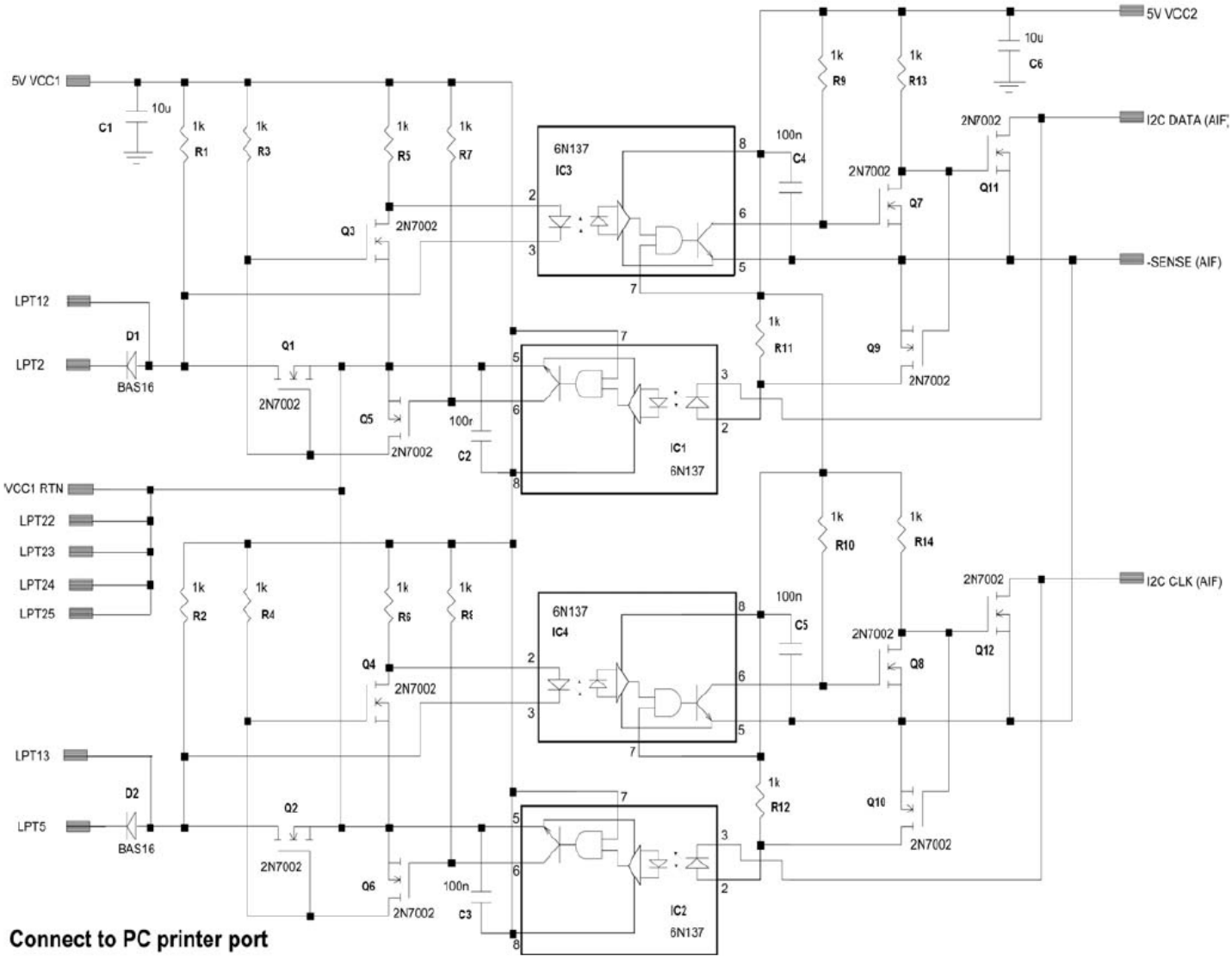


Figure 15. Recommended OPTO Isolation Circuit

Parallel Operation with OPTO Isolation Circuit

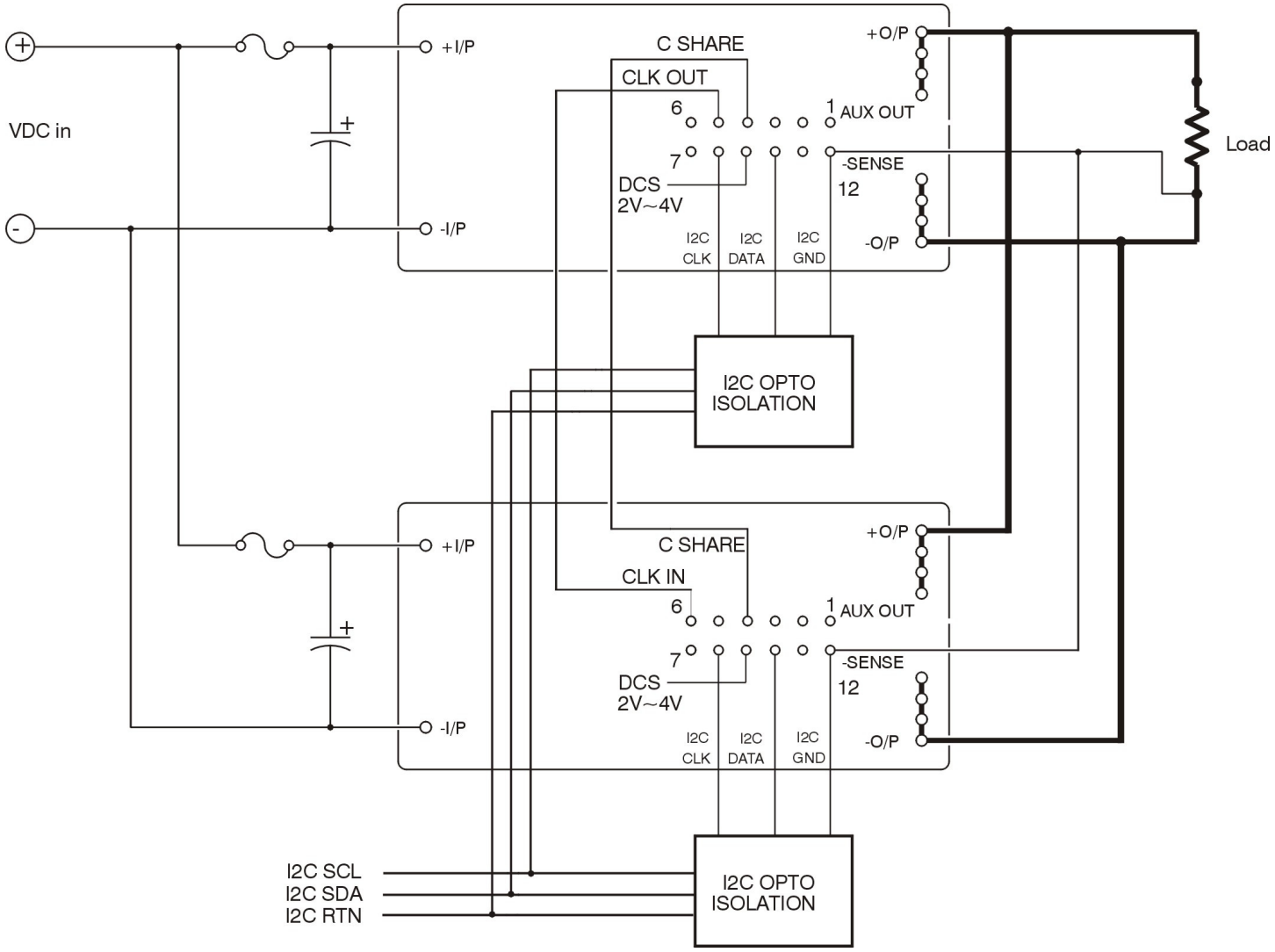


Figure 16. Parallel Operation with OPTO Isolation Circuit

Digital Control

The module shall be capable to be controlled by I²C interface, which is SMBus compatible, via I²C CLK and I²C DATA pins. These two pins share the same pin location of CLIM ADJ and V_ADJ pins respectively. Digital control is selected when Digital Control Select (DCS) pin voltage is between 2V - 4V.

There are 7 command registers for read operation, 4 command registers for read/write operation and 1 command register for write operation.

Command Register	Description
MODEL_NO (read only)	Read model name of the module
SERIAL_NO (read only)	Read serial number on bar code label
FIRMWARE_VER (read only)	Read firmware version
MODEL_REV (read only)	Read model revision
SLAVE_ADDRESS (read/write)	Read or set slave address of the module
OVP_ADJ (read/write)	Read or set overvoltage protection threshold of the module
V_ADJ (read/write)	Read or set output voltage of the module
CLIM ADJ (read/write)	Read or set current limit protection threshold of the module
TMON (read only)	Read baseplate temperature of the module
VOUT (read only)	Read output voltage of the module
CMON (read only)	Read output current of the module
RESET (write only)	Reset all control parameters to factory setting

Digital Data Conversion

Each control and monitoring data is in 10-bit format. The data conversion formulae are as follows.

OVP_ADJ:

The range of the OVP_ADJ can be adjusted from 125% to 145% of $V_{O,nom}$. The received/transmitted data is calculated by the equation below.

Receive Data (from module to PC):

Input Data: MCU OVP ADJ (integer)
Output Data: OVPADJ% (round to 1decimal place)

$$\text{OVPadj\%} = 145\% - \frac{\text{MCU OVPadj}}{205} \times 20\%$$

Transmit Data (from PC to module):

Input Data: OVPADJ (round to 1 decimal place)
Output Data: MCU OVPADJ (integer)

$$\text{MCU OVPadj} = \frac{145\% - \text{OVPadj\%}}{20\%} \times 205$$

V_ADJ:

V_ADJ range between 80% to 120% module: (5Vo and above model)

The range of the V_ADJ can be adjusted from 80% to 120% of $V_{O,nom}$. The received / transmitted data is calculated by the equation below.

Receive Data (from module to PC):
Input Data: MCU V_ADJ (integer)
Output Data: V_ADJ% (round to 1decimal place)

$$\text{Vadj\%} = 80\% + \frac{\text{MCU Vadj}}{410} \times 40\%$$

Transmit Data (from PC to module):
Input Data: V_ADJ (round to 1 decimal place)
Output Data: MCU V_ADJ (integer)

$$\text{MCU Vadj} = \frac{\text{Vadj\% - 80\%}}{40\%} \times 410$$

V_ADJ range between 50% to 110% module: (Below 5Vo model)

The range of the V_ADJ can be adjusted from 50% to 110% of V_O (nom). The received/transmitted data is calculated by the equation below.

V_ADJ between 50% ~100%:

Receive Data (from module to PC):
Input Data: MCU V_ADJ (integer)
Output Data: V_ADJ% (round to 1decimal place)

$$\text{Vadj\%} = 50\% + \frac{\text{MCU Vadj}}{205} \times 50\%$$

Transmit Data (from PC to module):
Input Data: V_ADJ (round to 1 decimal place)
Output Data: MCU V_ADJ (integer)

$$\text{MCU Vadj} = \frac{\text{Vadj\% - 50\%}}{50\%} \times 205$$

V_ADJ between 100% ~110%:

Receive Data (from module to PC):
Input Data: MCU V_ADJ (integer)
Output Data: V_ADJ% (round to 1decimal place)

$$\text{Vadj\%} = 100\% + \frac{\text{MCU Vadj - 205}}{205} \times 10\%$$

Transmit Data (from PC to module):
Input Data: V_ADJ (round to 1 decimal place)
Output Data: MCU V_ADJ (integer)

$$\text{MCU Vadj} = \frac{\text{Vadj\% - 90\%}}{10\%} \times 205$$

CLIM ADJ

The range of the CLIM ADJ can be adjusted from 0% to 102.5% or 110% of rated I_O. The received/transmitted data is calculated by the equation below.

Receive Data (from module to PC):

Input Data: MCU CLIM ADJ (integer)
Output Data: CLIM ADJ% (round to 1decimal place)

Case 1: MCU CLIM ADJ ≠ 841

$$\text{CLIMadj}\% = \frac{\text{MCU CLIMadj}}{840} \times 102.5\%$$

Case 2: MCU CLIM ADJ >= 841

$$\text{CLIMadj}\% = 110\%$$

Transmit Data (from PC to module):

Input Data: CLIM ADJ (round to 1 decimal place)
Output Data: MCU CLIM ADJ (integer)

Case1: CLIM ADJ% ≠ 110%

$$\text{MCU CLIMadj} = \frac{\text{CLIMadj}\%}{102.5\%} \times 840$$

Case2: CLIM ADJ% >= 110%

$$\text{MCU CLIMadj} = 841$$

TMON

Baseplate temperature monitoring is a read only data. It is ranged from -40^{O}C to 120^{O}C. The temperature of module can be calculated by the equation below:

Receive Data (from module to PC):

Input Data: MCU Tmon (integer)
Output Data: Baseplate Temperature in ^{O}C (round to 1 decimal place)

$$\text{Baseplate Temperature in °C} = \frac{\text{MCU Tmon}}{1024} \times 500 - 273$$

VOUT

Output Voltage is a read only data. The output voltage can be calculated by the equation below:
Receive Data (from module to PC):

Input Data: MCU Vout (integer)
Output Data: Output Voltage in $\%V_{O,nom}$ (round to 1 decimal place)

$$\text{Output Voltage in \%Vonom} = \frac{\text{MCU Vout}}{Vo\_REF} \times 100\%$$

Module name	Vo_REF
AIF120Y300-L/N-L/-NTL	369
AIF120F300-L/N-L/-NTL	676
AIF80A300-L/N-L/-NTL	813
AIF50B300-L/N-L/-NTL	820
AIF40C300-L/N-L/-NTL	830
AIF25H300-L/N-L/-NTL	820
AIF12W300-L/N-L/-NTL	820

CMON

Current monitoring is a read only data. It is ranged from 0% to 100% of rated I_O. The output current of module can be calculated by the equation below:

Receive Data (from module to PC):

Input Data: MCU CMON (round to 1 decimal place)

Output Data: Output Current Monitor in % $I_{O,max}$ (integer)

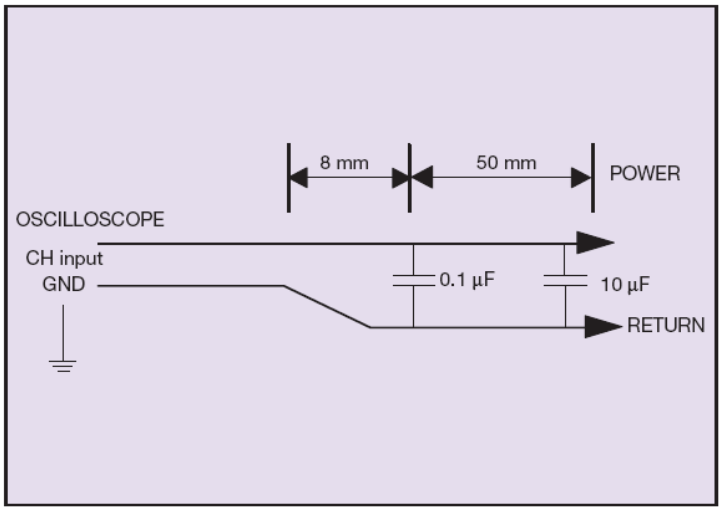
$$\text{Output Current Monitor in \%Iomax} = \frac{\text{MCU Cmon}}{614} \times 100\%$$

DEFAULT FACTORY SETTING

Control data	Factory Setting
Slave address	0010100000 (A0h = 160) (8 bit addressing)
OVP ADJ	0011001101 (00CDh = 205) (125% of V_O)
V ADJ	0011001101 (00CDh = 205) (100% of V_O (nom))
CLIM ADJ	1111111111 (0349h = 841) (110% of rated I_O)

Output Ripple and Noise Measurement

The setup outlined in the diagram below has been used for output voltage ripple and noise measurements on the AIF12W300 Series. When measuring output ripple and noise, a scope jack in parallel with a 0.1 uF ceramic chip capacitor, and a 10 uF aluminum electrolytic capacitor should be used. Oscilloscope should be set to 20 MHz bandwidth for this measurement.



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