# AIS226DS

## MEMS inertial sensor
## 2-axis, low *g* accelerometer with digital output

**Preliminary data**

## Features

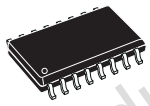
- 3.3 V single supply operation
- 1.8 V compatible IOs
- SPI digital output interface
- 16 bit internal representation, 14 bit resolution
- Interrupt activated by motion
- Programmable interrupt threshold
- Embedded self-test
- High shock survivability
- ECOPACK® compliant
- Extended temperature range -40 °C to +105 °C

## Applications

- Anti-theft systems and inertial navigation
- Motion activated functions
- Vibration monitoring and compensation
- Tilt measurements
- Black boxes, event recorders
- AEC-Q100 qualification

## Description

The AIS226DS is a two axes digital output accelerometer that includes a sensing element and an IC interface able to take the information from the sensing element and to provide the measured acceleration signals to the external world through an SPI serial interface.
$I^2C$ compatible interface also available.



SO16W

The sensing element, capable of detecting the acceleration, is manufactured using a dedicated process developed by ST to produce inertial sensors and actuators in silicon.

The IC interface instead is manufactured using a CMOS process that allows high level of integration to design a dedicated circuit which is factory trimmed to better match the sensing element characteristics.

The AIS226DS has a user selectable full scale of ±2 *g*, ±6 *g* and it is capable of measuring acceleration over a bandwidth of 640 Hz for all axes. The device bandwidth may be selected accordingly to the application requirements. The self-test capability allows the user to check the functioning of the system. The device is available in plastic SOIC package 300 mils reverse frame forming for EMI reduction and it is specified over a temperature range extending from -40 °C to +105 °C.
These characteristics make the AIS226DS suitable for a broad range of automotive applications.

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**Table 1. Device summary**

| Order code | Operating temperature range [° C] | Package | Packing |
|---|---|---|---|
| AIS226DS | -40 to +105 | SO16W | Tubes |
| AIS226DSTR | -40 to +105 | SO16W | Tape and reel |



This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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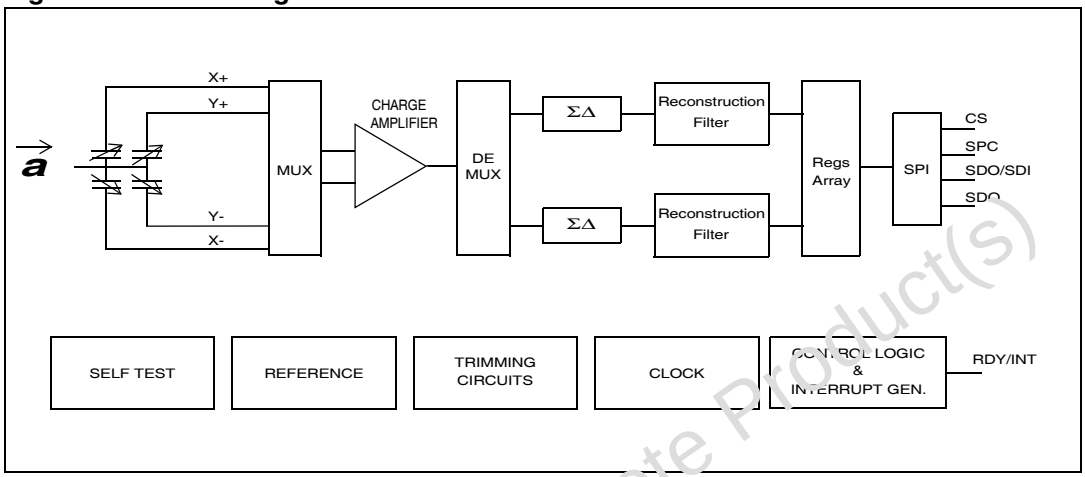
# 1 Block diagram and pin description

## 1.1 Block diagram

**Figure 1. Block diagram**




## 1.2 SO16W pin description

**Figure 2. Pin connection**

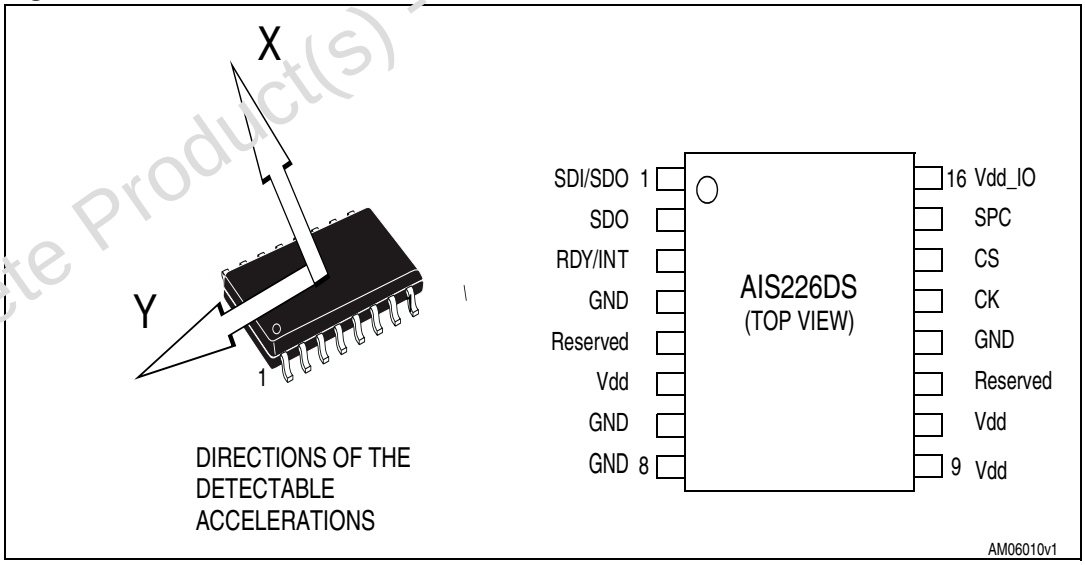



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**Table 2. Pin description**

| Pin# | Name | Function |
|---|---|---|
| 1 | SDI/<br>SDO | SPI serial data input (SDI)<br>3-wire Interface Serial Data Output (SDO) |
| 2 | SDO | SPI serial data output |
| 3 | RDY/INT | Data ready/inertial wake-up and free-fall interrupt |
| 4 | GND | 0 V supply |
| 5 | Reserved | Either leave unconnected or connect to GND |
| 6 | Vdd | Power supply |
| 7 | GND | 0 V supply |
| 8 | GND | 0 V supply |
| 9 | Vdd | Power supply |
| 10 | Vdd | Power supply |
| 11 | Reserved | Either leave unconnected or connect to Vdd_IO |
| 12 | GND | 0 V supply |
| 13 | CK | Optional external clock, if not used either leave unconnected or connect to GND |
| 14 | CS | Chip select (logic 0: SPI enabled, logic 1: SPI disabled) |
| 15 | SPC | SPI serial port clock |
| 16 | Vdd_IO | Power supply for I/O pads |

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# 2 Mechanical and electrical specifications

## 2.1 Mechanical characteristics

Vdd = 3.3 V, T = -40 °C to 105 °C unless otherwise noted[a]

**Table 3. Mechanical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| FS | Measurement range | FS bit set to 0 | | ±2.0 | | g |
| | | FS bit set to 1 | | ±6.0 | | |
| Dres | Device resolution | Full-scale = ±2 *g*<br>T = 25 °C, ODR1=40 Hz | | 0.25 | | mg |
| | | Full-scale = ±2 *g*<br>T = 25 °C, ODR2=160 Hz | | 0.5 | | |
| | | Full-scale = ±2 *g*<br>T = 25 °C, ODR3 = 640 Hz | | 1 | | |
| | | Full-scale = ±2 *g*<br>T = 25 °C, ODR4 = 2560 Hz | | 3.9 | | |
| So | Sensitivity | Full-scale = ±2 *g*<br>16 bit representation | | 16384 | | LSb/g |
| | | Full-scale = ±6 *g*<br>16 bit representation[1] | | 5461 | | |
| TCSo | Sensitivity change vs temperature | Full-scale = ±2 *g* | | 0.025 | | %/°C |
| Off | Zero-g level offset accuracy[2],[3] | Full-scale = ±2 *g* | -70 | | 70 | mg |
| | | Full-scale = ±6 *g*[2] | -70 | | 70 | |
| TCOff | Zero-g level change vs temperature | Max delta from 25 °C | | 0.05 | | mg/°C |
| NL | Non linearity[2] | Best fit straight line<br>Full-scale = ±2 *g*<br>ODR = 40 Hz | | ±2 | | % FS |
| CrAx | Cross axis[2] | | | ±3 | | % |
| $V_{st}$ | Self-test output change[4],[5] | Full-scale= ±2 *g* | | 7360 | | LSb |
| | | Full-scale= ±6 *g* | | 2560 | | LSb |
| BW | System bandwidth | | | ODRx/4 | | Hz |
| $T_{OP}$ | Operating temperature range | | -40 | | +105 | °C |

1. Guaranteed by design
2. Zero-g level offset value after MSL3 preconditioning
3. Offset can be eliminated by enabling the built-in high pass filter (HPF)

a. The product is factory calibrated at 3.3 V. Operation over 3.6 V might affect the reliability of the device

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4. Self test output changes with the power supply. “Self-test output change” is defined as OUTPUT[LSb]$_{(Self\text{-}test\ bit\ on\ CTRL\_REG1=1)}$ - OUTPUT[LSb]$_{(Self\text{-}test\ bit\ on\ CTRL\_REG1=0)}$. 1LSb = 1g/16384 at 16 bit representation, 2 g Full-scale
5. Output data reach 99% of final value after 5/ODR when enabling Self-test mode due to device filtering

*Note: Typical specifications are not guaranteed.*

## 2.2 Electrical characteristics

Vdd = 3.3 V, T = -40 °C to 105 °C unless otherwise noted[b]

**Table 4. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Vdd | Supply voltage | | 3.0 | 3.3 | 3.6 | V |
| Vdd_IO | I/O pads supply voltage(1) | | 1.71 | | Vdd | V |
| Idd | Supply current | Vdd = 3.3 V | | 0.6 | | mA |
| IddPdn | Current consumption in Power-down mode | | | 2 | | µA |
| ODR1 | Output data rate 1 | Dec factor = 512 | | 40 | | Hz |
| ODR2 | Output data rate 2 | Dec factor = 128 | | 160 | | |
| ODR3 | Output data rate 3 | Dec factor = 32 | | 640 | | |
| ODR4 | Output data rate 4 | Dec factor = 8 | | 2560 | | |
| BW | System bandwidth(2) | | | ODRx/4 | | Hz |
| Ton | Turn-on time(3) | | | 5/ODRx | | s |
| $T_{OP}$ | Operating temperature range | | -40 | | +105 | °C |

1. Guaranteed by design
2. Digital filter -3 dB frequency
3. Time to obtain valid data after exiting power-down mode

*Note: Typical specifications are not guaranteed.*

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b. The product is factory calibrated at 3.3 V. Operation over 3.6 V might affect the reliability of the device

# 3 Communication interface characteristics

## 3.1 SPI - serial peripheral interface

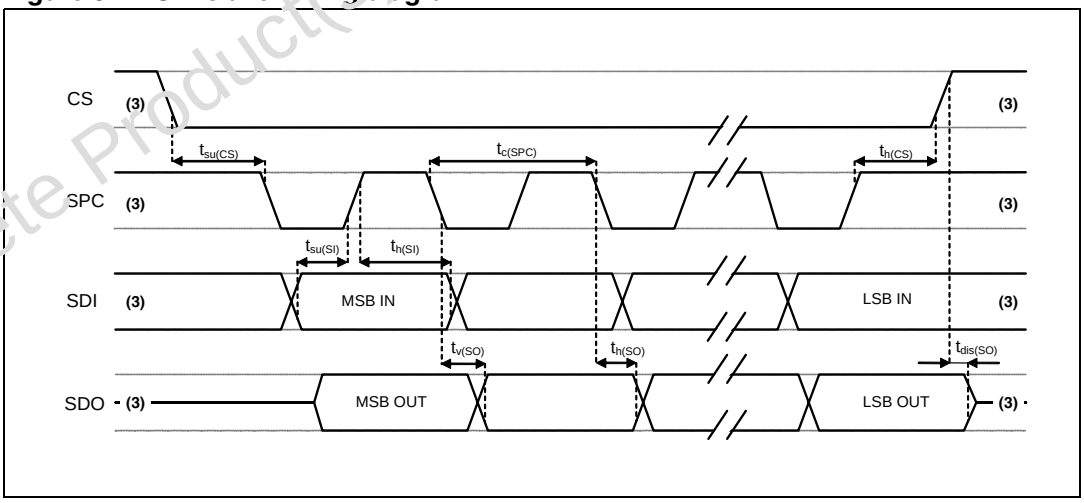
Subject to general operating conditions for Vdd and $T_{OP}$

**Table 5. SPI slave timing values**

| Symbol | Parameter | Value(1) | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| tc(SPC) | SPI clock cycle | 125 | | ns |
| fc(SPC) | SPI clock frequency | | 8 | MHz |
| tsu(CS) | CS setup time | 5 | | ns |
| th(CS) | CS hold time | 10 | | |
| tsu(SI) | SDI input setup time | 5 | | |
| th(SI) | SDI input hold time | 15 | | |
| tv(SO) | SDO valid output time | | 55 | |
| th(SO) | SDO output hold time | 7 | | |
| tdis(SO) | SDO output disable time | | 50 | |

1. Values are guaranteed at 8 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

**Figure 3. SPI slave timing diagram (2)**




2. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output port
3. When no communication is on-going, data on CS, SPC, SDI and SDO are driven by internal pull-up resistors

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# 4 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 6. Absolute maximum ratings**

| Symbol | Ratings | Maximum value | Unit |
|---|---|---|---|
| Vdd | Supply voltage(1) | -0.3 to 4.0 | V |
| Vdd_IO | I/O pins supply voltage(1) | -0.3 to Vdd +0.1 | V |
| Vin | Input voltage on any control pin(1) (CS, SPC, SDI/SDO, SDO, CK) | -0.3 to Vdd_IO +0.3 | V |
| $A_{POW}$ | Acceleration (any axis, powered, Vdd = 3.3 V) | 3000 *g* for 0.5 ms | |
| | | 10000 *g* for 0.1 ms | |
| $A_{UNP}$ | Acceleration (any axis, unpowered) | 3000 *g* for 0.5 ms | |
| | | 10000 *g* for 0.1 ms | |
| $T_{OP}$ | Operating temperature range | -40 to +105 | °C |
| $T_{STG}$ | Storage temperature range | -40 to +125 | °C |
| ESD | Electrostatic discharge protection | 2.0 (HBM) | kV |
| | | 200 (MM) | V |
| | | 500(CDM) | V |

1. Supply voltage on any pin should never exceed 4.0 V.

This is a mechanical shock sensitive device, improper handling can cause permanent damages to the part

This is an ESD sensitive device, improper handling can cause permanent damages to the part

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## 4.1 Terminology

### 4.1.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined e.g. by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the earth, noting the output value, rotating the sensor by 180 degrees (point to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also very little over time. The Sensitivity tolerance describes the range of sensitivities of a large population of sensors.

### 4.1.2 Zero-g level

Zero-*g* level offset (Off) describes the deviation of an actual output signal from the ideal output signal if there is no acceleration present. A sensor in a steady state on a horizontal surface will measure 0 *g* in X axis and 0 g in Y axis whereas the Z axis will measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, 00h with 16 bit representation, data expressed as 2's complement number). A deviation from ideal value in this case is called Zero-*g* offset. Offset is to some extent a result of stress to a precise MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level change vs. temperature". The Zero-*g* level of an individual sensor is stable over lifetime. The Zero-*g* level tolerance describes the range of Zero-*g* levels of a population of sensors.

### 4.1.3 Self test

Self test allows to test the mechanical and electric part of the sensor, allowing the seismic mass to be moved by means of an electrostatic test-force. The self-test function is off when the self-test bit of CTRL_REG1 (control register 1) is programmed to '0'. When the self-test bit of CTRL_REG1 is programmed to '1'an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which is related to the selected full scale and depending on the Supply voltage through the device sensitivity. When Self Test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside *Table 3* or *4* then the sensor is working properly and the parameters of the interface chip are within the defined specification.

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# 5 Functionality

The AIS226DS is a high performance, low-power, digital output 2-axes linear accelerometer packaged in a SOIC package. The complete device includes a sensing element and an IC interface able to take the information from the sensing element and to provide a signal to the external world through an SPI serial interface.

## 5.1 Sensing element

A proprietary process is used to create a surface micro-machined accelerometer. The technology allows to carry out suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. To be compatible with the traditional packaging techniques a cap is placed on top of the sensing element to avoid blocking the moving parts during the moulding phase of the plastic encapsulation.

When an acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the sense capacitor.

At steady state the nominal value of the capacitors are few pF and when an acceleration is applied the maximum variation of the capacitive load is up to 100 fF.

## 5.2 IC interface

The complete measurement chain is composed by a low-noise capacitive amplifier which converts into an analog voltage the capacitive unbalancing of the MEMS sensor and by three ΣΔ analog-to-digital converters, one for each axis, that translate the produced signal into a digital bitstream.

The ΣΔ converters are coupled with dedicated reconstruction filters which remove the high frequency components of the quantization noise and provide low rate and high resolution digital words.

The charge amplifier and the ΣΔ converters are operated respectively at 61.5 kHz and 20.5 kHz.

The data rate at the output of the reconstruction depends on the user selected decimation factor (DF) and spans from 40 Hz to 2560 Hz.

The acceleration data may be accessed through an SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The AIS226DS features a data-ready signal (RDY) which indicates when a new set of measured acceleration data is available thus simplifying data synchronization in digital system employing the device itself.

The AIS226DS may also be configured to generate an inertial wake-up, direction detection and free-fall interrupt signal accordingly to a programmed acceleration event along the enabled axes.

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## 5.3 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and Zero-*g* level (Off).

The trimming values are stored inside the device by a non volatile structure. Any time the device is turned on, the trimming parameters are downloaded into the registers to be employed during the normal operation. This allows the user to employ the device without further calibration.

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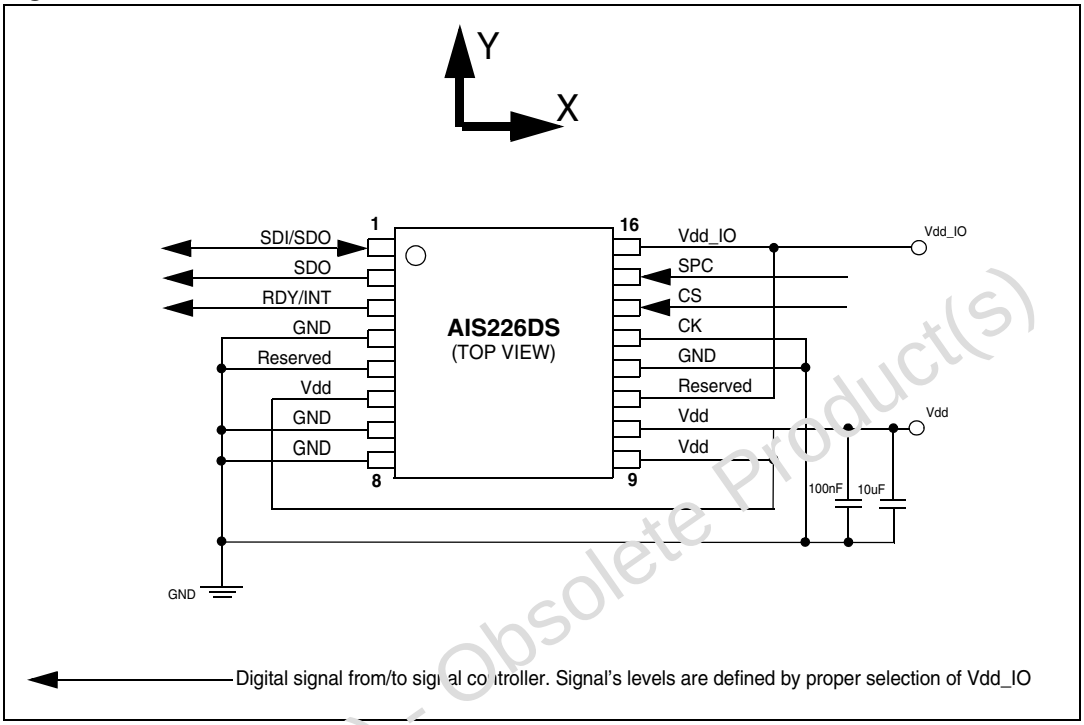
# 6 Application hints

**Figure 4. AIS226DS electrical connection**




The device core is supplied through Vdd line while the I/O pads are supplied through Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF Al) should be placed as near as possible to the pin 3 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 4*). It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses. In this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data is selectable and accessible through the SPI interface. The design of the application board should take in consideration that the AIS226DS is equipped also with an $I^2C$ compatible interface that it is activated when the signal on CS pin is high (logic:1).

The functions, the thresholds and the timing of the interrupt pin (INT) can be completely programmed by the user through the SPI interface.

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# 7 Digital interface

The registers embedded inside the AIS226DS may be accessed through SPI serial interface. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

**Table 7. Serial interface pin description**

| PIN name | Pin description |
|---|---|
| CS | Chip select (logic 0: SPI enabled, logic 1: SPI disabled) |
| SPC | SPI serial port clock |
| SDI/SDO | SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) |
| SDO | SPI serial data output (SDO) |

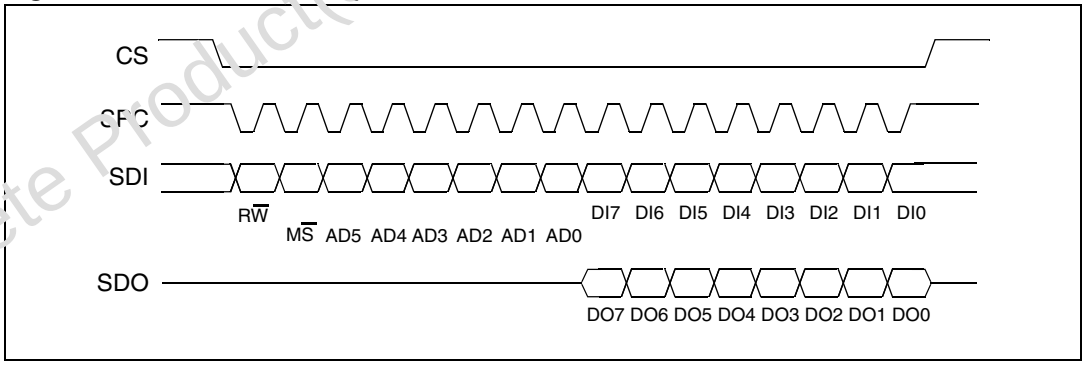
The embedded registers may be accessed also through an $I^2C$ interface. For $I^2C$ operation refer to LIS3LV02DQ datasheet.

## 7.1 SPI bus interface

The AIS226DS SPI is a bus slave. The SPI allows to write and read the registers of the device.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

**Figure 5. Read and write protocol**




**CS** is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end.

**SPC** is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission).

**SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiple of 8 in case of multiple byte read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge

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of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

***bit 0***: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

***bit 1***: M$\overline{S}$ bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address will be auto increased in multiple read/write commands.

***bit 2-7***: address AD(5:0). This is the address field of the indexed register.

***bit 8-15***: data DI(7:0) (write mode). This is the data that will be written into the device (MSb first).

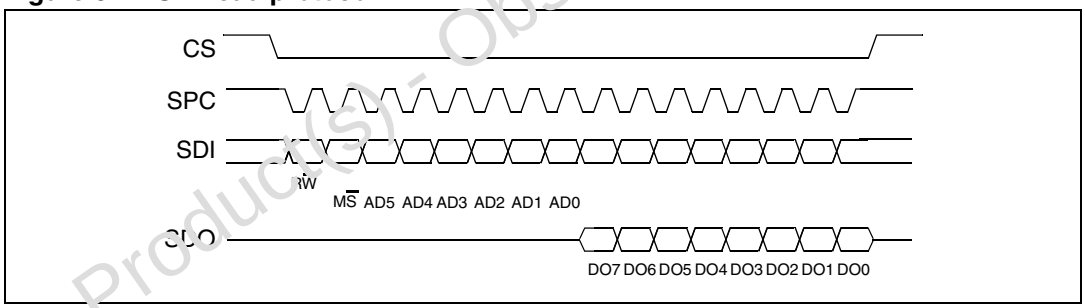
***bit 8-15***: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When M$\overline{S}$ bit is 0 the address used to read/write data remains the same for every block. When M$\overline{S}$ bit is '1' the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

### 7.1.1 SPI read

**Figure 6. SPI read protocol**




The SPI Read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

***bit 0***: READ bit. The value is 1.

***bit 1***: M$\overline{S}$ bit. When 0 do not increment address, when 1 increment address in multiple reading.

***bit 2-7***: address AD(5:0). This is the address field of the indexed register.

***bit 8-15***: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

***bit 16-...*** : data DO(...-8). Further data in multiple byte reading.

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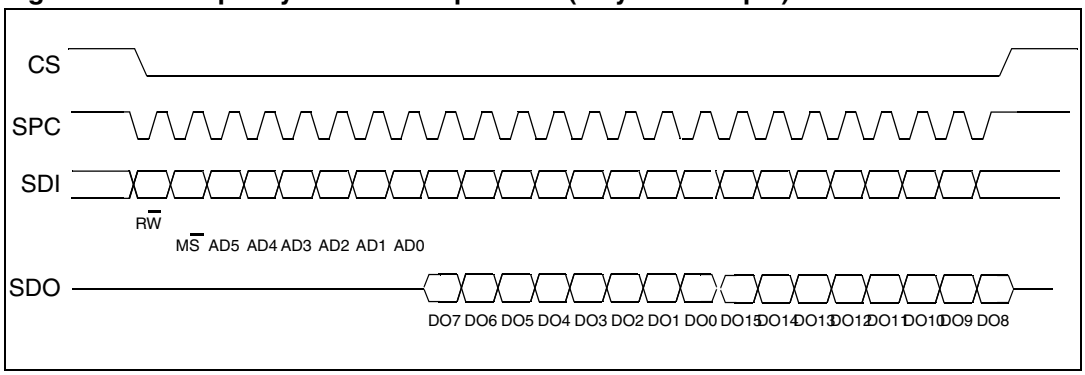
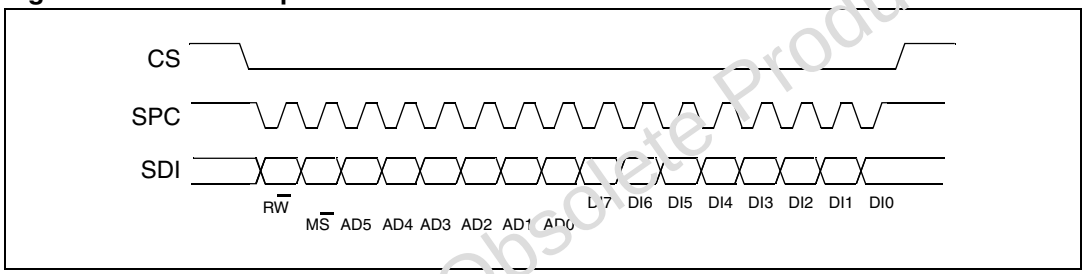
**Figure 7. Multiple bytes SPI read protocol (2 bytes example)**




## 7.1.2 SPI Write

**Figure 8. SPI Write protocol**




The SPI Write command is performed with 16 clock pulses. Multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

***bit 0***: WRITE bit. The value is 0.

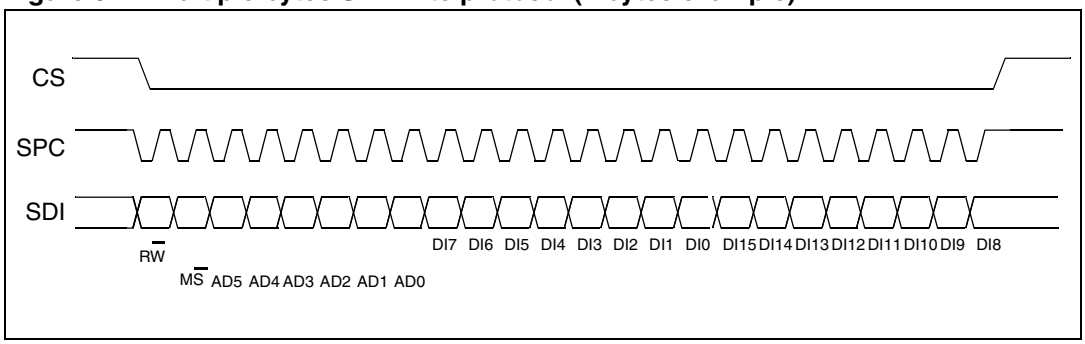
***bit 1***: MS bit. When 0 do not increment address, when 1 increment address in multiple writing.

***bit 2 -7***: address AD(5:0). This is the address field of the indexed register.

***bit 8-15***: data DI(7:0) (write mode). This is the data that will be written inside the device (MSb first).

***bit 16-...*** : data DI(...-8). Further data in multiple byte writing.

**Figure 9. Multiple bytes SPI write protocol (2 bytes example)**

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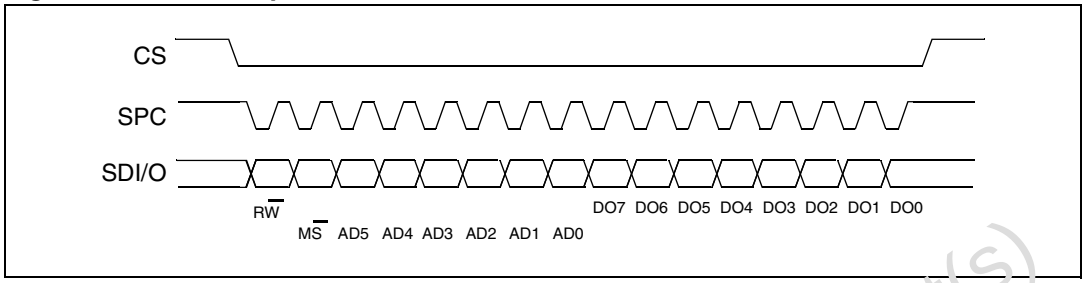
### 7.1.3 SPI Read in 3-wires mode

3-wires mode is entered by setting to '1' bit SIM (SPI serial interface mode selection) in CTRL_REG2.

**Figure 10. SPI read protocol in 3-wires mode**




The SPI read command is performed with 16 clock pulses:

***bit 0***: READ bit. The value is 1.

***bit 1***: MS bit. When 0 do not increment address, when 1 increment address in multiple reading.

***bit 2-7***: address AD(5:0). This is the address field of the indexed register.

***bit 8-15***: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

Multiple read command is also available in 3-wires mode.

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# 8 Register mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related address.

**Table 8. Registers address map**

| Register name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Binary | Hex | | |
| | rw | 0000000 - 0001110 | 00 - 0E | | Reserved |
| WHO_AM_I | r | 0001111 | 0F | 00111010 | Dummy register |
| | rw | 0010000 - 0010101 | 10 - 15 | | Reserved |
| OFFSET_X | rw | 0010110 | 16 | Calibration | Loaded at boot |
| OFFSET_Y | rw | 0010111 | 17 | Calibration | Loaded at boot |
| | | 0011000 | 18 | | Reserved |
| GAIN_X | rw | 0011001 | 19 | Calibration | Loaded at boot |
| GAIN_Y | rw | 0011010 | 1A | Calibration | Loaded at boot |
| | | 0011011 | 1B | | Reserved |
| | | 0011100 -0011111 | 1C-1F | | Reserved |
| CTRL_REG1 | rw | 0100000 | 20 | 00000111 | |
| CTRL_REG2 | rw | 0100001 | 21 | 00000000 | |
| CTRL_REG3 | rw | 0100010 | 22 | 00001000 | |
| HP_FILTER RESET | r | 0100011 | 23 | dummy | Dummy register |
| | | 0100100-0100110 | 24-26 | | Not used |
| STATUS_REG | rw | 0100111 | 27 | 00000000 | |
| OUTX_L | r | 0101000 | 28 | output | |
| OUTX_H | r | 0101001 | 29 | output | |
| OUTY_L | r | 0101010 | 2A | output | |
| OUTY_H | r | 0101011 | 2B | output | |
| | r | 0101100 | 2C | | Reserved |
| | r | 0101101 | 2D | | Reserved |
| | r | 0101110 | 2E | | Reserved |
| | | 0101111 | 2F | | Not used |
| FF_WU_CFG | rw | 0110000 | 30 | 00000000 | |
| FF_WU_SRC | rw | 0110001 | 31 | 00000000 | |
| FF_WU_ACK | r | 0110010 | 32 | dummy | Dummy register |
| | | 0110011 | 33 | | Not used |
| FF_WU_THS_L | rw | 0110100 | 34 | 00000000 | |

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**Table 8. Registers address map (continued)**

| Register name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Binary | Hex | | |
| FF_WU_THS_H | rw | 0110101 | 35 | 00000000 | |
| FF_WU_DURATION | rw | 0110110 | 36 | 00000000 | |
| | | 0110111 | 37 | | Not used |
| DD_CFG | rw | 0111000 | 38 | 00000000 | |
| DD_SRC | rw | 0111001 | 39 | 00000000 | |
| DD_ACK | r | 0111010 | 3A | dummy | Dummy register |
| | | 0111011 | 3B | | Not used |
| DD_THSI_L | rw | 0111100 | 3C | 00000000 | |
| DD_THSI_H | rw | 0111101 | 3D | 00000000 | |
| DD_THSE_L | rw | 0111110 | 3E | 00000000 | |
| DD_THSE_H | rw | 0111111 | 3F | 00000000 | |
| | | 1000000-1111111 | 40-7F | | Reserved |

Registers marked as *Reserved* must not be changed. The writing to those registers may cause permanent damages to the device

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

Obsolete Product(s) - Obsolete Product(s)

# 9 Register description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration data. The registers *9.2* to *9.27* contain the factory calibration values, it is not necessary to change their value for normal device operation.

## 9.1 WHO_AM_I (0Fh)

**Table 9. Register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| W7 | W6 | W5 | W4 | W3 | W2 | W1 | W0 |

**Table 10. Register description**

| | |
|---|---|
| W7, W0 | AIS226DS physical address equal to 3Ah |

Addressing this register the physical address of the device is returned. For AIS226DS the physical address assigned in factory is 3Ah.

## 9.2 OFFSET_X (16h)

**Table 11. OFFSET_X register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| OX7 | OX6 | OX5 | OX4 | OX3 | OX2 | OX1 | OX0 |

**Table 12. OFFSET_X register description**

| | |
|---|---|
| OX7, OX0 | Digital offset trimming for X-Axis |

## 9.3 OFFSET_Y (17h)

**Table 13. OFFSET_Y register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| OY7 | OY6 | OY5 | OY4 | OY3 | OY2 | OY1 | OY0 |

**Table 14. OFFSET_Y register description**

| | |
|---|---|
| OY7, OY0 | Digital offset trimming for Y-Axis |

## 9.4 GAIN_X (19h)

**Table 15. GAIN_X register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| GX7 | GX6 | GX5 | GX4 | GX3 | GX2 | GX1 | GX0 |

**Table 16. GAIN_X register description**

| | |
|---|---|
| GX7, GX0 | Digital gain trimming for X-Axis |

Obsolete Product(s) - Obsolete Product(s)

## 9.5 GAIN_Y (1Ah)

**Table 17. GAIN_Y register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| GY7 | GY6 | GY5 | GY4 | GY3 | GY2 | GY1 | GY0 |

**Table 18. GAIN_Y register description**

| | |
|---|---|
| GY7, GY0 | Digital gain trimming for Y-Axis |

## 9.6 CTRL_REG1 (20h)

**Table 19. CTRL_REG1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PD1 | PD0 | DF1 | DF0 | ST | res | Yen | Xen |

**Table 20. CTRL_REG1 register description**

| | |
|---|---|
| PD1, PD0 | Power down control<br>(00: power-down mode; 01, 10, 11: device on) |
| DF1, DF0 | Decimation factor control<br>(00: decimate by 512; 01: decimate by 128; 10: decimate by 32; 11: decimate by 8) |
| ST | Self test enable<br>(0: normal mode; 1: self-test active) |
| Yen | Y-axis enable<br>(0: axis off; 1: axis on) |
| Xen | X-axis enable<br>(0: axis off; 1: axis on) |

**PD1, PD0** bit allows to turn the device out of power-down mode. The device is in power-down mode when PD1, PD0= “00” (default value after boot). The device is in normal mode when either PD1 or PD0 is set to 1.

**DF1, DF0** bit allows to select the data rate at which acceleration samples are produced. The default value is “00” which corresponds to a data-rate of 40 Hz. By changing the content of DF1, DF0 to “01”, “10” and “11” the selected data-rate will be set respectively equal to 160 Hz, 640 Hz and to 2560 Hz.

**ST** bit is used to activate the self test function. When the bit is set to one, an output change will occur to the device outputs (refer to table 2 and 3 for specification) thus allowing to check the functionality of the whole measurement chain.

**Yen** bit enables the Y-axis measurement channel when set to 1. The default value is 1.

**Xen** bit enables the X-axis measurement channel when set to 1. The default value is 1.

Obsolete Product(s) Obsolete Product(s)

## 9.7 CTRL_REG2 (21h)

**Table 21. CTRL_REG2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FS | BDU | BLE | BOOT | IEN | DRDY | SIM | DAS |

**Table 22. CTRL_REG2 register description**

| | |
|---|---|
| FS | Full scale selection<br>(0: ±2 *g*; 1: ±6 *g*) |
| BDU | Block data update<br>(0: continuous update; 1: output registers not updated between MSB and LSB reading) |
| BLE | Big/little endian selection<br>(0: little endian; 1: big endian) |
| BOOT | Reboot memory content |
| IEN | Interrupt ENable<br>(0: data ready on RDY pad; 1: interrupt events on RDY pad) |
| DRDY | Enable data-ready generation |
| SIM | SPI serial interface mode selection<br>(0: 4-wire interface; 1: 3-wire interface) |
| DAS | Data alignment selection<br>(0: 12 bit right justified; 1: 16 bit left justified) |

**FS** bit is used to select full scale value. After the device power-up the default full scale value is +/-2 *g*. In order to obtain a +/-6 *g* full scale it is necessary to set FS bit to '1'.

**BDU** bit is used to inhibit output registers update between the reading of upper and lower register parts. In default mode (BDU = '0') the lower and upper register parts are updated continuously. If it is not sure to read faster than output data rate, it is recommended to set BDU bit to '1'. In this way, after the reading of the lower (upper) register part, the content of that output registers is not updated until the upper (lower) part is read too.
This feature avoids reading LSB and MSB related to different samples.

**BLE** bit is used to select Big Endian or Little Endian representation for output registers. In Big Endian's one MSB acceleration value is located at addresses 28h (X-axis), 2Ah (Y-axis) and 2Ch (Z-axis) while LSB acceleration value is located at addresses 29h (X-axis), 2Bh (Y-axis) and 2Dh (Z-axis). In Little Endian representation (Default, BLE='0') the order is inverted (refer to data register description for more details).

**BOOT** bit is used to refresh the content of internal registers stored in the flash memory block. At the device power up the content of the flash memory block is transferred to the internal registers related to trimming functions to permit a good behavior of the device itself. If for any reason the content of trimming registers was changed it is sufficient to use this bit to restore correct values. When BOOT bit is set to '1' the content of internal flash is copied inside corresponding internal registers and it is used to calibrate the device. These values are factory trimmed and they are different for every accelerometer. They permit a good behavior of the device and normally they have not to be changed. At the end of the boot process the BOOT bit is set again to '0'.

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**IEN** bit is used to switch the value present on data-ready pad between Data-Ready signal and Interrupt signal. At power up the Data-ready signal is chosen. It is however necessary to modify DRDY bit to enable Data-Ready signal generation.

**DRDY** bit is used to enable Data-Ready (RDY/INT) pin activation. If DRDY bit is '0' (default value) on Data-Ready pad a '0' value is present. If a Data-Ready signal is desired it is necessary to set to '1' DRDY bit. Data-Ready signal goes to '1' whenever a new data is available for all the enabled axis. For example if Z-axis is disabled, Data-Ready signal goes to '1' when new values are available for both X and Y axis. Data-Ready signal comes back to '0' when all the registers containing values of the enabled axis are read. To be sure not to loose any data coming from the accelerometer data registers must be read before a new Data-Ready rising edge is generated. In this case Data-ready signal will have the same frequency of the data rate chosen.

**SIM** bit selects the SPI Serial Interface Mode. When SIM is '0' (default value) the 4-wire interface mode is selected. The data coming from the device are sent to SDO pad. In 3-wire interface mode output data are sent to SDA/SDI pad.

**DAS** bit permits to decide between 12 bit right justified and 16 bit left justified representation of data coming from the device. The first case is the default case and the most significant bits are replaced by the bit representing the sign.

## 9.8 CTRL_REG3 (22h)

**Table 23. CTRL_REG3 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ECK | HPDD | HPFF | FDS | res | res | CFS1 | CFS0 |

**Table 24. CTRL_REG3 register description**

| | |
|---|---|
| ECK | External Clock. Default value: 0<br>(0: clock from internal oscillator; 1: clock from external pad) |
| HPDD | High Pass filter enabled for Direction Detection. Default value: 0<br>(0: filter bypassed; 1: filter enabled) |
| HPFF | High Pass filter enabled for Free-Fall and Wake-Up. Default value: 0<br>(0: filter bypassed; 1: filter enabled) |
| FDS | Filtered Data Selection. Default value: 0<br>(0: internal filter bypassed; 1: data from internal filter) |
| CFS1, CFS0 | High-pass filter Cut-off Frequency Selection. Default value: 00<br>(00: Hpc=512<br>01: Hpc=1024<br>10: Hpc=2048<br>11: Hpc=4096) |

**FDS** bit enables (FDS=1) or bypass (FDS=0) the high pass filter in the signal chain of the sensor.

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**CFS1, CFS0** bits defines the coefficient Hpc to be used to calculate the -3dB cut-off frequency of the high pass filter:

$$f_{cutoff} = \frac{0.318}{Hpc} \cdot \frac{ODRx}{2}$$

## 9.9 HP_FILTER_RESET (23h)

Dummy register. Reading at this address zeroes instantaneously the content of the internal high pass-filter. Read data is not significant.

## 9.10 STATUS_REG (27h)

**Table 25. STATUS_REG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| YXOR | res | YOR | XOR | YXDA | res | YDA | XDA |

**Table 26. STATUS_REG register description**

| | |
|---|---|
| YXOR | X, Y axis data overrun |
| YOR | Y axis data overrun |
| XOR | X axis data overrun |
| ZYXDA | X, Y axis new data available |
| YDA | Y axis new data available |
| XDA | X axis new data available |

The content of this register is updated every ODR cycle, regardless of BDU bit value in CTRL_REG2.

## 9.11 OUTX_L (28h)

**Table 27. OUTX_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| XD7 | XD6 | XD5 | XD4 | XD3 | XD2 | XD1 | XD0 |

**Table 28. OUTX_L register description**

| | |
|---|---|
| XD7, XD0 | X axis acceleration data LSB |

In big endian mode (bit BLE in CTRL_REG2 set to '1') the content of this register is the MSB acceleration data and depends on bit DAS in CTRL_REG2 register as described in the following section.

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## 9.12 OUTX_H (29h)

**Table 29. OUTX_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| XD15 | XD14 | XD13 | XD12 | XD11 | XD10 | XD9 | XD8 |

**Table 30. OUTX_H register description**

| | |
|---|---|
| XD15, XD8 | X axis acceleration data MSB |

When reading the register in “14 bit right justified” mode the most significant bits (15:14) are replaced with bit 13 (i.e. XD15-XD14=XD13, XD13, XD13, XD13).

In big endian mode (bit BLE in CTRL_REG2 set to ‘1’) the content of this register is the LSB acceleration data.

## 9.13 OUTY_L (2Ah)

**Table 31. OUTY_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| YD7 | YD6 | YD5 | YD4 | YD3 | YD2 | YD1 | YD0 |

**Table 32. OUTY_L register description**

| | |
|---|---|
| YD7, YD0 | Y axis acceleration data LSB |

In big endian mode (bit BLE in CTRL_REG2 set to ‘1’) the content of this register is the MSB acceleration data and depends on bit DAS in CTRL_REG2 register as described in the following section.

## 9.14 OUTY_H (2Bh)

**Table 33. OUTY_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| YD15 | YD14 | YD13 | YD12 | YD11 | YD10 | YD9 | YD8 |

**Table 34. OUTY_H register description**

| | |
|---|---|
| YD15, YD8 | Y axis acceleration data MSB |

When reading the register in “14 bit right justified” mode the most significant bits (15:14) are replaced with bit 11 (i.e. YD15-YD14=YD13, YD13, YD13, YD13).

In big endian mode (bit BLE in CTRL_REG2 set to ‘1’) the content of this register is the LSB acceleration data.

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## 9.15 FF_WU_CFG (30h)

**Table 35. FF_WU_CFG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| AOI | LIR | res | res | YHIE | YLIE | XHIE | XLIE |

**Table 36. FF_WU_CFG register description**

| | |
|---|---|
| AOI | And/Or combination of Interrupt events. Default value: 0.<br>(0: OR combination of interrupt events;<br>1: AND combination of interrupt events) |
| LIR | Latch interrupt request. Default value: 0.<br>(0: interrupt request not latched;<br>1: interrupt request latched) |
| YHIE | Enable Interrupt request on Y High event. Default value: 0.<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| YLIE | Enable Interrupt request on Y Low event. Default value: 0.<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |
| XHIE | Enable Interrupt request on X High event. Default value: 0.<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| XLIE | Enable Interrupt request on X Low event. Default value: 0.<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |

Free-fall and inertial wake-up configuration register.

## 9.16 FF_WU_SRC (31h)

**Table 37. FF_WU_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | IA | res | res | YH | YL | XH | XL |

**Table 38. FF_WU_SRC register description**

| | |
|---|---|
| IA | Interrupt Active. Default value: 0<br>(0: no interrupt has been generated;<br>1: one or more interrupt events have been generated) |
| YH | Y High. Default value: 0<br>(0: no interrupt; 1: Y High event has occurred) |
| YL | Y Low. Default value: 0<br>(0: no interrupt; 1: Y Low event has occurred) |

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Table 38. FF_WU_SRC register description (continued)

| | |
|---|---|
| XH | X High. Default value: 0<br>(0: no interrupt; 1: X High event has occurred) |
| XL | X Low. Default value: 0<br>(0: no interrupt; 1: X Low event has occurred) |

## 9.17 FF_WU_ACK (32h)

Dummy register. If LIR bit in FF_WU_CFG register is set to '1', a reading at this address refreshes the FF_WU_SRC register. Read data is not significant.

## 9.18 FF_WU_THS_L (34h)

Table 39. FF_WU_THS_L register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| THS7 | THS6 | THS5 | THS4 | THS3 | THS2 | THS1 | THS0 |

Table 40. FF_WU_THS_L register description

| | |
|---|---|
| THS7, THS0 | Free-fall / inertial wake up acceleration threshold LSB |

## 9.19 FF_WU_THS_H (35h)

Table 41. FF_WU_THS_H register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| THS15 | THS14 | THS13 | THS12 | THS11 | THS10 | THS9 | THS8 |

Table 42. FF_WU_THS_H register description

| | |
|---|---|
| THS15, THS8 | Free-fall / inertial wake up acceleration threshold MSB |

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## 9.20 FF_WU_DURATION (36h)

**Table 43. FF_WU_DURATION register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FWD7 | FWD6 | FWD5 | FWD4 | FWD3 | FWD2 | FWD1 | FWD0 |

**Table 44. FF_WU_DURATION register description**

| | |
|---|---|
| FWD7, FWD0 | Minimum duration of the Free-fall/Wake-up event |

This register sets the minimum duration of the free-fall/wake-up event to be recognized.

$$Duration(s) = \frac{FF\_WU\_DURATION\ (Dec)}{ODR}$$

## 9.21 DD_CFG (38h)

**Table 45. DD_CFG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| IEND | LIR | res | res | YHIE | YLIE | XHIE | XLIE |

**Table 46. DD_CFG register description**

| | |
|---|---|
| IEND | Interrupt enable on direction change. Default value: 0<br>(0: disabled;<br>1: interrupt signal enabled) |
| LIR | Latch Interrupt request into DD_SRC reg with the DD_SRC reg cleared by reading DD_ACK reg. Default value: 0.<br>(0: interrupt request not latched;<br>1: interrupt request latched) |
| YHIE | Enable interrupt generation on Y high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| YLIE | Enable interrupt generation on Y low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |
| XHIE | Enable interrupt generation on X high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| XLIE | Enable interrupt generation on X low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |

Direction-detector configuration register.

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## 9.22 DD_SRC (39h)

**Table 47. DD_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | IA | res | res | YH | YL | XH | XL |

**Table 48. DD_SRC register description**

| | |
|---|---|
| IA | Interrupt event from direction change.<br>(0: no direction changes detected;<br>1: direction has changed from previous measurement) |
| YH | Y High. Default value: 0<br>(0: Y below THSI threshold;<br>1: Y accel. exceeding THSE threshold along positive direction of acceleration axis) |
| YL | Y Low. Default value: 0<br>(0: Y below THSI threshold;<br>1: Y accel. exceeding THSE threshold along negative direction of acceleration axis) |
| XH | X High. Default value: 0<br>(0: X below THSI threshold;<br>1: X accel. exceeding THSE threshold along positive direction of acceleration axis) |
| XL | X Low. Default value: 0<br>(0: X below THSI threshold;<br>1: X accel. exceeding THSE threshold along negative direction of acceleration axis) |

Direction detector source register.

## 9.23 DD_ACK (3Ah)

Dummy register. If LIR bit in DD_CFG register is set to '1', a reading at this address refreshes the DD_SRC register. Read data is not significant.

## 9.24 DD_THSI_L (3Ch)

**Table 49. DD_THSI_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| THSI7 | THSI6 | THSI5 | THSI4 | THSI3 | THSI2 | THSI1 | THSI0 |

**Table 50. DD_THSI_L register description**

| | |
|---|---|
| THSI7, THSI0 | Direction detection internal threshold LSB |

## 9.25 DD_THSI_H (3Dh)

**Table 51. DD_THSI_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| THSI15 | THSI14 | THSI13 | THSI12 | THSI11 | THSI10 | THSI9 | THSI8 |

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Table 52. DD_THSI_H register description

| | |
|---|---|
| THSI15, THSI8 | Direction detection internal threshold MSB |

## 9.26 DD_THSE_L (3Eh)

Table 53. DD_THSE_L register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| THSE7 | THSE6 | THSE5 | THSE4 | THSE3 | THSE2 | THSE1 | THSE0 |

Table 54. DD_THSE_L register description

| | |
|---|---|
| THSE7, THSE0 | Direction detection external threshold LSB |

## 9.27 DD_THSE_H (3Fh)

Table 55. DD_THSE_H register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| THSE15 | THSE14 | THSE13 | THSE12 | THSE11 | THSE10 | THSE9 | THSE8 |

Table 56. DD_THSE_H register description

| | |
|---|---|
| THSE15, THSE8 | Direction detection external threshold MSB |

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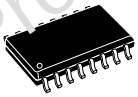
# 10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

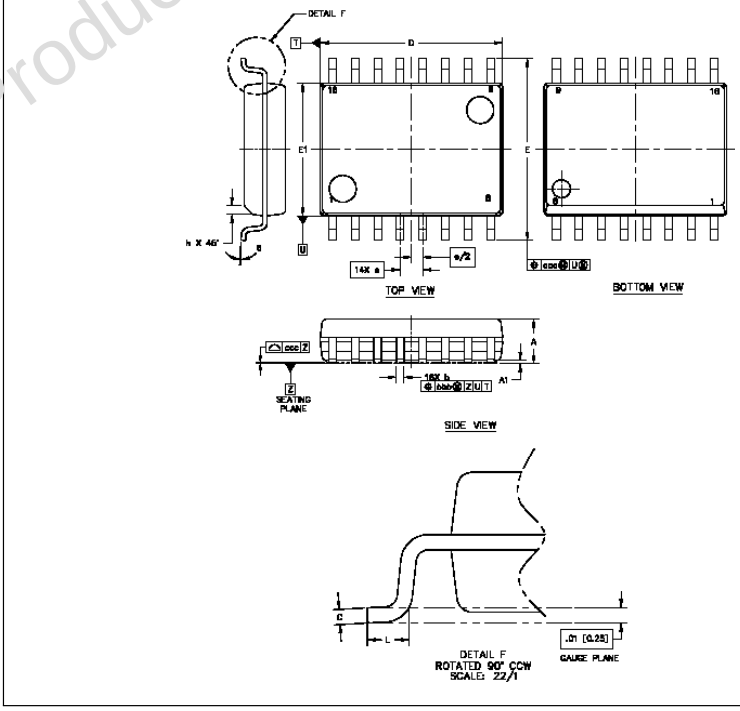
**Figure 11. SO16W mechanical data and package dimensions**

| Dimensions | | | |
|---|---|---|---|
| Ref. | mm | | |
| | Min. | Typ. | Max. |
| A | 2.36 | | 2.64 |
| A1 | 0.10 | | 0.25 |
| b | 0.35 | | 0.49 |
| c | 0.23 | | 0.33 |
| D | 10.15 | | 10.45 |
| E1 | 7.39 | | 7.59 |
| E | 10.05 | | 10.55 |
| e | | 1.27 | |
| L | 0.41 | | 1.00 |
| l | 0.25 | | 0.76 |
| θ | 0° | | 7° |
| qqq | | 0.25 | |
| bbb | | 0.25 | |
| ccc | | 0.10 | |

Outline and mechanical data



SO16W

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# 11 Revision history

Table 57. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 13-Nov-2008 | 1 | Initial release. |
| 30-Nov-2009 | 2 | Updated *Table 3 on page 9*. |
| 09-Apr-2010 | 3 | Updated *Section 6: Application hints*. |

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