# =Preliminary=

# AK8975/AK8975B

## 3-axis Electronic Compass

## 1. Features

A 3-axis electronic compass IC with high sensitive Hall sensor technology.
Best adapted to pedestrian city navigation use for cell phone and other portable appliance.

Functions:

- 3-axis magnetometer device suitable for compass application
- Built-in A to D Converter for magnetometer data out
- 13 bit data out for each 3 axis magnetic components
  - Sensitivity: 0.3 μT / LSB typ.
- Serial interface
  - $I^2C$ bus interface.
    Standard mode and Fast mode compliant with Philips I2C specification Ver.2.1
  - 4-wire SPI
- Operation mode:
  Power-down mode, Single Measurement mode, Self test mode and Fuse access mode.
- DRDY function for measurement data ready
- Magnetic sensor overflow monitor function
- Built-in oscillator for internal clock source
- Power on Reset circuit
- Self test function with built-in internal magnetic field generator

Operating temperatures:

- -30°C to +85°C

Operating supply voltage:

- Analog power supply +2.4V to +3.6V
- Digital Interface supply +1.65V to analog power supply voltage.

Current consumption:

- Power-down: 10 μA max.
- Measurement:
  - Average power consumption at 8 Hz repetition rate: 300 μA typ.

Package:

AK8975 16-pin QFN package: 4.0 mm × 4.0 mm × 0.75 mm
AK8975B 14-pin WL-CSP (BGA): 2.0 mm × 2.0 mm × 0.65 mm

# 2. Overview

AK8975/B is 3-axis electronic compass IC with high sensitive Hall sensor technology.
Small package of AK8975/B incorporates magnetic sensors for detecting terrestrial magnetism in the X-axis, Y-axis, and Z-axis, a sensor driving circuit, signal amplifier chain, and an arithmetic circuit for processing the signal from each sensor. Self test function is also incorporated. From its compact foot print and thin package feature, it is suitable for map heading up purpose in GPS-equipped cell phone to realize pedestrian navigation function.

AK8975/B has the following features:

(1) Silicon monolithic Hall-effect magnetic sensor with magnetic concentrator realizes 3-axis magnetometer on a silicon chip. Analog circuit, digital logic, power block and interface block are also integrated on a chip.

(2) Enhanced architecture of signal processor realizes wide dynamic measurement range and high resolution with lower current consumption.

| | |
|---|---|
| Output data resolution: | 13 bit (0.3 μT / LSB) |
| Measurement range: | ±1200 μT |
| Average power consumption at 8Hz repetition rate: | 300 μA typ. |

(3) Digital serial interface
- $I^2C$ bus interface to control AK8975/B functions and to read out the measured data by external CPU. A dedicated power supply for $I^2C$ bus interface can work in low-voltage apply as low as 1.65V.
- 4-wire SPI (Serial port interface) is also supported. A dedicated power supply for SPI interface can work in low-voltage apply as low as 1.65V.

(4) DRDY pin and register inform to system that measurement is end and set of data in registers are ready to be read.

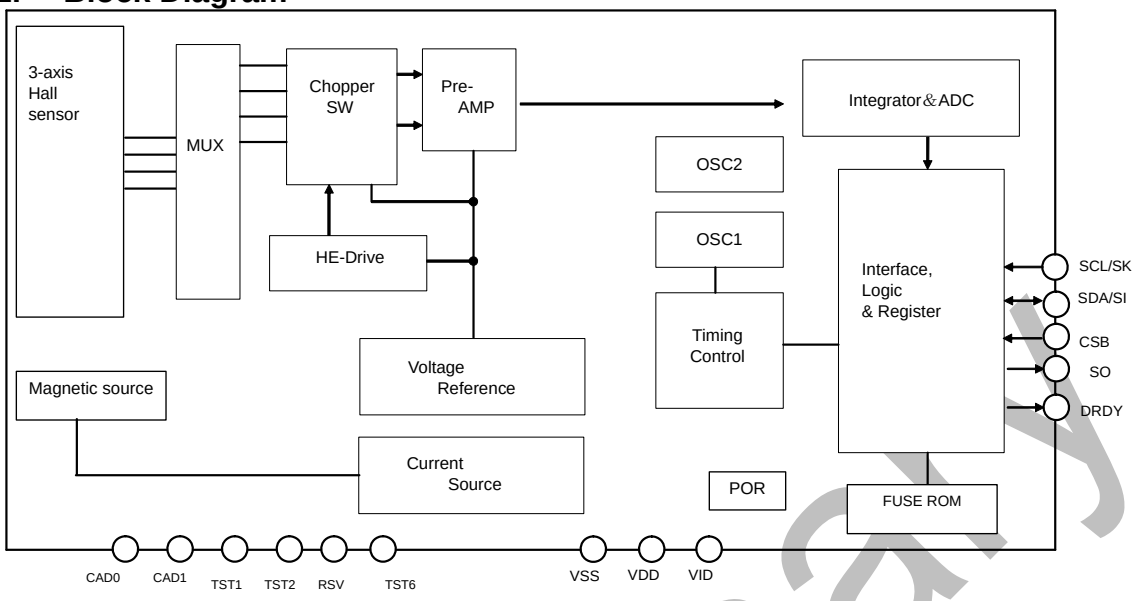
(5) Device is worked by on-chip oscillator so no external clock source is necessary.

(6) Self test function with internal magnetic source to confirm magnetic sensor operation on end products.

# 3. Table of Contents

# 4. Circuit Configuration

## 4.1. Block Diagram




## 4.2. Block Function

| Block | Function |
|---|---|
| 3-axis Hall sensor | Monolithic Hall elements. |
| MUX | Multiplexer for selecting Hall elements. |
| Chopper SW | Performs chopping. |
| HE-Drive | Magnetic sensor drive circuit for constant-current driving of sensor |
| Pre-AMP | Variable-gain differential amplifier used to amplify the magnetic sensor signal. |
| Integrator & ADC | Integrates and amplifies pre-AMP output and performs analog-to-digital conversion. |
| OSC1 | Generates an operating clock for sensor measurement.<br>6.144MHz(typ) |
| OSC2 | Generates a clock for measurement timing control<br>128kHz(typ) |
| POR | Power On Reset circuit. Generates reset signal on rising edge of VDD. |
| Interface Logic | Exchanges data with an external CPU.<br>DRDY pin indicates sensor measurement end and data is ready to be read.<br>$I^2C$ bus interface using two pins, namely, SCL and SDA. Standard mode and Fast mode are supported. The low-voltage specification can be supported by applying 1.65V to the VID pin.<br>4-wire SPI is also supported by SK, SI, SO and CSB pins.<br>4-wire SPI works in VID pin voltage down to 1.65V, too. |
| Timing Control | Generates a timing signal required for internal operation from a clock generated by the OSC1. |
| Magnetic Source | Generates magnetic field for self test of magnetic sensor. |
| Current Source | Generates current for generating magnetic field. |
| FUSE ROM | Fuse for adjustment |

## 4.3. Pin Function

| Pin No. | | Pin name | I/O | Power supply system | Type | Function |
|---|---|---|---|---|---|---|
| 75 | 75B | | | | | |
| 2 | A2 | CSB | I | VID | CMOS | Chip select pin for 4-wire SPI.<br>"L" active. Connect to VID when selecting $I^2C$ bus interface. |
| 4 | A3 | SCL | I | VID | CMOS | When the $I^2C$ bus interface is selected (CSB pin is connected to VID)<br>SCL: Control data clock input pin<br>Input: Schmidt trigger |
| | | SK | | | | When the 4-wire SPI is selected<br>SK: Serial clock input pin |
| 5 | B3 | SDA | I/O | VID | CMOS | When the $I^2C$ bus interface is selected (CSB pin is connected to VID)<br>SDA: Control data input/output pin<br>Input: Schmidt trigger, Output: Open drain |
| | | SI | I | | | When the 4-wire SPI is selected<br>SI: Serial data input pin |
| 6 | B4 | SO | O | VID | CMOS | When the $I^2C$ bus interface is selected (CSB pin is connected to VID)<br>Hi-Z output. Keep this pin electrically nonconnected, or connected to VSS. |
| | | | | | | When the 4-wire SPI is selected<br>Serial data output pin |
| 10 | C3 | DRDY | O | VID | CMOS | Data ready signal output pin. Active "H".<br>Informs measurement ended and data is ready to be read. |
| 7 | C4 | VID | - | - | Power | Digital interface positive power supply pin. |
| 16 | B1 | VDD | - | - | Power | Analog Power supply pin. |
| 15 | C1 | VSS | - | - | Power | Ground pin. |
| 13 | D1 | CAD0 | I | VDD | CMOS | When the $I^2C$ bus interface is selected (CSB pin is connected to VID)<br>CAD0: Slave address 0 input pin<br>When the 4-wire serial interface is selected<br>Connect to VSS. |
| 11 | D2 | CAD1 | I | VDD | CMOS | When the $I^2C$ bus interface is selected (CSB pin is connected to VID)<br>CAD1: Slave address 1 input pin<br>When the 4-wire serial interface is selected<br>Connect to VSS. |
| 8 | - | NC1 | O | VID | ANALOG | Hi-Z output. Keep this pin electrically nonconnected. |
| 12 | - | NC2 | O | VID | ANALOG | Hi-Z output. Keep this pin electrically nonconnected. |
| 3 | A4 | RSV | I | VID | CMOS | Reserved<br>Keep this pin electrically nonconnected or connect to VSS. |
| 1 | A1 | TST1 | O | VDD | ANALOG | Hi-Z output. Keep this pin electrically nonconnected. |
| 9 | D4 | TST6 | O | VDD | ANALOG | Hi-Z output. Keep this pin electrically nonconnected. |
| 14 | C2 | TST2 | O | VDD | ANALOG | Hi-Z output. Keep this pin electrically nonconnected. |

# 5. Overall Characteristics

## 5.1. Absolute Maximum Ratings

VSS=0V

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Power supply voltage (VDD, VID) | V+ | -0.3 | +6.5 | V |
| Input voltage | VIN | -0.3 | (V+)+0.3 | V |
| Input current | IIN | - | ±10 | mA |
| Storage temperature | TST | -40 | +125 | °C |

(Note 1) If the device is used in conditions exceeding these values, the device may be destroyed. Normal operations are not guaranteed in such exceeding conditions.

## 5.2. Recommended Operating Conditions

VSS=0V

| Parameter | Remark | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating temperature | | Ta | -30 | | +85 | °C |
| Power supply voltage | VDD pin voltage | VDD | 2.4 | 3.0 | 3.6 | V |
| | VID pin voltage | VID | 1.65 | | VDD | V |

## 5.3. Electrical Characteristics

The following conditions apply unless otherwise noted:
VDD=2.4V to 3.6V, VID=1.65V to VDD, Temperature range=-30°C to 85°C

### 5.3.1. DC Characteristics

| Parameter | Symbol | Pin | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| High level input voltage 1 | VIH1 | CSB<br>SK<br>SI | | 70%VID | | | V |
| Low level input voltage 1 | VIL1 | | | | | 30%VID | V |
| High level input voltage 2 | VIH2 | SCL<br>SDA | | 70%VID | | VID+0.5 | V |
| Low level input voltage 2 | VIL2 | | | -0.5 | | 30%VID | V |
| High level input voltage 3 | VIH3 | CAD0<br>CAD1 | | 70%VDD | | | V |
| Low level input voltage 3 | VIL3 | | | | | 30%VDD | V |
| Input current | IIN | SCL<br>SK<br>SDA<br>SI<br>CSB | Vin=VSS or VID | -10 | | +10 | μA |
| Hysteresis input voltage (Note 2) | VHS | SCL<br>SDA | VID≥2V | 5%VID | | | V |
| | | | VID<2V | 10%VID | | | V |
| High level output voltage 1 | VOH1 | SO<br>DRDY | IOH≥-100μA (Note 5) | 80%VID | | | V |
| Low level output voltage 1 | VOL1 | | IOL≤+100μA (Note 5) | | | 20%VID | V |
| Low level output voltage 2 (Note 3)(Note 4) | VOL2 | SDA | IOL≤3mA VID≥2V | | | 0.4 | V |
| | | | IOL≤3mA VID<2V | | | 20%VID | V |
| Current consumption | IDD1 | VDD<br>VID | Power-down mode VDD=VID=2.5V | | TBD | 10 | μA |
| | IDD2 | | When magnetic sensor is driven VDD=VID=2.5V | | TBD | TBD | mA |

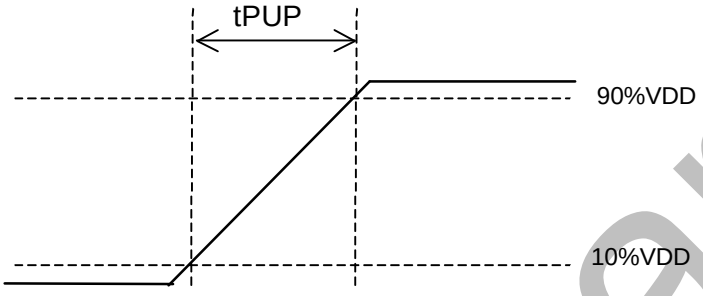
(Note 2) Schmitt trigger input (reference value for design)
(Note 3) Maximum load capacitance: 400pF (capacitive load of each bus line applied to the $I^2C$ bus interface)
(Note 4) Output is open-drain. Connect a pull-up resistor externally.
(Note 5) Load capacitance: 20pF

### 5.3.2. AC Characteristics

| Parameter | Symbol | Pin | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Power supply rise time effective for POR circuit (Note 6) | tPUP | VDD | Period of time from 10%VDD to 90%VDD (Note 7) | | | 200 | μs |
| Power-down mode transit time (Note 6) | | VDD | Period of time from 90%VDD at power-on to Power-down mode | | | TBD | μs |
| Wait time before mode setting | Twat | | | 100 | | | μs |

(Note 6) Reference value for design

(Note 7) Only when VDD meets this condition, POR circuit starts and resets AK8975/B. After reset, all registers are initialized and AK8975/B transits to Power-down mode.




### 5.3.3. Analog Circuit Characteristics

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Measurement data output bit | DBIT | | | 13 | | bit |
| Time for measurement | TSM | Single measurement mode | | 7.30 | | ms |
| Magnetic sensor sensitivity | BSE | Tc=25°C (Note 8) | TBD | 0.3 | TBD | μT/LSB |
| Magnetic sensor measurement range (Note 9) | BRG | Tc=25°C (Note 8) | ±1167 | ±1229 | ±1290 | μT |
| Magnetic sensor initial offset (Note 10) | | Tc=25°C | -1000 | | +1000 | LSB |

(Note 8) Value after sensitivity is adjusted using sensitivity fine adjustment data stored in Fuse ROM.

(Note 9) Reference value for design

(Note 10) Value of measurement data register on shipment without applying artificial magnetic field.

### 5.3.4. 4-wire SPI Interface

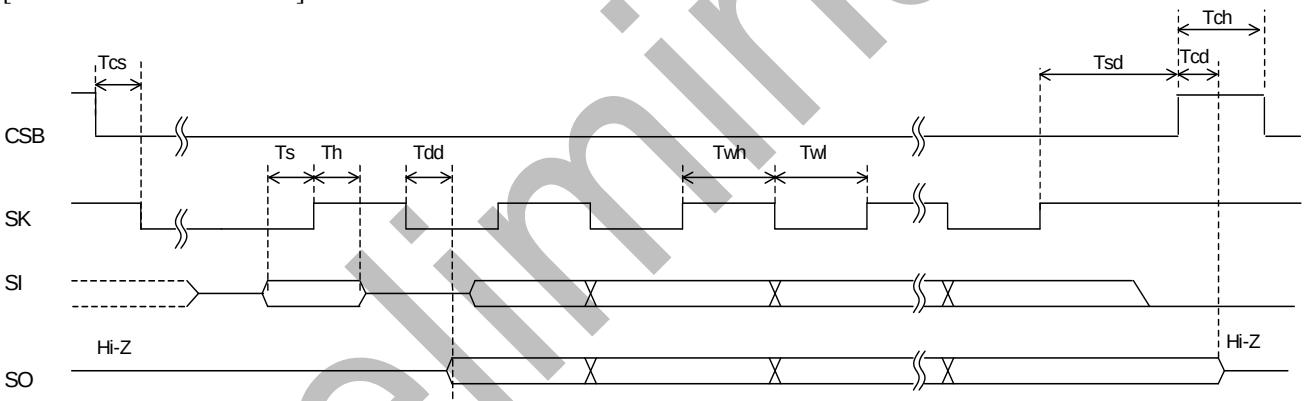
4-wire SPI interface is compliant with mode 3

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| CSB setup time | Tcs | | 50 | | | ns |
| Data setup time | Ts | | 50 | | | ns |
| Data hold time | Th | | 50 | | | ns |
| SK high time | Twh | VID≥2.5V | 100 | | | ns |
| | | 2.5V>VID≥1.65V | 150 | | | ns |
| SK low time | Twl | VID≥2.5V | 100 | | | ns |
| | | 2.5V>VID≥1.65V | 150 | | | ns |
| SK setup time | Tsd | | 50 | | | ns |
| SK to SO delay time (Note 11) | Tdd | | | | 50 | ns |
| CSB to SO delay time (Note 11) | Tcd | | | | 50 | ns |
| SK rise time (Note 12) | Tr | | | | 100 | ns |
| SK fall time (Note 12) | Tf | | | | 100 | ns |
| CSB high time | Tch | | 150 | | | ns |

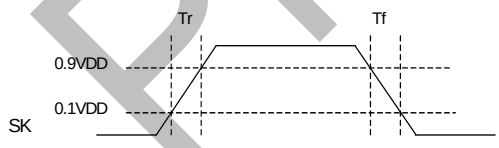
(Note 11) SO load capacitance: 20pF

(Note 12) These parameter values are sample values; not all values are measured.

[Four-wire serial interface]




[Rise time and fall time]



### 5.3.5. I2C Bus Interface

CSB pin = "H"

$I^2C$ bus interface is compliant with Standard mode and Fast mode. Standard/Fast mode is selected automatically by fSCL.

(1) Standard mode

fSCL≤100kHz

1.65V≤VID≤VDD

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| fSCL | SCL clock frequency | | | 100 | kHz |
| tHIGH | SCL clock "High" time | 4.0 | | | µs |
| tLOW | SCL clock "Low" time | 4.7 | | | µs |
| tR | SDA and SCL rise time | | | 1.0 | µs |
| tF | SDA and SCL fall time | | | 0.3 | µs |
| tHD:STA | Start Condition hold time | 4.0 | | | µs |
| tSU:STA | Start Condition setup time | 4.7 | | | µs |
| tHD:DAT | SDA hold time (vs. SCL falling edge) | 0 | | | µs |
| tSU:DAT | SDA setup time (vs. SCL rising edge) | 250 | | | ns |
| tSU:STO | Stop Condition setup time | 4.0 | | | µs |
| tBUF | Bus free time | 4.7 | | | µs |

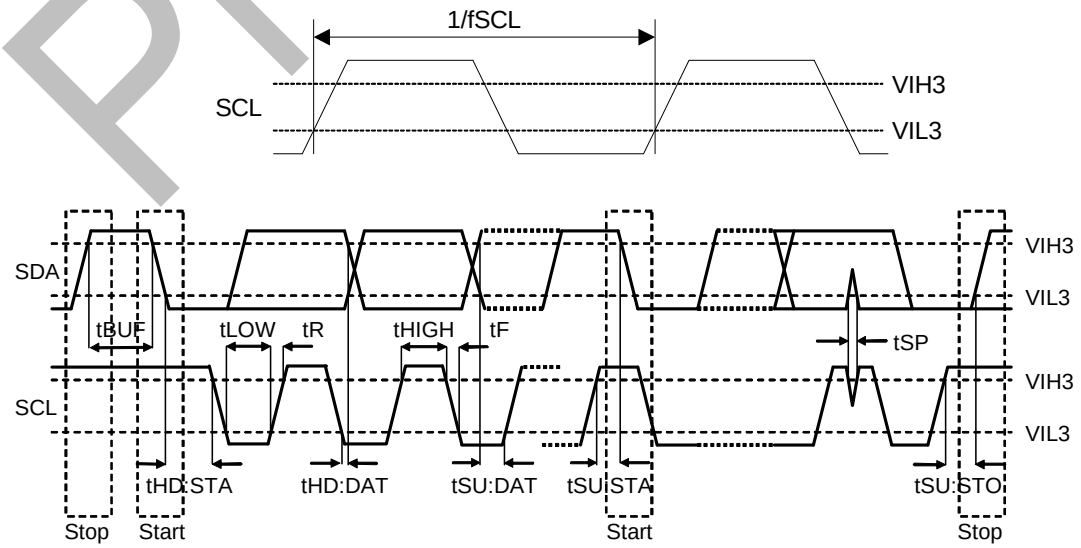
(2) Fast mode

100kHz<fSCL≤400kHz

1.65V≤VID≤VDD

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| fSCL | SCL clock frequency | | | 400 | kHz |
| tHIGH | SCL clock "High" time | 0.6 | | | µs |
| tLOW | SCL clock "Low" time | 1.3 | | | µs |
| tR | SDA and SCL rise time | | | 0.3 | µs |
| tF | SDA and SCL fall time | | | 0.3 | µs |
| tHD:STA | Start Condition hold time | 0.6 | | | µs |
| tSU:STA | Start Condition setup time | 0.6 | | | µs |
| tHD:DAT | SDA hold time (vs. SCL falling edge) | 0 | | | µs |
| tSU:DAT | SDA setup time (vs. SCL rising edge) | 100 | | | ns |
| tSU:STO | Stop Condition setup time | 0.6 | | | µs |
| tBUF | Bus free time | 1.3 | | | µs |
| tSP | Noise suppression pulse width | | | 50 | ns |

[$I^2C$ bus interface timing]



# 6. Functional Explanation

## 6.1. Power state

When VDD and VID is turned on from VDD=OFF (0V) and VID=OFF (0V), all registers in AK8975/B are initialized by POR circuit and AK8975/B transits to Power-down mode.

| VDD | VID | Power state |
|---|---|---|
| OFF (0V) | OFF (0V) | OFF (0V).<br>SCL, SDA should not exceed VID voltage. Other digital pins should be fixed to L(0V). |
| OFF (0V) | 1.65V to 3.6V | OFF (0V). It doesn't affect external interface. |
| 2.4V to 3.6V | OFF (0V) | OFF (0V). It consumes current same as Power-down mode.<br>SCL, SDA should not exceed VID voltage. Other digital pins should be fixed to L (0V). |
| 2.4V to 3.6V | 1.65V to VDD | ON |

Table 6.1

## 6.2. Reset functions

AK8975/B has two types of reset;

(1) Power on reset (POR)
When VDD reaches approximately 2V (reference value for design), POR (power on reset) circuit operates, and AK8975/B is reset.

(2) VID monitor
When VID is turned OFF (0V), AK8975/B is reset.

When AK8975/B is reset, all registers are initialized and AK8975/B transits to Power-down mode.

## 6.3. Operation Modes

AK8975/B has following four operation modes:

(1) Power-down mode
(2) Single measurement mode
(3) Self-test mode
(4) Fuse ROM access mode

By setting CNTL register MODE[3:0] bits, the operation set for each mode is started.
A transition from one mode to another is shown below.

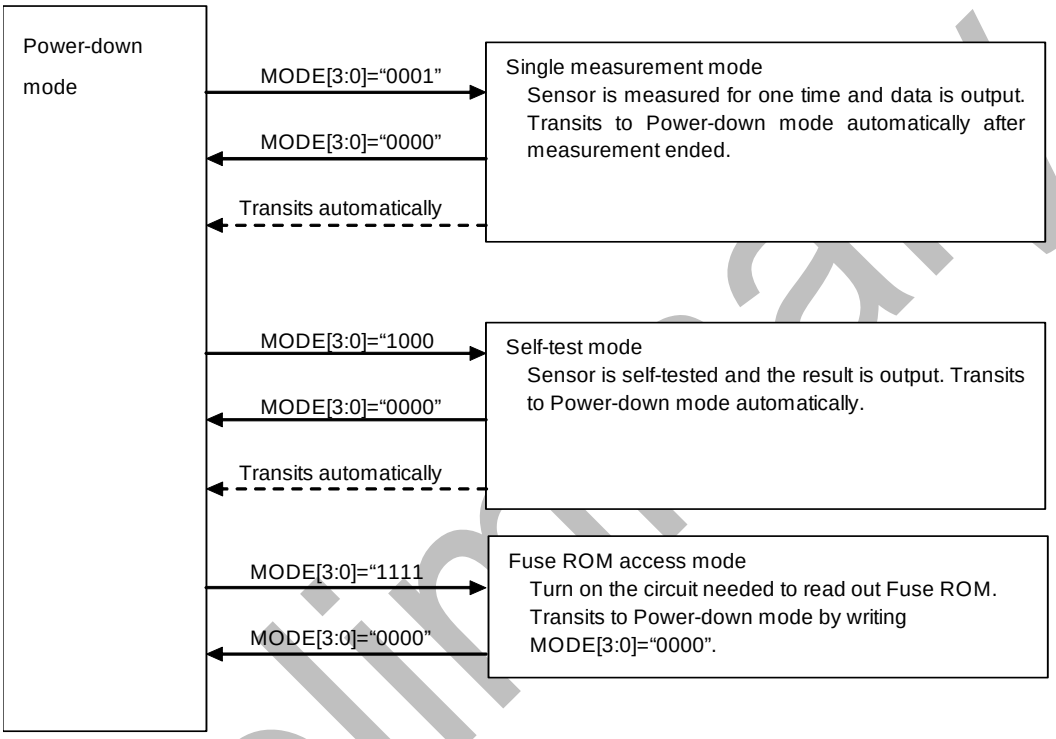



Figure 6.1 Operation modes

When power is turned ON, AK8975/B is in power-down mode. When MODE[3:0] is set, AK8975/B transits to the specified mode and starts operation. When user wants to change operation mode, transit to power-down mode first and then transit to other modes. After power-down mode is set, at least 100μs(Twat) is needed before setting another mode.

## 6.4. Description of Each Operation Mode

### 6.4.1. Power-down Mode

Power to all internal circuits is turned off. All registers are accessible in power-down mode. Fuse ROM address are accessible but correct data can not be read.
Data stored in read/write registers are remained.

### 6.4.2. Single Measurement Mode

When single measurement mode (MODE[3:0]="0001") is set, sensor is measured, and after sensor measurement and signal processing is finished, measurement data is stored to measurement data registers (HXL to HZH), then AK8975/B transits to power-down mode automatically. On transition to power-down mode, MODE[3:0] turnes to "0000". At the same time, DRDY bit in ST1 register turnes to "1". This is called "Data Ready". When any of measurement data register (HXL to HZH) or ST2 register is read, or operation mode is changed from power-down mode to other mode, DRDY bit turnes to "0". DRDY pin is in the same state as DRDY bit.

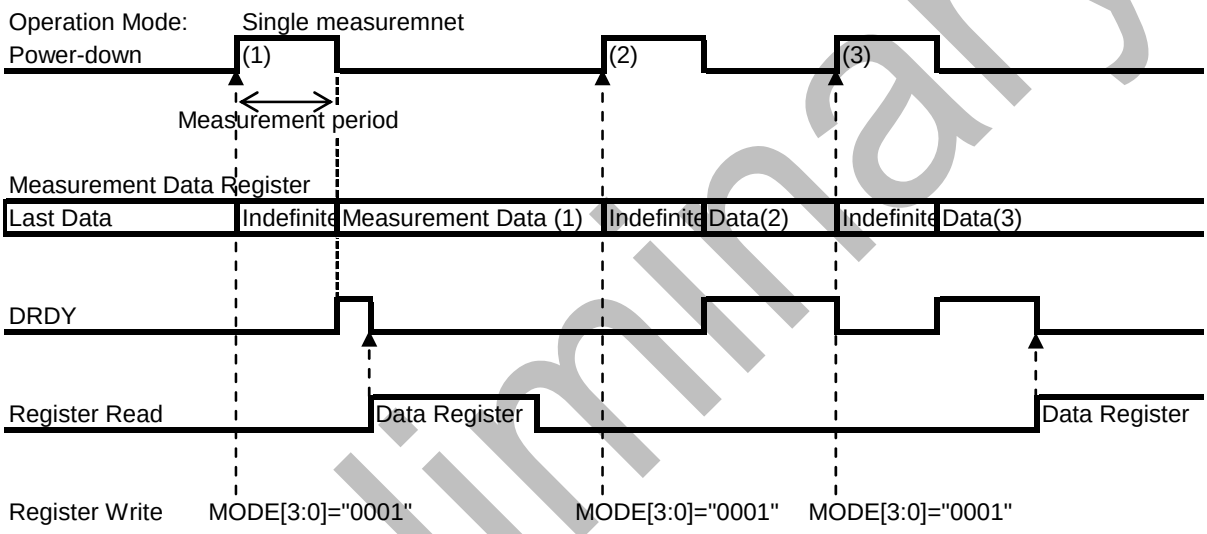



Figure 6.2 Single measurement mode

#### 6.4.2.1. Data Ready

When measurement data is stored and ready to be read, DRDY bit in ST1 register turnes to "1". This is called "Data Ready". DRDY pin is in the same state as DRDY bit. When measurement is performed correctly, AK8975/B becomes Data Ready on transition to PD after measurement. The period from the end of Nth measurement to the start of (N+1)th measurement is called "Data Readable Period". Stored measurement data should be read during Data Readable Period.

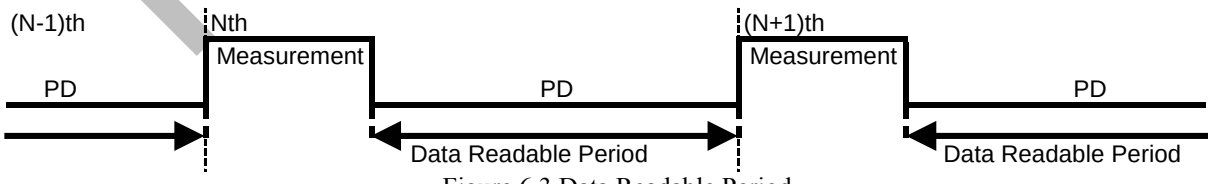



Figure 6.3 Data Readable Period

#### 6.4.2.2. Data Error

When data reading is started out of data readable period, read data is not correct. In this case, DERR bit of ST2 register turnes to "1" so that read data can be checked at the end of data reading. DERR turnes to "0" when ST2 register is read.

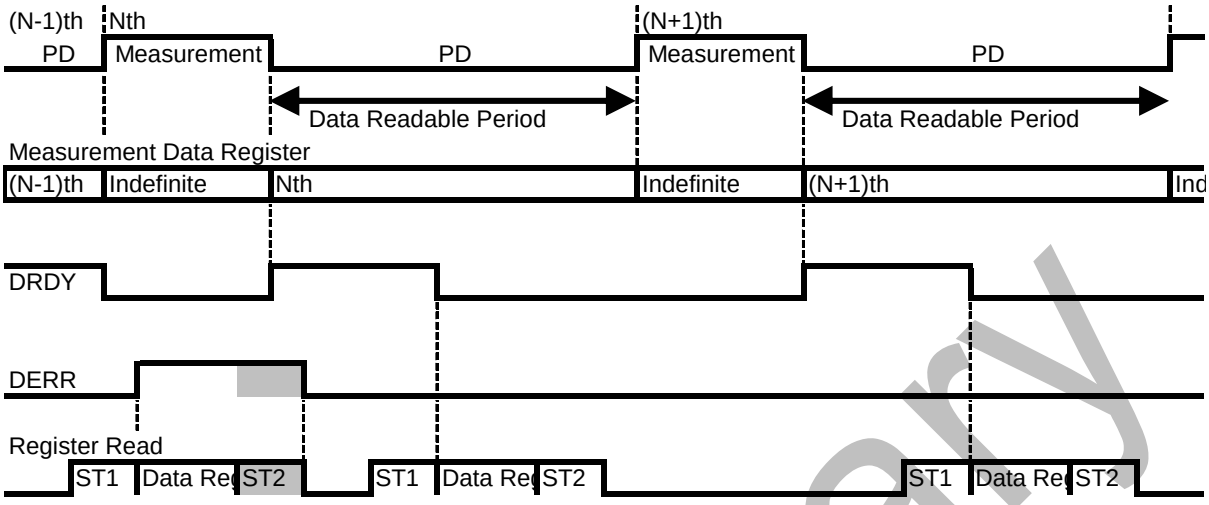



Figure 6.4 Data Error

#### 6.4.2.3. Magnetic Sensor Overflow

AK8975/B has the limitation for measurement range that the sum of absolute values of each axis should be smaller than 2400μT.

$$|X|+|Y|+|Z| < 2400\mu T$$

When the magnetic field exceeded this limitation, data stored at measurement data are not correct. This is called Magnetic Sensor Overflow.

When magnetic sensor overlow occurs, HOFL bit turns to "1". When the next measurement starts, it returns to "0".

### 6.4.3. Self-test Mode

Self-test mode is used to check if the sensor is working.
When self-test mode (MODE[3:0]="1000") is set, magnetic field is generated by the internal magnetic source and sensor is measured. Measurement data is stored to measurement data registers (HXL to HZH), then AK8975/B transits to power-down mode automatically.
Before setting self-test mode, write "1" to SELF bit of ASTC register. Data read sequence and functions of read-only registers in self-test mode is the same as single measurement mode.
When measurement data is in the range of following table, AK8975/B is working normally.

| | X | Y | Z |
|---|---|---|---|
| Criteria | ≤TBD | ≤TBD | ≥TBD |

When self-test is end, write "0" to SELF bit then proceed to other operation.

<Self-test Sequence>
(1) Set Power-down mode
(2) Write "1" to SELF bit of ASTC register
(3) Set Self-test Mode
(4) Check Data Ready or not by any of the following method.
- Polling DRDY bit of ST1 register
- Monitor DRDY pin
When Data Ready, proceed to the next step.
(5) Read measurement data (HXL to HZH)
(6) Write "0" to SELF bit of ASTC register

### 6.4.4. Fuse ROM Access Mode

Fuse ROM access mode is used to read Fuse ROM data.Sensitivity adjustment data for each axis is stored in fuse ROM. These data are used in calculation of direction by the external CPU.
When Fuse ROM mode (MODE[3:0]="1111") is set, circuits reauired for reading fuse ROM are turned on. After reading fuse ROM data, set power-down mode (MODE[3:0]="0000").

# 7. Serial Interface

AK8975/B supports $I^2C$ bus interface and 4-wire SPI. A selection is made by CSB pin. When used as 3-wire SPI, set SI pin and SO pin wired-OR externally.

CSB pin="L": Four-wire serial interface
CSB pin="H": $I^2C$ bus interface

## 7.1. 4-wire SPI

The 4-wire SPI consists of four digital signal lines: SK, SI, SO, and CSB. It is compliant with sequencial read operation.
Data consists of Read/Write control bit (R/W), register address (7bits) and control data (8bits).
CSB pin is low active. Input data is taken in on the rising edge of SK pin, and output data is changed on the falling edge of SK pin. (SPI MODE3)
Communication starts when CSB pin transits to "L" and stops when CSB pin transits to "H". SK pin must be "H" during CSB pin is in transition. Also, it is prohibited to change SI pin during CSB pin is "H" and SK pin is "H".

### 7.1.1. Writing Data

Input 16 bits data on SI pin in synchronous with the 16-bit serial clock input on SK pin. Out of 16 bits input data, the first 8 bits specify the R/W control bit (R/W="0" when writing) and register address (7bits), and the latter 8 bits are control data (8bits). When any of addresses listed on Table 8.1 is input, AK8975/B recognizes that it is selected and takes in latter 8 bits as setting data.
If the number of clock pulses is less than 16, no data is written. If the number of clock pulses is more than 16, data after the 16th clock pulse on SI pin are ignored.
It is not compliant with sereal write operation for multiple addresses.

### 7.1.2. Reading Data

Input the R/W control bit (R/W="1") and 7 bit register address on SI pin in synchronous with the first 8 bits of the 16 bits of a serial clock input on SK pin. Then AK8975/B outputs the data held in the specified register with MSB first from SO pin.
When clocks are input continuously after one byte of data is read, the address is incremented and data in the next address is output. Accordingly, after the falling edge of the 15th clock and CSB pin is "L", the data in the next address is output on SO pin. When CSB pin is driven "L" to "H", SO pin is placed in the high-impedance state.
AK8975/B has two incrementation lines; 02H to 09H and 10H to 12H. For example, data is read as follows: 00H -> 01H ... -> 0BH -> 0CH -> 00H -> 01H ..., and 10H -> 11H -> 12H -> 10H …
When specified address is other than 00H to 12H, AK8975/B recognizes that it is not selected and keeps SO pin in high-impedance state. Therefore, user can use other addresses for other devices.

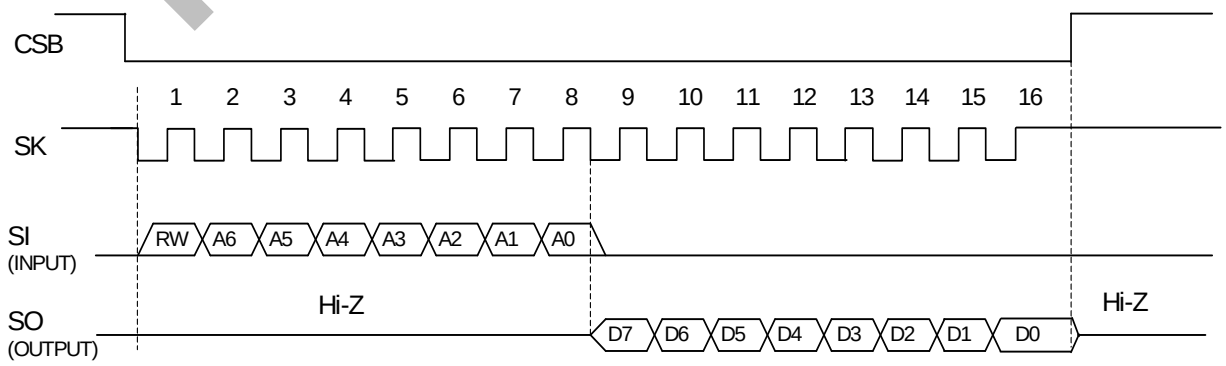



Figure 7.1 4-wire SPI

## 7.2. I2C Bus Interface

The $I^2C$ bus interface of AK8975/B supports the standard mode (100 kHz max.) and the fast mode (400 kHz max.).

### 7.2.1. Data Transfer

To access AK8975/B on the bus, generate a start condition first.
Next, transmit a one-byte slave address including a device address. At this time, AK8975/B compares the slave address with its own address. If these addresses match, AK8975/B generates an acknowledgement, and then executes READ or WRITE instruction. At the end of instruction execution, generate a stop condition.

#### 7.2.1.1. Change of Data

A change of data on the SDA line must be made during "Low" period of the clock on the SCL line. When the clock signal on the SCL line is "High", the state of the SDA line must be stable. (Data on the SDA line can be changed only when the clock signal on the SCL line is "Low".)
During the SCL line is "High", the state of data on the SDA line is changed only when a start condition or a stop condition is generated.

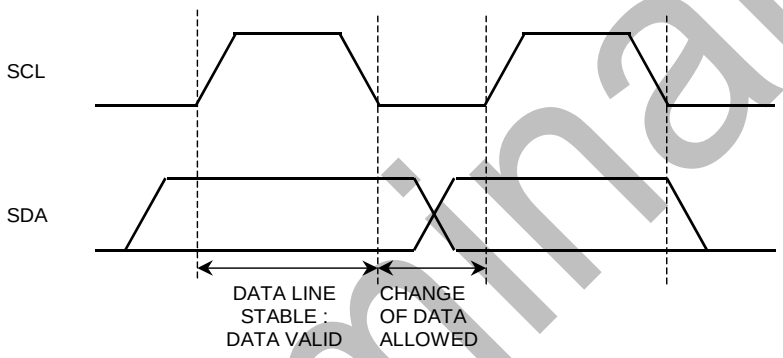



Figure 7.2 Data Change

#### 7.2.1.2. Start/Stop Condition

If the SDA line is driven to "Low" from "High" when the SCL line is "High", a start condition is generated. Any instruction starts with a start condition.
If the SDA line is driven to "High" from "Low" when the SCL line is "High", a stop condition is generated. Any instruction stops with a stop condition.

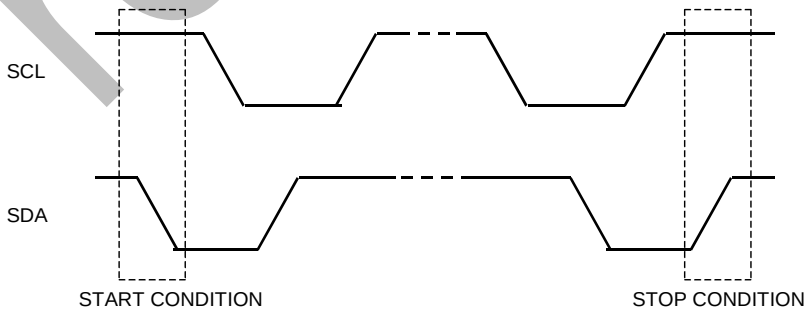



Figure 7.3 Start and Stop Conditions

#### 7.2.1.3. Acknowledge

The IC that is transmitting data releases the SDA line (in the "High" state) after sending 1-byte data.
The IC that receives the data drives the SDA line to "Low" on the next clock pulse. This operation is referred to acknowledge. With this operation, whether data has been transferred successfully can be checked.
AK8975/B generates an acknowledge after reception of a start condition and slave address.
When a WRITE instruction is executed, AK8975/B generates an acknowledge after every byte is received.
When a READ instruction is executed, AK8975/B generates an acknowledge then transfers the data stored at the specified address. Next, AK8975/B releases the SDA line then monitors the SDA line. If a master IC generates an acknowledge instead of a stop condition, AK8975/B transmits the 8bit data stored at the next address. If no acknowledge is generated, AK8975/B stops data transmission.

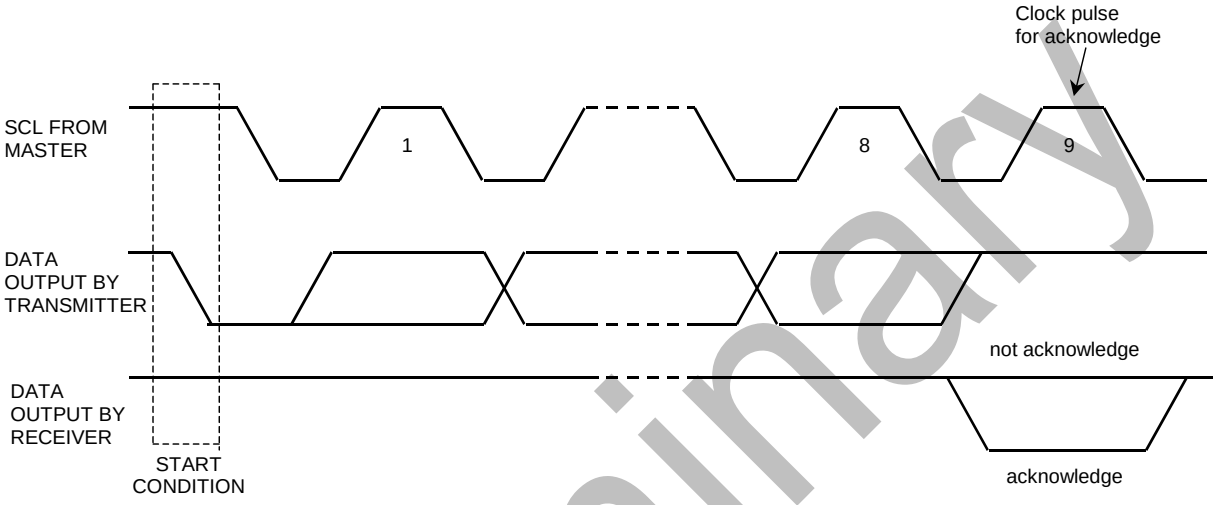



Figure 7.4 Generation of Acknowledge

#### 7.2.1.4. Slave Address

The slave address of AK8975/B can be selected from the following list by setting CAD0/1 pin. When CAD pin is fixed to VSS, the corresponding slave address bit is “0”. When CAD pin is fixed to VDD, the corresponding slave address bit is “1”.

| CAD1 | CAD0 | Slave Address |
|---|---|---|
| 0 | 0 | 0CH |
| 0 | 1 | 0DH |
| 1 | 0 | 0EH |
| 1 | 1 | 0FH |

Table 7.1 Slave Address and CAD0/1 pin

The first byte including a slave address is transmitted after a start condition, and an IC to be accessed is selected from the ICs on the bus according to the slave address.
When a slave address is transferred, the IC whose device address matches the transferred slave address generates an acknowledge then executes an instruction. The 8th bit (least significant bit) of the first byte is a R/W bit.
When the R/W bit is set to "1", READ instruction is executed. When the R/W bit is set to "0", WRITE instruction is executed.

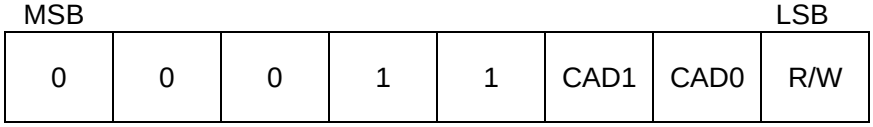



Figure 7.5 Slave Address

### 7.2.2. WRITE Instruction

When the R/W bit is set to "0", AK8975/B performs write operation.
In write operation, AK8975/B generates an acknowledge after receiving a start condition and the first byte (slave address) then receives the second byte. The second byte is used to specify the address of an internal control register and is based on the MSB-first configuration.

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

Figure 7.6 Register Address

After receiving the second byte (register address), AK8975/B generates an acknowledge then receives the third byte.
The third and the following bytes represent control data. Control data consists of 8 bits and is based on the MSB-first configuration. AK8975/B generates an acknowledge after every byte is received. Data transfer always stops with a stop condition generated by the master.

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Figure 7.7 Control Data

### 7.2.3. READ Instruction

When the R/W bit is set to "1", AK8975/B performs read operation.

If a master IC generates an acknowledge instead of a stop condition after AK8975/B transfers the data at a specified address, the data at the next address can be read.

Address can be from 02H to 09H and/or from 10H to 12H.When address is counted up to 0CH in the range of 00H to 0CH, the next address returns to 00H. When address is counted up to 12H in the range of 10H to 12H, the next address returns to 10H.

AK8975/B supports one byte read and multiple byte read.

#### 7.2.3.1. One Byte READ

AK8975/B has an address counter inside the LSI chip. In current address read operation, the data at an address specified by this counter is read.

The internal address counter holds the next address of the most recently accessed address.

For example, if the address most recently accessed (for READ instruction) is address "n", and a current address read operation is attempted, the data at address "n+1" is read.

In one byte read operation, AK8975/B generates an acknowledge after receiving a slave address for the READ instruction (R/W bit="1"). Next, AK8975/B transfers the data specified by the internal address counter starting with the next clock pulse, then increments the internal counter by one. If the master IC generates a stop condition instead of an acknowledge after AK8975/B transmits one byte of data, the read operation stops.

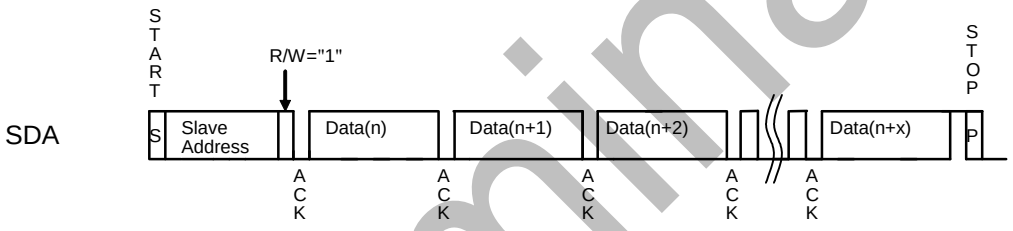



Figure 7.8 One Byte READ

#### 7.2.3.2. Multiple Byte READ

By multiple byte read operation, data at an arbitrary address can be read.

The multiple byte read operation requires to execute WRITE instruction as dummy before a slave address for the READ instruction (R/W bit="1") is transmitted. In random read operation, a start condition is first generated then a slave address for the WRITE instruction (R/W bit="0") and a read address are transmitted sequentially.

After AK8975/B generates an acknowledge in response to this address transmission, a start condition and a slave address for the READ instruction (R/W bit="1") are generated again. AK8975/B generates an acknowledge in response to this slave address transmission. Next, AK8975/B transfers the data at the specified address then increments the internal address counter by one. If the master IC generates a stop condition instead of an acknowledge after data is transferred, the read operation stops.

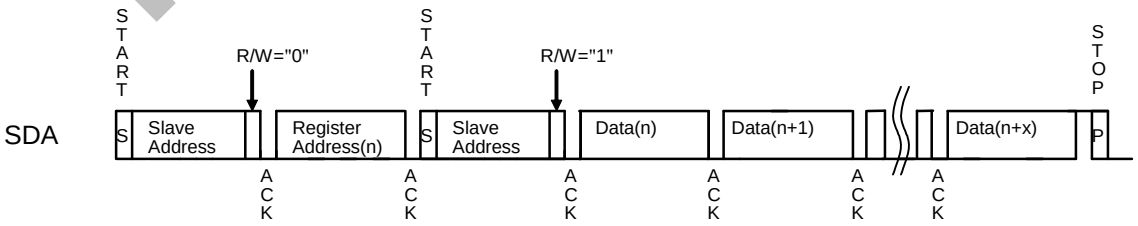



Figure 7.9 Multiple Byte READ

# 8. Registers

## 8.1. Description of Registers

AK8975/B has registers of 19 addresses as indicated in Table 8.1. Every address consists of 8 bits data. Data is transferred to or received from the external CPU via the serial interface described previously.

| Name | Address | READ/ WRITE | Description | Bit width | Explanation |
|---|---|---|---|---|---|
| WIA | 00H | READ | Device ID | 8 | Company ID |
| INFO | 01H | READ | Information | 8 | Device Information |
| ST1 | 02H | READ | Status 1 | 8 | Data status |
| HXL | 03H | READ | Measurement data register | 8 | X-axis data |
| HXH | 04H | | | 8 | |
| HYL | 05H | | | 8 | Y-axis data |
| HYH | 06H | | | 8 | |
| HZL | 07H | | | 8 | Z-axis data |
| HZH | 08H | | | 8 | |
| ST2 | 09H | READ | Status 2 | 8 | Data status |
| CNTL | 0AH | READ/ WRITE | Control | 8 | Control settings |
| RSV | 0BH | READ/ WRITE | Reserved | 8 | DO NOT ACCESS |
| ASTC | 0CH | READ/ WRITE | Self-test | 8 | |
| TS1 | 0DH | READ/ WRITE | Test 1 | 8 | DO NOT ACCESS |
| TS2 | 0EH | READ/ WRITE | Test 2 | 8 | DO NOT ACCESS |
| I2CDIS | 0FH | READ/ WRITE | I2C disable | 8 | |
| ASAX | 10H | READ | X-axis sensitivity adjustment value | 8 | Fuse ROM |
| ASAY | 11H | READ | Y-axis sensitivity adjustment value | 8 | Fuse ROM |
| ASAZ | 12H | READ | Z-axis sensitivity adjustment value | 8 | Fuse ROM |

Table 8.1 Register Table

Addresses from 02H to 09H and from 10H to 12H are compliant with automatic increment function of serial interface respectively. Values of addresses from 10H to 12H can be read only in Fuse access mode. In other modes, these addresses are accessible but can not be read correctly.

## 8.2. Register Map

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| **Read-only Register** | | | | | | | | | |
| 00H | WIA | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 01H | INFO | INFO7 | INFO6 | INFO5 | INFO4 | INFO3 | INFO2 | INFO1 | INFO0 |
| 02H | ST1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DRDY |
| 03H | HXL | HX7 | HX6 | HX5 | HX4 | HX3 | HX2 | HX1 | HX0 |
| 04H | HXH | HX15 | HX14 | HX13 | HX12 | HX11 | HX10 | HX9 | HX8 |
| 05H | HYL | HY7 | HY6 | HY5 | HY4 | HY3 | HY2 | HY1 | HY0 |
| 06H | HYH | HY15 | HY14 | HY13 | HY12 | HY11 | HY10 | HY9 | HY8 |
| 07H | HZL | HZ7 | HZ6 | HZ5 | HZ4 | HZ3 | HZ2 | HZ1 | HZ0 |
| 08H | HZH | HZ15 | HZ14 | HZ13 | HZ12 | HZ11 | HZ10 | HZ9 | HZ8 |
| 09H | ST2 | 0 | 0 | 0 | 0 | HOFL | DERR | 0 | 0 |
| **Write/read Register** | | | | | | | | | |
| 0AH | CNTL | 0 | 0 | 0 | 0 | MODE3 | MODE2 | MODE1 | MODE0 |
| 0BH | RSV | - | - | - | - | - | - | - | - |
| 0CH | ASTC | - | SELF | - | - | - | - | - | - |
| 0DH | TS1 | - | - | - | - | - | - | - | - |
| 0EH | TS2 | - | - | - | - | - | - | - | - |
| 0FH | I2CDIS | - | - | - | - | - | - | - | I2CDIS |
| **Read-only Register** | | | | | | | | | |
| 10H | ASAX | COEFX7 | COEFX6 | COEFX5 | COEFX4 | COEFX3 | COEFX2 | COEFX1 | COEFX0 |
| 11H | ASAY | COEFY7 | COEFY6 | COEFY5 | COEFY4 | COEFY3 | COEFY2 | COEFY1 | COEFY0 |
| 12H | ASAZ | COEFZ7 | COEFZ6 | COEFZ5 | COEFZ4 | COEFZ3 | COEFZ2 | COEFZ1 | COEFZ0 |

Table 8.2 Register Map

When VDD is turned ON, POR function works and all registers of AK8975/B are initialized regardless of VID status. To write data to or to read data from register, VID must be ON.
TS1 and TS2 are test registers for shipment test. Do not use these registers.
RSV is reserved register. Do not use this register.

## 8.3. Detailed Description of Registers

### 8.3.1. WIA: Device ID

| Addr | Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Read-only register | | | | | | | | | |
| 00H | WIA | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

Device ID of AKM. It is described in one byte and fixed value.
48H: fixed

### 8.3.2. INFO: Information

| Addr | Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Read-only register | | | | | | | | | |
| 01H | INFO | INFO7 | INFO6 | INFO5 | INFO4 | INFO3 | INFO2 | INFO1 | INFO0 |

INFO[7:0]: Device information for AKM.

### 8.3.3. ST1: Status 1

| Addr | Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Read-only register | | | | | | | | | |
| 02H | ST1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DRDY |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DRDY: Data Ready
"0": Normal
"1": Data is ready
DRDY bit turns to "1" when data is ready in single measurement mode or self-test mode. It returns to "0" when any one of ST2 register or measurement data register (HXL to HZH) is read.

### 8.3.4. HXL to HZH: Measurement Data

| Addr | Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Read-only register | | | | | | | | | |
| 03H | HXL | HX7 | HX6 | HX5 | HX4 | HX3 | HX2 | HX1 | HX0 |
| 04H | HXH | HX15 | HX14 | HX13 | HX12 | HX11 | HX10 | HX9 | HX8 |
| 05H | HYL | HY7 | HY6 | HY5 | HY4 | HY3 | HY2 | HY1 | HY0 |
| 06H | HYH | HY15 | HY14 | HY13 | HY12 | HY11 | HY10 | HY9 | HY8 |
| 07H | HZL | HZ7 | HZ6 | HZ5 | HZ4 | HZ3 | HZ2 | HZ1 | HZ0 |
| 08H | HZH | HZ15 | HZ14 | HZ13 | HZ12 | HZ11 | HZ10 | HZ9 | HZ8 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Measurement data of magnetic sensor X-axis/Y-axis/Z-axis

HXL[7:0]: X-axis measurement data lower 8bit
HXH[7:0]: X-axis measurement data higher 8bit
HYL[7:0]: Y-axis measurement data lower 8bit
HYH[7:0]: Y-axis measurement data higher 8bit
HZL[7:0]: Z-axis measurement data lower 8bit
HZH[7:0]: Z-axis measurement data higher 8bit

Measuremnet data is stored in two's complement and Little Endian format. Measurement range of each axis is from -4096 to +4095 in decimal.

| Measurement data (each axis) [15:0] | | | Magnetic flux density [μT] |
|---|---|---|---|
| Two's complement | Hex | Decimal | |
| 0000 1111 1111 1111 | 0FFF | 4095 | 1229(max.) |
| \| | \| | \| | \| |
| 0000 0000 0000 0001 | 0001 | 1 | 0.3 |
| 0000 0000 0000 0000 | 0000 | 0 | 0 |
| 1111 1111 1111 1111 | FFFF | -1 | -0.3 |
| \| | \| | \| | \| |
| 1111 0000 0000 0000 | F000 | -4096 | -1229(min.) |

Table 8.3 Measurement data format

### 8.3.5. ST2: Status 2

| Addr | Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Read-only register | | | | | | | | | |
| 09H | ST2 | 0 | 0 | 0 | 0 | HOFL | DERR | 0 | 0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DERR: Data Error
"0": Normal
"1": Data read error occurred
When data reading is started out of data readable period, the read data are not correct. In this case, data read error occurs and DERR bit turns to "1". When ST2 register is read, it returns to "0".

HOFL: Magnetic sensor overflow
"0": Normal
"1": Magnetic sensor overflow occurred
In single measurement mode and self-test mode, magnetic sensor may overflow even though measurement data regiseter is not saturated. In this case, measurement data is not correct and HOFL bit turns to "1". When next measurement stars, it returns to "0". Refer to 6.4.2.3 for detailed information.

### 8.3.6. CNTL: Control

| Addr | Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Read-only register | | | | | | | | | |
| 0AH | CNTL | 0 | 0 | 0 | 0 | MODE3 | MODE2 | MODE1 | MODE0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

MODE[3:0]: Operation mode setting
"0000": Power-down mode
"0001": Single measurement mode
"1000": Self-test mode
"1111": Fuse ROM access mode
Other code settings are prohibited

When each mode is set, AK8975/B transits to set mode. Refer to 6.3 for detailed information.
When CNTL register is accessed to be written, registers from 02H to 09H are initialized.

### 8.3.7. RSV: Reserved

| Addr | Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Read-only register | | | | | | | | | |
| 0BH | RSV | - | - | - | - | - | - | - | - |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RSV register is reserved. Do not use this register.

### 8.3.8. ASTC: Self Test Control

| Addr | Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Write/read register | | | | | | | | | |
| 0CH | ASTC | - | SELF | - | - | - | - | - | - |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SELF: Self test control

"0": Normal

"1": Generate magnetic field for self-test

Do not write "1" to any bit other than SELF bit in ASTC register. If "1" is written to any bit other than SELF bit, normal measurement can not be done.

### 8.3.9. TS1, TS2: Test 1, 2

| Addr | Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Write/read register | | | | | | | | | |
| 0DH | TS1 | - | - | - | - | - | - | - | - |
| 0EH | TS2 | - | - | - | - | - | - | - | - |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

TS1 and TS2 registers are test registers for shipment test. Do not use these registers.

### 8.3.10. I2CDIS: I2C Disable

| Addr | Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Write/read register | | | | | | | | | |
| 0FH | I2CDIS | - | - | - | - | - | - | - | I2CDIS |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

This register disables $I^2C$ bus interface. $I^2C$ bus interface is enabled in default. To disable $I^2C$, write "00011011" to I2CDIS register. Then I2CDIS bit turns to "1" and $I^2C$ bus interface is disabled.
Once I2CDIS is turned to "1" and $I^2C$ bus interface is disabled, re-setting I2CDIST to "0" is prohibited. To enable $I^2C$ bus interface, reset AK8975/B by turning VDD or VID to OFF (0V) once.

### 8.3.11. ASAX, ASAY, ASAZ: Sensitivity Adjustment values

| Addr | Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Read-only register | | | | | | | | | |
| 10H | ASAX | COEFX7 | COEFX6 | COEFX5 | COEFX4 | COEFX3 | COEFX2 | COEFX1 | COEFX0 |
| 11H | ASAY | COEFY7 | COEFY6 | COEFY5 | COEFY4 | COEFY3 | COEFY2 | COEFY1 | COEFY0 |
| 12H | ASAZ | COEFZ7 | COEFZ6 | COEFZ5 | COEFZ4 | COEFZ3 | COEFZ2 | COEFZ1 | COEFZ0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

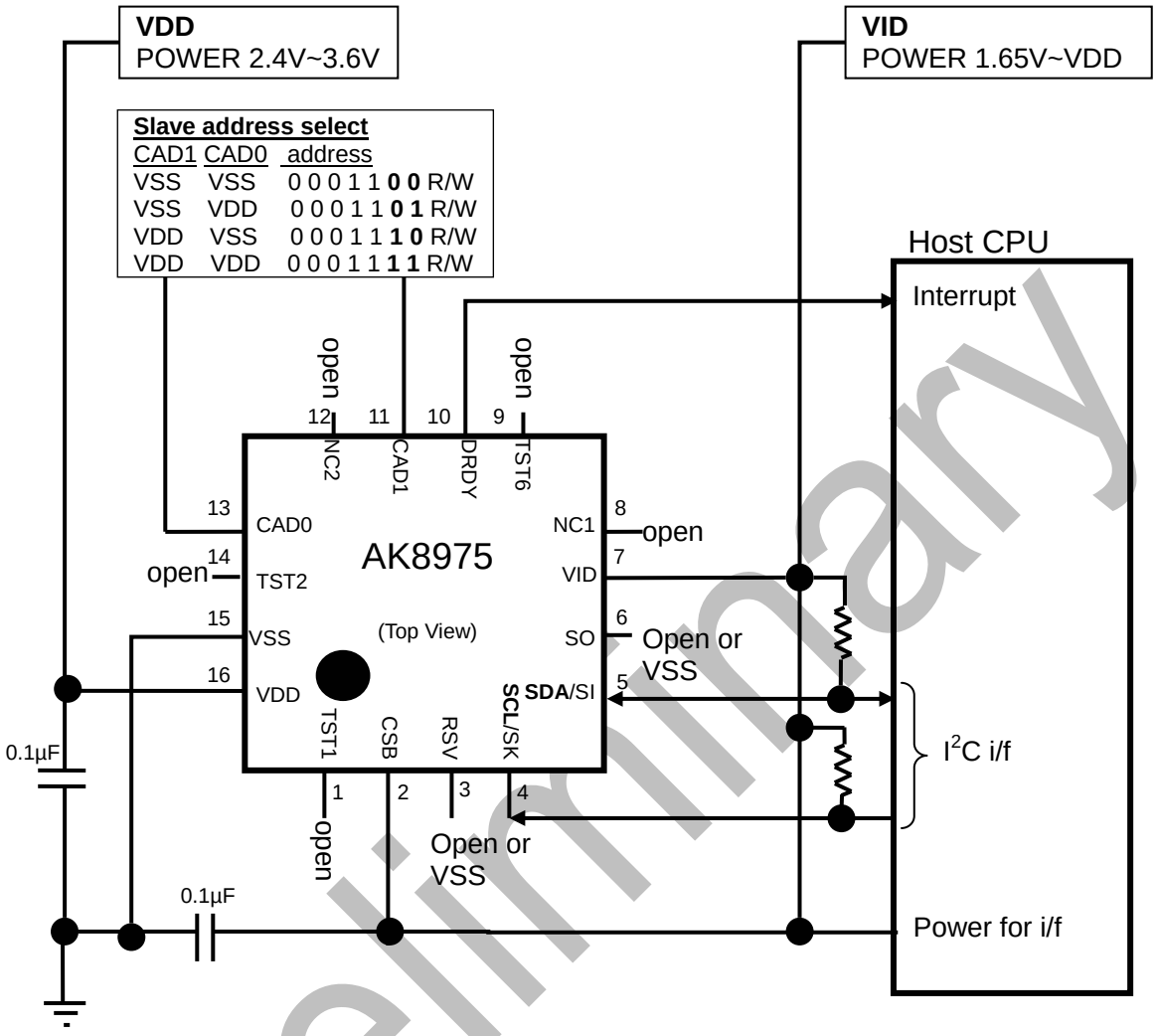
Sensitivity adjustment data for each axis is stored to fuse ROM on shipment.

ASAX[7:0]: Magnetic sensor X-axis sensitivity adjustment data
ASAY[7:0]: Magnetic sensor Y-axis sensitivity adjustment data
ASAZ[7:0]: Magnetic sensor Z-axis sensitivity adjustment data

# 9. Example of Recommended External Connection

## 9.1. I2C Bus Interface

**<AK8975>**

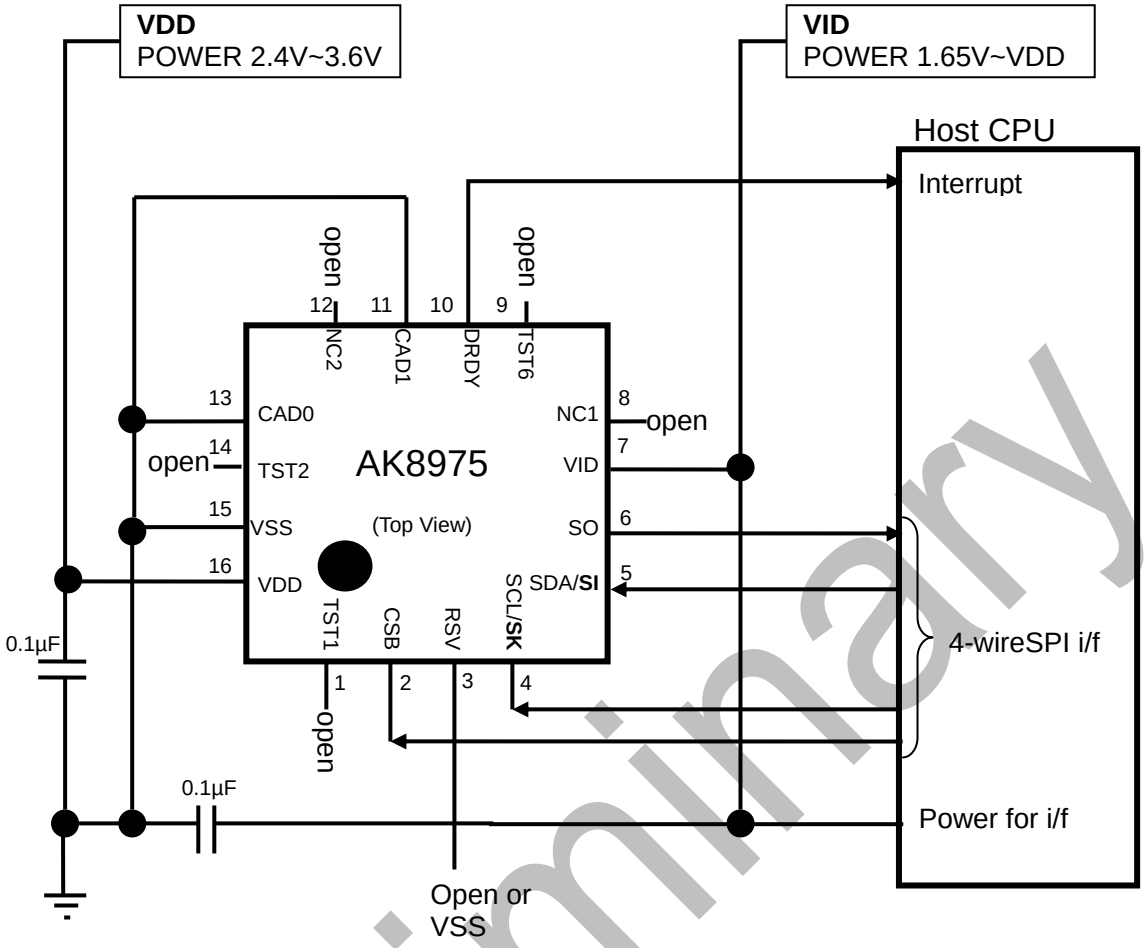



**<AK8975B>**

Same as AK8975

## 9.2. 4-wire SPI Interface

**<AK8975>**




**<AK8975B>**

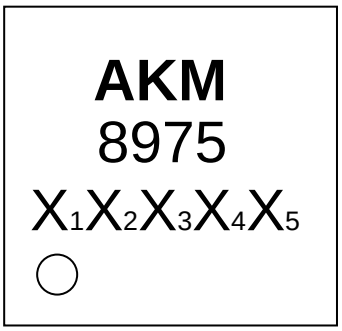
Same as AK8975

# 10. Package

## 10.1. Marking

**<AK8975>**

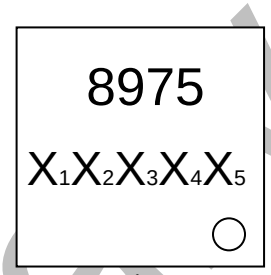
- Company logo: AKM
- Product name: 8975
- Date code: $X_1X_2X_3X_4X_5$
  - $X_1$ = ID
  - $X_2$ = Year code
  - $X_3X_4$ = Week code
  - $X_5$ = Lot




<Top view>

**<AK8975B>**

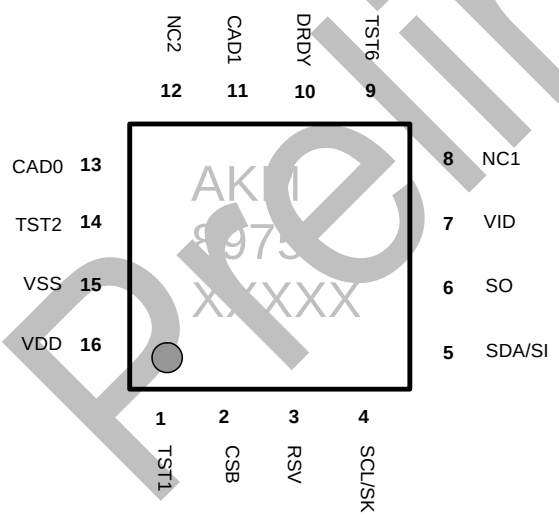
- Product name: 8975
- Date code: $X_1X_2X_3X_4X_5$
  - $X_1$ = ID
  - $X_2$ = Year code
  - $X_3X_4$ = Week code
  - $X_5$ = Lot




<Top view>

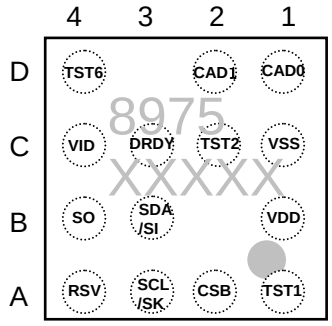
## 10.2. Pin Assignment

**<AK8975>**




<Top view>

**<AK8975B>**

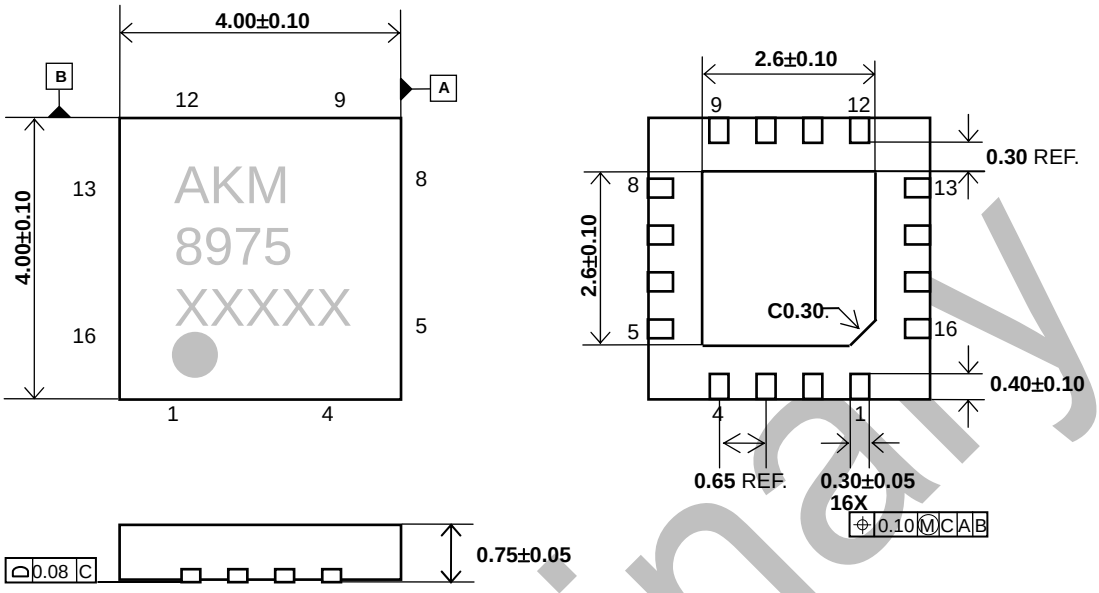



<Top view>

## 10.3. Outline Dimensions

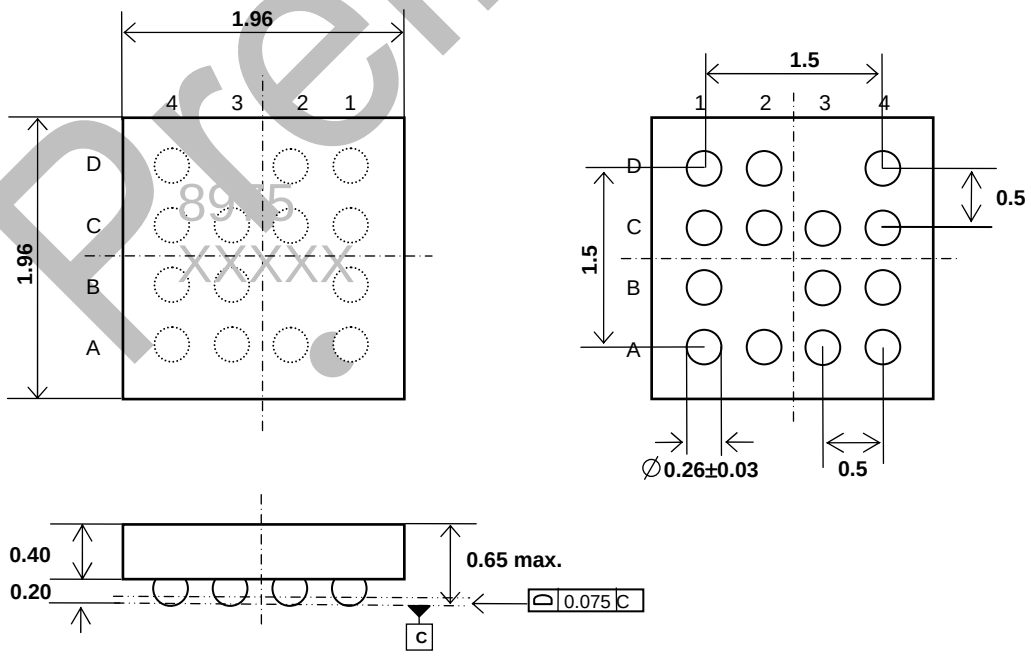
**<AK8975>**

[mm]




**<AK8975B>**

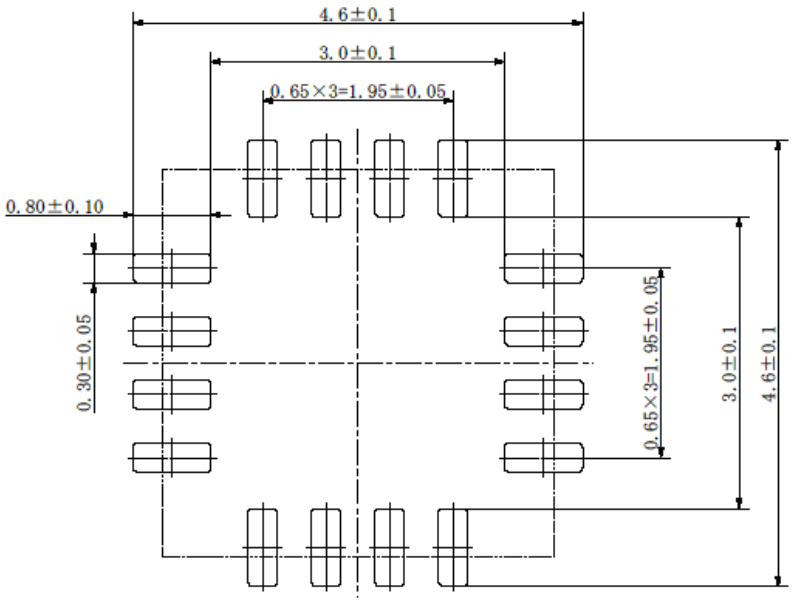
[mm]



## 10.4. Recommended Foot Print Pattern

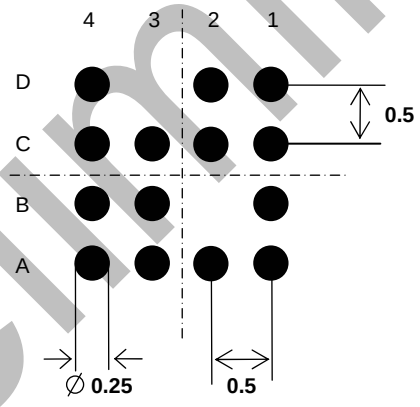
**<AK8975>**

[mm]



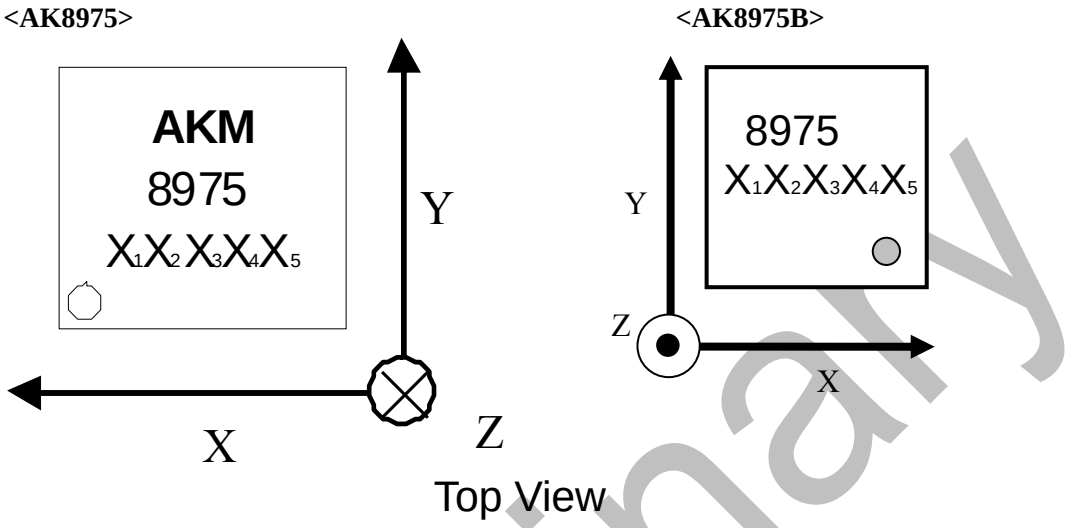

**<AK8975B>**

[mm]



# 11. Relationship between the Magnetic Field and Output Code

The measurement data increases as the magnetic flux density increases in the arrow directions.
For AK8975B, on the Z-axis, data increases as the magnetic flux density in the direction from the back of the package to the front face increases.



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