



QUAD PRECISION CMOS VOLTAGE COMPARATOR WITH OPEN DRAIN DRIVER

GENERAL DESCRIPTION

The ALD4301A/ALD4301 is a monolithic high performance quad voltage comparator built with advanced silicon gate CMOS technology. It features very high typical input impedance of $10^{12}\Omega$; low input bias current of 10pA; fast response time of 300ns; very low power dissipation of 55 μ A per comparator; high output drive and single (+5V) or dual ($\pm$ 5V) power supply operation.

The input voltage range includes ground, making this comparator ideal for low level signal detection with high source impedance. The outputs are open-drain configuration, allowing maximum application flexibility. The outputs can be connected to a higher external voltage than V^+ and used in a wired-OR connection with other open drain circuits such as the ALD2301 and ALD2303. They can also be used with push-pull output types, such as the ALD2302 and ALD4302 voltage comparators, simultaneously with open drain comparators using a common V^+ . The ALD4301A/ALD4301 is ideal for a great variety of voltage comparator applications, especially detection circuits requiring very low input currents and low standby power, yet retaining high output current capability.

FEATURES

- Fanout of 30LS TTL loads
- Low supply current of 55 μ A/comparator typical
- Pinout/Functional equivalent to LM393 types
- Extremely low input bias currents -- typically 10pA
- Virtually eliminates source impedance effects
- Low operating supply voltage of 3V to 10V
- Single (+5V) and dual supply ($\pm$ 5V) operation
- High speed for both large signal and low level signals -- 300ns typical for TTL inputs
- CMOS, NMOS and TTL compatible
- Wired-OR open drain outputs
- High output sinking current -- typically 60mA
- Low supply current spikes
- High gain

ORDERING INFORMATION ("L" suffix for lead free version)

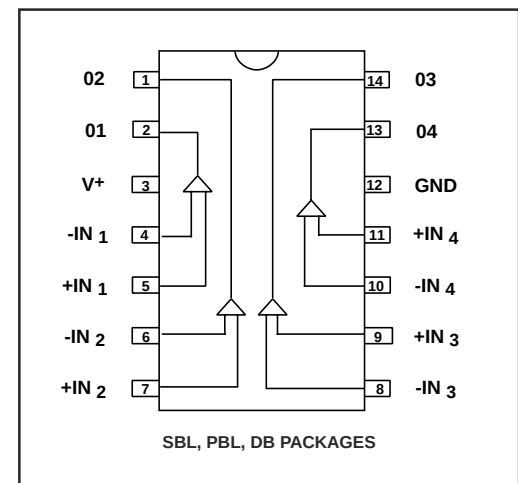
Operating Temperature Range *		
0°C to +70°C	0°C to +70°C	-55°C to +125°C
14-Pin Small Outline Package (SOIC)	14-Pin Plastic Dip Package	14-Pin CERDIP Package
ALD4301ASBL ALD4301SBL	ALD4301APBL ALD4301PBL	ALD4301ADB ALD4301DB

* Contact factory for leaded (non-RoHS) or high temperature versions.

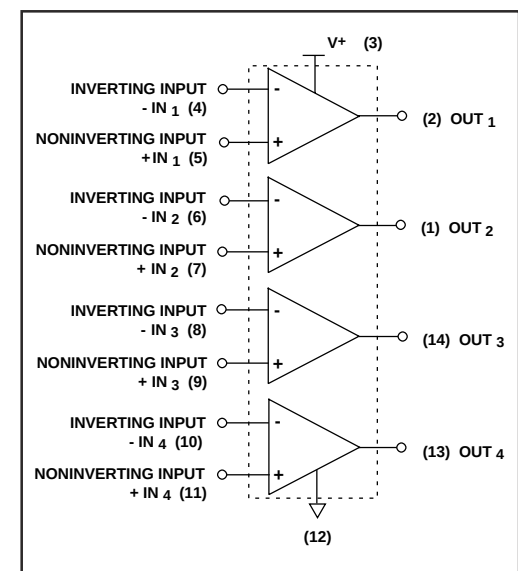
APPLICATIONS

- High source impedance voltage comparison circuits
- Dual/Quad limit window comparator
- Power supply voltage monitor
- Photo-detector sensor circuit
- Relay or LED driver
- Oscillators
- Battery operated instruments
- Remote signal detection

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply voltage, V^+ _____ 10.6V
Differential input voltage range _____ -0.3V to $V^+ + 0.3V$
Power dissipation _____ 600 mW
Operating temperature range SBL, PBL packages _____ $0^{\circ}C$ to $+70^{\circ}C$
DB package _____ $-55^{\circ}C$ to $+125^{\circ}C$
Storage temperature range _____ $-65^{\circ}C$ to $+150^{\circ}C$
Lead temperature, 10 seconds _____ $+260^{\circ}C$

OPERATING ELECTRICAL CHARACTERISTICS

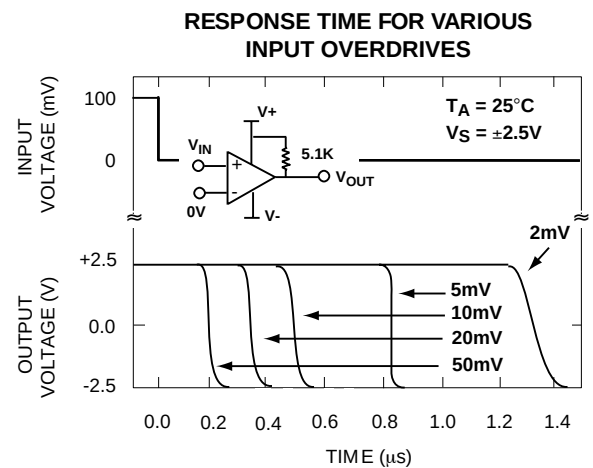
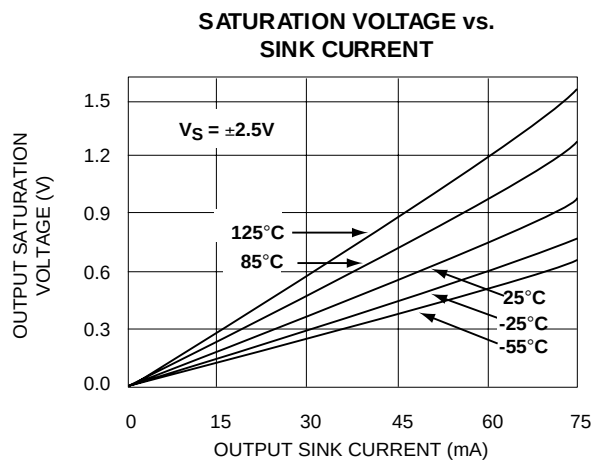
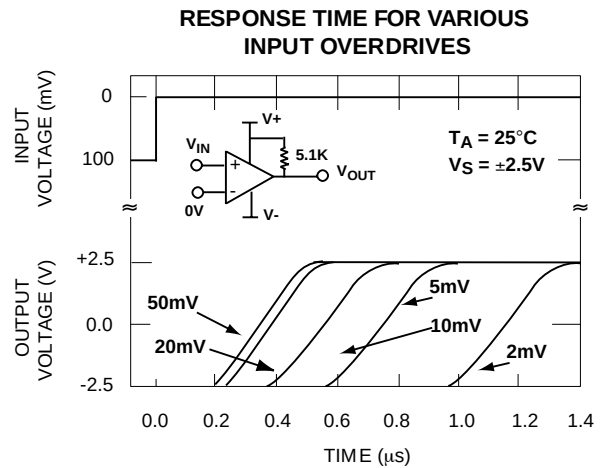
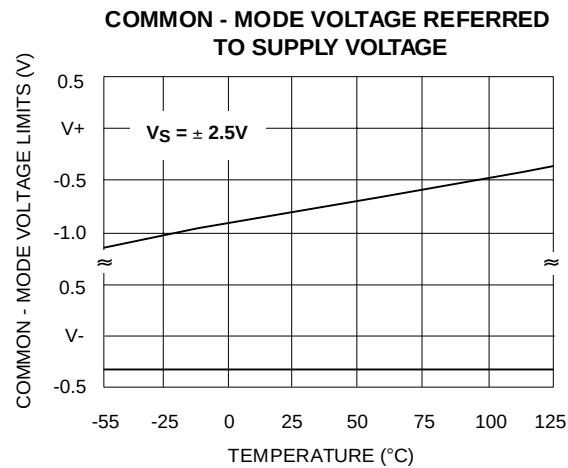
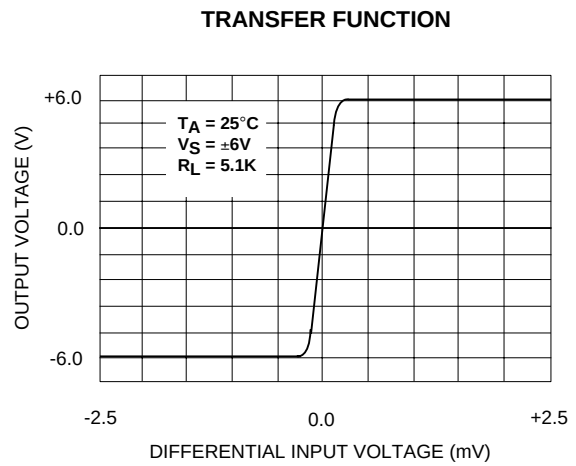
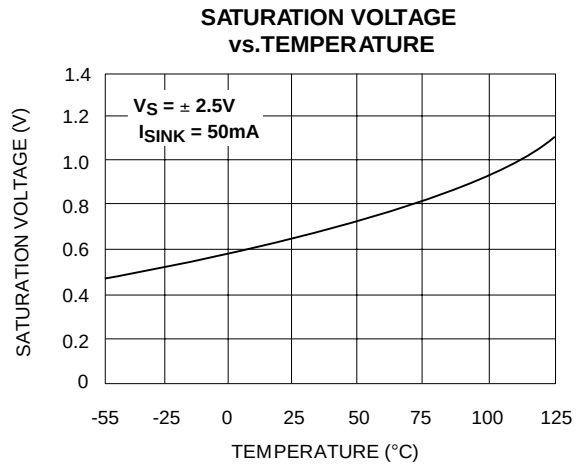
$T_A = 25^{\circ}C$ $V^+ = +5V$ unless otherwise specified

Parameter	Symbol	4301A			4301			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Supply Voltage	V_S V^+	± 1.5 3		± 5 10	± 1.5 3		± 5 10	V V	Dual Supply Single Supply
Supply Current	I_S		220	350		220	350	μA	No load
Voltage Gain	A_{VD}	50	150		50	150		V/mV	$R_{LOAD} \geq 15K\Omega$
Input Offset Voltage	V_{OS}			5			10	mV	$R_{LOAD} \geq 1.5K\Omega$
Input Offset Current ¹	I_{OS}		0.1	30		0.1	30	pA	
Input Bias Current ¹	I_B		0.1	30		0.1	30	pA	
Common Mode Input Voltage Range ²	V_{ICR}	-0.3		$V^+ - 1.5$	-0.3		$V^+ - 1.5$	V	
Low Level Output Voltage	V_{OL}		0.15	0.4		0.15	0.4	V	$I_{SINK} = 12mA$ $V_{INPUT} = 1V$ Differential
Low Level Output Current	I_{OL}	24	60		24	60		mA	$V_{OL} = 1.0V$
High Level Leakage Current	I_{LH}		0.1	20		0.1	20	nA	$V_{OH} = 5.0V$
Response Time ²	t_{RP}		650			650		ns	$R_L = 5.1K\Omega$ $C_L = 15pF$ 100mV Input Step/5mV Overdrive
			300			300		ns	$R_L = 5.1K\Omega$ $C_L = 15pF$ TTL- Level Input Step

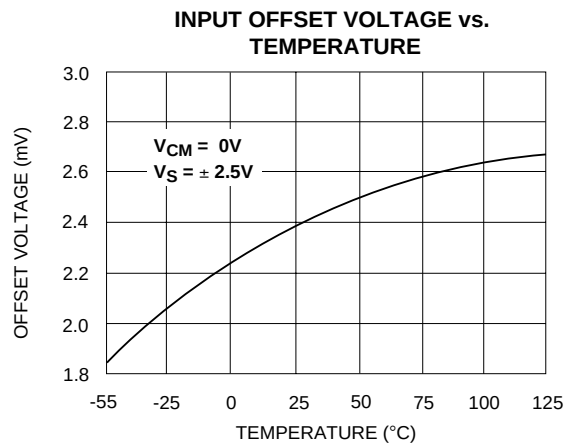
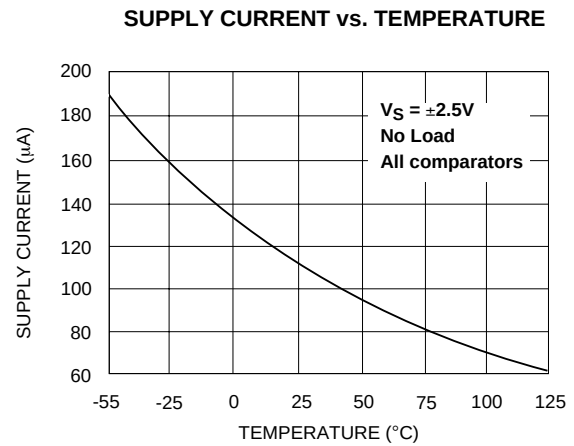
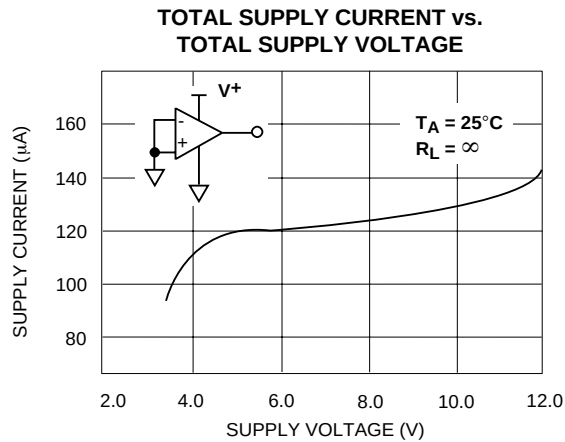
Notes: ¹ Consists of junction leakage currents

² Sample tested parameters

TYPICAL PERFORMANCE CHARACTERISTICS

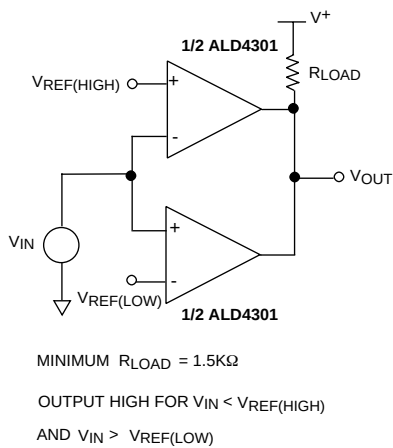


TYPICAL PERFORMANCE CHARACTERISTICS (cont'd)

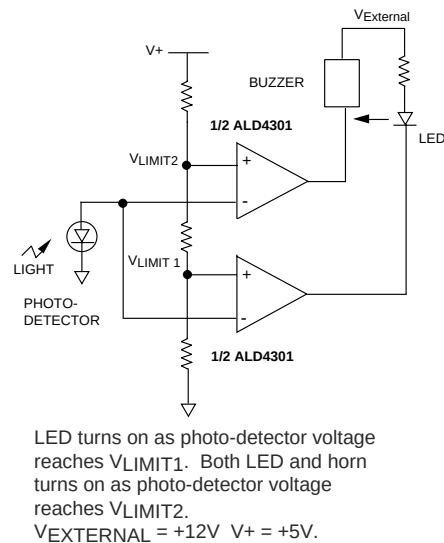


TYPICAL APPLICATIONS

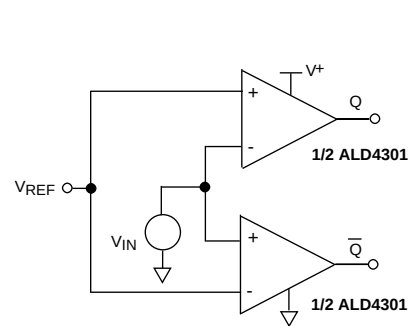
QUAD LIMIT WINDOW COMPARATOR



QUAD LIMIT PHOTO-DETECTOR MONITOR

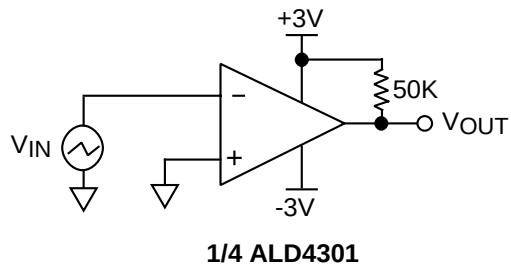


VOLTAGE COMPARATOR WITH COMPLEMENTARY OUTPUTS

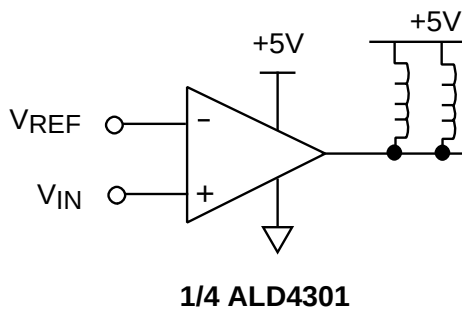


TYPICAL APPLICATIONS (cont'd)

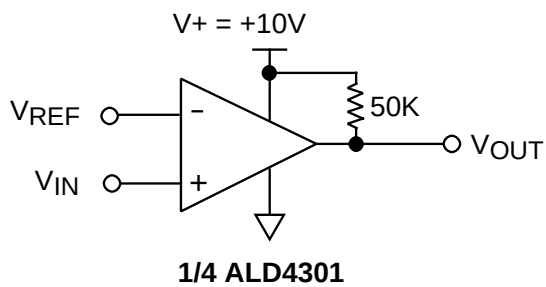
ZERO CROSSING DETECTOR



MULTIPLE RELAY DRIVE



VOLTAGE LEVEL TRANSLATOR

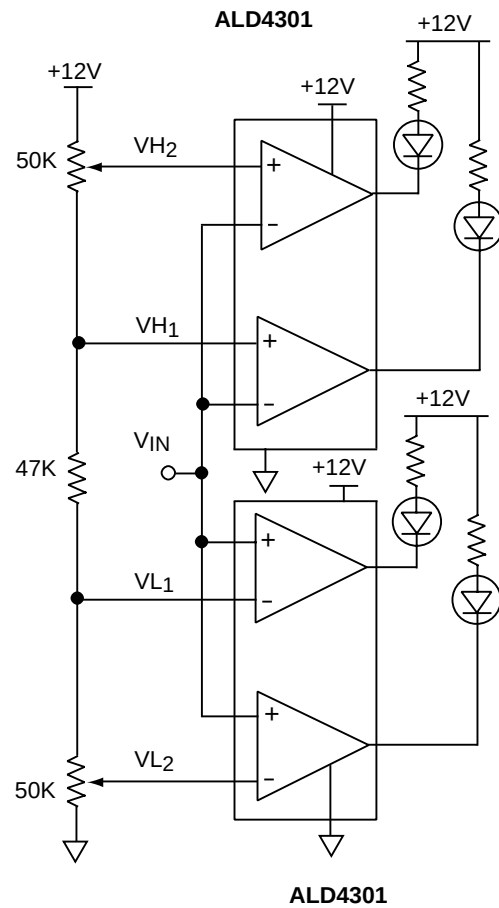


$V_{REF} = 1.4V$ for TTL input

$V_{REF} = \frac{V^+}{2}$ for CMOS input

Output V_{OUT} swings from rail-to-rail

DOUBLE DUAL LIMIT WINDOW COMPARATOR



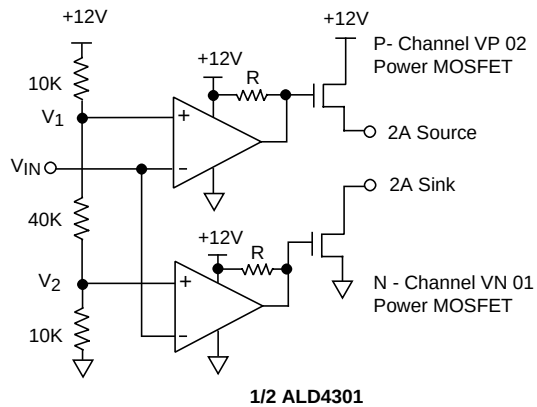
VL_1 and VH_1 first limit window send warning.
 VL_2 and VH_2 second limit window execute system cutoff.

TYPICAL APPLICATIONS (cont'd)

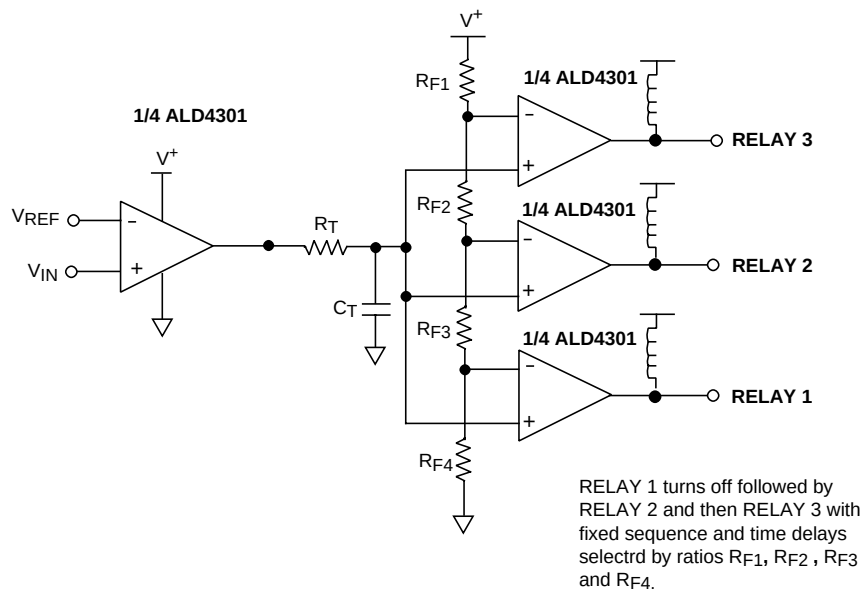
PUSH-PULL COMPLEMENTARY POWER MOSFET DRIVER

$R \geq 50 \text{ K}\Omega$

This circuit eliminates crossover current in the complementary power transistors. The outputs can be used to source and sink different loads or tied together to provide push-pull drive of the same load.



TIME DELAY GENERATOR

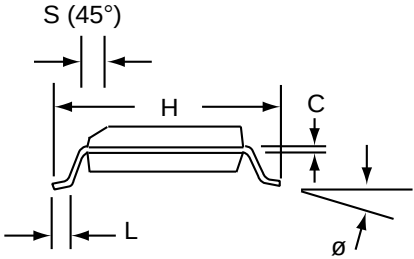
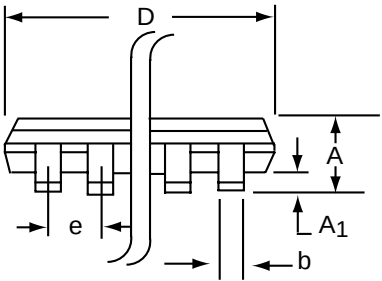
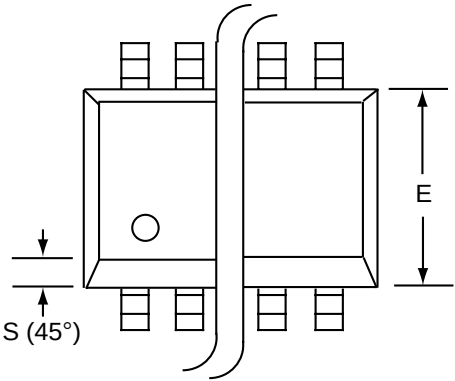


Design & Operating Notes:

1. In order to minimize stray oscillation, all unused inputs must be tied to ground.
2. The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 1pA at room temperature. These currents are a function of ambient temperature, and would have to be considered in applications where very high source impedance or high accuracy are involved.
3. The high output sinking current of 60mA for each output offers flexibility in many applications, as a separate buffer or driver would not be necessary to drive the intended load. However, as the circuit normally operates close to ambient temperature due to its very low power consumption, thermal effects caused by large output current transients must be considered in certain applications.

SOIC-14 PACKAGE DRAWING

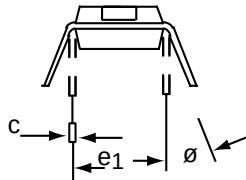
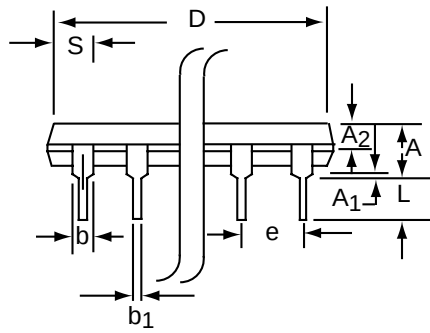
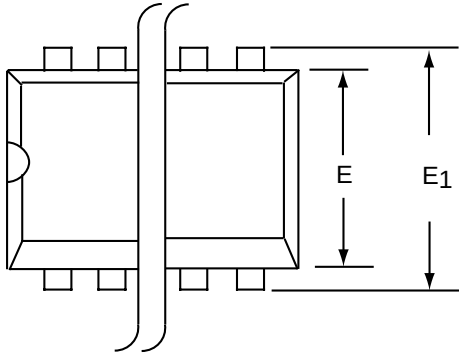
14 Pin Plastic SOIC Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-14	8.55	8.75	0.336	0.345
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

PDIP-14 PACKAGE DRAWING

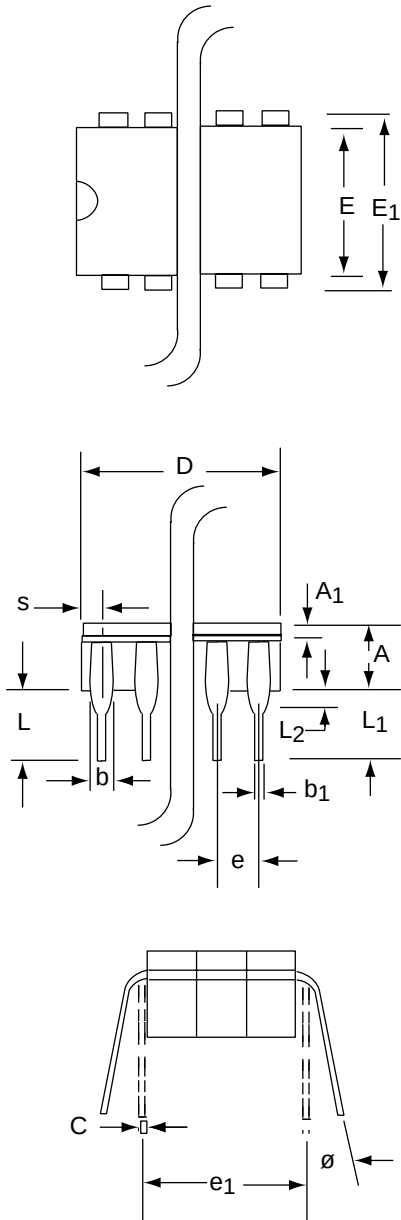
14 Pin Plastic DIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A ₁	0.38	1.27	0.015	0.050
A ₂	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b ₁	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-14	17.27	19.30	0.680	0.760
E	5.59	7.11	0.220	0.280
E ₁	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e ₁	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-14	1.02	2.03	0.040	0.080
Ø	0°	15°	0°	15°

CERDIP-14 PACKAGE DRAWING

14 Pin CERDIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.55	5.08	0.140	0.200
A₁	1.27	2.16	0.050	0.085
b	0.97	1.65	0.038	0.065
b₁	0.36	0.58	0.014	0.023
C	0.20	0.38	0.008	0.015
D-14	--	19.94	--	0.785
E	5.59	7.87	0.220	0.310
E₁	7.73	8.26	0.290	0.325
e	2.54 BSC		0.100 BSC	
e₁	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L₁	3.18	--	0.125	--
L₂	0.38	1.78	0.015	0.070
S	--	2.49	--	0.098
Ø	0°	15°	0°	15°

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