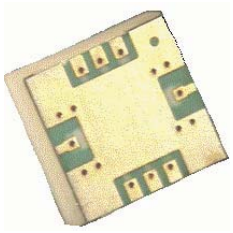
AMMP-6532
20-32 GHz GaAs MMIC LNA/IRM Receiver
in SMT Package

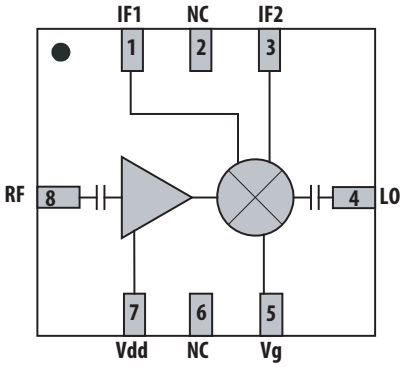
Data Sheet



Description

Avago Technologies' AMMP-6532 is an easy-to-use broadband integrated receiver in a surface mount package. The MMIC includes a 4, -stage LNA to provide gain amplification and a gate-pumped image-reject mixer for frequency translation. The overall receiver performs Single Side Band down-conversion in the 20 to 32 GHz RF signal range. The LO and RF are matched to 50Ω. The IF output is provided in 2-port format where an external 90-degree hybrid can be utilized for full image rejection. The LNA requires a 3V, 83mA power supply, where the mixer bias is a simple –1V, 0.1mA. The MMIC is fabricated using PHEMT technology. The surface mount package allows elimination of "chip & wire" assembly for lower cost. This MMIC is a cost effective alternative to multi-chip solution that have higher loss and complex assembly.

Pin Connections (top View)



Top view
Package base: GND

Pin	Function
1	IF1
2	NC
3	IF2
4	LO
5	Vg
6	NC
7	Vdd
8	RF

Note:
1. This MMIC uses depletion mode pHEMT devices.
2. Negative supply is used for mixer bias.

Features

- Surface Mount Package (5.0 x 5.0 x 1.25 mm)
- Integrated Low Noise Amplifier
- Integrated Image Reject Mixer
- 50 Ω Input and Output Match
- Single Supply Bias Pin

Specifications Vd=3.0V (83mA), Vg=-1.0V (0.1mA)

- RF Frequency: 20 to 32 GHz
- IF frequency: 1 to 5 GHz
- Conversion Gain (RF/IF): 13dB
- Input Intercept Point: -4dBm
- Image Supression: > 15 db
- Total Noise Figure: 3 dB

Applications

- Microwave Radio systems
- Satellite VSAT, DBS Up/Down Link
- LMDS & Pt-Pt mmW Long Haul
- Broadband Wireless Access
  (including 802.16 and 802.20 WiMax)
- WLL and MMDS loops

Attention: Observe Precautions for handling electrostatic sensitive devices.
ESD Machine Mode (Class A): 50V
(Class 0): 150V
ESD Human Body Model (Class 1A)
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

Absolute Maximum Ratings [1]

Symbol	Parameters/Condition	Units	Max
Vdd	Drain to Ground Voltage	V	5.5
Vg	Gate to Ground Voltage	V	+0.8
Idd	Drain Current	mA	100
Ig	Gate Current	mA	1
Pin	RF CW Input Power Max	dB	10
Tch	Max Channel Temperature	C	+150
Tstg	Storage Temperature	C	-65 to +150
Tmax	Maximum Assembly Temp	C	360 for 60s

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.

DC Specifications/ Physical Properties [2]

Symbol	Parameters and Test Conditions	Units	Min	Typ	Max
Vdd	Drain Supply Voltage	V		3	5
Idd	Drain Supply Current (Vd=4.0 V)	mA	60		90
Vg	Gate Supply Voltage (Ig= 0.1mA)	V		-1.0	
Tjc	Thermal Resistance[3]	C/W		27	

Notes:
2. Ambient operational temperature T_A=25°C unless noted
3. Channel-to-backside Thermal Resistance (Tchannel = 34°C) as measured using infrared microscopy. Thermal Resistance at backside temp. (T_b) = 25°C calculated from measured data.

Operating Conditions

Symbol	Parameters and Test Conditions	Units	Minimum	Typical	Maximum
RFfreq	RF Frequency	GHz	20		32
LOfreq	LO Frequency	GHz	18		34
IFfreq	IF Frequency	GHz	1		3.5
LO	LO Drive Power	dBm	+10	+15	+22

AMMP-6532 RF Specifications [4,5,6]

T_A= 25°C, V_{dd} = 3.0 V, I_{dq} =83 mA, V_g = -1V, Z_o=50Ω, LO=+15 dBm, IF=2GHz.

Symbol	Parameters and Test Conditions	Freq (GHz)	Unit	Minimum	Typical	Maximum
NF	Noise Figure into 50Ω [5]	RF=22,LO=24 RF=30,LO=32	dB		3	4.5
CG	Conversion Gain[5]	RF=22,LO=24 RF=30,LO=32	dB	10	13	
IIP3	Input Third Order Intercept Point	RF=22,LO=24 RF=30,LO=32	dBm	-5	-4	
SUP	Image Rejection	RF=22,LO=24 RF=30,LO=32	dB	15		

Notes:
4. Small/Large -signal data measured in a fully de-embedded test fixture form T_A = 25°C.
5. This final package part performance is verified by a functional test correlated to actual performance at one or more frequencies
6. Specifications are derived from measurements in a 50Ω test environment. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity, or low noise (Γopt) matching.

AMMP-6532 Typical Performance

Data obtained from 2.4-mm connector based test fixture, and this data is including connecter loss, and board loss. (T_A = 25°C, Vdd=3V, Idq=83mA, V_g=-1.1 V, Z_{in} = Z_{out} = 50Ω)

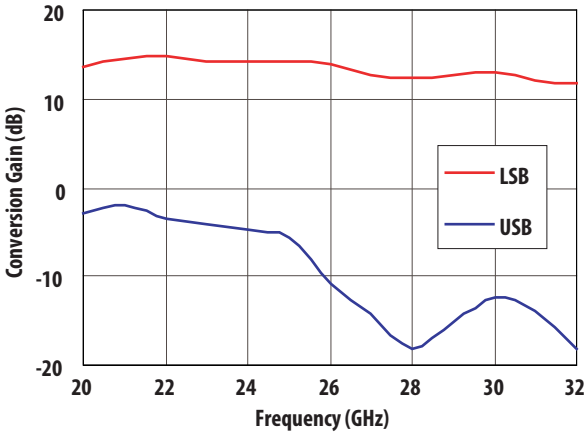


Figure 1. Receiver Conversion Gain

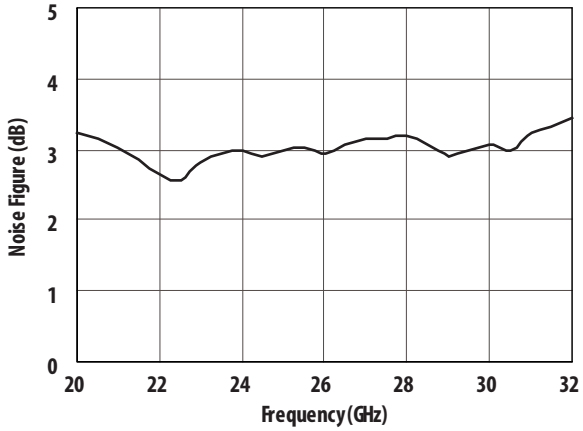


Figure 2. Typical Noise Figure

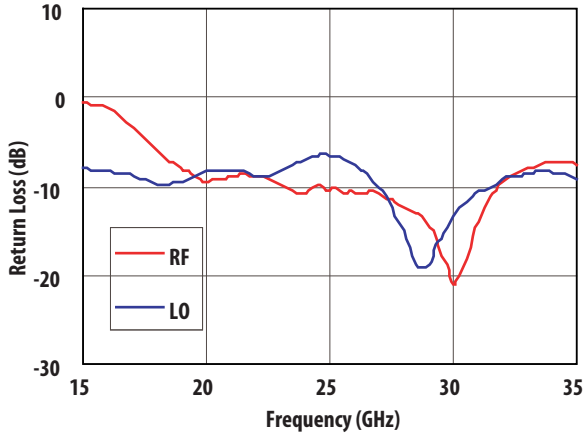


Figure 3. Return Loss at RF & LO Ports

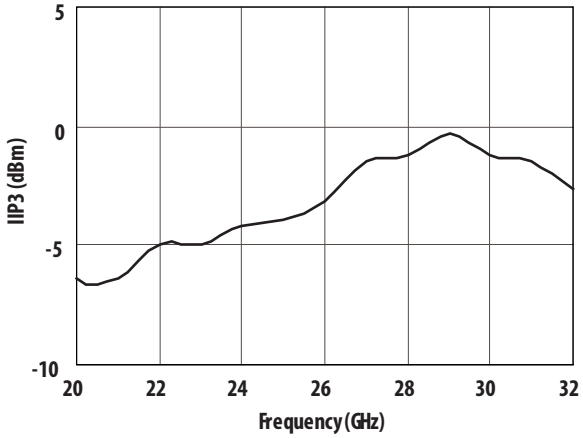


Figure 4. Typical Input IP3

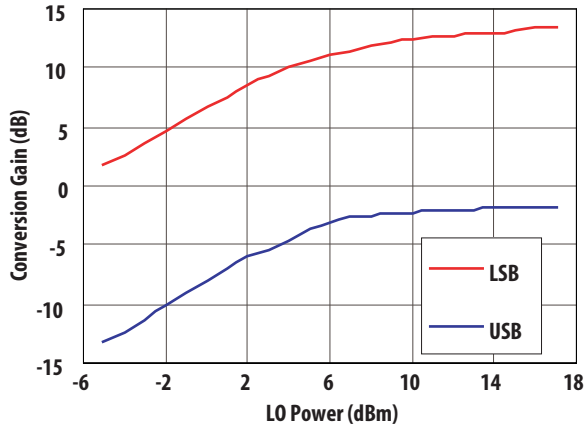


Figure 5. Cony Gain vs. LO Power (RF=23GHz)

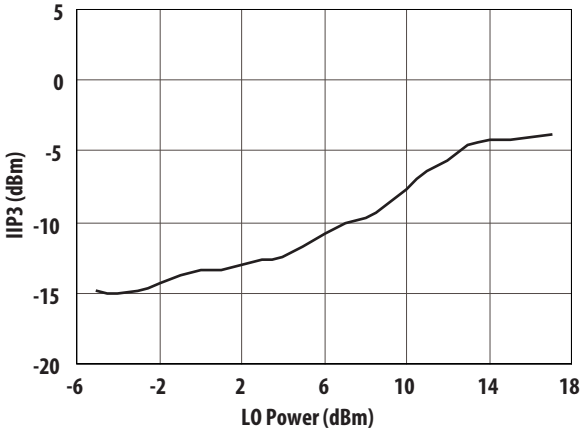


Figure 6. Input IP3 vs. LO Power (RF=23GHz)

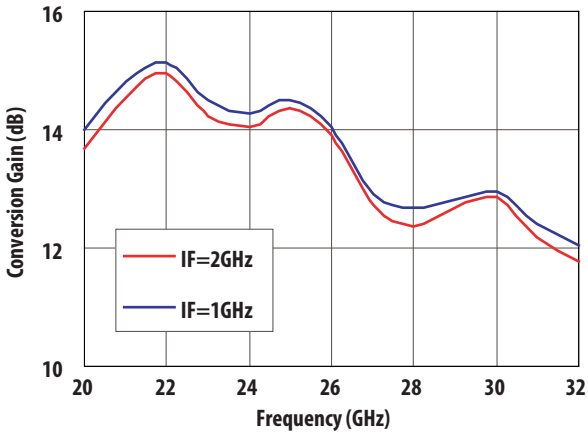


Figure 7. LSB Conversion Gain at Two IF Frequencies

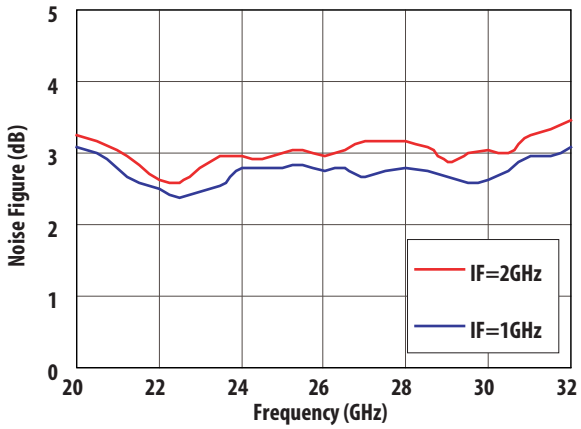


Figure 8. Noise Figure at Two IF Frequencies

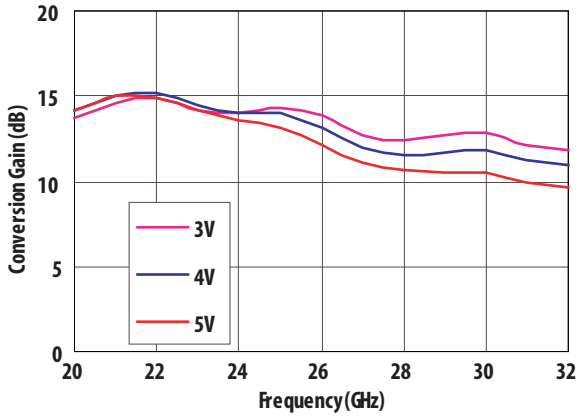


Figure 11. Receiver Conversion Gain over Vdd

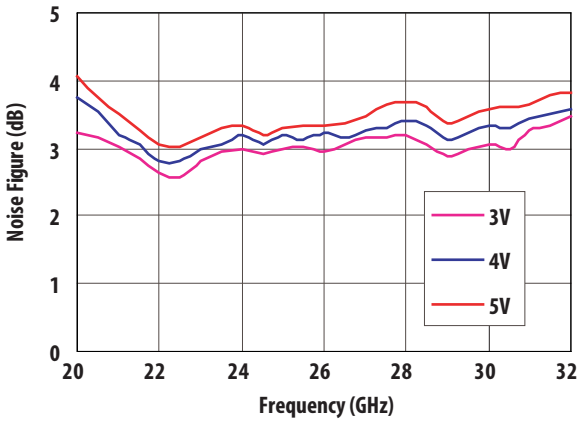


Figure 12. Noise Figure over Vdd

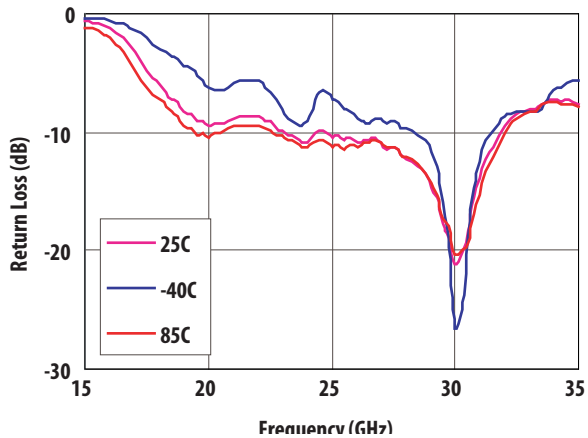


Figure 13. Return Loss at RF oaver Temp

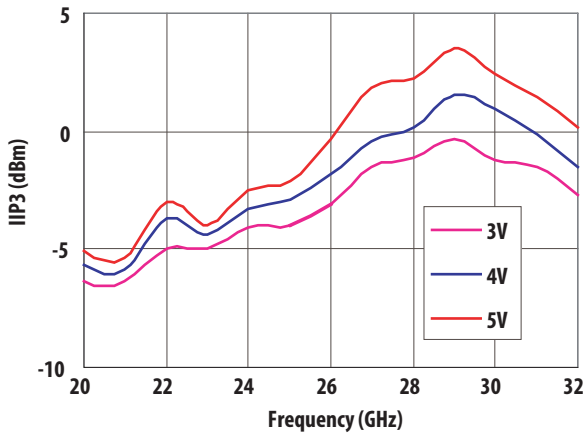


Figure 14. Input IP3 over Vdd

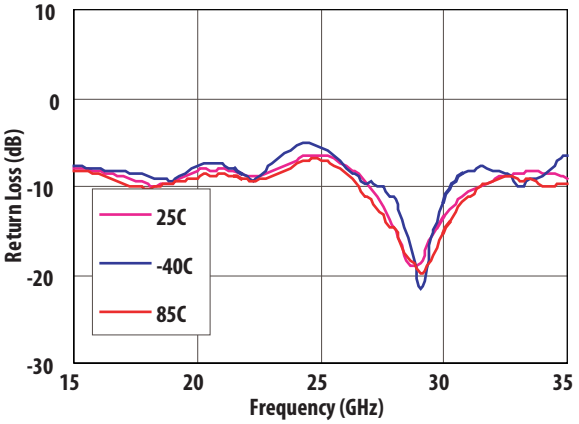


Figure 15. Return Loss at LO over Temp

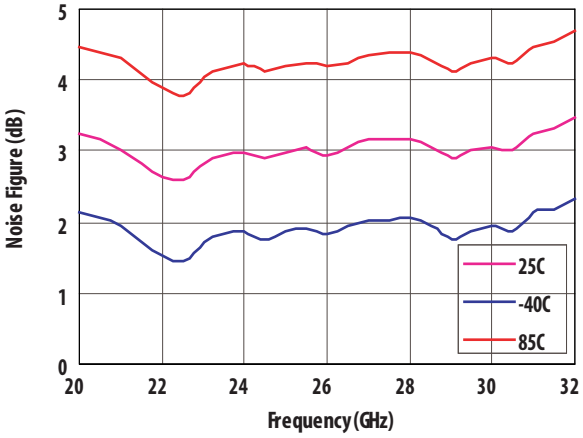


Figure 16. Noise Figure over Temp

AMMP-6532 Application and Usage

Biasing and Operation

The AMMP-6532 is normally biased with a positive drain supply connected to the VDD pin and a negative gate voltage connected to the Vg pin through bypass capacitors as shown in Figure 17. The recommended drain supply voltage is 3 V and gate bias voltage is -1V. The corresponding currents are 83mA and 0.1mA respectively. The typical required LO level is +15dBm and it should come from a low noise driver to ensure that overall Front End NF is low.

The image rejection performance is dependent on the selection of the IF quadrature hybrid. The performance of the IF hybrid as well as the phase balance and VSWR of the interface to the AMMP-6532 will affect the overall front end performance. It should be noted that the placement of the external IF Hybrid coupler should be as symmetrical as possible in regard to the two IF outputs to obtain optimal performance.

The NF will be lowest when the IF hybrid's phase and magnitude imbalance are smallest since noise from image signal is greatly rejected.

Theoretically, IF frequencies can be as low as DC. However, when direct conversion is used (IF=DC), a so-called phenomenon DC-offset could occur at the two IF outputs. In most practical applications, IF should be more than a few hundreds KHz to avoid DC-offset correction.

Refer the Absolute Maximum Ratings table for allowed DC and thermal condition.

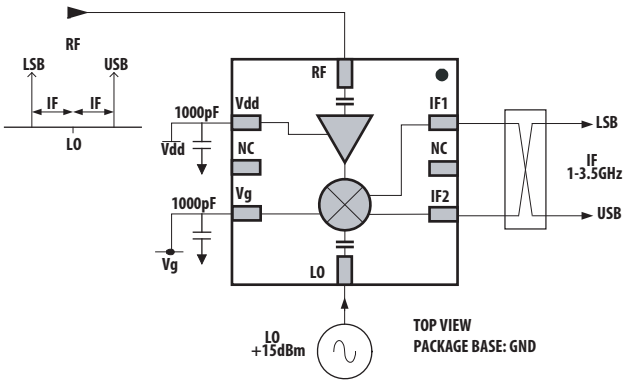


Figure 17. Application of Receiver with IF Balun

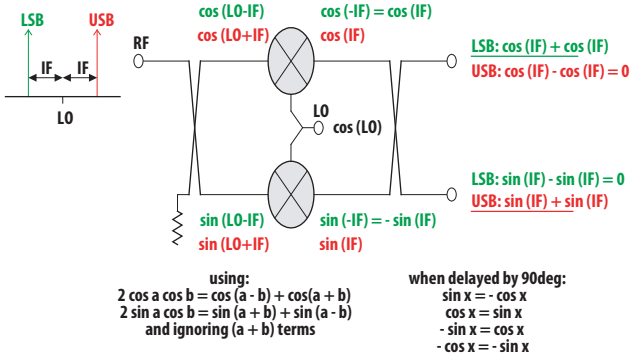


Figure 18. Theory of Harmonic Rejection

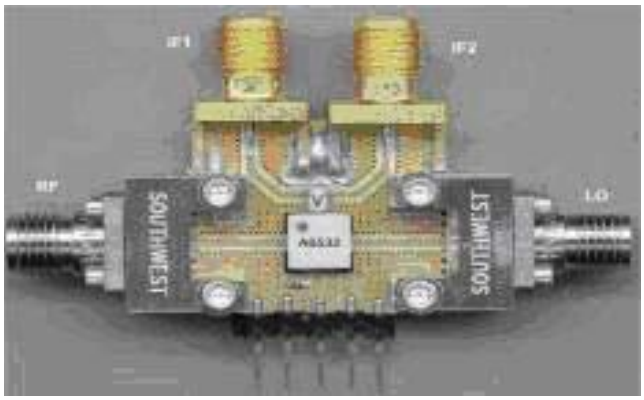


Figure 19. Evaluation / Test Board

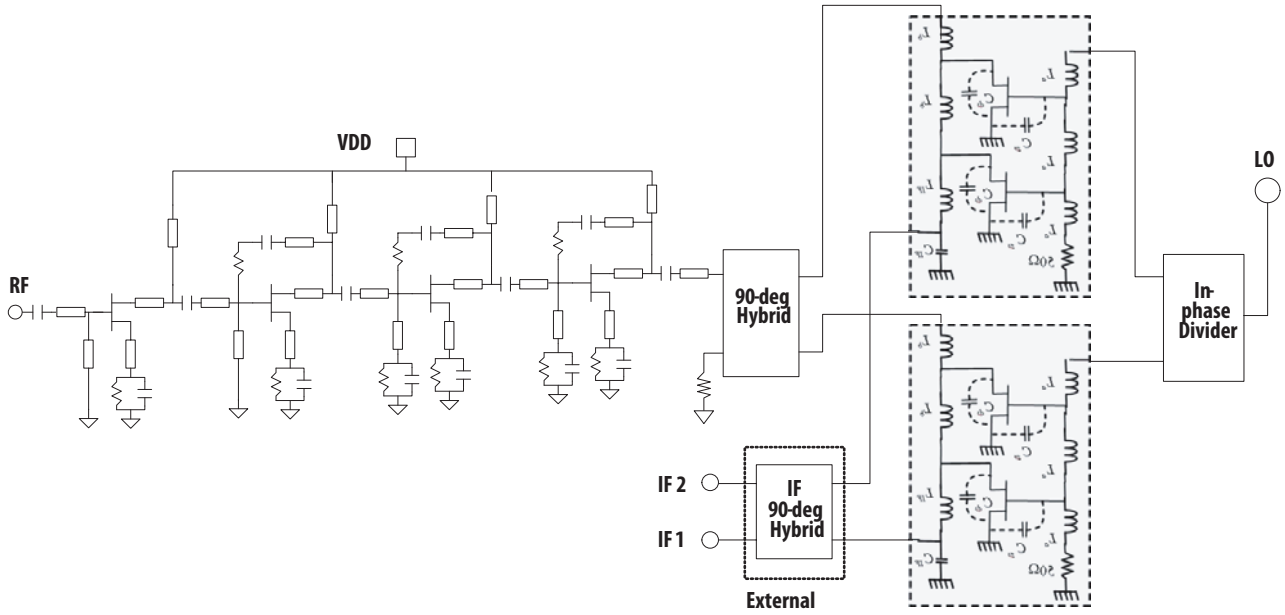
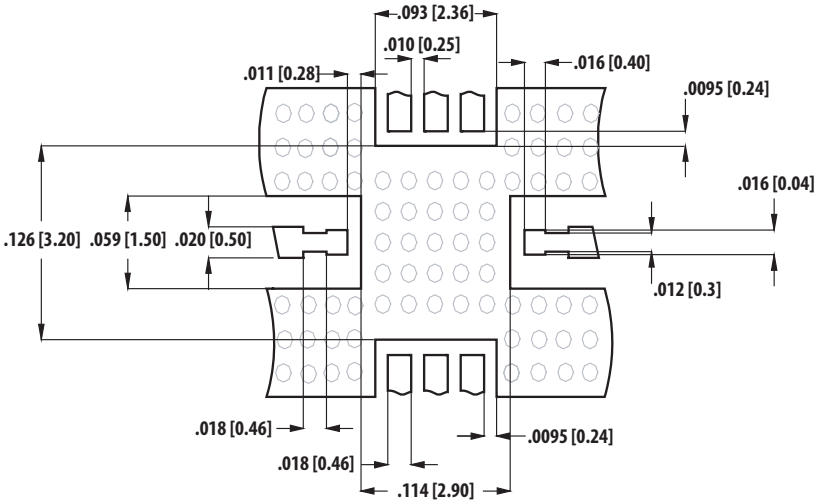
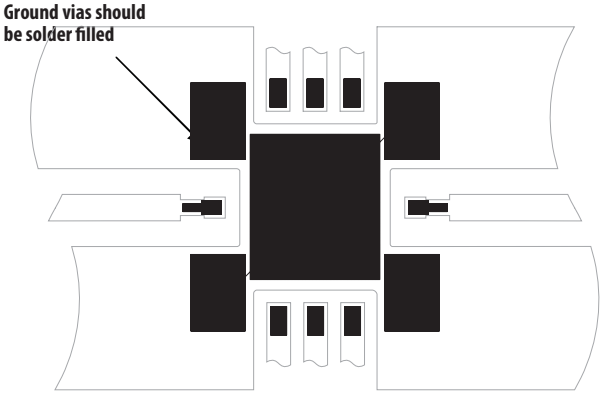


Figure 20. Simplified LNA with IRM Receiver Schematic (the IF quadrature hybrid is external to the circuit)

Recommended SMT Attachment for 5x5 Package





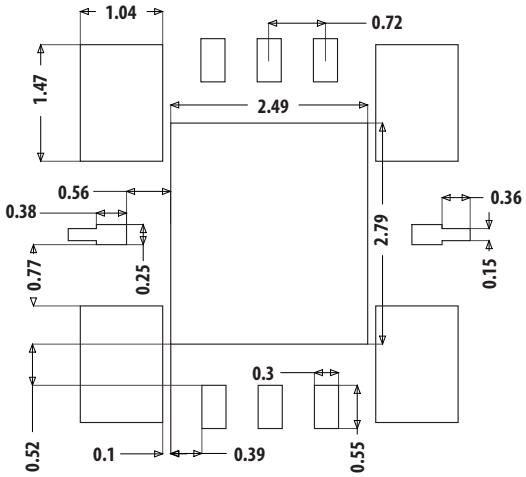


Figure 21. PCB Land Pattern and Stencil Layouts

The AMMP Packaged Devices are compatible with high volume surface mount PCB assembly processes.

The PCB material and mounting pattern, as defined in the data sheet, optimizes RF performance and is strongly recommended. An electronic drawing of the land pattern is available upon request from Avago Sales & Application Engineering.

Manual Assembly

- Follow ESD precautions while handling packages.
- Handling should be along the edges with tweezers.
- Recommended attachment is conductive solder paste. Please see recommended solder reflow profile. Neither Conductive epoxy or hand soldering is recommended.
- Apply solder paste using a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance.
- Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temp. to avoid damage due to thermal shock.
- Packages have been qualified to withstand a peak temperature of 260°C for 20 seconds. Verify that the profile will not expose device beyond these limits.A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads. The recommended stencil layout is shown in Figure 15b. The stencil has a solder paste deposition opening approximately 70% to 90% of the PCB pad. Reducing stencil opening can potentially generate more voids underneath. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use a laser cut stencil composed of 0.127mm (5 mils) thick stainless steel which is capable of producing the required fine stencil outline.

AMMP-6532 Part Number Ordering Information

Part Number	Devices Per Container	Container
AMMP-6532-BLKG	10	Antistatic bag
AMMP-6532-TR1G	100	7″ Reel
AMMP-6532-TR2G	500	7″ Reel

The most commonly used solder reflow method is accomplished in a belt furnace using convection heat transfer. The suggested reflow profile for automated reflow processes is shown in Figure 22. This profile is designed to ensure reliable finished joints. However, the profile indicated in Figure 1 will vary among different solder pastes from different manufacturers and is shown here for reference only.

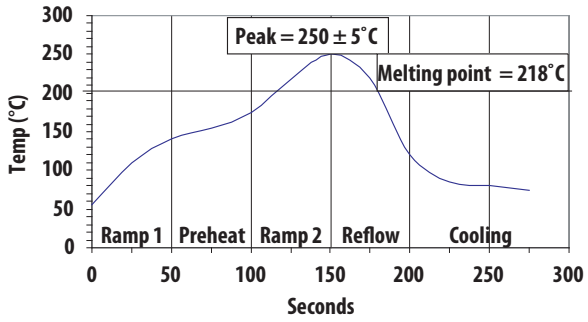
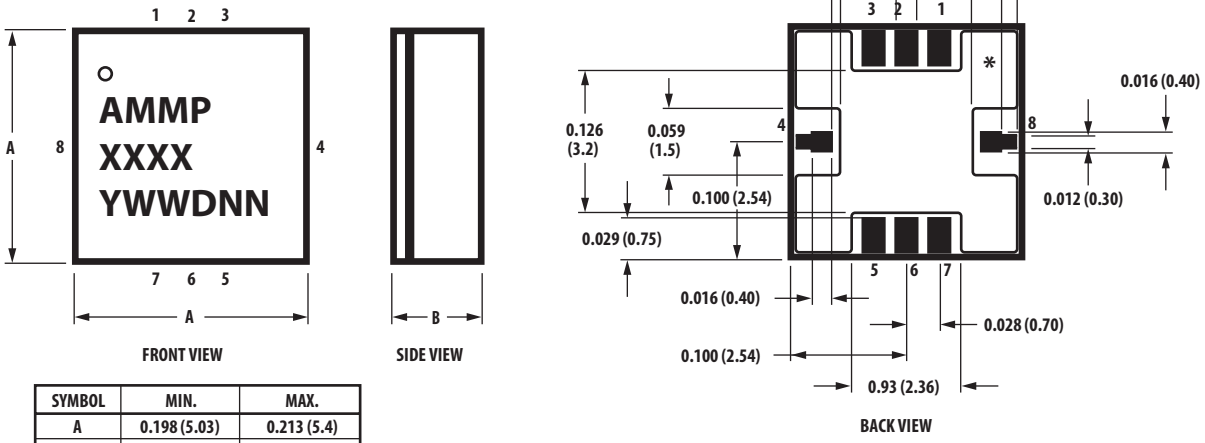


Figure 22. Suggested Lead-Free Reflow Profile for SnAgCu Solder Paste

Package Dimensions



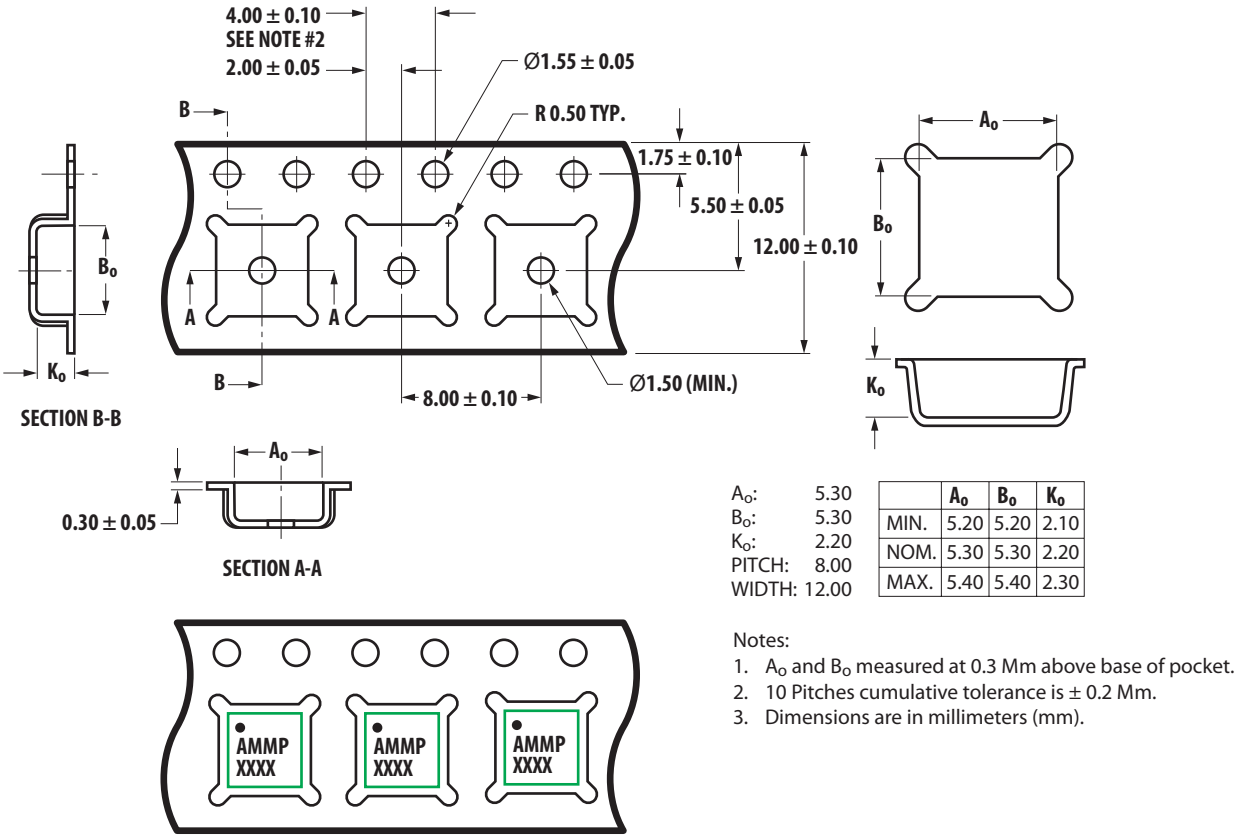
SYMBOL	MIN.	MAX.
A	0.198 (5.03)	0.213 (5.4)
B	0.0685 (1.74)	0.088 (2.25)

DIMENSIONS ARE IN INCHES (MM)

DIMENSIONAL TOLERANCE FOR BACK VIEW: 0.002" (0.05 mm)

NOTES:
1. * INDICATES PIN 1
2. DIMENSIONS ARE IN INCHES (MILLIMETERS)
3. ALL GROUNDS MUST BE SOLDERED TO PCB RF GROUND

Tape Dimensions



Ao: 5.30
Bo: 5.30
Ko: 2.20
PITCH: 8.00
WIDTH: 12.00

	Ao	Bo	Ko
MIN.	5.20	5.20	2.10
NOM.	5.30	5.30	2.20
MAX.	5.40	5.40	2.30

Notes:
1. A_o and B_o measured at 0.3 Mm above base of pocket.
2. 10 Pitches cumulative tolerance is ± 0.2 Mm.
3. Dimensions are in millimeters (mm).

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-1022EN - January 20, 2010