ALPHA & OMEGA SEMICONDUCTOR

# AO4830

## 80V Dual N-Channel MOSFET

### General Description

The AO4830 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge . This device is suitable for use as a load switch or in PWM applications.

### Product Summary

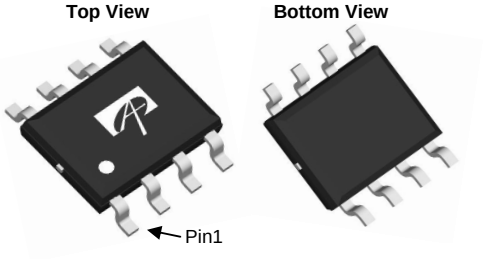
$V_{DS}$ (V) = 80V
$I_D$ = 3.5A ($V_{GS}$ = 10V)
$R_{DS(ON)}$ < 75mΩ ($V_{GS}$ = 10V)

100% UIS Tested
100% Rg Tested

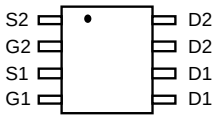
Green Product

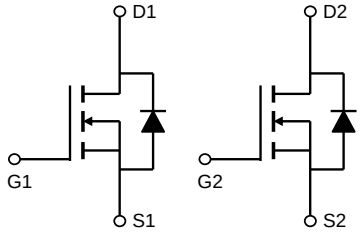
**SOIC-8**

**Top View** **Bottom View**




**Top View**




**Absolute Maximum Ratings $T_A$=25℃ unless otherwise noted**

| Parameter | | Symbol | Maximum | Units |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 80 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±30 | V |
| Continuous Drain Current | $T_A$=25℃ | $I_D$ | 3.5 | A |
| | $T_A$=70℃ | | 2.9 | |
| Pulsed Drain Current [C] | | $I_{DM}$ | 18 | |
| Avalanche Current [C] | | $I_{AR}$ | 16 | A |
| Repetitive avalanche energy L=0.1mH [C] | | $E_{AR}$ | 12.8 | mJ |
| Power Dissipation [B] | $T_A$=25℃ | $P_D$ | 2 | W |
| | $T_A$=70℃ | | 1.3 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | ℃ |

**Thermal Characteristics**

| Parameter | | Symbol | Typ | Max | Units |
|---|---|---|---|---|---|
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 48 | 62.5 | ℃/W |
| Maximum Junction-to-Ambient [A D] | Steady-State | | 74 | 90 | ℃/W |
| Maximum Junction-to-Lead | Steady-State | $R_{\theta JL}$ | 32 | 40 | ℃/W |

**Electrical Characteristics ($T_J$=25°C unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=250µA, $V_{GS}$=0V | 80 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=80V, $V_{GS}$=0V | | | 1 | µA |
| | | $T_J$=55°C | | | 5 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$= ±30V | | | 100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ $I_D$=250µA | 3.5 | 4.2 | 5 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=10V, $V_{DS}$=5V | 18 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=10V, $I_D$=3.5A | | 62 | 75 | mΩ |
| | | $T_J$=125°C | | 113.0 | 135 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=3.5A | | 15 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=1A,$V_{GS}$=0V | | 0.77 | 1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | 2.5 | A |
| $I_{SM}$ | Pulsed Body-diode Current[C] | | | | 18 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=40V, f=1MHz | 510 | 640 | 770 | pF |
| $C_{oss}$ | Output Capacitance | | 28 | 40 | 52 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | 12 | 20 | 30 | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | 0.9 | 1.8 | 2.7 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$=10V, $V_{DS}$=40V, $I_D$=3.5A | 8 | 11 | 13 | nC |
| $Q_g$(4.5V) | Total Gate Charge | | 4 | 5.5 | 7 | |
| $Q_{gs}$ | Gate Source Charge | | 4 | 5 | 6 | nC |
| $Q_{gd}$ | Gate Drain Charge | | 0.7 | 1.2 | 1.7 | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=40V, $R_L$=8Ω, $R_{GEN}$=3Ω | | 7.2 | | ns |
| $t_r$ | Turn-On Rise Time | | | 2.2 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 17 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 2 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=3.5A, dI/dt=300A/µs | 14 | 20 | 26 | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=3.5A, dI/dt=300A/µs | 35 | 50 | 65 | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial$T_J$=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in$^2$ FR-4 board with

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## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

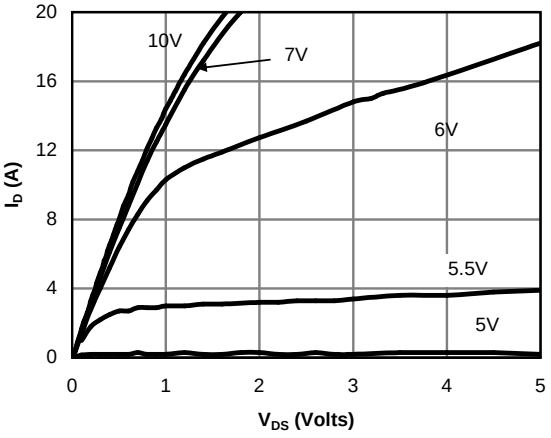



Fig 1: On-Region Characteristics (Note E)

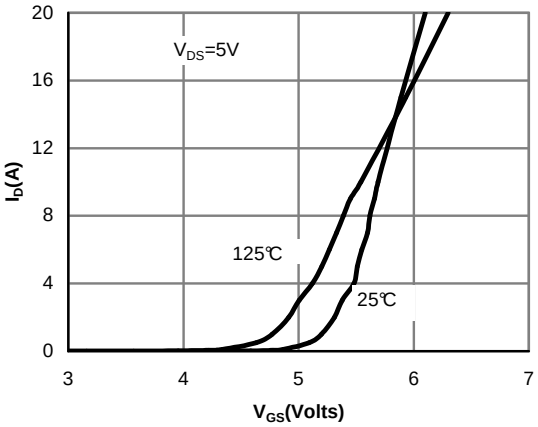



Figure 2: Transfer Characteristics (Note E)

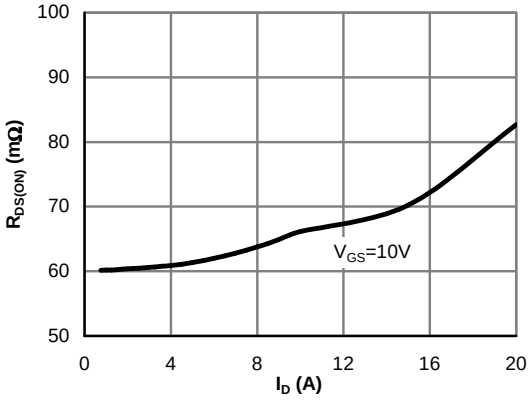



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

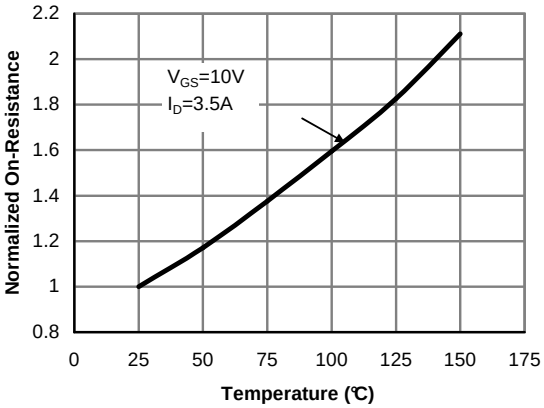



Figure 4: On-Resistance vs. Junction Temperature (Note E)

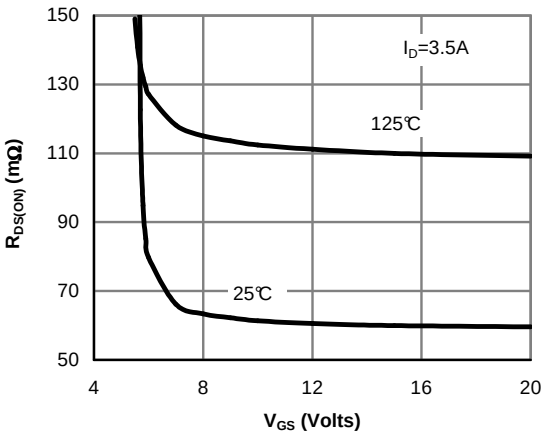



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

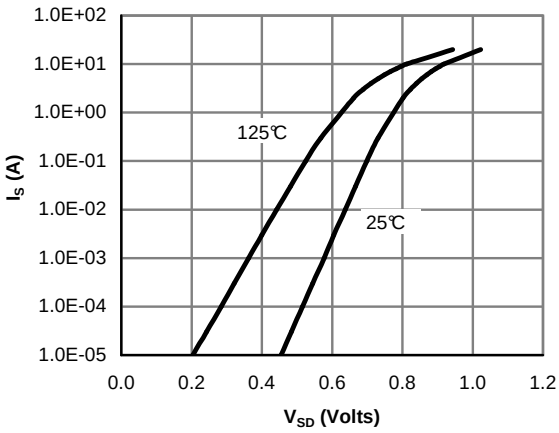



Figure 6: Body-Diode Characteristics (Note E)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

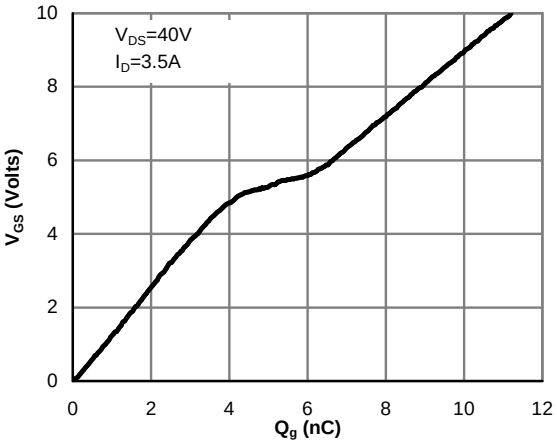



Figure 7: Gate-Charge Characteristics

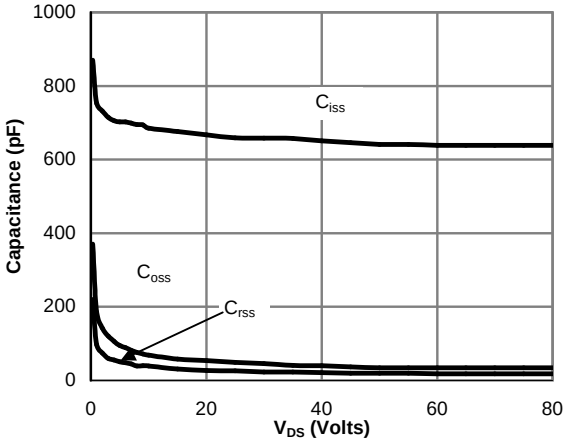



Figure 8: Capacitance Characteristics

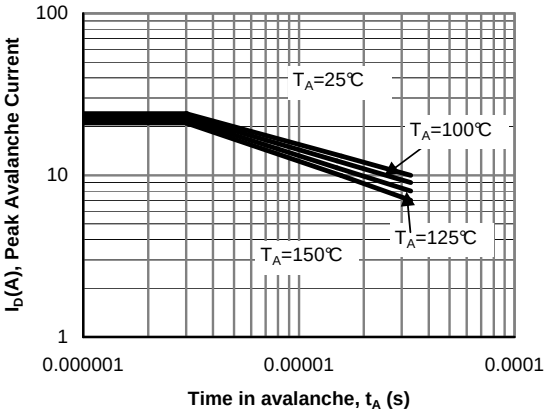



Figure 12: Single Pulse Avalanche capability

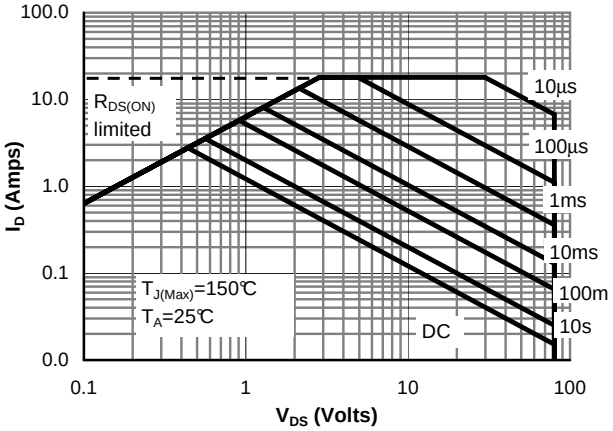



Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

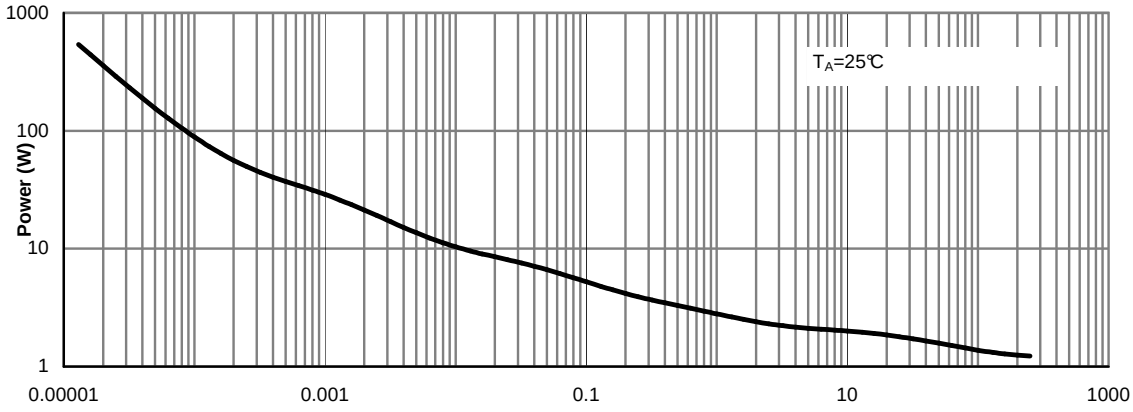



Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

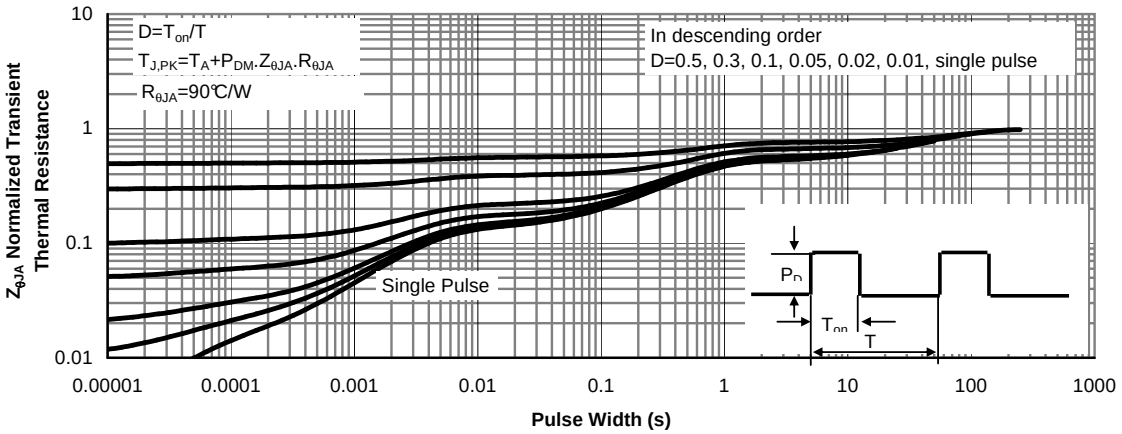
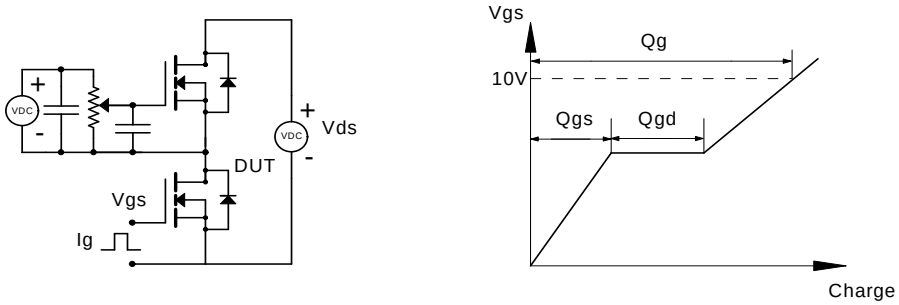
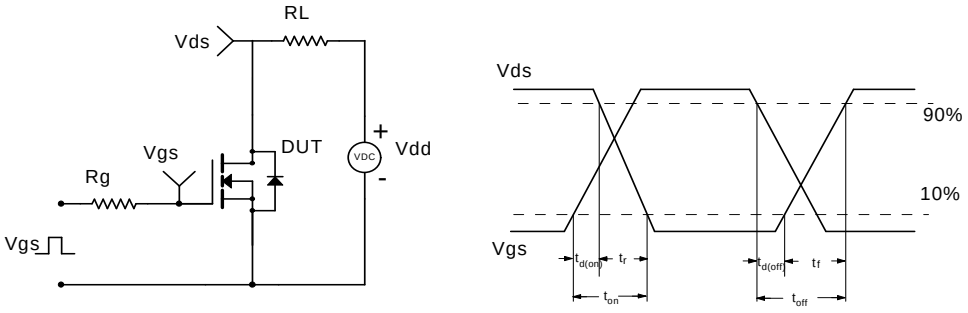



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

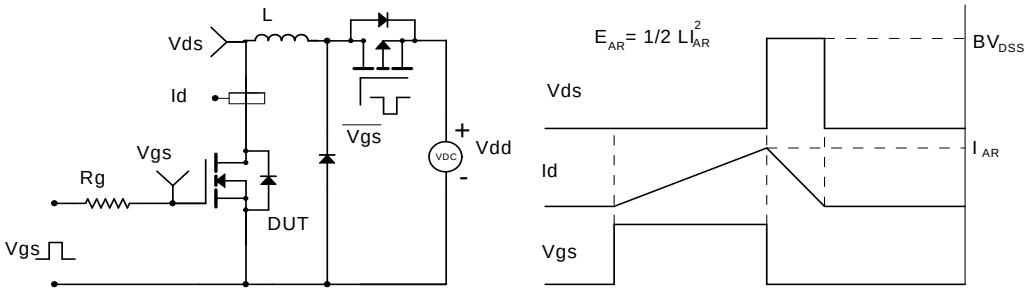
## Gate Charge Test Circuit & Waveform




## Resistive Switching Test Circuit & Waveforms




## Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




## Diode Recovery Test Circuit & Waveforms