AP2403

Current-Mode PWM Step-Down DC-DC Converter

1. Genaral Description

The AP2403 is a Current-Mode Synchronous Step-Down DC-DC Converter with excellent transient response. The output voltage is selectable from the range of 0.8V to 5.0V by an external resistor. The input voltage ranges from 3.0V to 5.5V which is most suitable to generate a 1.0V, a 1.2V, and a 1.8V power supplies. Power MOSFETs are built in the AP2403; the maximum output current of the AP2403 is 2.5A. The switching frequency is selectable from 300 kHz to 4 MHz by the external resistor. For the protections, the AP2403 has Over-Current protection, Low-Input Voltage protection, Thermal protection and Power-Good function.

2. Features

1. **Input Voltage Range:** **Vin = 3.0V to 5.5V**
2. **Output Voltage Range:** **Vout = 0.8V to 5.0V**
   (by the external resistor)
3. **Maximum Output Load Current:** **Iout(max) = 2.5A**
4. **Operation Temperature:** **Ta = -40°C to 105°C**
5. **Switching Frequency:** **300kHz to 4MHz (Selectable by an external resistor and External Synchronous Mode is available by an external clock)**
6. **Internal Reference Voltage:** **0.6V ±1.5%**
7. **Maximum Duty:** **100%**
8. **Low Input Voltage Protection**
9. **Power-Good Function**
10. **Over-Current Protection (Automatic recovery type)**
11. **Thermal Protection**
12. **Soft Start Function**
13. **Package: 16-pin HTSSOP**

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3. Table of Contents

4. Block Diagram and Functions

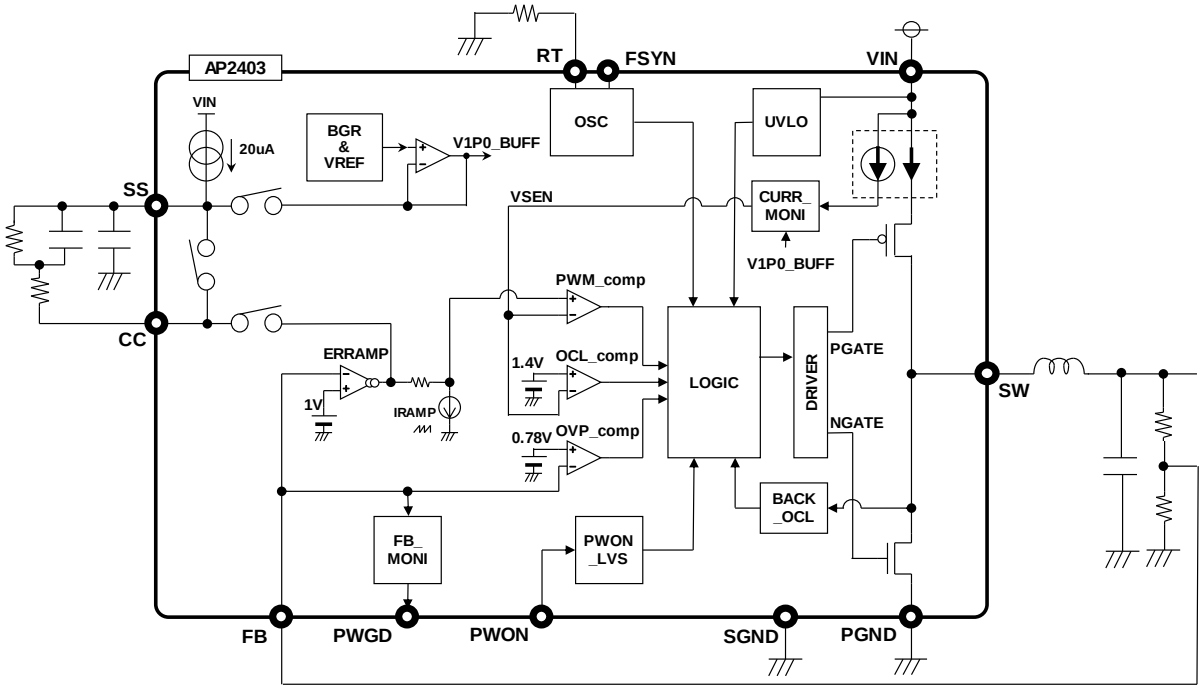


Figure 1. Block Diagram

5. Pin Configurations and Functions

■ Ordering Guide

AP2403	-40°C to 105°C	16-pin HTSSOP

■ Pin Layout

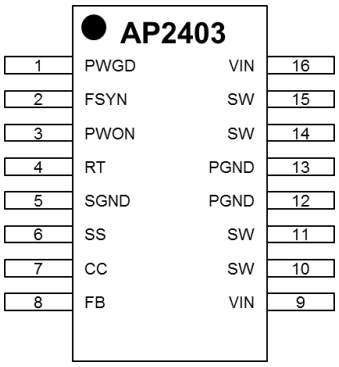


Figure 2. Pin Layout

■ Pin Functions

No.	Pin Name	I/O	Function	Condition (Note 1)
1	PWGD	O	Power-Good Pin When the output voltage reaches the level that is ±20% of the setting voltage, this pin becomes "H".	GND
2	FSYN	I	External Synchronous Clock Input Pin An external clock within ±20% of setting value which is set by the resistor at the RT pin is available.	Internal pull-up resistor to VIN pin is 300kΩ.
3	PWON	I	Power-ON Pin The AP2403 starts operation by inputting a 1.5V or more voltage to this pin.	-
4	RT	O	Operation Frequency Setting Pin The operation frequency is determined by a resistor connected to this pin.	HiZ (connect an external resistor between the GND)
5	SGND		Signal Ground	-
6	SS	O	Soft Start Pin Connect a capacitor of 0.047μF or more between the SS pin and the GND. The AP2403 charges this external capacitor when starts up, and a Soft Start operation is executed. When the over current protection is activated, the external capacitor is discharged and it generates a suspended time in a hiccup operation.	GND
7	CC	O	Output pin of Output Voltage Feedback Amplifier (Error Amp.) Connect a resistor and a capacitor between the CC pin and the SS pin in parallel. These devices compensate the amplifier phase.	GND

8	FB	I	Input pin of Output Voltage Feedback Amplifier (Error Amp.) It controls the output voltage so that the voltage at this pin becomes 0.6V. Connect two resistors for feedback between the output stage and the GND in series, and the FB pin must be connected to the middle point of these two resistors.	HiZ (there is an external resistor between the GND)
9	VIN		Main Power Voltage Input Connect a capacitor of 4.7μF or more between the VIN pin and the GND.	-
10	SW	O	Internal Switching MOSFET Output It is connected to the middle point of the internal output N-channel MOSFET and the P-channel MOSFET.	HiZ
11	SW	O	Internal Switching MOSFET Output It is connected to the middle point of the internal output N-channel MOSFET and the P-channel MOSFET.	HiZ
12	PGND		Power Ground	-
13	PGND		Power Ground	-
14	SW	O	Internal Switching MOSFET Output It is connected to the middle point of the internal output N-channel MOSFET and the P-channel MOSFET.	HiZ
15	SW	O	Internal Switching MOSFET Output It is connected to the middle point of the internal output N-channel MOSFET and the P-channel MOSFET.	HiZ
16	VIN		Main Power Voltage Input Connect a capacitor of 4.7μF or more between the VIN pin and the GND.	-

Note 1. Pin state when the PWON pin = “L”

6. Absolute Maximum Ratings

(GND=0V: Note 2)

Parameters	Symbol	min	max	Unit
VIN pin	Vin	–0.3	6.0	V
SW pin	VSW	–0.3	Vin + 0.3	V
All pins (Except SW pin, VIN pin)	VIND	–0.3	Vin	V
Junction Temperature (Note 4)	Tj1	–40	150	°C
Junction Temperature (Guaranteed Lifetime)	Tj2	–40	135	°C
Operating Ambient Temperature	Ta	–40	105	°C
Storage Ambient Temperature	T_{STG}	–40	150	°C
Power Dissipation (Ta=25°C) (Note 3)	Pd		2750	mW

Note 2. All voltages with respect to the GND pin

Note 3. Thermal Resistance of the package (Rth): 40°C/W (JEDEC51, four layers PCB)

Note 4. Continuous operation above Tj=135°C may impair device reliability.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(GND=0V)

Parameter	Symbol	min	typ	max	Unit
VIN pin voltage	Vin	3.0	–	5.5	V
Output Current	Iout	0	–	2.5	A
Operating Ambient Temperature	Top	–40	–	105	°C

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Electrical Characteristics

(VIN=5.0V, Tj=–40°C to 135°C, unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit	Conditions
Operating Input Voltage Range	Vin	3.0	-	5.5	V	
Feedback REF Voltage	V_{FBref}	591	600	609	mV	Tj=25°C
Operation Current Consumption (No Switching)	ISUPPLY	0.48	0.8	1.12	mA	Tj=25°C
Stand-by Current	Istandby	-	-	10	μA	Tj=25°C
Load Regulation (Note 5)	ΔVLOAD	-	1	-	%	0A to 2A, Ta=-40°C to 105°C
Output Pch MOSFET $R_{DS(ON)}$	Rpmos	-	65	100	mΩ	Tj=25°C
Output Nch MOSFET $R_{DS(ON)}$	Rnmos	-	65	100	mΩ	Tj=25°C
Over-Current Detection	Ioclpeak	3.15	4.5	-	A	Tj=25°C
Oscillator Frequency	Fosc	300	-	4000	kHz	RT=702kΩ to 47kΩ
FSYN Input Frequency Range	Fext300	240	-	360	kHz	RT=702kΩ (at 300kHz)
	Fext2000	1600	-	2400	kHz	RT=100kΩ (at 2MHz)
Oscillator Accuracy	Facu	–20	0	20	%	RT=100kΩ (at 2MHz), Tj=25°C
Maximum ON Duty (Note 5)	MAXDuty	-	-	100	%	
UVLO Detection Voltage	Vuvlo	2.30	2.50	2.85	V	
UVLO Release Voltage	Vuvlorel	2.35	2.70	2.90	V	
UVLO Hysteresis	Vuvhys	0.05	0.20	0.50	V	
Output Over Voltage Detection	Vovp	+26	+30	+34	%	against VFBref
Charge Current (to Capacitor of Soft Start)	Iss+	18.0	20.0	22.0	μA	Css=0V → 1.0V (at rise) Tj=25°C
Discharge Current (to Capacitor of Soft Start)	Iss-	0.70	1.0	1.30	μA	Css=1.0V→0.40V (at fall) Tj=25°C (in hiccup operation)
Thermal Protection Detection (Note 6)	Tsd	135	155	185	°C	
Thermal Protection Hysteresis (Note 6)	Tsdhys	5	15	25	°C	
High side Power Good Detection	Vpgonh	+16	+20	+24	%	by contrast with VFBref
High side Power Good Release	Vpgoffh	+21	+25	+29	%	by contrast with VFBref
Low side Power Good Detection	Vpgonl	–16	–20	–24	%	by contrast with VFBref
Low side Power Good Release	Vpgoffl	–21	–25	–29	%	by contrast with VFBref
Power Good Hysteresis	Vpghys	3	5	7	%	
Power-OFF Threshold	Vponl	-	-	0.4	V	
Power-ON Threshold	Vponh	1.5	-	-	V	
Power-ON Hysteresis	Vponhys	50	100	150	mV	
Gm (Error amplifier)	Gm	360	500	730	μA/V	Tj=25°C
Threshold voltage (of FSYN pin)	VEih	0.7*VIN	-	-	V	Tj=25°C
	VEil	-	-	0.3*VIN	V	Tj=25°C
Output voltage (of PWGD pin)	VPoh	VIN–0.4	-	-	V	Ipoh=–100μA
	VPol	-	-	0.4	V	Ipol=100μA

Note 5. A reference value with the recommended circuit
Note 6. Design assurance values

9. Functional Descriptions

1. Shutdown

The AP2403 is in shutdown condition when a Low signal is input to the PWON pin even if power supply was input to the VIN pin. When a High signal is input to the PWON pin, the AP2403 is powered up in soft-start mode.

2. Soft Start Mode:

This function prevents an overshoot of the output voltage when the AP2403 is powered up. It controls the output voltage slowly. During the soft-start period a capacitor connected to the SS pin is charged from 0V to 1.0V by a 20μA constant current. In soft start, an output voltage rising is controlled by changing the over-voltage limitation value linearly in accordance with the SS pin voltage. When this function starts, the over-current limitation value is fixed in 50% (2.25A typ.). It changes linearly during the period which the SS pin voltage increases to 1.0V from 0.5V. When a soft start operation is completed, the AP2403 shifts to a PWM control.

3. Constant Voltage Operation:

The AP2403 operates by Current-mode PWM controls. It determines the target value of inductance current by amplifying the voltage difference between the FB pin and 0.6V which is feedback reference voltage. The internal P-channel MOSFET is powered on until the inductance current meets the target value. When the inductance current reaches the target value, the built-in P-channel MOSFET becomes OFF and the built-in N-channel MOSFET becomes ON. Then the AP2403 operates in synchronous rectification mode.

4. Prevention of Incorrect Operation in Low Voltage (UVLO: Under Voltage Lock Out):

When the V5 pin voltage becomes less than 2.5V by a main power supply voltage decrease, all circuit blocks in the AP2403 are stopped and the AP2403 becomes UVLO state. The UVLO state has hysteresis, and the AP2403 keeps UVLO state until the main power supply voltage rises again and exceeds 2.5V. When the UVLO state is released, the AP2403 restarts by a soft start operation.

5. Output Over-Voltage Protection (OVP):

When the output voltage becomes +30% or more of the setting value, the built-in P-channel MOSFET and the built-in N-channel MOSFET become OFF state and the AP2403 enters protection mode. This state is maintained until the built-in P-channel MOSFET is turned on by the FB amplifier. The AP2403 is in normal operation when recovering from the output over-voltage protection. It does not shift to soft-start mode.

6. Hiccup type Output Over-Current Limitation (OCL):

This function reduces the output voltage and the output current by Hiccup operation in an over-current condition. When the over-current condition is detected, the built-in P-channel MOSFET and the built-in N-channel MOSFET become OFF and the SS pin voltage which is 1.0V discharged from 1.0V to 0.4V by a continuous current of 1.0uA. The AP2403 stops its operation without shifting to a soft start operation in this discharging period of the SS pin. When the SS pin voltage decreases to 0.4V, the AP2403 enters a soft start operation after the SS pin voltage is discharged further to the GND level by the internal switch. The AP2403 repeats this sequence until the over current condition is removed.

7. Thermal Protection (TSD: Thermal Shutdown)

The chip temperature is monitored, and the built-in P-channel MOSFET and the built-in N-channel MOSFET are stopped when the chip temperature becomes about 150°C. The thermal protection function discharges electrical charge of the SS pin at this time, therefore a recovery sequence from the thermal protection is always in a soft start operation. This function has a hysteresis, and the AP2403 is restarted by soft start when the chip temperature decreases 15°C from the thermal shutdown threshold.

8. Oscillation Frequency Setting:

The oscillation frequency is determined by a resistor which is connected between the RT pin and the GND. Refer to the equation of this resistor value for frequency setting in the page of the application information.

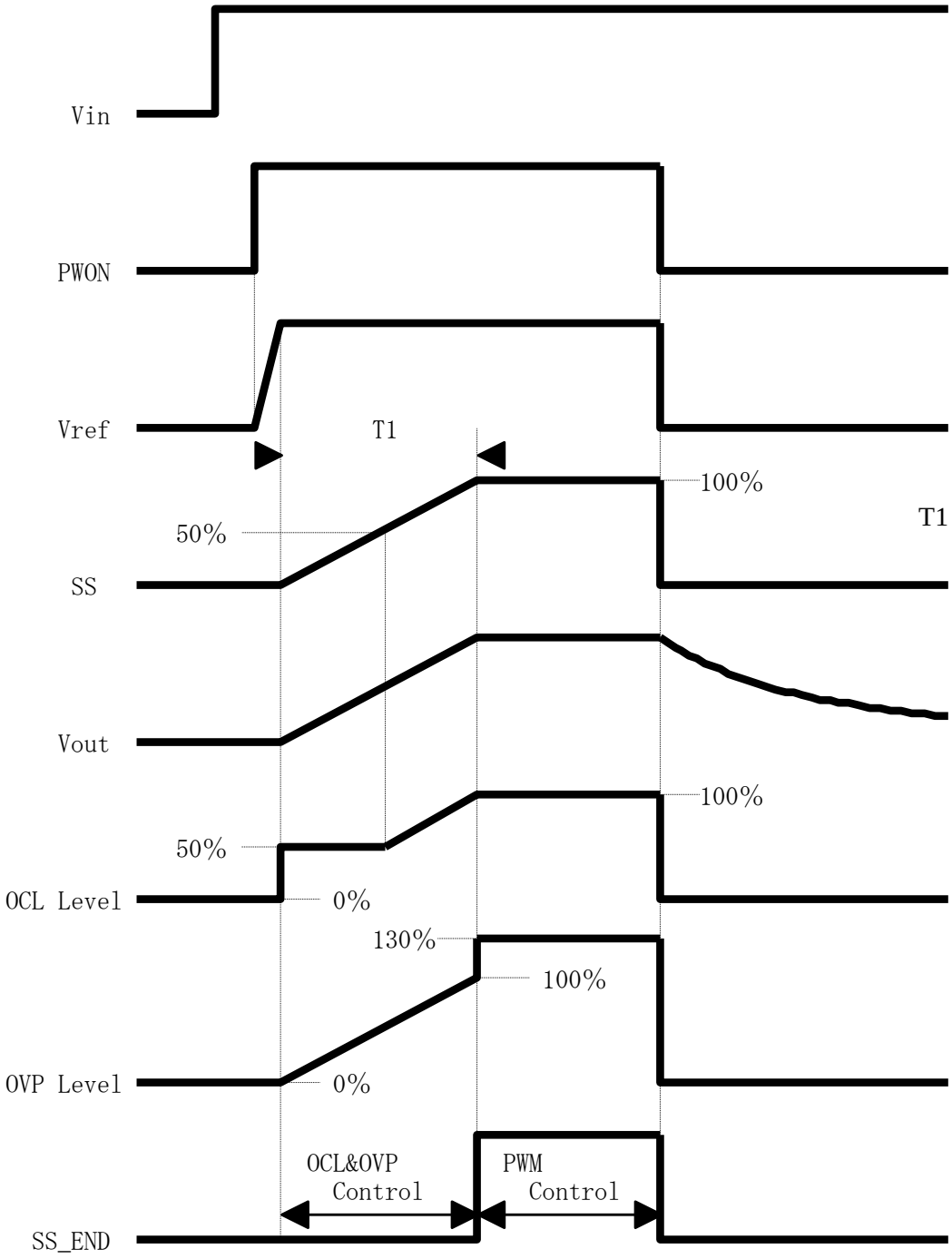
9. External Synchronization

External synchronization is available by inputting a clock to the FSYN pin. The external synchronization frequency is determined by a resistor which is connected between the RT pin and the GND, and the AP2403 accepts a frequency within ±20% of this setting value.

10. Power Good

The AP2403 has a power-good function which indicates output voltage condition. The PWGD pin becomes High level (VIN level), when the output voltage reaches a level that is within ±25% of the setting value. The PWGD pin is always in Low level, during a power-off condition and a soft start operation.

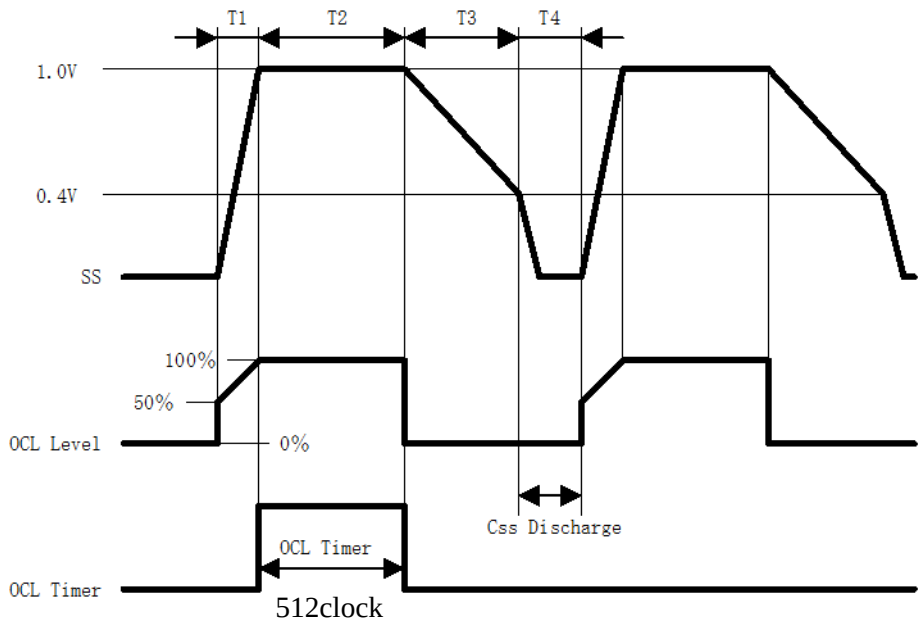
■ Start-up Timing



$$T1 : \frac{Css}{20 \times 10^{-6}} \quad [s]$$

Figure 3. Start Up Timing

■ Over Current Protection Timing



T1: $\frac{Css}{20\times10^{-6}}$ [s]

T2: 512clock

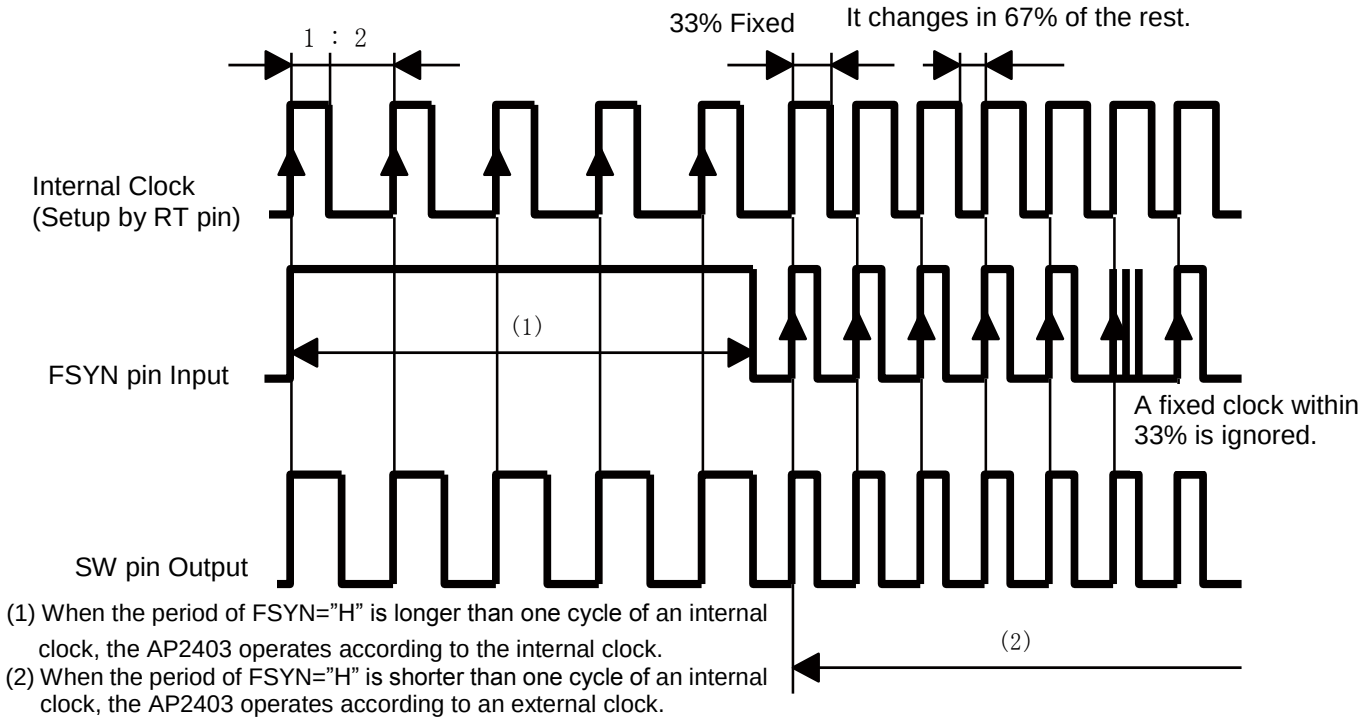
T3: $\frac{0.6\times Css}{1\times10^{-6}}$ [sec]

T4: 384clock

When SS=0.1µF,	T1: Soft Start Time is 5ms,	T3: Rest Time is 60ms
	T2: 256µs (512 clocks/2MHz),	T4: 192µs (384 clocks/2MHz)
When Css=0.22µF,	T1: Soft Start Time is 11ms,	T3: Rest Time is 132ms

Figure 4. Over Current Protection Timing

■ External Synchronization Timing



(1) When the period of FSYN="H" is longer than one cycle of an internal clock, the AP2403 operates according to the internal clock.
(2) When the period of FSYN="H" is shorter than one cycle of an internal clock, the AP2403 operates according to an external clock.

The AP2403 accepts an external clock within ±20% of the setting frequency which is determined by the resistor of the RT pin for an external synchronization.

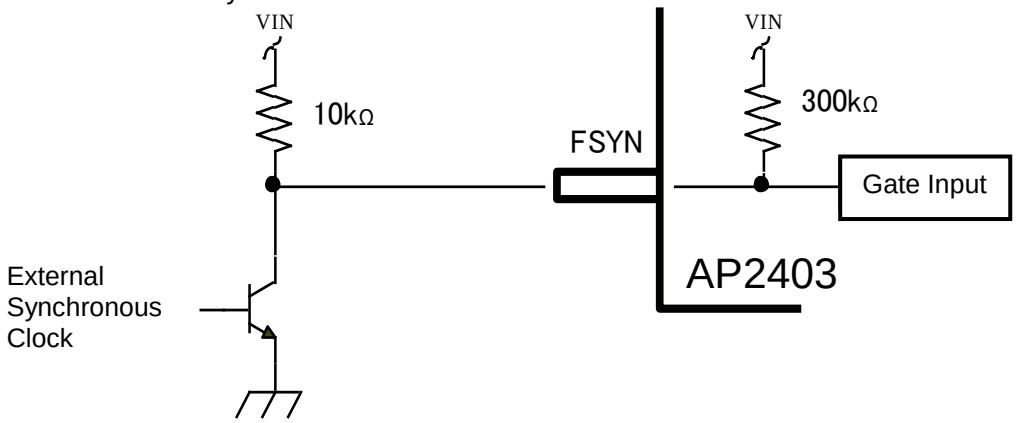


Figure 5. External Synchronous Timing

10. Application Information

1. Inductance:

An external inductor must be selected so that the maximum ripple current will be 30% of the rated current. The main power voltage (Vin) is the maximum value of input voltage range. The external inductor value is determined by following equation.

$$L = \frac{Vout\ (Vin - Vout)}{0.6 \times Vin \times Frequency} \quad [H]$$

2. Phase Compensation:

Resistors and a capacitor for phase compensation are connected between the CC pin and the Vref/SS pin. Recommended values of these are shown below but they are not fixed. These values can be changed according to the VIN and VOUT frequency settings to optimize the phase compensation.
(values shown below is in the case of "11. Recommended External Circuits")

R4＝220[kΩ], R5＝4.7[kΩ], C5=2200[pF]

3. Soft Start Time:

Soft-start time is determined by the C4 capacitor which is connected between the SS pin and the GND. The relation of the capacitance and the soft-start time is calculated by the following equation.

$$Tss = C4 / 20 \times 10^{-6} \quad [s]$$

4. Suspended Time in Hiccup Operation:

The suspended time in Hiccup operation is determined by the C4 capacitor which is connected between the SS pin and the GND. The relation of the capacitance and the suspended time is calculated by the following equation.

$$T_{HIC} = \frac{0.6 \times C4}{1 \times 10^{-6}} \quad [s]$$

5. Output Voltage:

The output voltage is determined by the feedback resistors, and those two resistors are placed in series between the output capacitor and the GND. Those resistor value of R2 (the output capacitor to FB pin) and R1 (FB pin to GND) are calculated by the following equation.

$$Vout = 0.6 \times \left(1 + \frac{R2}{R1} \right) \quad [V]$$

Please note that the operation may become unstable by an influence of the switching noise when the current which flows in the resistor becomes too small.

6. Oscillation Frequency:

The oscillation frequency is determined by the R3 resistor which is connected between the RT pin and the GND. The relation of the resistor value and the oscillation frequency is calculated by the following equation.

$$R3 = \frac{0.6 \times (1/Frequency - 33 \times 10^{-9})}{1.2 \times 2.35 \times 10^{-12}} \quad [\Omega]$$

7. Power Dissipation

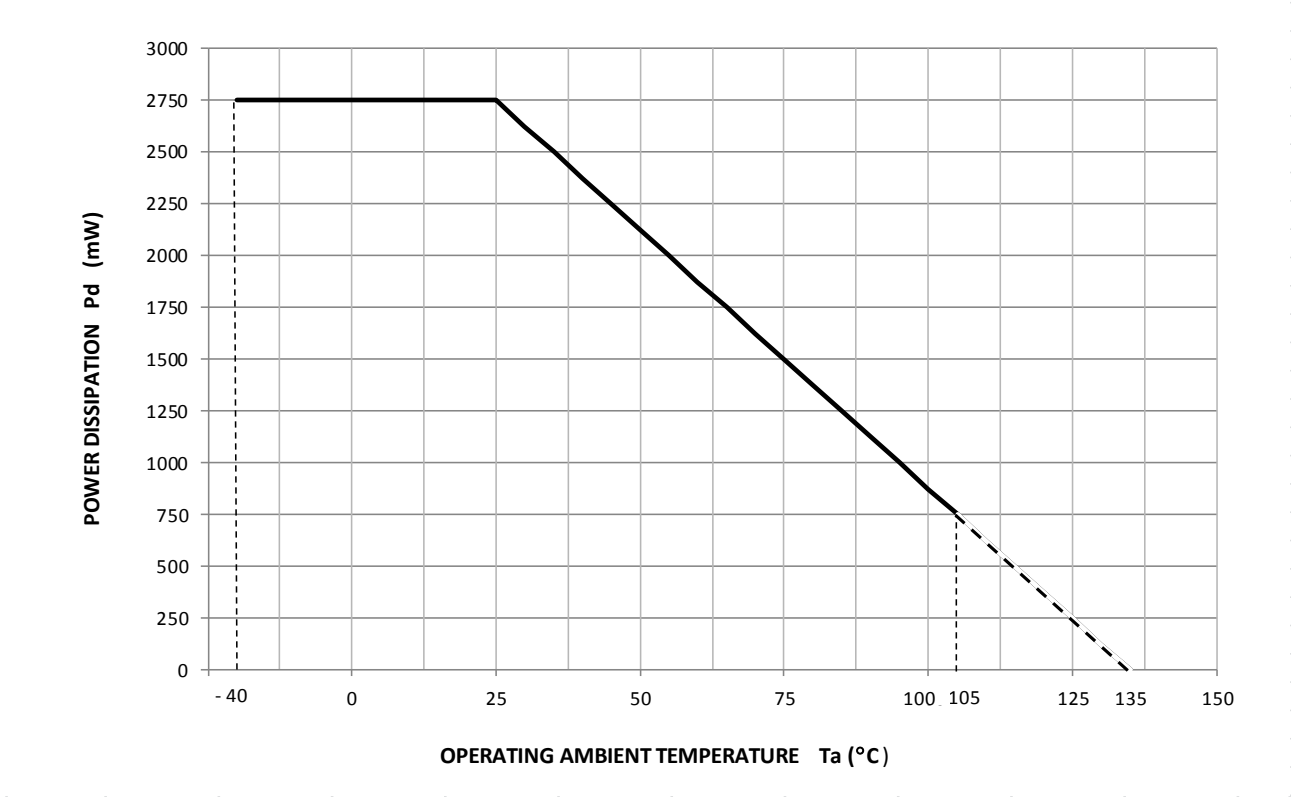


Figure 6. HTSSOP-16 DERATING CURVE

The derating curve of Package of HTSSOP-16 is above. The junction temperature (Tj) may become high temperature, even if the operating ambient temperature (Ta) is room temperature (25°C). This IC must be operated within the power dissipation.

11. Recommended External Circuits

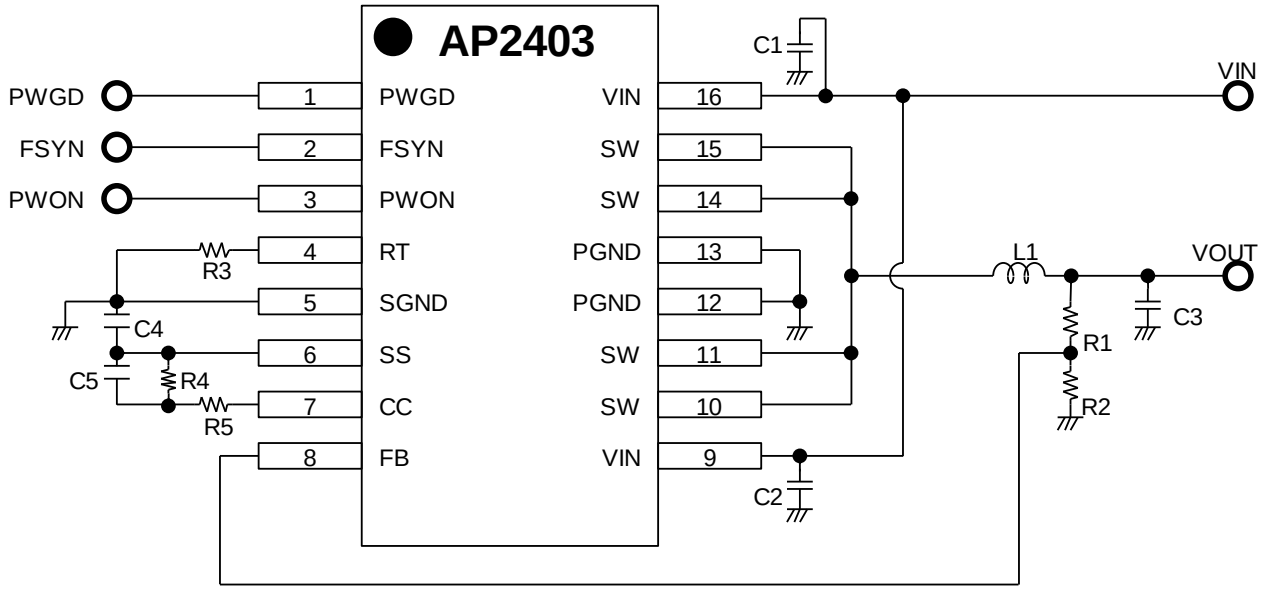


Figure 7. Standard Recommended Circuit Example

Parts List (VIN=5V, VOUT=1.8V, F=2MHz)

Symbol	Parts name	Parts value	Manufacturer
C1	Input capacitor	10μF Ceramic	
C2	Input capacitor	10μF Ceramic	
C3	Output capacitor	10μF Ceramic	
C4	SS capacitor	0.1μF Ceramic	
C5	Phase compensation capacitor	2200pF Ceramic	
R1	FB resistor (High)	150kΩ	
R2	FB resistor (Low)	100kΩ	
R3	Frequency set-up resistor	100kΩ	
R4	Phase compensation resistor	220kΩ	
R5	Phase compensation resistor	4.7kΩ	
L1	Power Inductor	2.7μH	TDK LTF5022-2R2N3R2-LC

12. PCB Layout Example

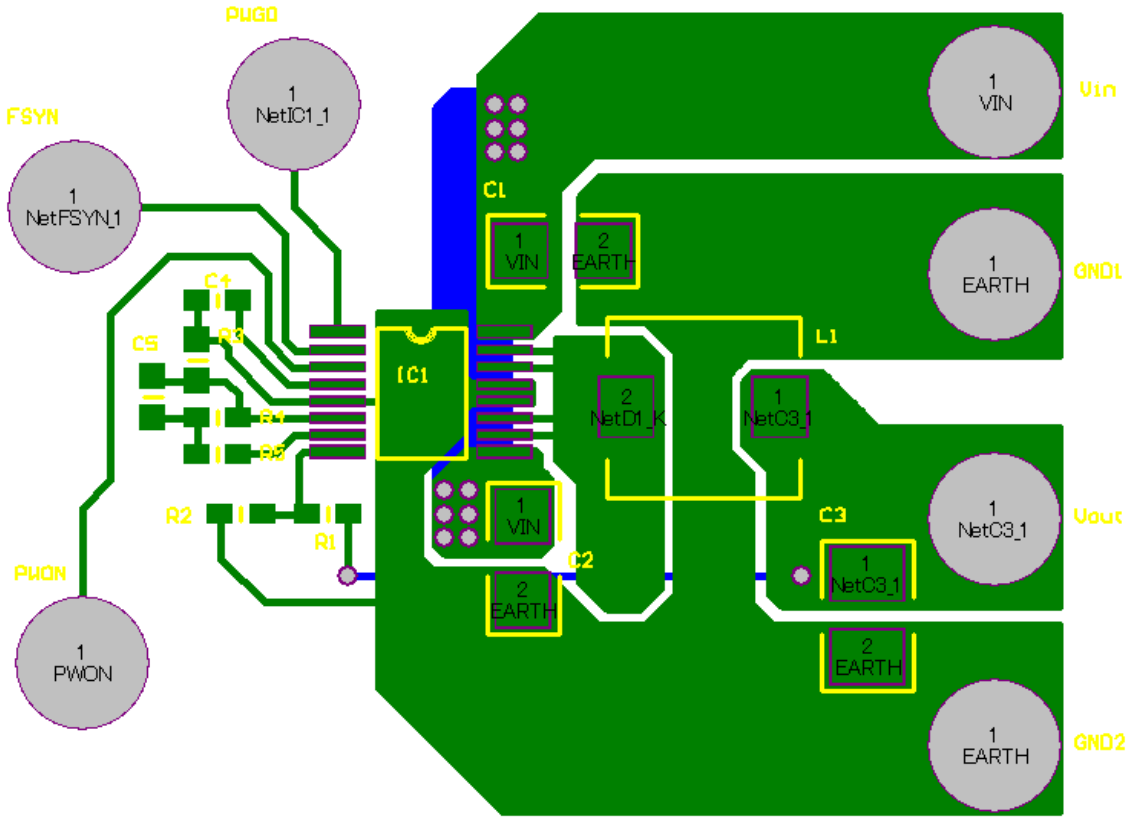
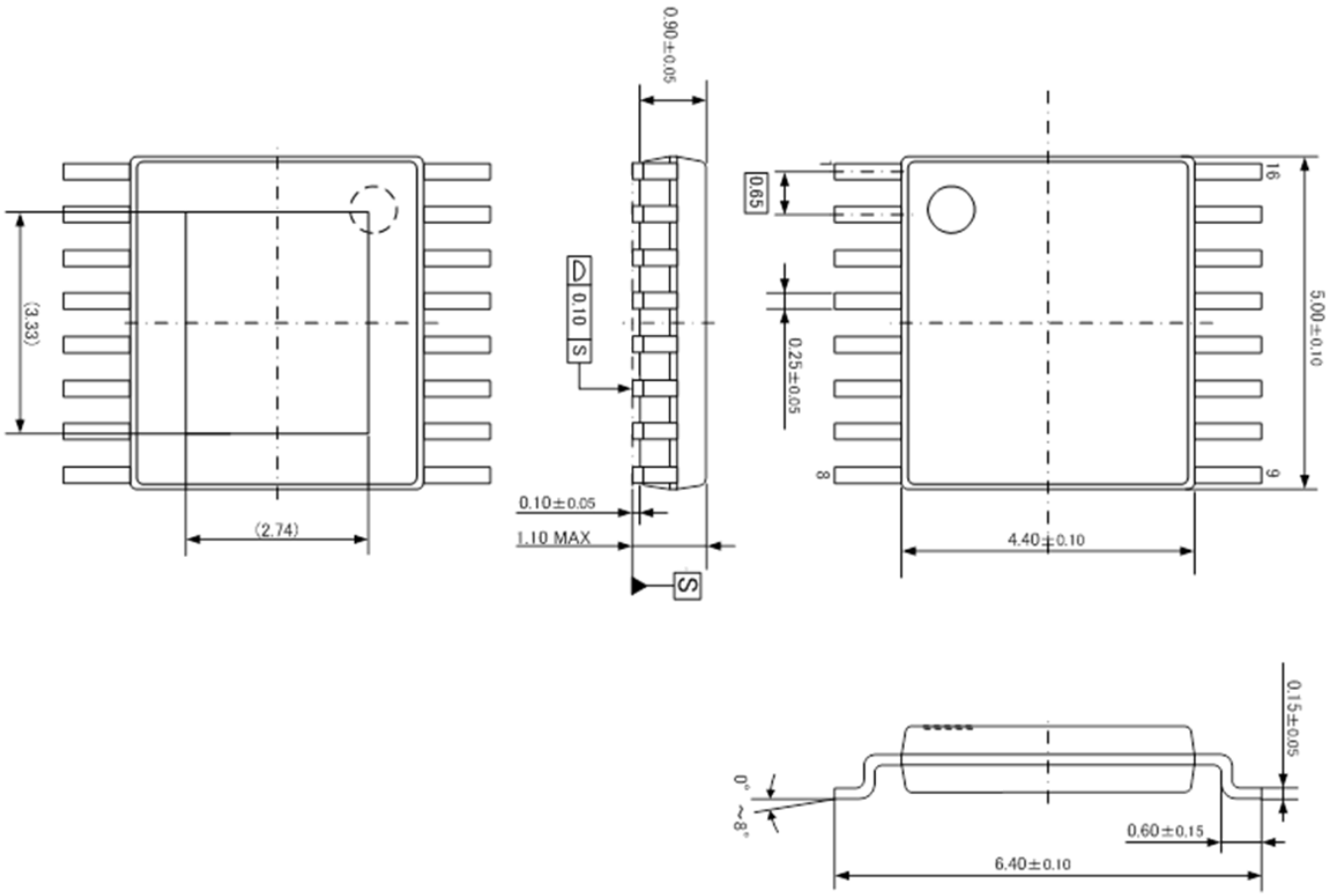


Figure 8. Recommended Layout Pattern

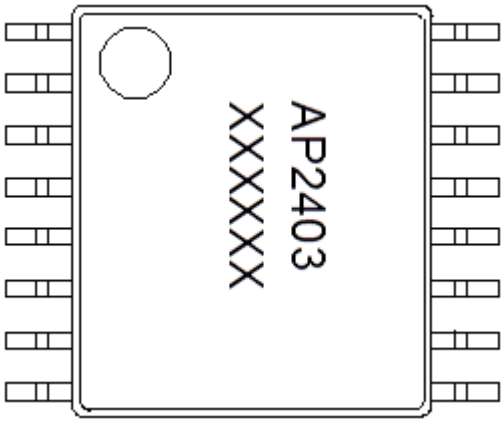
13. Package

■ Outline Dimensions

HTSSOP 16-pin (Unit: mm)



■ Marking



1) Pin #1 indication
2) Date Code : XXXXXX (6 digits: Date Code)
3) Marketing Code : AP2403

14. Revision History

Date (Y/M/D)	Revision	Page	Contents
13/04/23	00		First edition
13/07/02	01	4, 9, 12, 13	• The correction of the description of I/O in Pin Configuration and Functions • The correction of the type error in TIMING CHART AT OVER CURRENT PROTECTION (the shifting of the equations of T3 and T4) • Deletion of the diode of D1 in Figure 7 • Deletion of the symbol of D1 in Figure 8
14/01/24	02	14	• Addition of “Power Dissipation”

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