AS1324

DataSheet

1.5MHz, 600mA, DC/DC Step-Down Regulator

1 General Description

The AS1324 is a high-efficiency, constant-frequency synchronous buck converter available in adjustable- and fixed-voltage versions. The wide input voltage range (2.7 to 5.5V), automatic powersave mode and minimal external component requirements make the AS1324 perfect for any single Li-Ion battery-powered application.

Typical supply current with no load is 30µA and decreases to ≤1µA in shutdown mode.

The AS1324 is available as the standard versions listed in Table 1.

Table 1. Standard Versions

Model	Output Voltage
AS1324-AD	Adjustable via External Resistors
AS1324-12	Fixed: 1.2V
AS1324-15	Fixed: 1.5V
AS1324-18	Fixed: 1.8V

An internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode. The internally fixed switching frequency (1.5MHz) allows for the use of small surface mount external components.

Very low output voltages can be delivered with the internal 0.6V feedback reference voltage.

The AS1324 is available in a 5-pin TSOT-23 package.

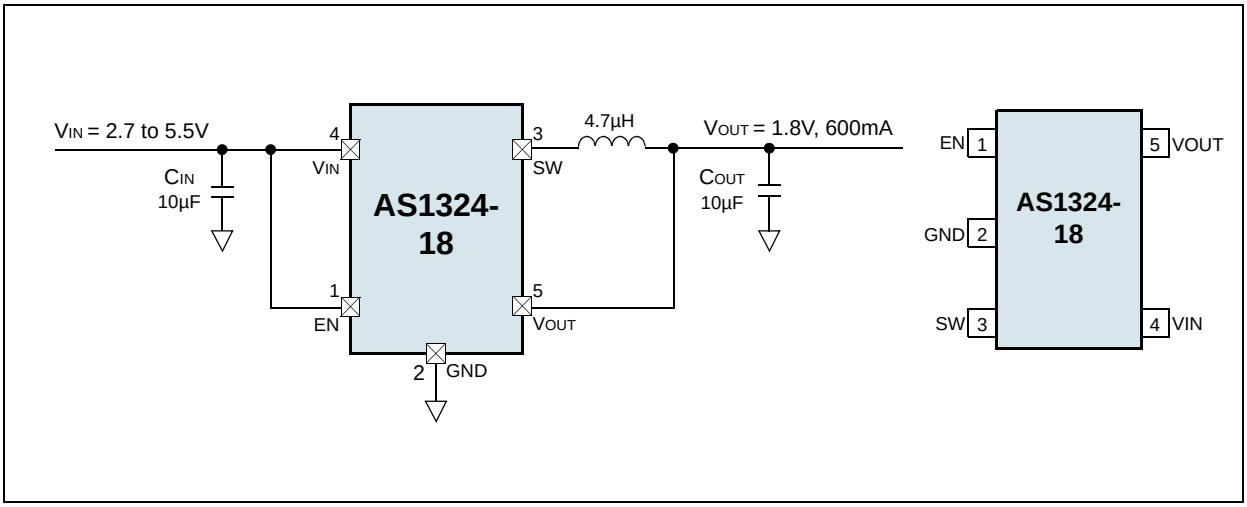
2 Key Features

- High Efficiency: Up to 96%
- Output Current: 600mA
- Input Voltage Range: 2.7 to 5.5V
- Constant Frequency Operation: 1.5MHz
- Variable- and Fixed-Output Voltages
- No Schottky Diode Required
- Automatic Powersave Operation
- Low Quiescent Current: 30µA
- Internal Reference: 0.6V
- Shutdown Mode Supply Current: ≤1µA
- Thermal Protection
- 5-pin TSOT-23 Package

3 Applications

The device is ideal for mobile communication devices, laptops and PDAs, ultra-low-power systems, threshold detectors/discriminators, telemetry and remote systems, medical instruments, or any other space-limited application with low power-consumption requirements.

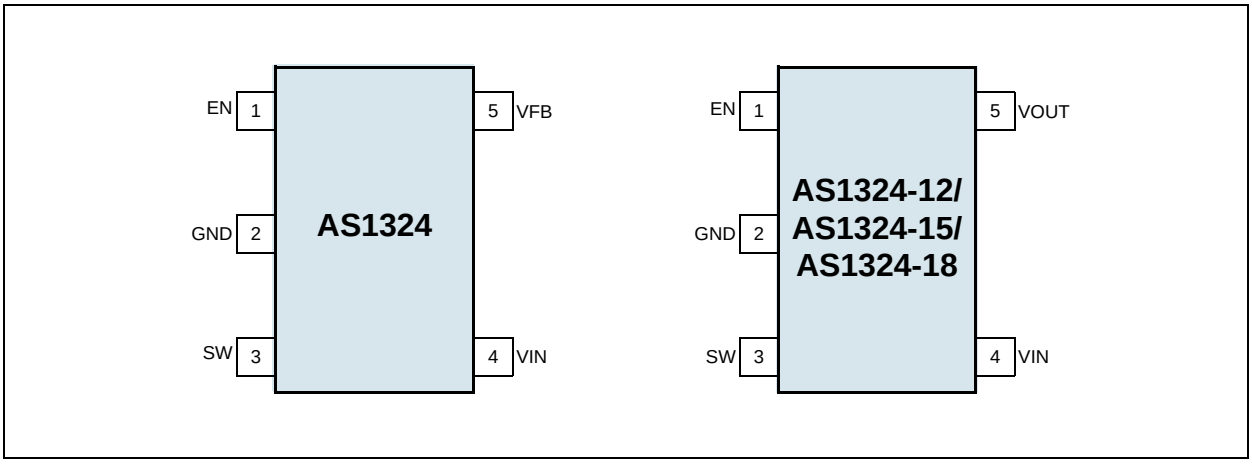
Figure 1. Typical Application Diagram – High Efficiency Step Down Converter



4 Pinout and Packaging

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 2. Pin Descriptions

Pin Number	Pin Name	Description
1	EN	**Enable Input**. Driving this pin above 1.5V enables the device. Driving this pin below 0.3V puts the device in shutdown mode. In shutdown mode all functions are disabled while SW goes high impedance, drawing <1µA supply current. **Note:** This pin should not be left floating.
2	GND	**Ground.**
3	SW	**Switch Node Connection to Inductor.** This pin connects to the drains of the internal main and synchronous power MOSFET switches.
4	VIN	**Input Supply Voltage**. This pin must be closely decoupled to GND with a ≥ 4.7µF ceramic capacitor. Connect to any supply voltage between 2.7 to 5.5V.
5	VFB	**Feedback Pin**. This pin receives the feedback voltage from the external resistor divider across the output. (Adjustable voltage variant only.)
	VOUT	**Output Voltage Feedback Pin**. An internal resistor divider steps the output voltage down for comparison to the internal reference voltage. (Fixed voltage variants only.)

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
V_{IN} to GND	-0.3	7	V	
SW, EN, FB to GND	-0.3	V_{IN} + 0.3	V	
Thermal Resistance Θ_{JA}		207.4	ºC/W	on PCB
ESD	2		kV	*HBM MIL-Std. 883E 3015.7* methods
Latch-Up	-100	+100	mA	*JEDEC 78*
Operating Temperature Range	-40	+85	ºC	
Storage Temperature Range	-65	+125	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Junction Temperature		125	ºC	Junction temperature (T_J) is calculated from the ambient temperature (T_{AMB}) and power dissipation (PD) as: $T_J = T_{AMB} + (PD)(207.4ºC/W)$ *(EQ 1)*

6 Electrical Characteristics

V_{IN} = EN = 3.6V, V_{OUT} < V_{IN} - 0.5V, T_{AMB} = -40 to +85°C, typ. values @ T_{AMB} = +25ºC (unless otherwise specified).

Table 4. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range		2.7		5.5	V
I_Q	Quiescent Current	Powersave Mode; V_{FB} = 0.62V or V_{OUT} = 103%, I_{OUT} = 0mA, T_{AMB} = +25ºC		30	35	µA
I_{SHDN}	Shutdown Current	Shutdown Mode; V_{EN} = 0V, T_{AMB} = +25ºC		0.1	1	
Regulation						
V_{FB}	Regulated Feedback Voltage [1]	AS1324, I_{OUT} = 100mA	0.585	0.6	0.615	V
ΔV_{FB}	Reference Voltage Line Regulation	V_{IN} = 2.7V to 5.5V		0.1	1	%/V
I_{VFB}	Feedback Current	T_{AMB} = +25ºC	-30		30	nA
V_{OUT}	Regulated Output Voltage	AS1324-AD, I_{OUT} = 100mA [2]	V_{FB}			V
		AS1324-12, I_{OUT} = 100mA	1.164	1.20	1.236	
		AS1324-15, I_{OUT} = 100mA	1.455	1.50	1.545	
		AS1324-18, I_{OUT} = 100mA	1.746	1.80	1.854	
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 2.7 to 5.5V		0.1	1	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	I_{OUT} = 0 to 100mA		0.02		%/mA
DC-DC Switches						
I_{PK}	Peak Inductor Current	V_{IN} = 3V, V_{FB} = 0.5V or V_{OUT} = 90%, T_{AMB} = 25ºC	0.5	0.75	1	A
R_{PFET}	P-Channel FET $R_{DS(ON)}$	I_{LSW} = 100mA		0.4		Ω
R_{NFET}	N-Channel FET $R_{DS(ON)}$	I_{LSW} = -100mA		0.35		Ω
I_{LSW}	SW Leakage	V_{EN} = 0V, V_{SW} = 0V or 5V		±0.01	±1	µA
Control Inputs						
V_{EN}	EN Threshold		0.3	1	1.5	V
I_{EN}	EN Leakage Current			±0.01	±1	µA
Oscillator						
f_{OSC}	Oscillator Frequency	V_{FB} = 0.6V or V_{OUT} = 100%	1.2	1.5	1.8	MHz
		V_{FB} = 0V or V_{OUT} = 0V, T_{AMB} = 25ºC		115		kHz

1. The device is tested in a proprietary test mode where V_{FB} is connected to the output of the error amplifier.
2. Please see Feedback Resistor Selection on page 13 for resistor values.

7 Typical Operating Characteristics

Parts used for measurement: 4.7µH (MOS6020-472) Inductor, 10µF (GRM188R60J106ME47) CIN and COUT.

Figure 3. Efficiency vs. Input Voltage; VOUT = 1.8V

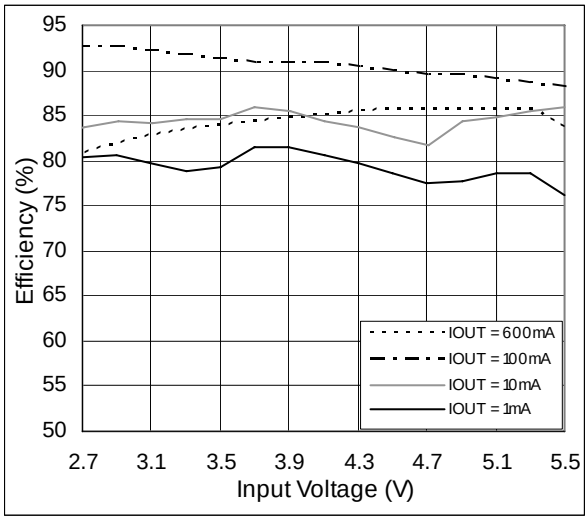


Figure 4. Efficiency vs. Output Current; VOUT = 1.2V

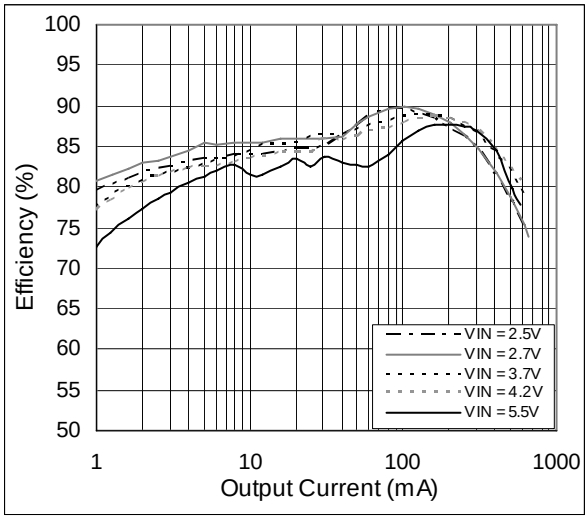


Figure 5. Efficiency vs. Output Current; VOUT = 1.5V

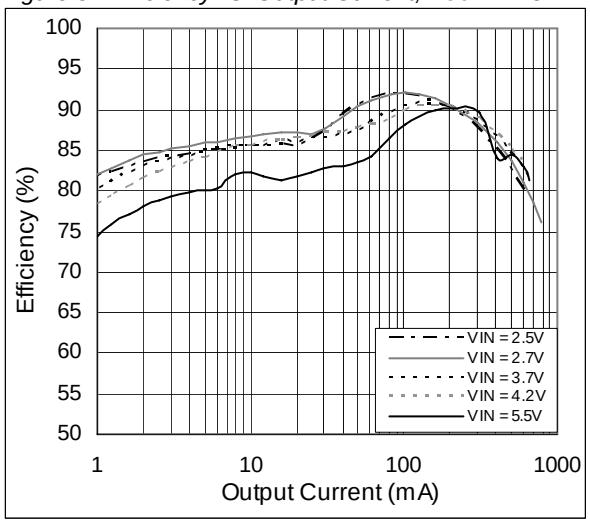


Figure 6. Efficiency vs. Output Current; VOUT = 1.8V

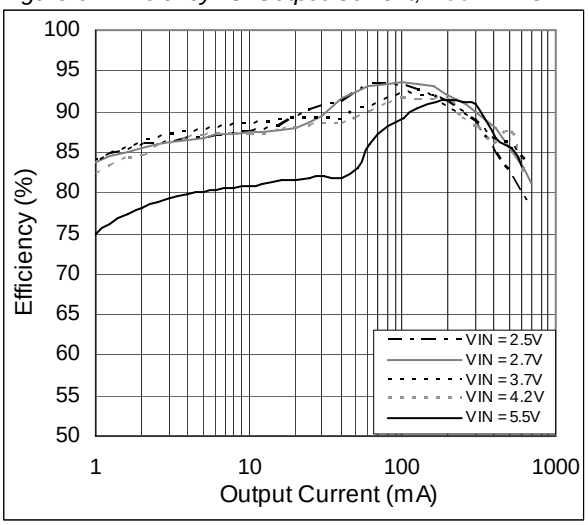


Figure 7. Efficiency vs. Output Current; VOUT = 2.5V

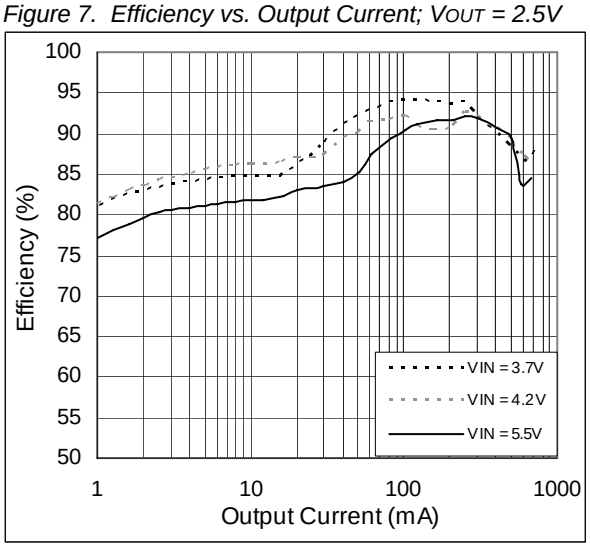


Figure 8. Efficiency vs. Output Current; VOUT = 3.3V

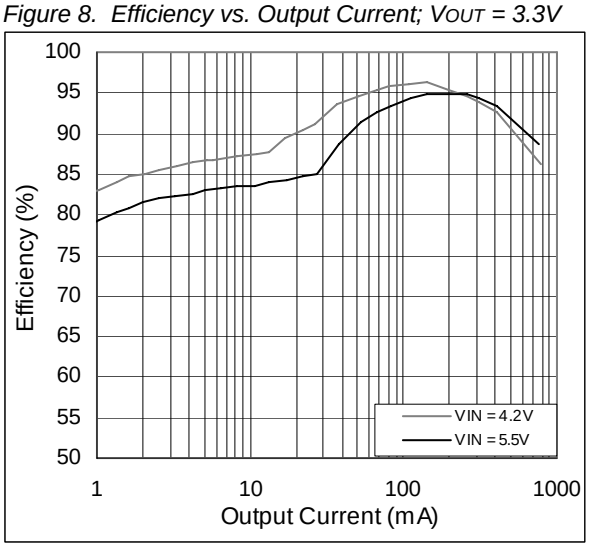


Figure 9. Switching Frequency vs. Supply Voltage

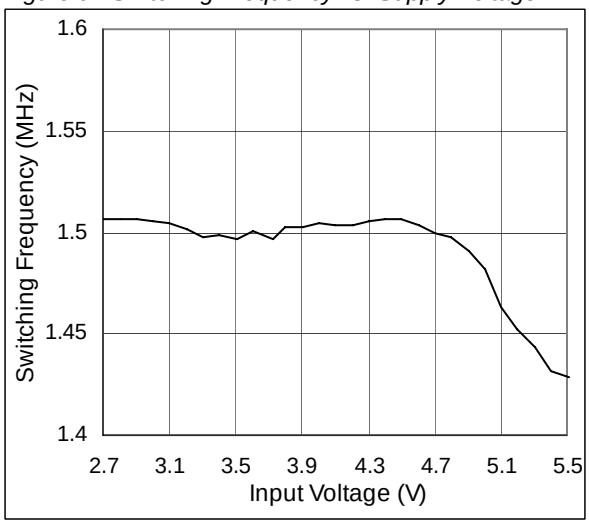


Figure 10. Switching Frequency vs. Temperature

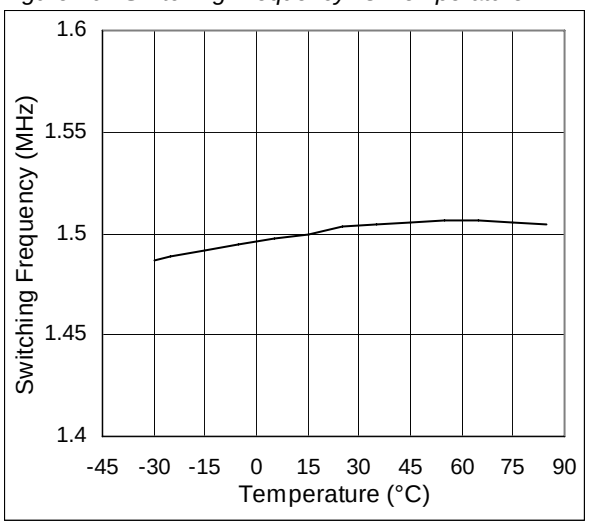


Figure 11. Feedback Voltage vs. Temperature

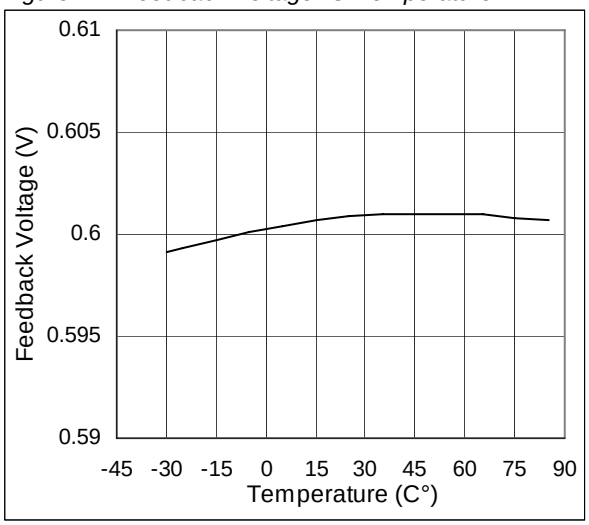


Figure 12. Output Voltage vs. Input Voltage

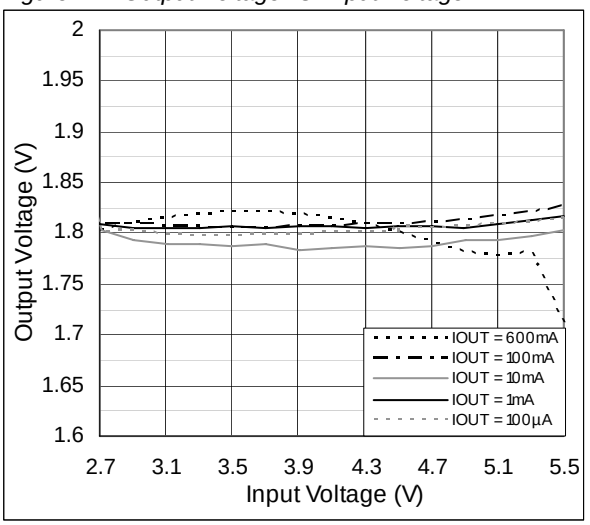


Figure 13. VOUT vs. IOUT; VOUTNOM = 1.2V

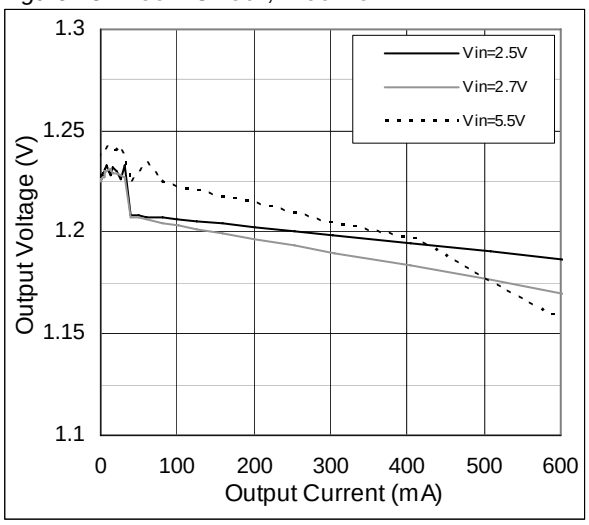


Figure 14. VOUT vs. IOUT; VOUTNOM = 1.5V

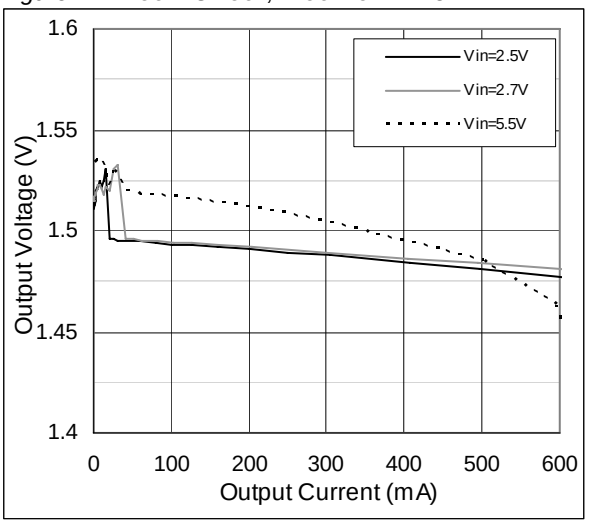


Figure 15. Quiescent Current vs. Input Voltage

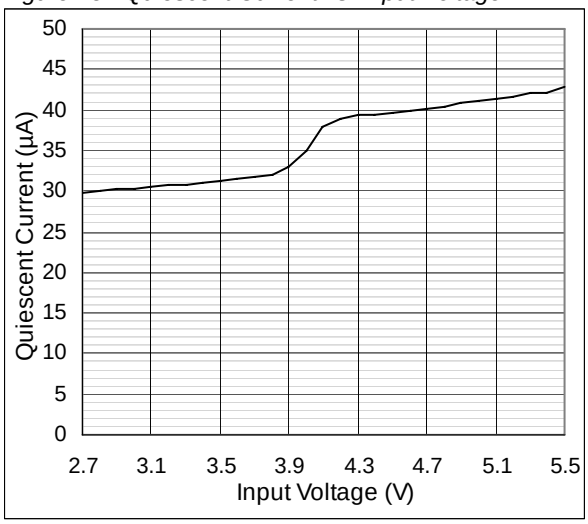


Figure 16. Quiescent Current vs. Temperature

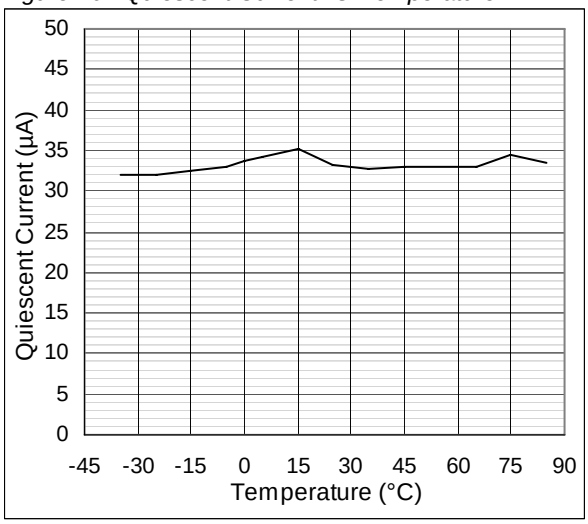


Figure 17. Load Step 0mA to 600mA

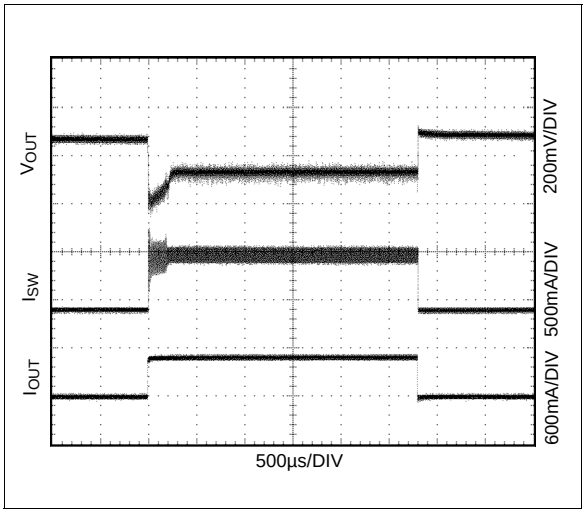


Figure 18. Load Step 10mA to 200mA

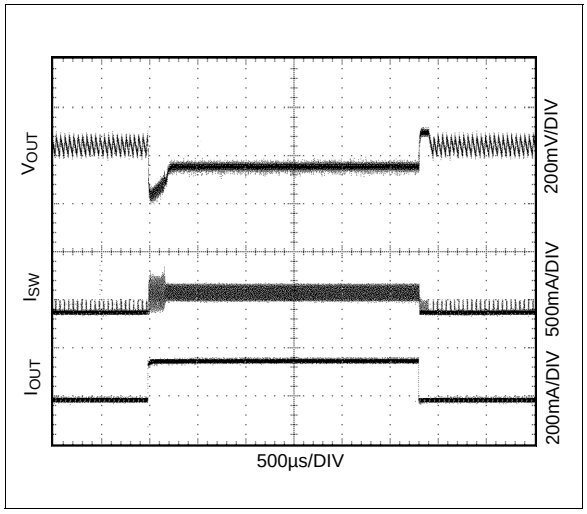


Figure 19. Startup

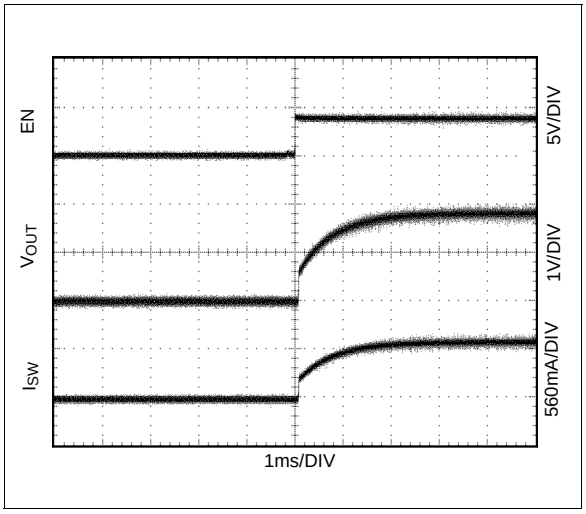
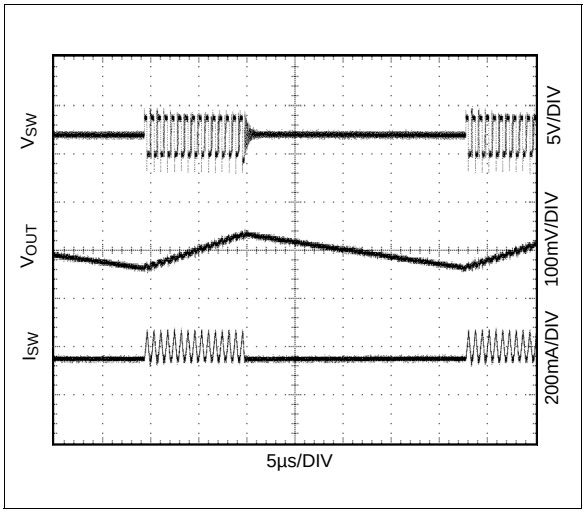


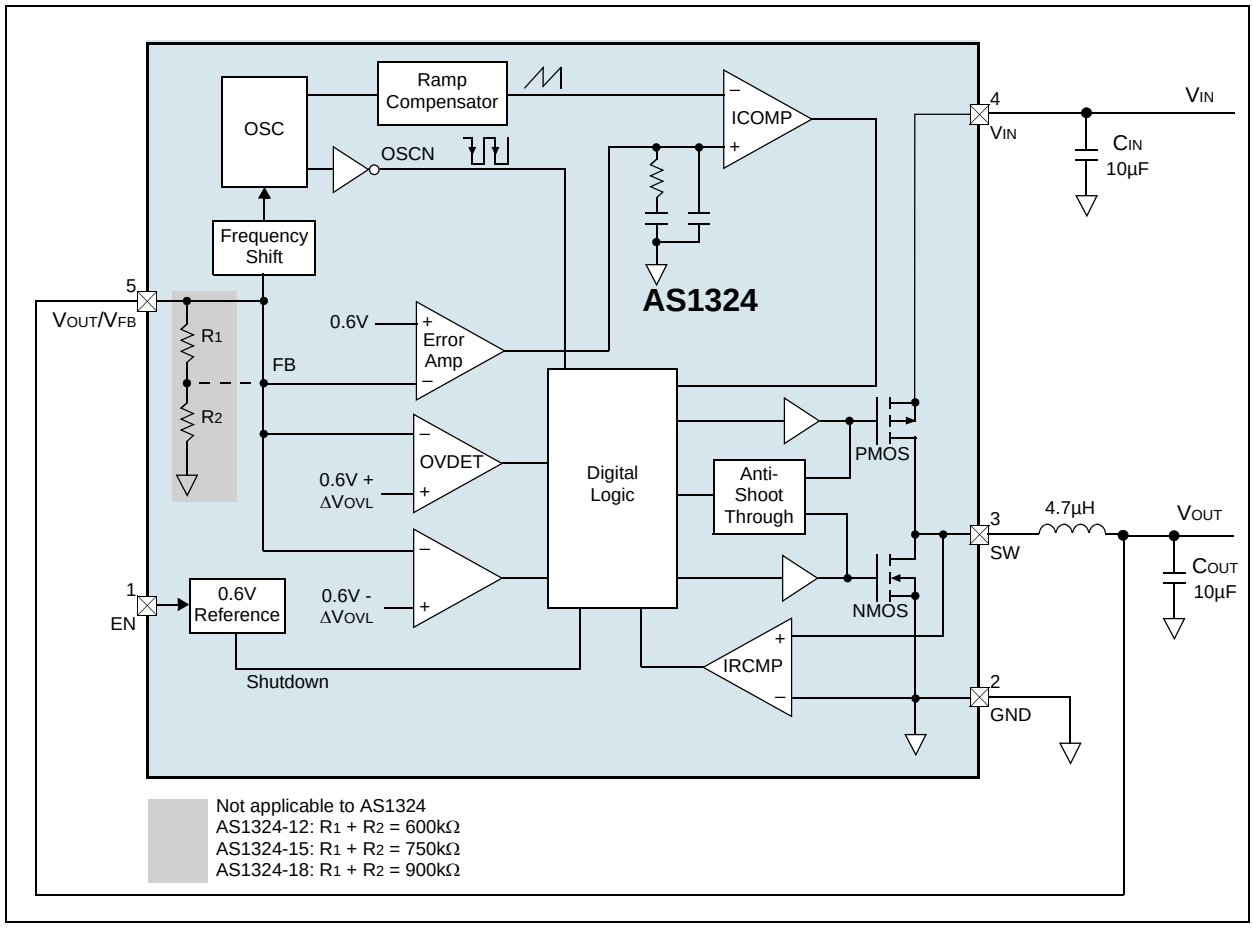
Figure 20. Powersave Mode



8 Detailed Description

The AS1324 is a high-efficiency buck converter that uses a constant-frequency current-mode architecture. The device contains two internal MOSFET switches and is available in adjustable- and fixed-output voltage versions.

Figure 21. Block Diagram



Main Control Loop

During PWM operation the converters use a 1.5MHz fixed-frequency, current-mode control scheme. Basis of the current-mode PWM controller is an open-loop, multiple input comparator that compares the error-amp voltage feedback signal against the sum of the amplified current-sense signal and the slope-compensation ramp. At the beginning of each clock cycle, the internal high-side PMOS turns on until the PWM comparator trips. During this time the current in the inductor ramps up, sourcing current to the output and storing energy in the inductor's magnetic field. When the PMOS turns off, the internal low-side NMOS turns on. Now the inductor releases the stored energy while the current ramps down, still providing current to the output. The output capacitor stores charge when the inductor current exceeds the load and discharges when the inductor current is lower than the load. Under overload conditions, when the inductor current exceeds the current limit, the high-side PMOS is turned off and the low-side NMOS remains on until the next clock cycle.

When the PMOS is off, the NMOS is turned on until the inductor current starts to reverse (as indicated by the current reversal comparator (IRCMP)), or the next clock cycle begins. The IRCMP detects the zero crossing.

The peak inductor current (I_{PK}) is controlled by the error amplifier. When I_{OUT} increases, V_{FB} decreases slightly relative to the internal 0.6V reference, causing the error amplifier's output voltage to increase until the average inductor current matches the new load current.

The over-voltage detection comparator (OVDET) guards against transient overshoots by turning the main switch off and keeping it off until the transient is removed.

Powersave Operation

The AS1324 uses an automatic powersave mode where the peak inductor current (I_{PK}) is set to approximately 200mA while independent of the output load. In powersave mode, load current is supplied solely from the output capacitor. As the output voltage drops, the error amplifier output rises above the powersave threshold signaling to switch into PWM fixed frequency mode and turn the PMOS on. This process repeats at a rate determined by the load demand.

Each burst event can last from a few cycles at light loads to almost continuous cycling (with short sleep intervals) at moderate loads. In between bursts, the power MOSFETs are turned off, as is any unneeded circuitry, reducing quiescent current to 30µA.

Short-Circuit Protection

In cases where the AS1324 output is shorted to ground, the oscillator frequency (f_{OSC}) is reduced to 1/13 the nominal frequency ($\simeq$115kHz). This frequency reduction ensures that the inductor current has more time to decay, thus preventing runaway conditions. f_{OSC} will progressively increase to 1.5MHz when V_{FB}/V_{OUT} > 0V.

Shutdown

Connecting EN to GND or logic low places the AS1324 in shutdown mode and reduces the supply current to 0.1µA. In shutdown the control circuitry and the internal NMOS and PMOS turn off and SW becomes high impedance disconnecting the input from the output. The output capacitance and load current determine the voltage decay rate. For normal operation connect EN to V_{IN} or logic high.

Note: Pin EN should not be left floating.

9 Application Information

The AS1324 is perfect for mobile communications equipment like cell phones and smart phones, digital cameras and camcorders, portabel MP3 and DVD players, PDA's and palmtop computers and any other handheld instruments.

Figure 22. Single Li-Ion 1.2V/600mA Regulator for High-Efficiency

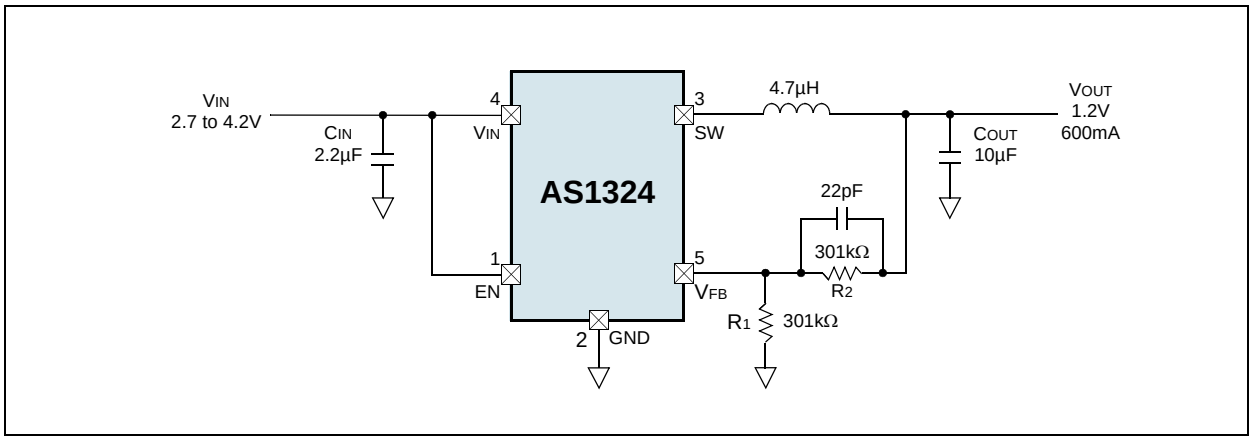


Figure 23. 5V Input to 3.3V/600mA Buck Regulator

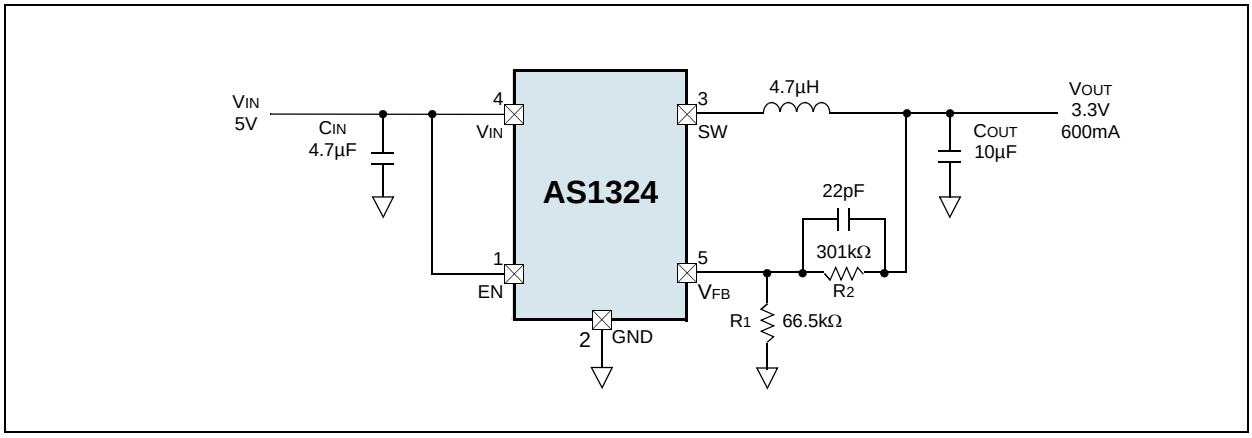


Figure 24. Single Li-Ion 1.5V/600mA Regulator for High-Efficiency

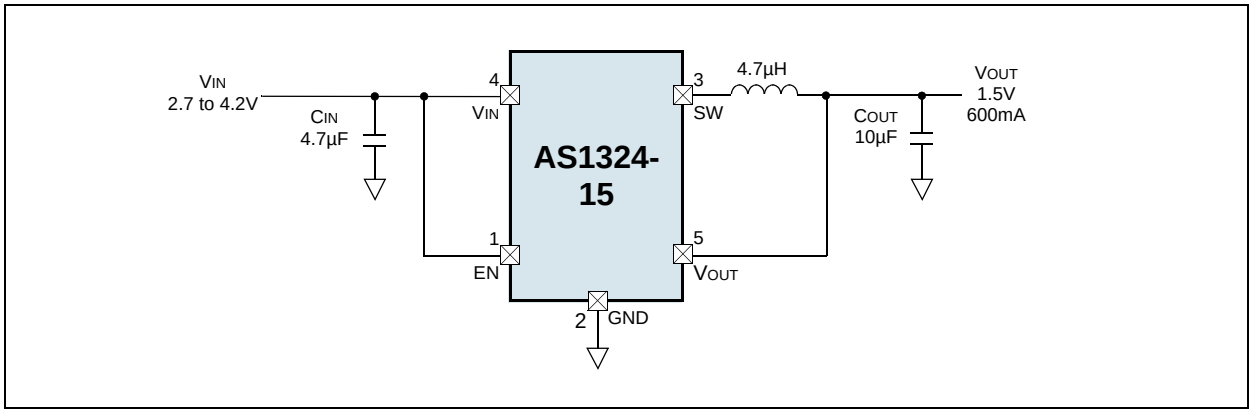
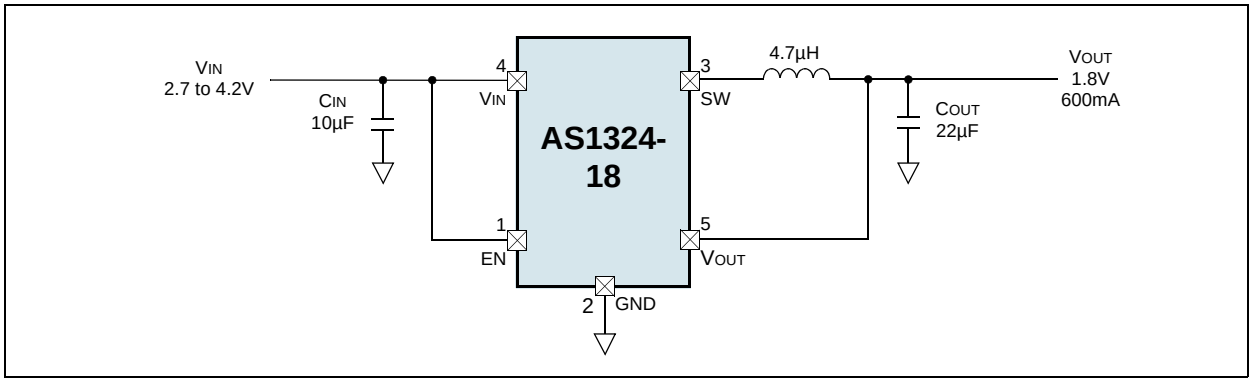


Figure 25. Single Li-Ion 1.8V/600mA Regulator for Low Output Ripple



External Component Selection

Inductor Selection

For most applications the value of the external inductor should be in the range of 2.2 to 6.8µH as the inductor value has a direct effect on the ripple current. The selected inductor must be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

In Equation (EQ 2) the maximum inductor current in PWM mode under static load conditions is calculated. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation (EQ 3). This is recommended because the inductor current will rise above the calculated value during heavy load transients.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \quad \textit{(EQ 2)}$$

$$I_{LMAX} = I_{OUTMAX} + \frac{\Delta I_L}{2} \quad \textit{(EQ 3)}$$

Where:
f = Switching Frequency (1.5 MHz typical)
L = Inductor Value
I_{Lmax} = Maximum Inductor current
ΔI_L = Peak to Peak inductor ripple current
The recommended starting point for setting ripple current is ΔI_L = 240mA (40% of 600mA).

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 720mA rated inductor should be sufficient for most applications (600mA + 120mA). A easy and fast approach is to select the inductor current rating fitting to the maximum switch current limit of the converter.

Note: For highest efficiency, a low DC-resistance inductor is recommended.

Accepting larger values of ripple current allows the use of low inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability.

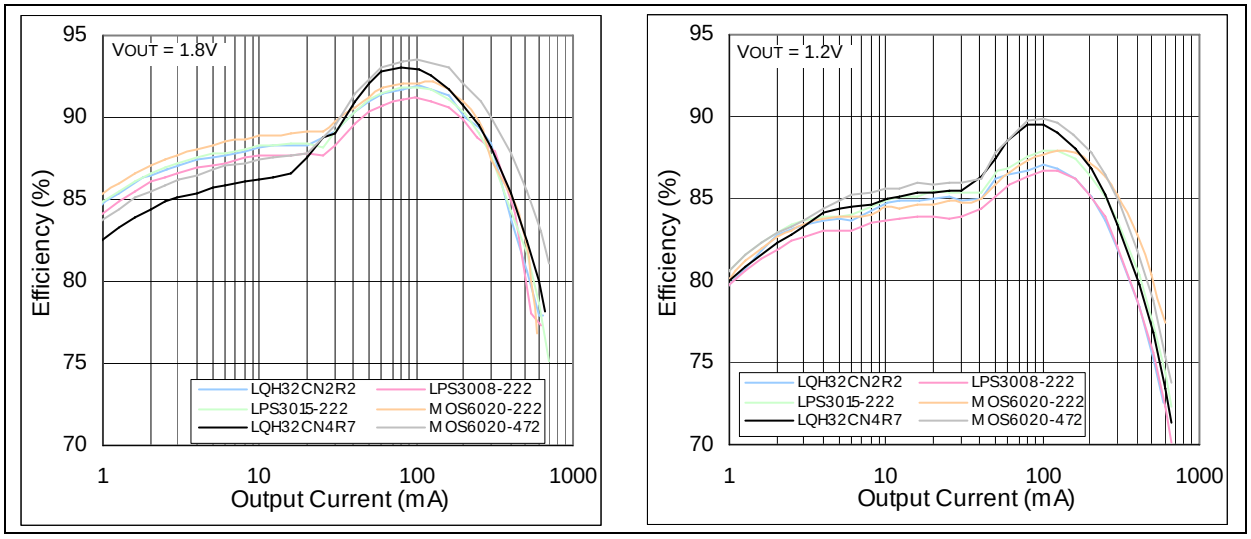
The total losses of the coil have a strong impact on the efficiency of the dc/dc conversion and consist of both the losses in the dc resistance and the following frequency-dependent components:

1. The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
2. Additional losses in the conductor from the skin effect (current displacement at high frequencies)
3. Magnetic field losses of the neighboring windings (proximity effect)
4. Radiation losses

Table 5. Recommended Inductors

Part Number	L	DCR	Current Rating	Dimensions (L/W/T)	Manufacturer
LQH32CN2R2M33	2.2µH	97mΩ	790mA	3.2x2.5x2.0mm	Murata www.murata.com
LQH32CN4R7M33	4.7µH	150mΩ	650mA	3.2x2.5x2.0mm	
LPS3008-222MLC	2.2µH	175mΩ	1100mA	3.1x3.1x0.8mm	Coilcraft www.coilcraft.com
LPS3015-222MLC	2.2µH	110mΩ	2000mA	3.1x3.1x1.5mm	
MOS6020-222MLC	2.2µH	35mΩ	3260mA	6.0x6.8x2.4mm	
MOS6020-472MLC	4.7µH	50mΩ	1820mA	6.0x6.8x2.4mm	
CDRH3D16NP-2R2N	2.2µH	72mΩ	1200mA	4.0x4.0x1.8mm	Sumida www.sumida.com
CDRH3D16ND-4R7N	4.7µH	105mΩ	900mA	4.0x4.0x1.8mm	

Figure 26. Efficiency Comparison of Different Inductors, V_{IN} = 2.7V, V_{OUT} = 1.8V and 1.2V



Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the AS1324 allows the use of tiny ceramic capacitors. Because of their lowest output voltage ripple low ESR ceramic capacitors are recommended. X7R or X5R dielectric output capacitor are recommended.

At high load currents, the device operates in PWM mode and the RMS ripple current is calculated as:

$$I_{RMSC_{OUT}} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad \textit{(EQ 4)}$$

While operating in PWM mode the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \quad \textit{(EQ 5)}$$

Higher value, low cost ceramic capacitors are available in very small case sizes, and their high ripple current, high voltage rating, and low ESR make them ideal for switching regulator applications. Because the AS1324 control loop is not dependant on the output capacitor ESR for stable operation, ceramic capacitors can be used to achieve very low output ripple and accommodate small circuit size.

At light loads, the converter operates in powersave mode and the output voltage ripple is in direct relation to the output capacitor and inductor value used. Larger output capacitor and inductor values minimize the voltage ripple in powersave mode and tighten DC output accuracy in powersave mode.

Input Capacitor Selection

In continuous mode, the source current of thePMOS is a square wave of the duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients while minimizing the interference with other circuits caused by high input voltage spikes, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given as:

$$I_{RMS} = I_{MAX} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \quad \textit{(EQ 6)}$$

where the maximum average output current I_{MAX} equals the peak current minus half the peak-to-peak ripple current, $I_{MAX} = I_{LIM} - \Delta I_L/2$

This formula has a maximum at $V_{IN} = 2V_{OUT}$ where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations only provide negligible affects.

The input capacitor can be increased without any limit for better input voltage filtering. Take care when using small ceramic input capacitors. When a small ceramic capacitor is used at the input, and the power is being supplied through long wires, such as from a wall adapter, a load step at the output, or V_{IN} step on the input, can induce ringing at the VIN pin. This ringing can then couple to the output and be mistaken as loop instability, or could even damage the part by exceeding the maximum ratings.

Ceramic Input and Output Capacitors

When choosing ceramic capacitors for C_{IN} and C_{OUT}, the X5R or X7R dielectric formulations are recommended. These dielectrics have the best temperature and voltage characteristics for a given value and size. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies and therefore should not be used.

Table 6. Recommended Input and Output Capacitor

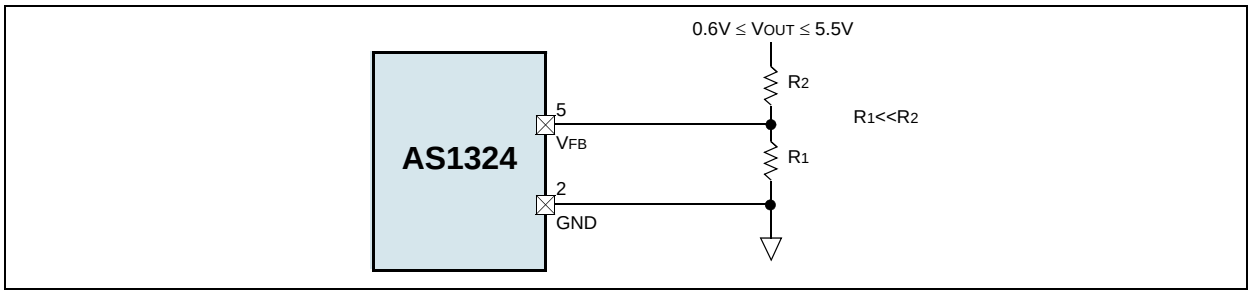
Part Number	C	TC Code	Rated Voltage	Dimensions (L/W/T)	Manufacturer
JMK212BJ226MG-T	22µF	X5R	6.3V	0805	Taiyo Yuden www.t-yuden.com
GRM188R60J106ME47	10µF	X5R	6.3V	0603	Murata www.murata.com
GRM21BR71A475KA73	4.7µF	X7R	10V	0805	

Because ceramic capacitors lose a lot of their initial capacitance at their maximum rated voltage, it is recommended that either a higher input capacity or a capacitance with a higher rated voltage is used.

Feedback Resistor Selection

In the AS1324-AD, the output voltage is set by an external resistor divider connected to V_{FB} (see Figure 27). This circuitry allows for remote voltage sensing and adjustment.

Figure 27. Setting the AS1324 Output Voltage



Resistor values for the circuit shown in Figure 27 can be calculated as:

$$V_{OUT} = 0,6 \times \left[1 + \frac{R_2}{R_1}\right] \quad \textit{(EQ 7)}$$

The output voltage can be adjusted by selecting different values for R_1 and R_2. For R_1 a value between 10kΩ and 500kΩ is recommended. A higher resistance of R_1 and R_2 will result in a lower leakage current at the output. It is recommended to keep V_{IN} 500mV higher than V_{OUT}.

Efficiency

The efficiency of a switching regulator is equivalent to:

$$Efficiency = (P_{OUT}/P_{IN})100\% \quad \textit{(EQ 8)}$$

For optimum design, an analysis of the AS1324 is needed to determine efficiency limitations and to determine design changes for improved efficiency. Efficiency can be expressed as:

$$Efficiency = 100\% - (L_1 + L_2 + L_3 + ...) \quad \textit{(EQ 9)}$$

Where:

L_1, L_2, L_3, etc. are the individual losses as a percentage of input power.

Althought all dissipative elements in the circuit produce losses, those four main sources should be considered for efficiency calculation:

Input Voltage Quiescent Current Losses

The V_{IN} current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small (<0.1%) loss that increases with V_{IN}, even at no load. The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents.

I²R Losses

Most of the efficiency loss at medium to high load currents are attributed to I²R loss, and are calculated from the resistances of the internal switches (R_{SW}) and the external inductor (R_L). In continuous mode, the average output current flowing through inductor L is split between the internal switches. Therefore, the series resistance looking into the SW pin is a function of both NMOS & PMOS $R_{DS(ON)}$ as well as the the duty cycle (DC) and can be calculated as follows:

$$R_{SW} = (R_{DS(ON)PMOS})(DC) + (R_{DS(ON)NMOS})(1 - DC) \quad \textit{(EQ 10)}$$

The $R_{DS(ON)}$ for both MOSFETs can be obtained from the Electrical Characteristics on page 4. Thus, to obtain I²R losses calculate as follows:

$$I^2R\ losses = I_{OUT}^2(R_{SW} + R_L) \quad \textit{(EQ 11)}$$

Switching Losses

The switching current is the sum of the control currents and the MOSFET driver. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. If a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the DC bias current. In continuous mode:

$$I_{GC} = f(Q_{PMOS} + Q_{NMOS}) \quad \text{(EQ 12)}$$

Where: Q_{PMOS} and Q_{NMOS} are the gate charges of the internal MOSFET switches.

The losses of the gate charges are proportional to V_{IN} and thus their effects will be more visible at higher supply voltages.

Other Losses

Basic losses in the design of a system should also be considered. Internal battery resistances and copper trace can account for additional efficiency degradations in battery operated systems. By making sure that CIN has adequate charge storage and very low ESR at the given switching frequency, the internal battery and fuse resistance losses can be minimized. CIN and COUT ESR dissipative losses and inductor core losses generally account for less than 2% total additional loss.

Thermal Shutdown

Due to its high-efficiency design, the AS1324 will not dissipate much heat in most applications. However, in applications where the AS1324 is running at high ambient temperature, uses a low supply voltage, and runs with high duty cycles (such as in dropout) the heat dissipated may exceed the maximum junction temperature of the device.

As soon as the junction temperature reaches approximately 150ºC the AS1324 goes in thermal shutdown. In this mode the internal PMOS & NMOS switch are turned off. The device will power up again, as soon as the temperature falls below +145°C again.

Checking Transient Response

The main loop response can be evaluated by examining the load transient response. Switching regulators normally take several cycles to respond to a step in load current. When a load step occurs, VOUT immediately shifts by an amount equivalent to:

$$V_{DROP} = \Delta I_{OUT} \times ESR \qquad \text{(EQ 13)}$$

Where:

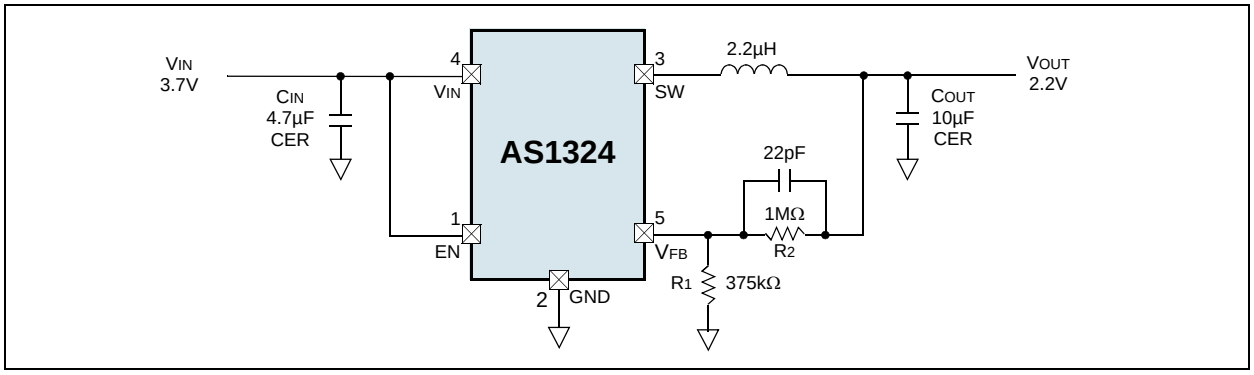
ESR is the effective series resistance of COUT.

ΔIOUT also begins to charge or discharge COUT, which generates a feedback error signal. The regulator loop then acts to return VOUT to its steady-state value. During this recovery time VOUT can be monitored for overshoot or ringing that would indicate a stability problem.

Design Example

Figure 28 shows the AS1324 used in a single lithium-ion (3.7V typ) battery-powered mobile phone application. The load current requirement is 600mA (max) but most of the time the device will require only 2mA (standby mode current).

Figure 28. Design Example



For the circuit shown in Figure 28, efficiency at low- and high-load currents is an important consideration when selecting the value for the external inductor, which is calculated as:

$$L = \frac{V_{OUT}}{f\Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad \text{(EQ 14)}$$

From (EQ 14), substituting VOUT = 2.2V, VIN = 3.7V, ΔI_L = 240mA and f = 1.5MHz gives:

$$L = \frac{2{,}2V}{(1{,}5MHz \times 240mA)} \times \left(1 - \frac{2{,}2V}{3{,}7V}\right) = 2{,}48\mu H \qquad \text{(EQ 15)}$$

Therefore, a standard 2.2µH inductor should be used for this design.

For best overall efficiency use an inductor with a rating of 720mA or greater and less than 0.2Ω series resistance. C_{IN} will require an RMS current rating of at least 0.3A ≅ $I_{LOAD(MAX)}$/2, whereas C_{OUT} will require an ESR of less than 0.25Ω. In most cases, a ceramic capacitor will satisfy this requirement.

For the feedback resistors, select the value for R_1 = 375kΩ. R_2 can then be calculated from (EQ 7) to be:

$$R_2 = (V_{OUT}/0.6 - 1)375k = 1000k\Omega$$

Layout Considerations

The AS1324 requires proper layout and design techniques for optimum performance.

- The power traces (GND, SW, and V_{IN}) should be kept as short, direct, and wide as is practical.
- Pin V_{FB} (AS1324 only) should be connected directly to the feedback resistors (R_1 and R_2). A potentiometer as replacement for R_1 and R_2 should be avoided to minimize the output voltage ripple and to maintain the stability of the regulator.
- The resistive divider (R_1/R_2) must be connected between the positive plate of C_{OUT} and ground.
- The positive plate of C_{IN} should be connected as close to V_{IN} as is practical since C_{IN} provides the AC current to the internal power MOSFETs.
- Switching node SW should be kept far away from the sensitive V_{FB} node.
- The negative plates of C_{IN} and C_{OUT} should be kept as close to each other as is practical. A starpoint to Ground is recommended.

Figure 29. AS1324 Basic PCB Layout

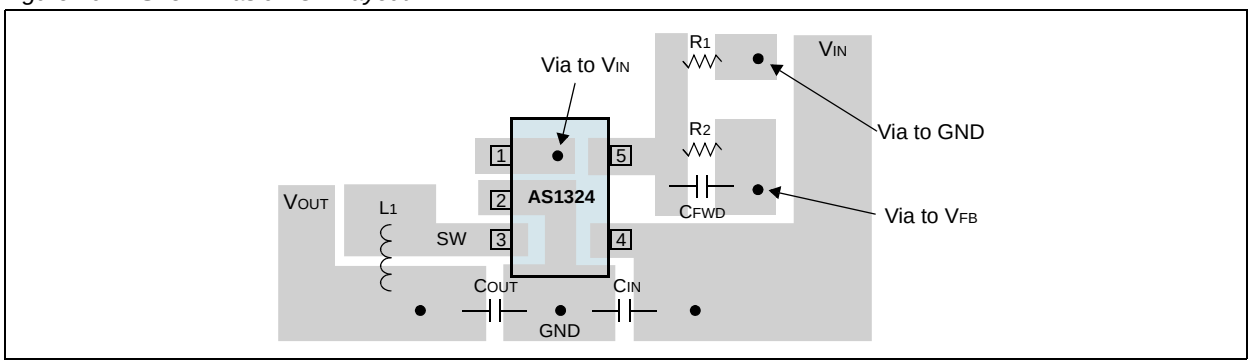


Figure 30. AS1324 Basic Diagram

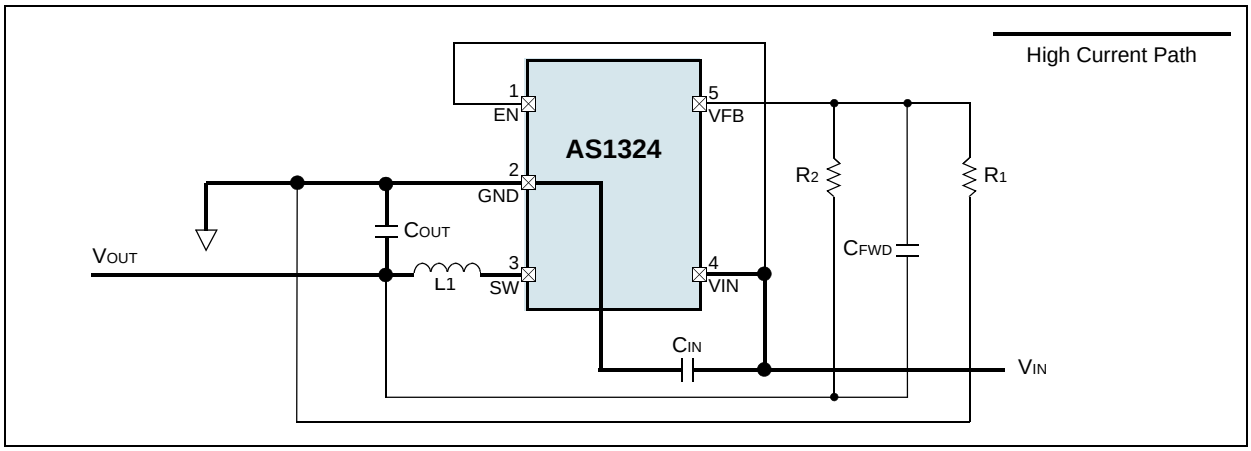


Figure 31. AS1324-18 Basic PCB Layout

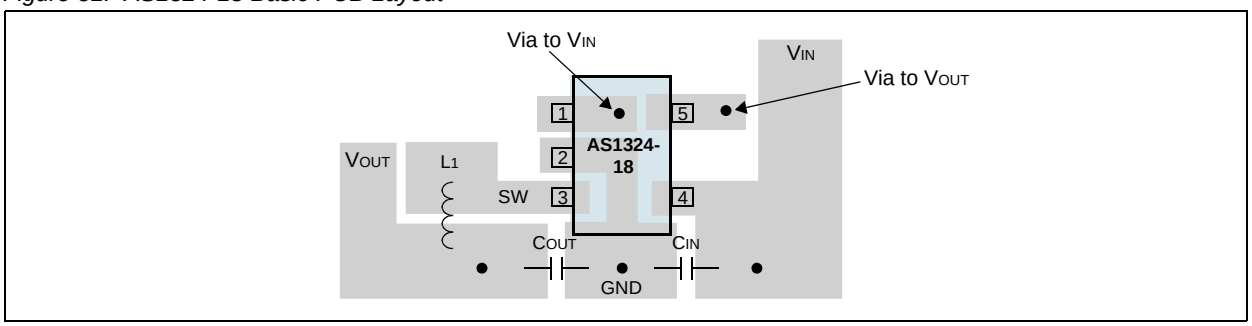
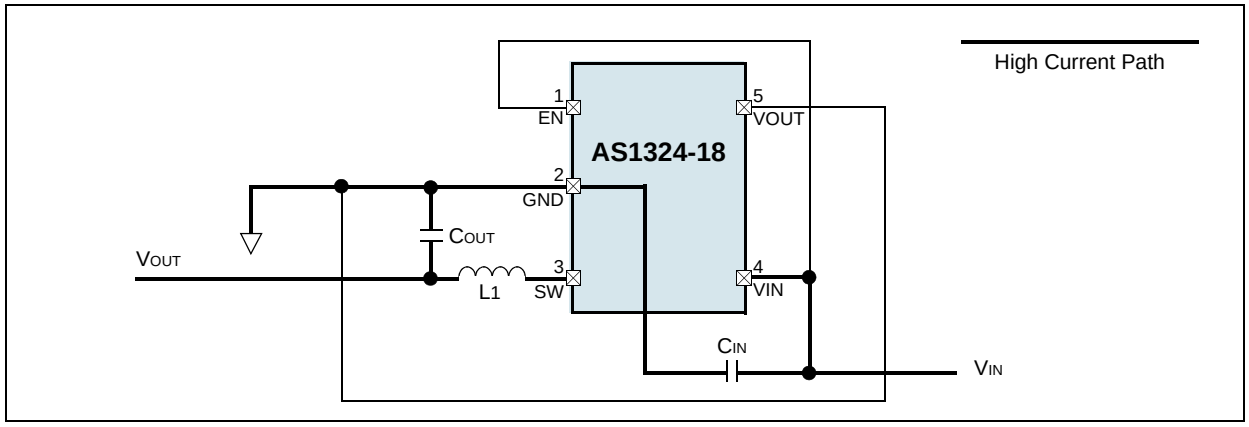


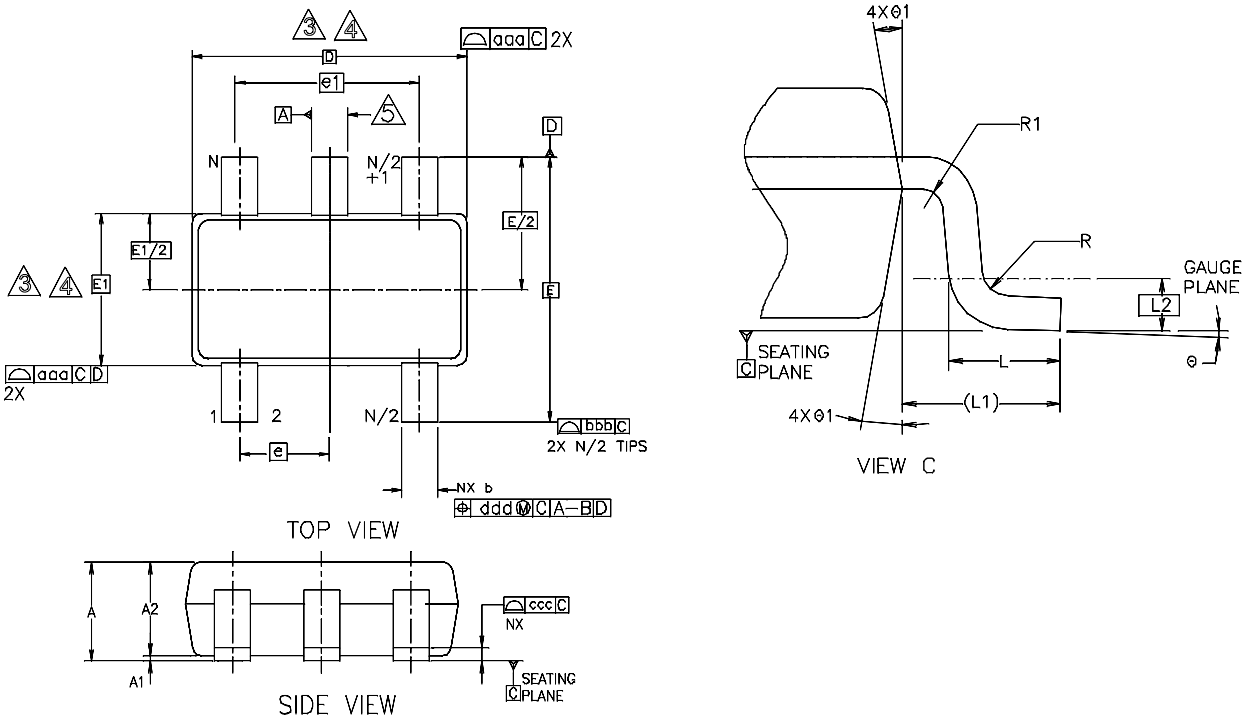
Figure 32. AS1324-18 Basic Diagram



10 Package Drawings and Markings

The device is available in an 5-pin TSOT-23 package.

Figure 33. 5-pin TSOT-23 Package



Symbol	Min	Typ	Max	Notes		Symbol	Min	Typ	Max	Notes
A			1.00			L	0.30	0.40	0.50	
A1	0.01	0.05	0.10			L1		0.60REF		
A2	0.84	0.87	0.90			L2		0.25BSC		
b	0.30		0.45			N		5		
b1	0.31	0.35	0.39			R	0.10			
c	0.12	0.15	0.20			R1	0.10		0.25	
c1	0.08	0.13	0.16			θ	0º	4º	8º	
D		2.90BSC		3,4		θ1	4º	10º	12º	
E		2.80BSC		3,4		**Tolerances of Form and Position**				
E1		1.60BSC		3,4		aaa		0.15		
e		0.95BSC				bbb		0.25		
e1		1.90BSC				ccc		0.10		
						ddd		0.20		

Notes:

1. Dimensioning and tolerancing conform to *ASME Y14.5M - 1994.*
2. Dimensions are in millimeters.
3. Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15mm per side. Dimensions D and E1 are determined at datum H.
4. The package top can be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but include any mistmatches between the top of the package body and the bottom. D and E1 are determined at datum H.

11 Ordering Information

The device is available as the following standard versions.

Table 7. Ordering Information

Model	Marking	Output	Description	Delivery Form	Package
AS1324-BTTT-AD	ASKR	adjustable	1.5MHz, 600mA Synchronous DC/DC Converter	Tape and Reel	5-pin TSOT-23
AS1324-BTTT-12	ASKT	1.2V	1.5MHz, 600mA Synchronous DC/DC Converter	Tape and Reel	5-pin TSOT-23
AS1324-BTTT-15	ASKU	1.5V	1.5MHz, 600mA Synchronous DC/DC Converter	Tape and Reel	5-pin TSOT-23
AS1324-BTTT-18	ASKS	1.8V	1.5MHz, 600mA Synchronous DC/DC Converter	Tape and Reel	5-pin TSOT-23

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