AS3420

Mono Bluetooth Noise-Cancelling Speaker Driver

1 General Description

The AS3420 is a fully differential speaker driver with Ambient Noise Cancelling function designed for Mono Bluetooth applications. It is intended to improve speech intelligibility of a phone conversation etc. by reducing background ambient noise.The fully analog implementation allows the lowest power consumption, lowest system BOM cost and most natural received voice enhancement otherwise difficult to achieve with DSP implementations. The device is designed to be easily applied to existing architectures. An internal OTP-ROM can be optionally used to store the microphones gain calibration settings if a standard I2C interface on the bluetooth chipset is not available.

The AS3420 can be used in different configurations for best trade-off of noise cancellation, required filtering functions and mechanical designs.The simpler feed-forward topology is used to effectively reduce low frequency background noise. The feed-back topology with either 1 or 2 filtering stages can be used to reduce noise for a larger frequency range.

2 Key Features

Microphone Input

- 128 gain steps @ 0.375dB and MUTE with AGC
- Fully differential, low noise microphone amplifier
- MIC gain OTP programmable

Efficiency Headphone Amplifier

- 80mW, 0.03% THD @ 32Ω, 1.8V supply
- Click and pop less start-up and mode switching

Line Input

- Volume control via serial interface or volume pin
- 64 steps @ 0.75dB and MUTE, pop-free gain setting
- Fully differential input mode

ANC processing

- Feed-forward cancellation
- Feed-back cancellation
- Simple in production SW calibration
- 12-30dB noise reduction (headset dependent)

Performance Parameter

- 3.8mA @ 1.5V mono ANC; <1µA quiescent
- Extended PSRR for 217Hz

Interfaces

- 2-wire serial control mode & volume inputs
- Single cell or fixed 1.0-1.8V supply with internal CP

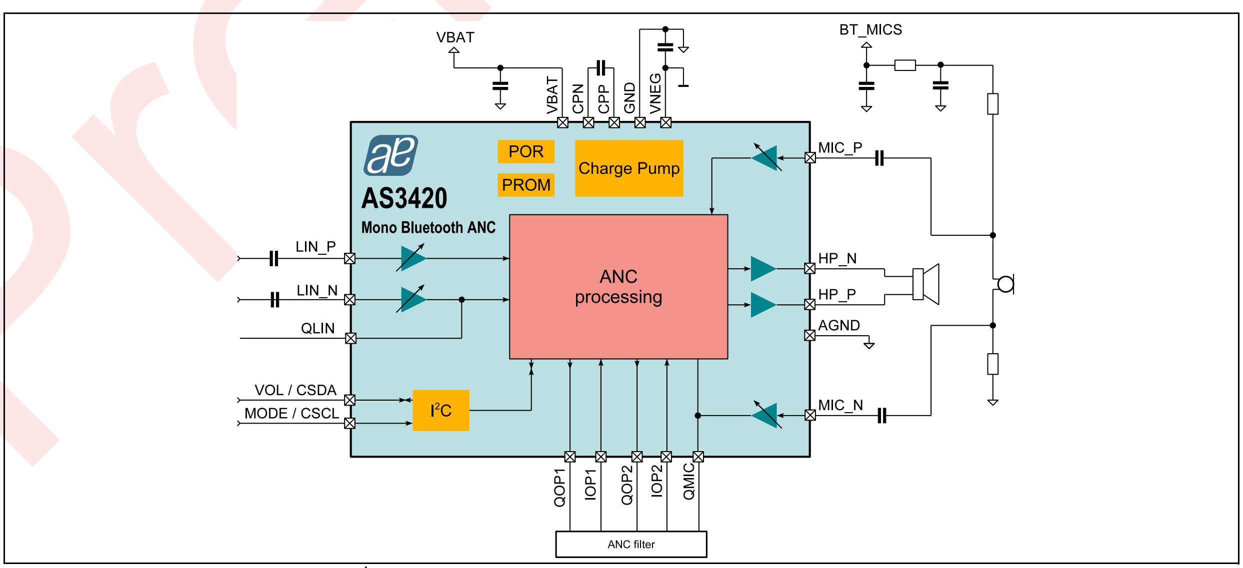
Package

- AS3420, QFN20 [4x4mm] 0.5mm pitch

3 Applications

The devices are ideal for Mono Bluetooth applications.

Figure 1. AS3420 Block Diagram

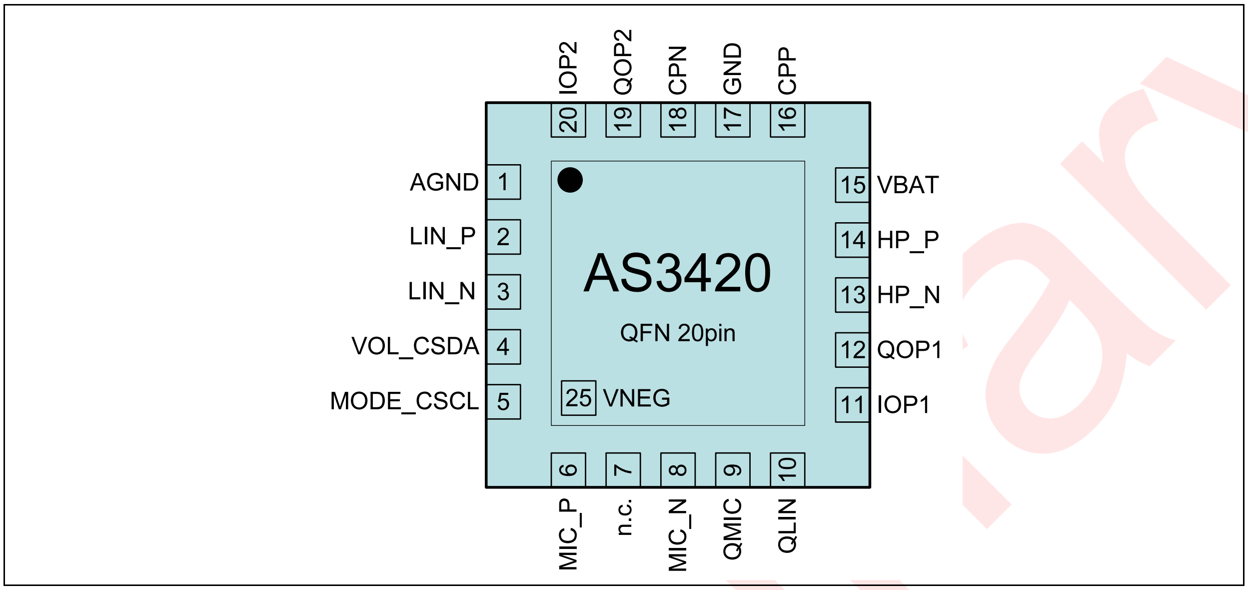


Contents

4 Pin Assignments

Note: Pin assignment may change in preliminary data sheets.

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Note: Pin description may change in preliminary data sheets.

Table 1. Pin Description for AS3420

Pin Name	Pin Number	Type	Description
AGND	1	ANA IN	Analog Reference for all audio related blocks of AS3420.
LIN_P	2	ANA IN	Positive input terminal for differential line input. This input is supposed to be connected to the differential output of a audio codec or audio output of a bluetooth chipset.
LIN_N	3	ANA IN	Negative input terminal for differential line input. This input is supposed to be connected to the differential output of a audio codec or audio output of a bluetooth chipset.
VOL_CSDA	4	MIXED IO	If the device is connected to a CPU the pin is used as a serial interface data input for I2C communication with AS3420. If the AS3420 operates in stand alone mode without a CPU connection the pin can be used to control the line input volume with a potentiometer or two push buttons.
MODE_CSCL	5	DIG IN	If the device is connected to a CPU the pin is used as a serial interface clock input for I2C communication with AS3420. If the AS3420 operates in stand alone mode without a CPU connection the pin can be used to switch the device ON / OFF or change into monitor mode.
MIC_P	6	ANA IN	Positive input terminal pin for the differential microphone input.
n.c.	7		Leave this pin unconnected.
MIC_N	8	ANA IN	Negative input terminal pin for the differential microphone input.
QMIC	9	ANA OUT	This is the microphone preamplifier output pin. This pin can be connected to a filter network for gain and phase compensation of the microphoen path in order to get a good ANC performance.
QLIN	10	ANA OUT	This pin is the line input gain stage amplifier output pin. It is supposed to be used for ANC systems with feedback topology where it is necessary to substract the audio line input signal from the microphone feedback path.
IOP1	11	ANA IN	Negative input terminal for filter OpAmp1 in inverting mode.
QOP1	12	ANA OUT	Output terminal for filter OpAmp1.
HP_N	13	ANA OUT	Negative differential headphone amplifier output. In single ended output mode this pin can be left unconnected.
HP_P	14	ANA OUT	Positiv differential headphone amplifier output. In single ended output mode this must be connected to the speaker.
VBAT	15	SUP IN	This is the positive supply terminal for AS3420. This pin supplies internally the charge pump for creating the negative supply voltgae of the chip in order to operate the device as true ground headphone amplifier. This pin requires a 10µF bypass capacitor.
CPP	16	ANA OUT	VNEG ChargePump flying capacitor positive terminal. This pin needs a 1µF flying capacitor connected to pin CPN.
GND	17	ANA OUT	VNEG ChargePump 0V ground supply terminal.
CPN	18	ANA OUT	VNEG ChargePump flying capacitor negative terminal.
QOP2	19	ANA OUT	Output terminal for filter OpAmp2.
IOP2	20	ANA IN	Negative input terminal for filter OpAmp2 in inverting mode.
VNEG	21	SUP IO	VNEG ChargePump output. This pin is the exposed pad of the QFN package and needs an external 10µF bypass capacitor.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 6 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated under recommended operating conditions.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Reference Ground				Defined as in GND
Supply terminals	-0.5	2.0	V	Applicable for pin VBAT, HPVDD
Ground terminals	-0.5	0.5	V	Applicable for pins AGND
Negative terminals	-2.0	0.5	V	Applicable for pins VNEG, VSS, HPVSS
Voltage difference at VSS terminals	-0.5	0.5	V	Applicable for pins VSS, HPVSS
Pins with protection to VBAT	VNEG -0.5	5.0 VBAT+0.5	V	Applicable for pins CPP, CPN
Pins with protection to HPVDD	VSS -0.5	5.0 HPVDD+0.5	V	Applicable for pins LINL/R, MICL/R, ILED, HPR, HPL, QMICL/R, QLINL/R, IOPx, QOPx
other pins	VSS -0.5	5		Applicable for pins MICS, VOL_CSDA, MODE_CSCL
Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC 17
Continuous Power Dissipation (T_A = +70ºC)				
Continuous Power Dissipation	-	200	mW	P_T[1] for QFN16/24/32 package
Electrostatic Discharge				
Electrostatic Discharge HBM		+/-2	kV	Norm: JEDEC JESD22-A114C
Temperature Ranges and Storage Conditions				
Junction Temperature		+110	ºC	
Storage Temperature Range	-55	+125	ºC	
Humidity non-condensing	5	85	%	
Moisture Sensitive Level	3			Represents a max. floor life time of 168h
Package Body Temperature		260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020"Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".*

1. Depending on actual PCB layout and PCB used

6 Electrical Characteristics

VBAT = 1.0V to 1.8V, T_A = -20ºC to +85ºC. Typical values are at VBAT = 1.5V, T_A = +25ºC, unless otherwise specified.

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
T_A	Ambient Temperature Range		-20	+85	°C
Supply Voltages					
GND	Reference Ground		0	0	V
VBAT, HPVDD	Battery Supply Voltage	normal operation with MODE pin high	1.0	1.8	V
		Two wire interface operation	1.4	1.8	V
VNEG	ChargePump Voltage		-1.8	-0.7	V
VSS	Analog neg. Supply Voltages HPVSS, VSS, VNEG		-1.8	-0.7	V
V_{DELTA-}	Difference of Ground Supplies GND, AGND	To achieve good performance, the negative supply terminals should be connected to low impedance ground plane.	-0.1	0.1	V
$V_{DELTA--}$	Difference of Negative Supplies VSS, VNEG, HPVSS	Charge pump output or external supply	-0.1	0.1	V
V_{DELTA+}	Difference of Positive Supplies	VBAT-HPVDD	-0.25	0.25	V
Other pins					
V_{MICS}	Microphone Supply Voltage	MICS	0	3.6	V
V_{HPVDD}	Pins with diode to HPVDD	MICL/R, ILED, HPR, HPL, QMICL/R, QLINL/R, IOPx, QOPx	VSS	3.6	V
V_{VBAT}	Pins with diode to VBAT	CPP, CPN	VNEG	VBAT	V
$V_{CONTROL}$	Control Pins	MODE_CSCL, VOL_CSDA	VSS	3.7	V
V_{TRIM}	Line Input & Application Trim Pins	LINL, LINR	VNEG -0.5 or -1.8	HPVDD +0.5 or 1.8	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{leak}	Leakage current	VBAT<0.8V			20	µA
		VBAT<0.6V			10	µA
Block Power Requirements @ 1.5V VBAT						
I_{SYS}	Reference supply current	Bias generation, oscillator, ILED current sink, ADC6		0.25		mA
I_{LIN}	LineIn gain stage current	no signal, stereo		0.64		mA
I_{MIC}	Mic gain stage current	no signal, stereo		2.10		mA
I_{HP}	Headphone stage current	no signal		1.70		mA
I_{VNEG}	VNEG charge pump current	no load		0.25		mA
I_{MICS}	MICS charge pump current	no load		0.06		mA
I_{MIN}	Minimal supply current	Sum of all above blocks		5.00		mA
I_{OP1}	OP1 supply current	no load		0.64		mA
I_{OP2}	OP2 supply current	no load		0.64		mA

7 Typical Operating Characteristics

VBAT = +1.5V, T_A = +25ºC, unless otherwise specified.

Figure 3. THD+N vs. Pout; Line to HPH; 16Ω bridged tied load

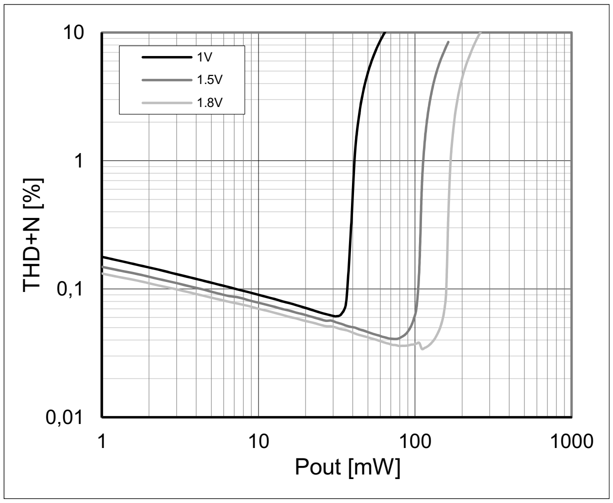


Figure 4. THD+N vs. Pout; Line to HPH; 32Ω bridged tied load

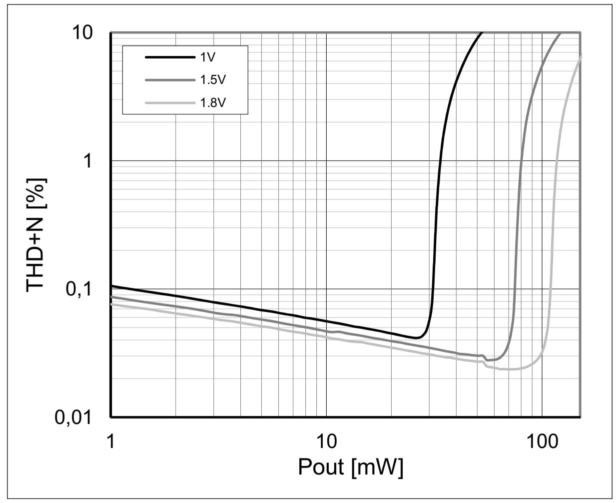


Figure 5. THD+N vs. Pout; Line to HPH; 64Ω bridged tied load

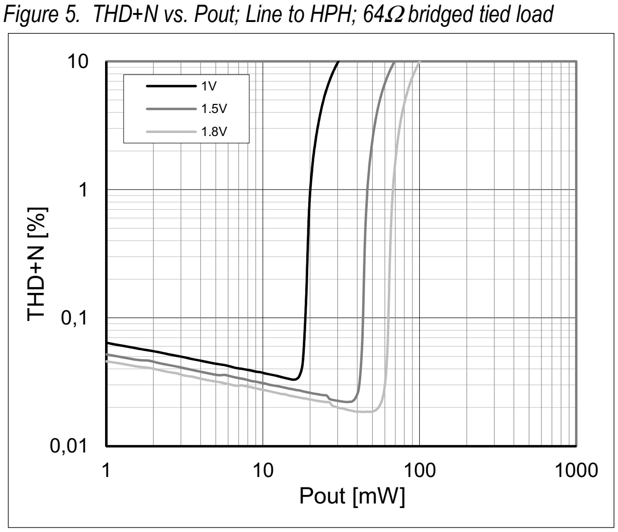


Figure 6. THD+N vs. f; Line to HPH; 1mW bridged tied load

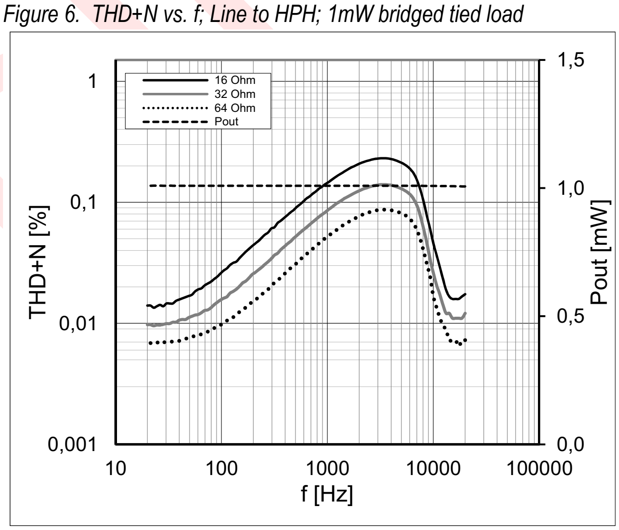


Figure 7. THD+N vs. f; Line to HPH; 20mW bridged tied load

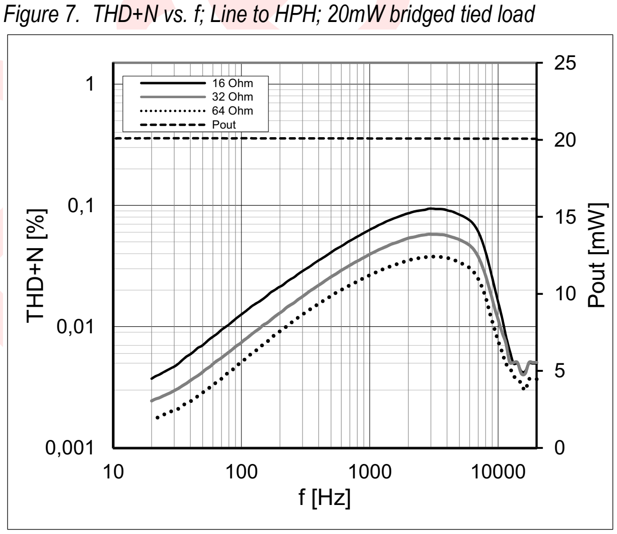


Figure 8. THD+N vs. f; Line to HPH; bridged tied load conditions

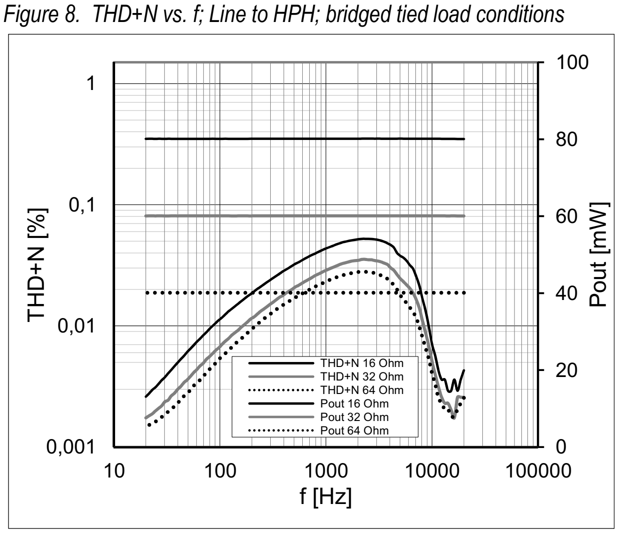


Figure 9. Frequency Response line input to headphone with 64Ω bridged tied load and 40mW output power

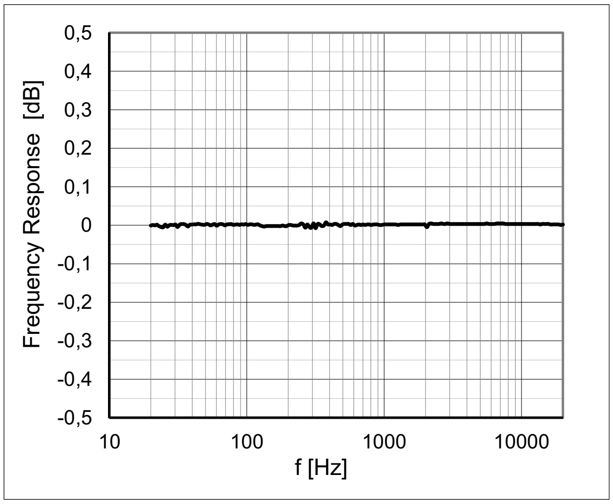


Figure 10. Frequency Response line input to headphone with 32Ω bridged tied load and 60mW output power

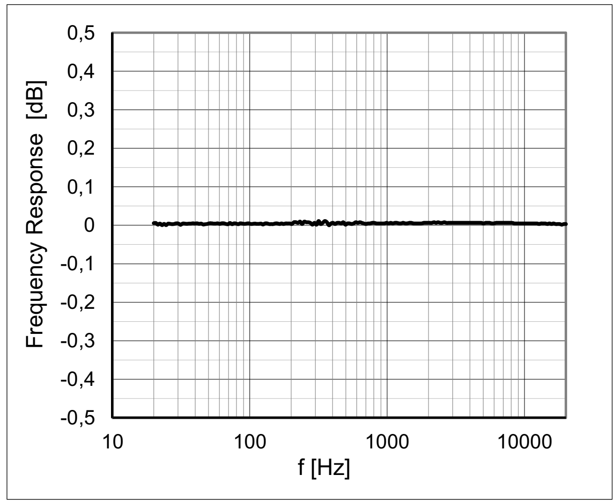


Figure 11. Frequency Response line input to headphone with 16Ω bridged tied load and 80mW output power

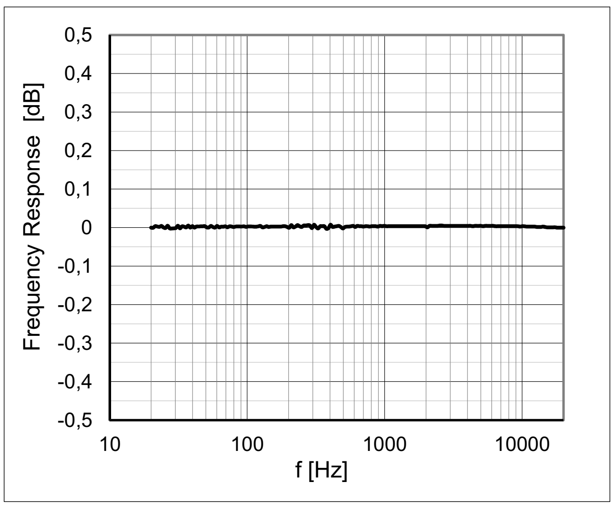


Figure 12. VNEG CP Voltage vs. load current with different supply voltages

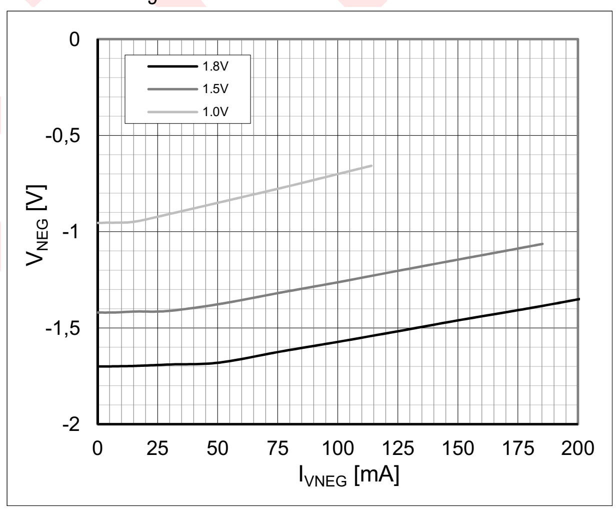


Figure 13. V_{NEG} Efficiency vs. I_{VNEG}

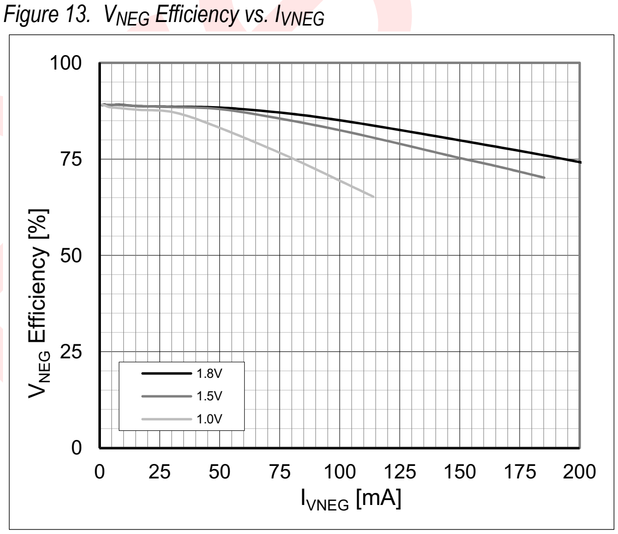
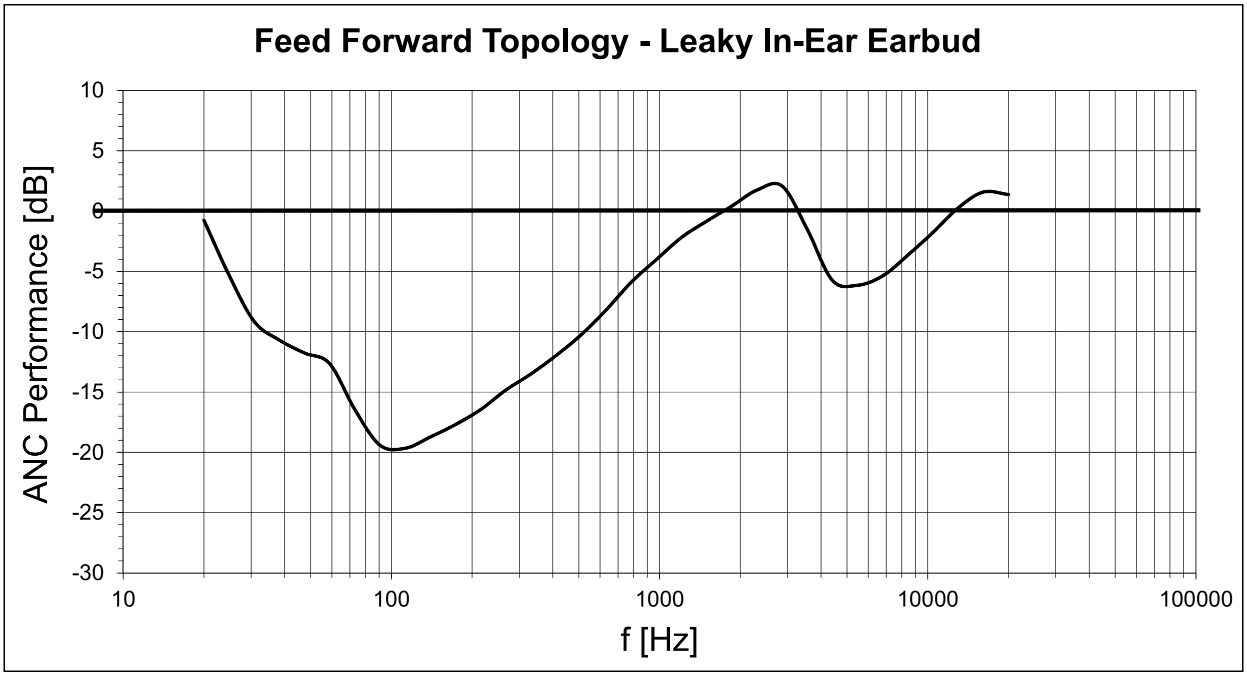


Figure 14. Performance Data, FF Configuration



8 Detailed Description

This section provides a detailed description of the device related components.

8.1 Audio Line Input

The chip features one differential line input.

In addition to the internal 12.5-25kΩ gain change resistors, the Line Input has a termination resistor of 10kΩ against AGND which is also effective during MUTE to charge eventually given input capacitors.

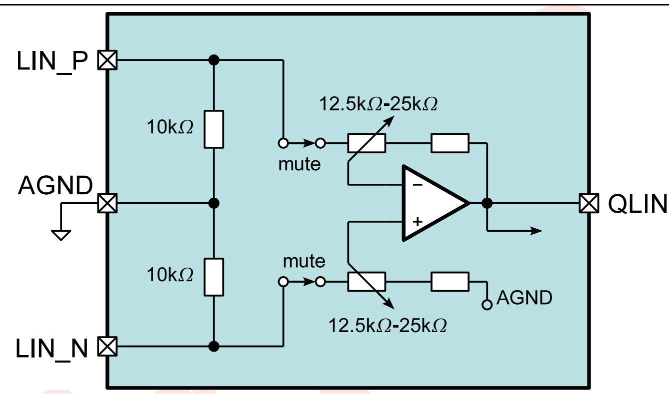
8.1.1 Gain Stage

The Line Input gain stage is designed to have 63 gain steps of 0.75dB with a max gain of 0dB plus MUTE.

In default, the gain will be ramped up from MUTE to 0dB during startup. There is a possibility to make the playback volume user controlled with an external potentiometer connected to VOL_CSDA pin or with simple UP/DOWN push-buttons.

In monitor mode, the gain stage can be set to an fixed default attenuation level for reducing the loudness of the music.

Figure 15. Line Inputs



8.1.2 Parameter

VBAT=1.5V, T_A= 25ºC, unless otherwise specified.

Table 4. Line Input Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{LIN}	Input Signal Level			0.6* VBAT	VBAT	V_{PEAK}
R_{LIN}	Input Impedance	0dB gain (25k // 20k)		11.1		kΩ
		-46.5dB gain (50k // 20k)		14.3		kΩ
		MUTE		20		kΩ
Δ_{RLIN}	Input Impedance Tolerance			±30		%
C_{LIN}	Input Capacitance			2.5		pF
A_{LIN}	Programmable Gain		-46.5		+0	dB
	Gain Steps	Discrete logarithmic gain steps		0.75		dB
	Gain Step Accuracy			0.5		dB
$A_{LINMUTE}$	Mute Attenuation			100		dB
Δ_{ALIN}	Gain Ramp Rate	Poti Mode, Tinit=100ms		20		ms/step
		Button Mode, Tinit=400ms		80		
		Monitor Mode		8		

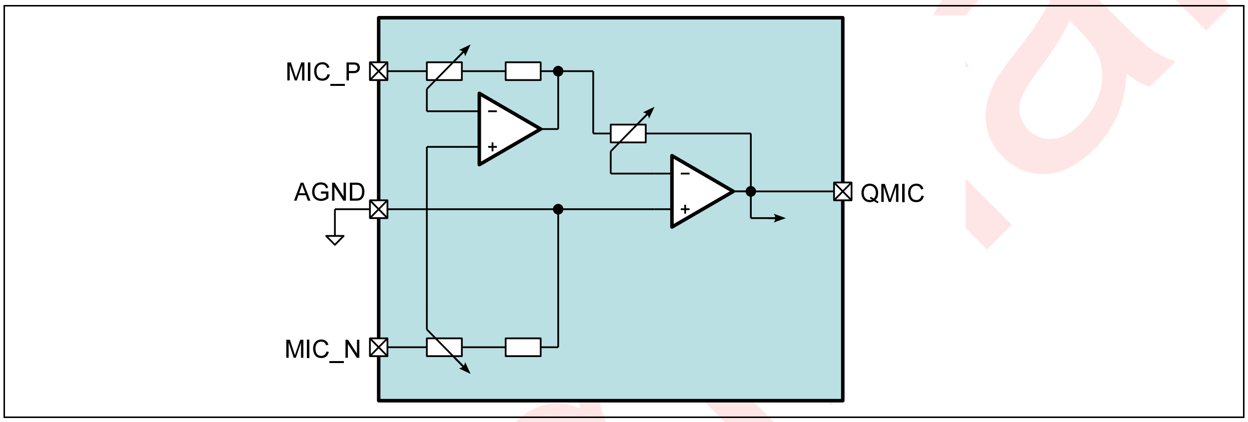
Table 4. Line Input Parameter (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ATTACK}	Limiter Activation Level	HPL/R start of neg. clipping				V_{PEAK}
V_{DECAY}	Limiter Release Level	HPL/R		VNEG +0.3		V_{PEAK}
t_{ATTACK}	Limiter Attack Time			4		µs
t_{DECAY}	Limiter Decay Time			8		ms

8.2 Microphone Input

The AS3420 offers one fully differential microphone input.

Figure 16. Microphone Input



8.2.1 Gain Stage & Limiter

The Mic GainStage has programmable Gain within -6dB…+41.625dB in 128 steps of 0.375dB.

As soft-start function is implemented for an automatic gain ramping implemented with steps of 4ms to fade in the audio at the end of the start-up sequence.

A limiter automatically attenuates high input signals. The AGC has 127 steps with 0.375dB with a dynamic range of the full gain stage.

In monitor mode, the gain stage can be set to an fixed (normally higher) gain level or be controlled by the VOL pin.

8.2.2 Parameter

VBAT=1.5V, T_A= 25ºC unless otherwise specified.

Table 5. Microphone Input Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{MICIN}0$	Input Signal Level	A_{MIC} = 30dB		20		mV_P
$V_{MICIN}1$		A_{MIC} = 36dB		10		mV_P
$V_{MICIN}2$		A_{MIC} = 42dB		5		mV_P
R_{MICIN}	Input Impedance	MICP to AGND		7.5		kΩ
Δ_{MICIN}	Input Impedance Tolerance			-7 +33		%
C_{MICIN}	Input Capacitance			2.5		pF
A_{MIC}	Programmable Gain		-6		+41.6	dB
	Gain Steps	Discrete logarithmic gain steps		0.375		dB
	Gain Step Precision			0.15		dB
Δ_{AMIC}	Gain Ramp Rate	Tinit=64ms		4		ms/step

Table 5. Microphone Input Parameter (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ATTACK}	Limiter Activation Level	V_{PEAK} related to VBAT or VNEG		0.67		1
V_{DECAY}	Limiter Release Level			0.4		1
$A_{MICLIMIT}$	Limiter Gain Overdrive	127 @ 0.375dB		41.625		dB
t_{ATTACK}	Limiter Attack Time			5		µs/step
$t_{DECAY-DEB}$	Limiter Decay Debouncing Time			64		ms
t_{DECAY}	Limiter Decay Time			4		ms/step

8.3 Headphone Output

The headphone output is a true ground output using VNEG as negative supply, designed to provide the audio signal with 2x12mW @ 16Ω-64Ω, which are typical values for headphones. It is also capable to operate in bridged mode for higher impedance (e.g. 300Ω) headphone. In this mode the left output is carrying the inverted signal of the right output shown in Figure 17. If an application doesn't need the full output power it is recommended to operate the headphone amplifier in single ended mode due to power savings.

Figure 17. Headphone Output Mono Differential Mode

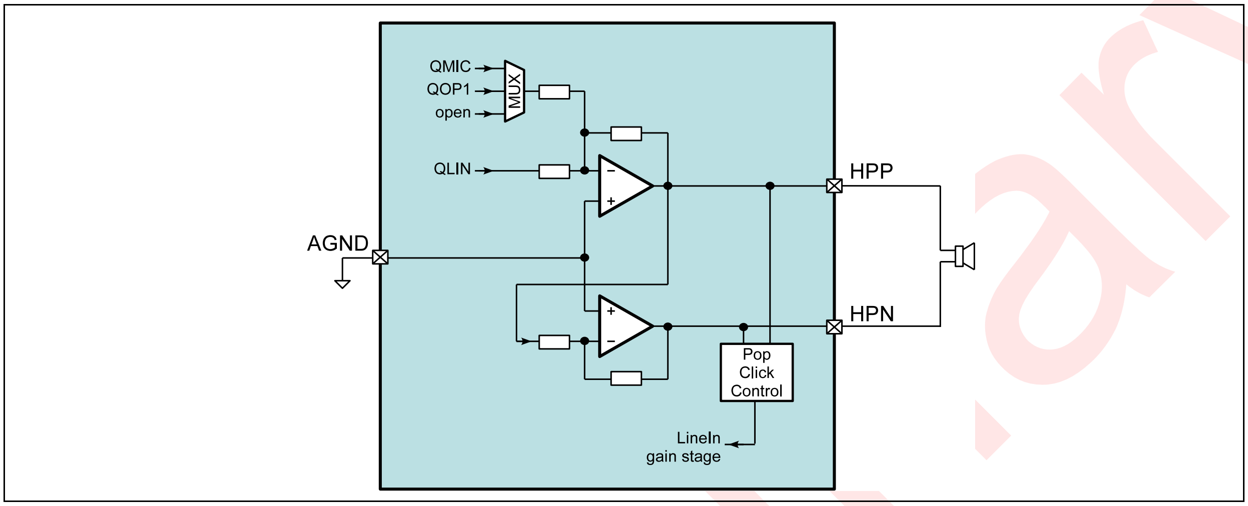
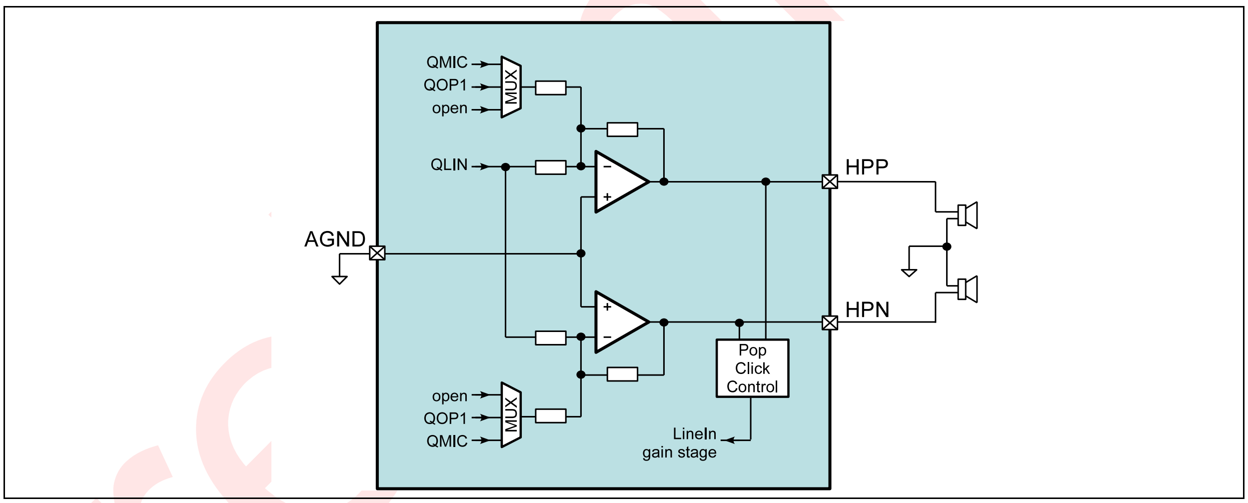


Figure 18. Headphone Output Single Ended Mode



8.3.1 Input Multiplexer

The signal from the line-input gain stage gets summed at the input of the headphone stage with the microphone gain stage output or the first filter opamp output . The microphone gain stage output is used per default. It is also possible to playback without ANC by only using the line-input gain stage with no other signal on the multiplexer.

For the monitor mode, the setting of this input multiplexer can be changed to another source, normally to the microphone.

8.3.2 No-Pop Function

The No-Pop startup of the headphone stage takes 60ms to 120ms dependent on the supply voltage.

8.3.3 No-Clip Function

The headphone output stage gets monitored by comparator stages which detect if the output signal starts to clip.

This signal is used to reduce the LineIn gain to avoid distortion of the output signal. A hystereses avoids jumping between 2 gain steps for a signal with constant amplitude.

8.3.4 Over-Current Protection

The over-current protection has a threshold of 150-200mA and a debouncing time of 8µs. The stage is forced to OFF mode in an over-current situation. After this, the headphone stage tries to power up again every 8ms as long as the over-current situation still exists or the stage is turned off manually.

8.3.5 Parameter

VBAT=1.5V, T_A= 25ºC, unless otherwise specified.

Table 6. Headphone Output Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{L_HP}	Load Impedance	Stereo mode	16			Ω
C_{L_HP}	Load Capacitance	Stereo mode			100	pF
P_{HP}	Nominal Output Power	RL=64Ω single ended	12			mW
		RL=32Ω single ended	24			mW
		RL=16Ω single ended	34			mW
P_{SRRHP}	Power Supply Rejection Ratio	200Hz-20kHz, 720mVpp, RL=16Ω		90		dB

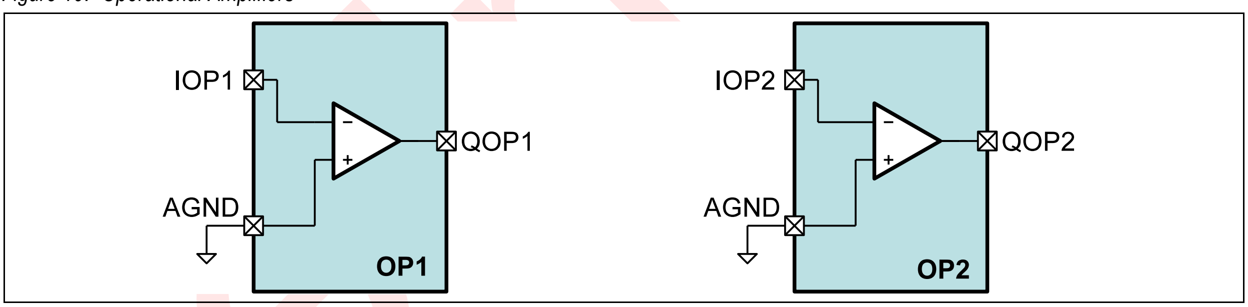
8.4 Operational Amplifier

The AS3420 features two general purpose amplifiers which can be used for filter development. With these two filter stages it is possible to go either for complex mono feedback filters or with the more simple feed forward approach for Active Noise Cancelling.

If only one operational amplifier is used it is mandatory to use OP1, because only OP1 can be connected with the headphone multiplexer to the headphone amplifier. If both operational amplifiers are used it is important to use first OP2 and as secondly OP1 because of the headphone multiplexer input. If you use OP1 first and afterwards OP2 in the signal chain you can not link the headphone amplifier to the output of OP2. Therefore it is always important to use the right OpAmp alignment.

Both amplifiers work as inverting amplifiers with the positive pin conected internally to AGND.

Figure 19. Operational Amplifiers



8.4.1 Parameter

VBAT=1.5V, T_A= 25ºC, unless otherwise specified.

Table 7. Headphone Output Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{L_OP}	Load Impedance	Single ended	1			kΩ
C_{L_OP}	Load Capacitance	Single ended			100	pF
GBW_{OP}	Gain Band Width			4.3		MHz
V_{OS_OP}	Offset Voltage				6	mV
V_{EIN_HP}	Equivalent Input Noise	200Hz-20kHz		2.6		µV

8.5 SYSTEM

The system block handles the power up and power down sequencing, as well as, the mode switching.

8.5.1 Power Up/Down Conditions

The chip powers up when one of the following conditions is true:

Table 8. Power UP Conditions

#	Source	Description
1	MODE pin	In stand-alone mode, MODE pin has to be driven high to turn on the device
2	I2C start	In I2C mode, a I2C start condition turns on the device

The chip automatically shuts off if one of the following conditions arises:

Table 9. Power DOWN Conditions

#	Source	Description
1	MODE pin	Power down by driving MODE pin to low
2	SERIF	Power down by SERIF writing 0h to register 20h bit <0>
3	Low Battery	Power down if VBAT is lower than the supervisor off-threshold
4	VNEG CP OVC	Power down if VNEG is higher than the VNEG off-threshold

8.5.2 Start-up Sequence

The start-up sequence depends on the used mode.

In stand-alone mode the sequence runs automatically, in I2C mode the sequence runs till a defined state and waits then for an I2C command. Either the automatic sequence is started by setting the CONT_PWRUP bit in addition to the PWR_HOLD bit. If only the PWR_HOLD is set all enable bits for headphone, microphone, etc have to be set manually.

Figure 20. Stand-Alone Mode Start-Up Sequence

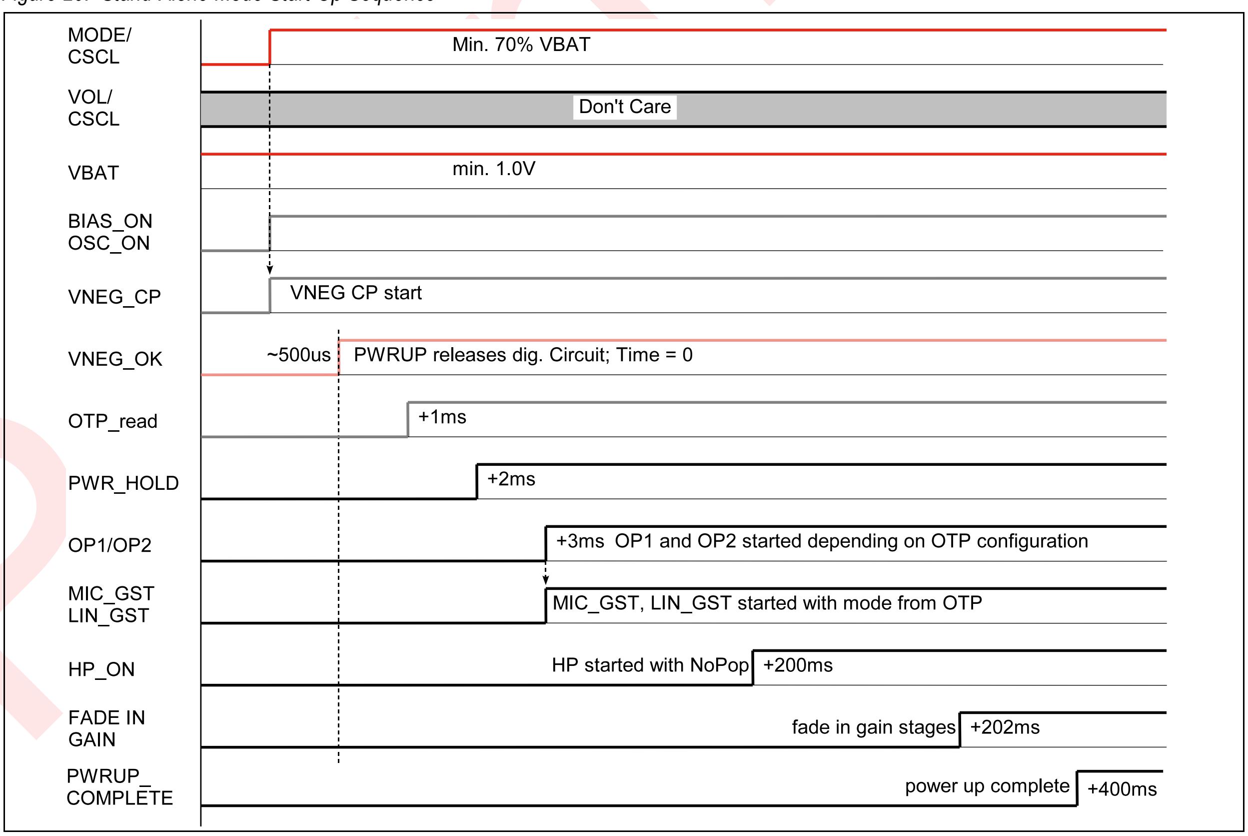
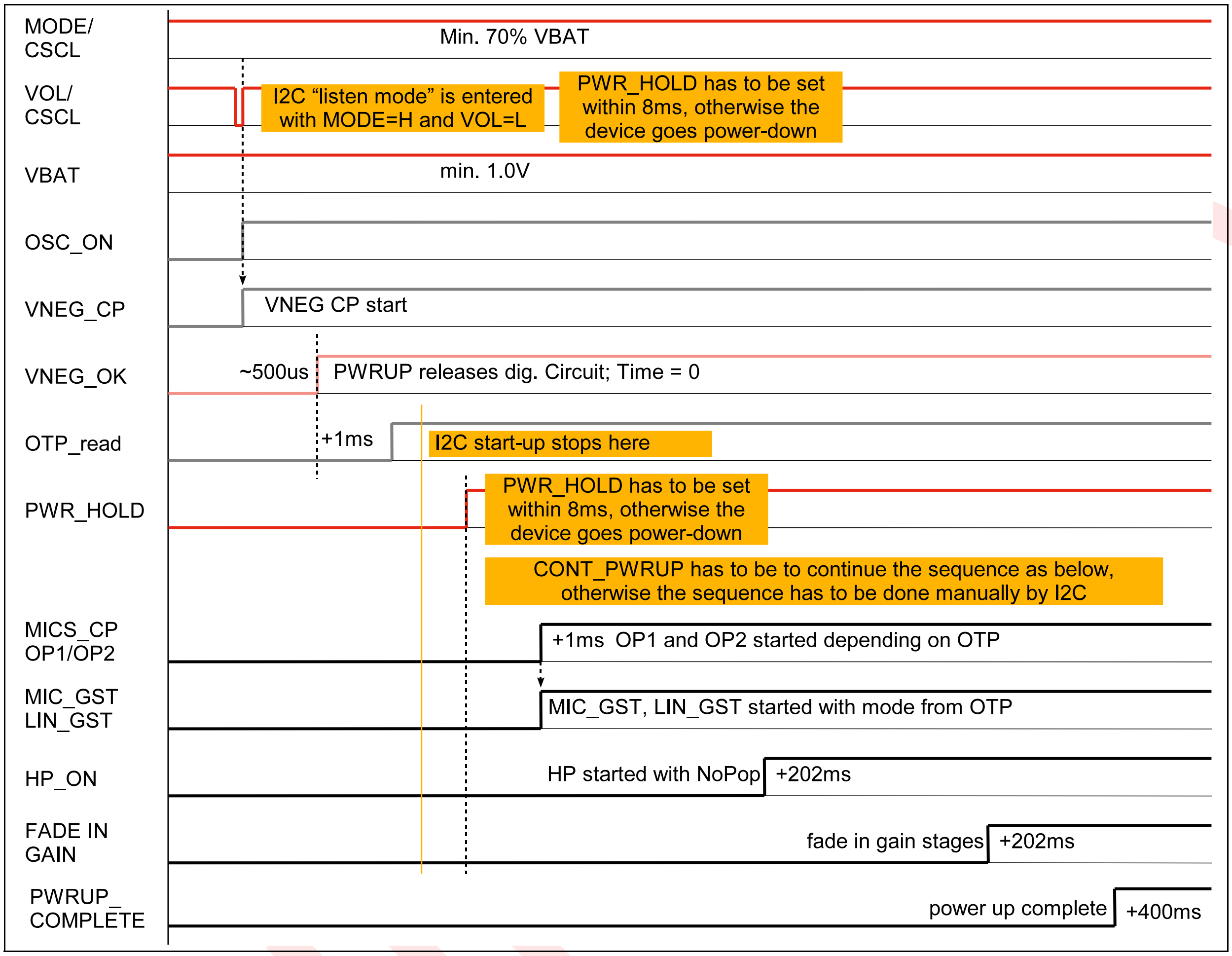


Figure 21. I2C Mode Start-Up Sequence



The total start-up time (inlcuding fade-in of the gain stages) can be reduced from 800ms to 600ms by OTP setting.

8.5.3 Mode Switching

When the chip is in stand-alone mode (no I2C control), the mode can be switched with different levels on the MODE pin.

Table 10. Operation Modes

MODE	MODE pin	Description
OFF	LOW (VSS)	Chip is turned off
ANC	HIGH (VBAT)	Chip is turned on and active noise cancellation is active
MONITOR	VBAT/2	Chip is turned on and monitor mode is active In Monitor mode, a different (normally higher) microphone preamplifier gain can be chosen to get an amplification of the surrounding noise. This volume can be either fixed or be controlled by the VOL input. To get rid of the low pass filtering needed for the noise cancellation, the headphone input multiplexer can be set to a different (normally to MIC) source. In addition, the LineIn gain can be lowered to reduce the loudness of the music currently played back.

In I2C mode, the monitor mode can be activated be setting the corresponding bit in the system register.

8.6 VNEG Charge Pump

The VNEG charge pump uses one external 1uF capacitor to generate a negative supply voltage out of the battery input voltage to supply all audio related blocks. This allows a true-ground headphone output with no more need of external DC-decoupling capacitors.

8.6.1 Parameter

VBAT=1.5V, T_A= 25ºC, unless otherwise specified.

Table 11. Headphone Output Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN}	Input voltage	VBAT	1.0	1.5	1.8	V
V_{OUT}	Output voltage	VNEG	-0.7	-1.5	-1.8	V
C_{EXT}	External flying capacitor			1		µF

8.7 OTP Memory & Internal Registers

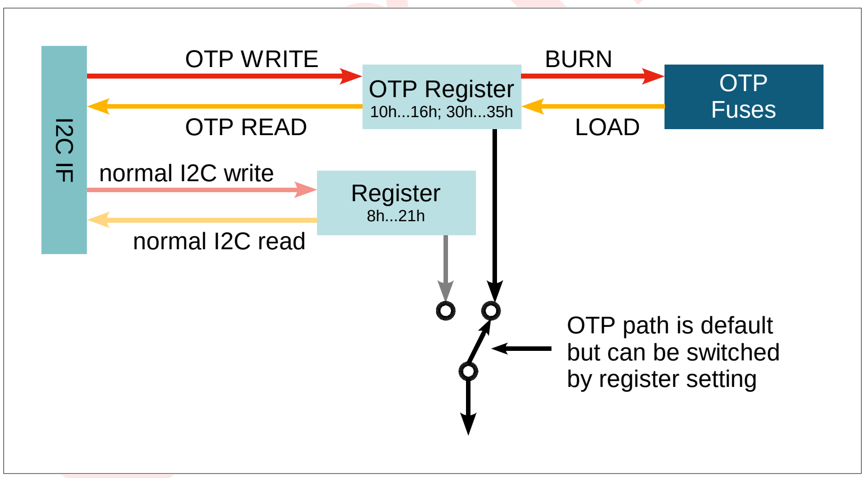
The OTP memory consists of OTP register and the OTP fuses.The OTP register can be written as often as wanted but will lose the content on power off. The OTP fuses are intended to store basic chip configurations as well as the microphone gain settings to optimize the ANC performance and get rid of sensitivity variations of different microphones. Burning the fuses can only be done once and is a permanent change, which means the fuses keep the content even if the chip is powered down. This AS3420 offers 4 register set for storing the microphone gain making it possible to change the gain 3 times for re-calibration or other purposes.

When the chip is controlled by a microcontroller via I2C, the OTP memory don't has to be used.

8.7.1 Register & OTP Memory Configuration

Figure 22 is showing the principal register interaction.

Figure 22. Register Access



Registers 0x8, 0x9, 0xA, 0xB, 0xC and 0x21 have only effect when the corresponding "REG_ON" bit is set, otherwise the chip operates with the OTP Register settings which are loaded from the OTP fuses at every start-up.

All registers settings can be changed several times, but will loose the content on power off. When using the I2C mode, the chip configuration has to be loaded from the microcontroller after every start-up. In stand alone mode the OTP fuses have to be programmed for a permanent change of the chip configuration.

A single OTP cell can be programmed only once. Per default, the cell is "0"; a programmed cell will contain a "1". While it is not possible to reset a programmed bit from "1" to "0", multiple OTP writes are possible, but only additional unprogrammed "0"-bits can be programmed to "1".

Independent of the OTP programming, it is possible to overwrite the OTP register temporarily with an OTP write command at any time. This setting will be cleared and overwritten with the hard programmed OTP settings at each power-up sequence or by a LOAD operation.

The OTP memory can be accessed in the following ways:

LOAD Operation. The LOAD operation reads the OTP fuses and loads the contents into the OTP register. A LOAD operation is automatically executed after each power-on-reset.

WRITE Operation. The WRITE operation allows a temporary modification of the OTP register. It does not program the OTP. This operation can be invoked multiple times and will remain set while the chip is supplied with power and while the OTP register is not modified with another WRITE or LOAD operation.

READ Operation. The READ operation reads the contents of the OTP register, for example to verify a WRITE command or to read the OTP memory after a LOAD command.

BURN Operation. The BURN operation programs the contents of the OTP register permanently into the OTP fuses. Don't use old or nearly empty batteries for burning the fuses.

Attention: If you once burn the OTP_LOCK bit, no further programming, e.g. setting additional "0" to "1", of the OTP can be done.

For production, the OTP_LOCK bit must be set to avoid an unwanted change of the OTP content during the livetime of the product.

8.7.2 OTP Fuse Burning

In most stand alone applications, the I2C pins are not accessible. Burning the fuses can be done by switching the line inputs into a special mode to access the chip by I2C over the line input connections. This allows trimming of the microphone gain with no openings in the final housing and so no influence to the acoustic of the headset.

This mode is called "Application Trimm" mode, or short "APT". (Patent Pending)

During the application trimm mode LINR has to provide the clock, while LINL has to provide the data for the I2C communication.

Please note that the OTP register cannot be accessed directly but have to be enabled before a read or write access. This is independent whether you access the OTP register via the normal I2C pins or in application trimm mode via LINL and LINR. Please refer to the detailed register description to get more information on how the registers can be accessed.

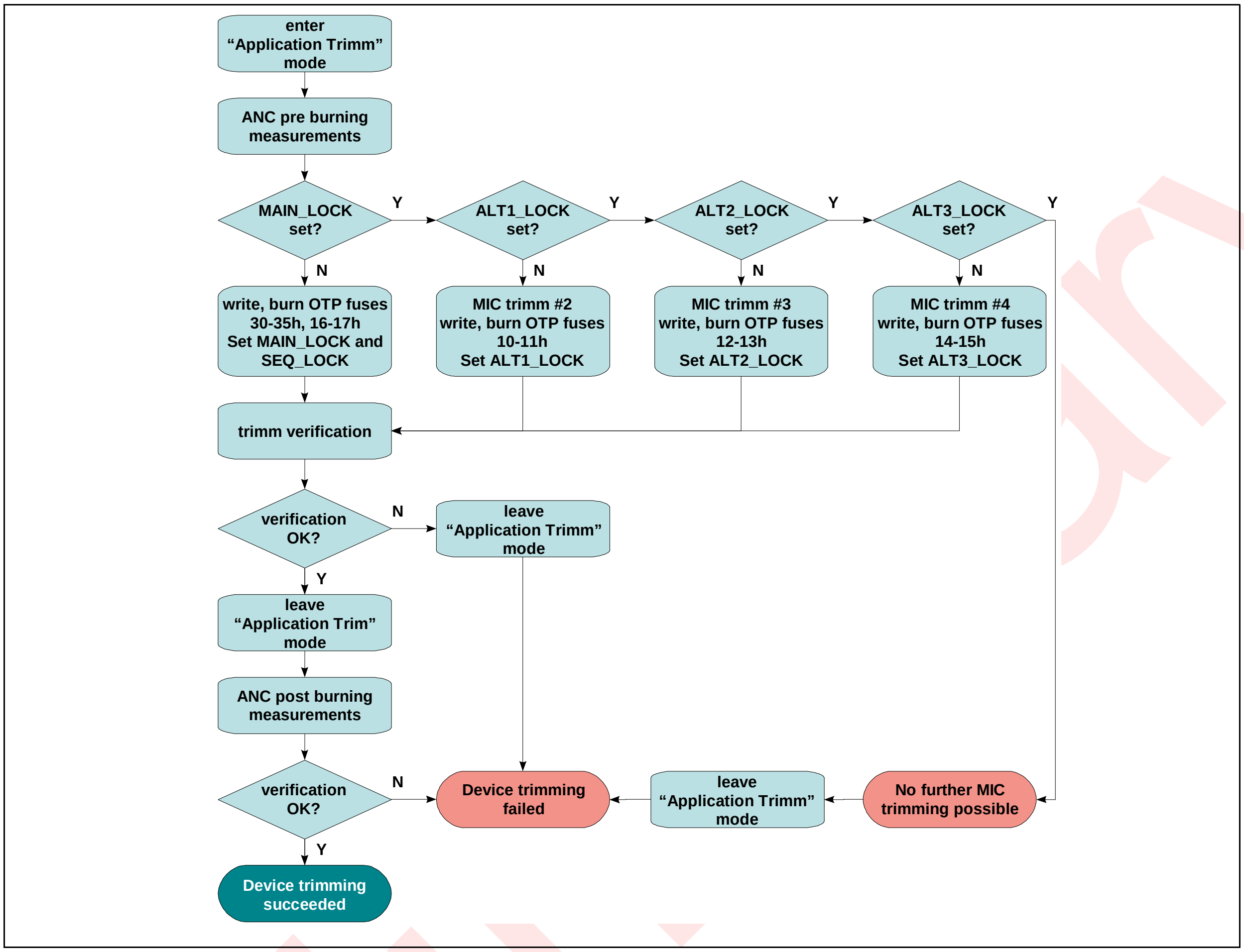
To achieve a proper burning of the fuses, the negative supply has to be buffered by applying an external negative supply during burning. This voltage can also be applied to the LINL terminal. An internal switch is connecting LINL and VNEG during the fuse burning. LINR has to provide the clock for burning the fuses.

The below flow chart shows the principle steps of the OTP burning process. The application trimm mode can only be entered at a specific timing during the start-up sequence.

The device offers the possibility to change microphone gain settings 3 times by using alternative registers. The selection which register set is being used to set the microphone gain is done by the "lock" bits of the corresponding registers.

A more detailed description of the individual steps is available in an application note.

Figure 23. OTP Burning Process



8.8 2-Wire-Serial Control Interface

There is an I2C slave block implemented to have access to 64 byte of setting information.

The I2C address is: Adr_Group8 - audio processors

- 8Eh_write
- 8Fh_read

8.8.1 Protocol

Table 12. 2-Wire Serial Symbol Definition

Symbol	Definition	RW	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	1000 1110b (8Eh)
DR	Device address for read	R	1000 1111b (8Fh)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit

Table 12. 2-Wire Serial Symbol Definition

Symbol	Definition	RW	Note
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	during acknowledge
(shaded)	AS3420 (=slave) receives data		
	AS3420 (=slave) transmits data		

Figure 24. Byte Write

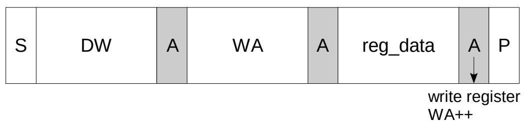
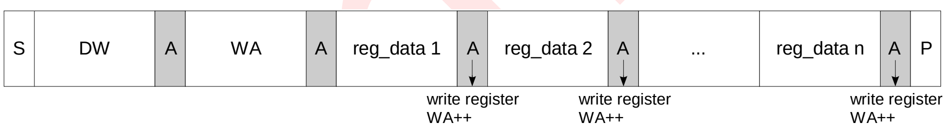


Figure 25. Page Write



Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

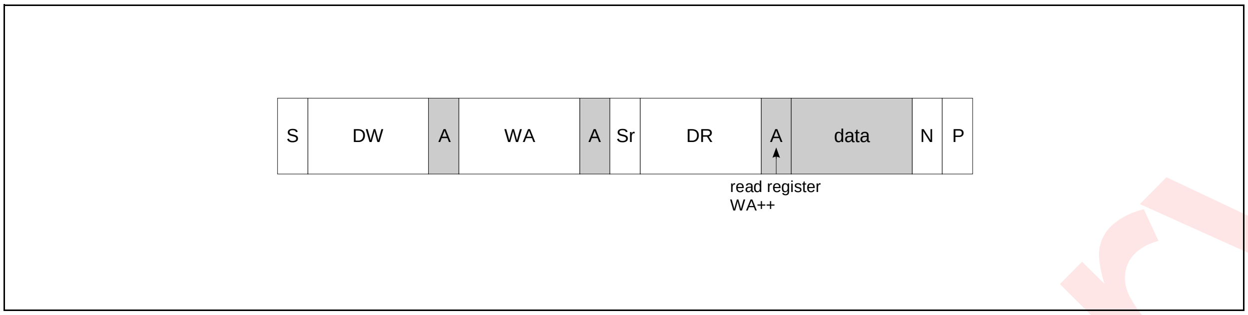


Figure 26. Random Read

Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

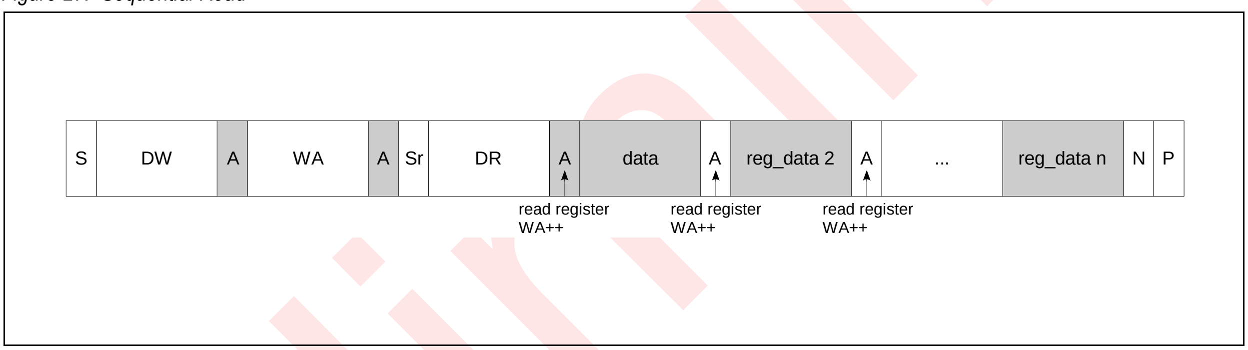


Figure 27. Sequential Read

Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

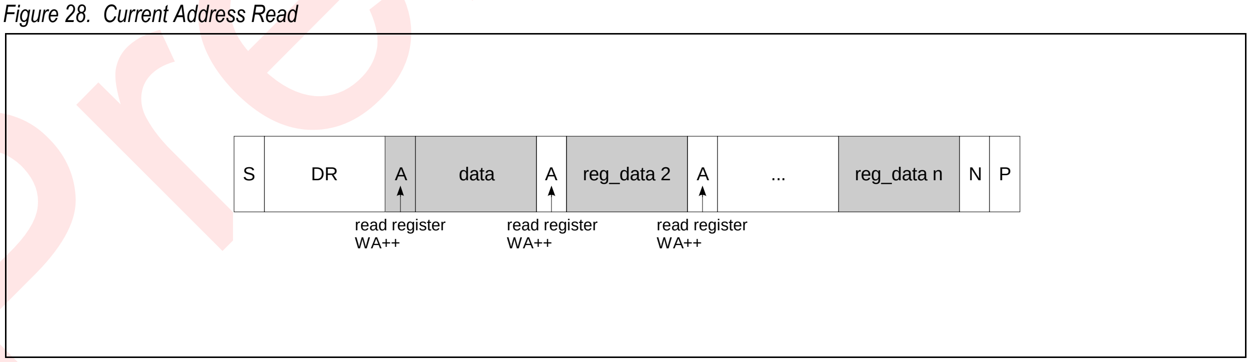
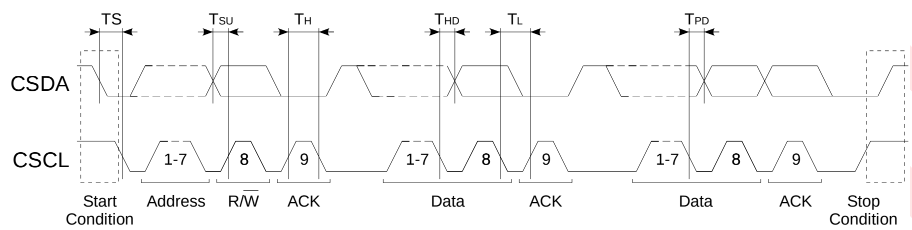


Figure 28. Current Address Read

To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

8.8.2 Parameter

Figure 29. 2-Wire Serial Timing



VBAT >=1.4V[1], T_A=25ºC, unless otherwise specified.

Table 13. 2-Wire Serial Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CSL}	CSCL, CSDA Low Input Level	(max 30%DVDD)	0	-	0.87	V
V_{CSH}	CSCL, CSDA High Input Level	CSCL, CSDA (min 70%DVDD)	2.03	-	5.5	V
HYST	CSCL, CSDA Input Hysteresis		200	450	800	mV
V_{OL}	CSDA Low Output Level	at 3mA	-	-	0.4	V
Tsp	Spike insensitivity		50	100	-	ns
T_H	Clock high time	max. 400kHz clock speed	500			ns
T_L	Clock low time	max. 400kHz clock speed	500			ns
T_{SU}		CSDA has to change Tsetup before rising edge of CSCL	250	-	-	ns
T_{HD}		No hold time needed for CSDA relative to rising edge of CSCL	0	-	-	ns
TS		CSDA H hold time relative to CSDA edge for start/stop/rep_start	200	-	-	ns
T_{PD}		CSDA prop delay relative to lowgoing edge of CSCL		50		ns

1. Serial interface operates down to VBAT = 1.0V but with 100kHz clock speed and degraded parameters.

9 Register Description

Table 14. I2C Register Overview

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
Audio Registers									
00-07h	reserved								
08h	MIC_CNTR	MIC_ON_N							
09h	MIC	MIC_REG_ON 0: use reg 30h & 31h 1: use reg 08h & 09h	MICP_VOL<6:0> Gain from MICP to QMIC or Mixer = -6dB...+41.6dB; 127 steps of 0.375dB						
0Ah	LINE_IN	LIN_REG_ON 0: use reg 33h and VOL pin 1: use reg 0Ah	LIN_ON_N	LIN_VOL<5:0> 0: MUTE; 0x01..0x3F: Gain from LINP/N to QLIN or Mixer = -46.5dB...+0dB; 63 steps of 0.75dB					
0Bh	GP_OP_2	HP_MUX<1:0> 0: MIC; 1: OP1; 2: - ; 3: open							OP2_ON
0Ch	GP_OP_1	OP_REG_ON 0: use reg 34h 1: use reg 0Bh & 0Ch	HP_ON_N 0: HPH switched off 1: HPH switched on						OP1_ON
0Dh-0Fh	reserved								
18h-1Fh	reserved								
System Register									
20h	SYSTEM	Design_Version<3:0> 0100				REG3F_ON	MONITOR_ON	CONT_PWRUP	PWR_HOLD
21h	PWR_SET	PWR_REG_ON 0: - 1: use reg 21h	LOW_BAT	PWRUP_ COMPLETE	HP_ON_P 0: HPH switched off 1: HPH switched on	MIC_ON_P	LIN_ON_P	EN_PWR_SAVE_1	EN_PWR_SAVE_2
22h-2Fh	reserved								

Table 14. I2C Register Overview

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
OTP Register									
10h	ANC_N2	TEST_BIT_5	MICN_VOL_OTP2<6:0> Gain from MICN to QMIC or Mixer = MUTE, -5.625dB...+41.6dB; 127 steps of 0.375dB						
11h	ANC_P2	ALT1_LOCK	MICP_VOL_OTP2<6:0> Gain from MICP to QMIC or Mixer = MUTE, -5.625dB...+41.6dB; 127 steps of 0.375dB						
12h	ANC_N3	TEST_BIT_6	MICN_VOL_OTP3<6:0> Gain from MICN to QMIC or Mixer = MUTE, -5.625dB...+41.6dB; 127 steps of 0.375dB						
13h	ANC_P3	ALT2_LOCK	MICP_VOL_OTP3<6:0> Gain from MICP to QMIC or Mixer = MUTE, -5.625dB...+41.6dB; 127 steps of 0.375dB						
14h	ANC_N4	TEST_BIT_7	MICN_VOL_OTP4<6:0> Gain from MICN to QMIC or Mixer = MUTE, -5.625dB...+41.6dB; 127 steps of 0.375dB						
15h	ANC_P4	ALT3_LOCK	MICP_VOL_OTP4<6:0> Gain from MICP to QMIC or Mixer = MUTE, -5.625dB...+41.6dB; 127 steps of 0.375dB						
17h	PWRUP	SEQ_LOCK	FAST_START<4:0> 0: ~900ms; 0Eh: ~600ms					LIN_AGC_OFF	MIC_AGC_OFF
31h	ANC_MIC	TEST_BIT_2	MIC_VOL_OTP<6:0> Gain from MICP to QMIC or Mixer =MUTE, -5.625dB...+41.6dB; 127 steps of 0.375dB						
32h	MIC_MON	MON_MODE 0: fixed volume 1: adj. volume	MIC_MON_OTP<6:0> Gain from MIC to QMIC or Mixer = MUTE, -5.625dB...+41.6dB; 0.375dB steps, if MON_MODE is set to 0 Gain from MIC to QMIC or Mixer = MUTE, -5.625dB...+41.6dB; 0.375dB steps, adjustable by VOL pin if MON_MODE is set to 1						
33h	AUDIO_SET	VOL_PIN_OFF	VOL_PIN_ MODE 0: potentiometer 1: up/down button	LIN_EN_OTP	MIC_EN_OTP	HP_ON_OTP 0: off 1: on	LIN_MON_ATTEN<2:0> 0: no attenuation; 1..6: LIN_VOL<6:0> shift by -6dB...-36dB 7: MUTE		
34h	GP_OP	HP_MUX_OTP<1:0> 0: MIC; 1: OP1; 2: -; 3: open							OP_ON_OTP
35h	OTP_SYS	MAIN_LOCK 0: write reg 30h.. 35h 1: lock reg 30h..35h	TEST_BIT_3	MON_HP_MUX<1:0> 0: MIC; 1: OP1; 2: -; 3: -				EN_PWR_SAVE_ OTP	I2C_MODE
3Eh	CONFIG_1					EXTBURNCLK			
3Fh	CONFIG_2			TM34	BURNSW	TM_REG34-35	TM_REG30-33	OTP_MODE<1:0> 0: READ; 1: LOAD; 2: WRITE; 3: BURN	

Table 15. MIC_L Register

<table>
<tr><th colspan="3">Name</th><th colspan="2">Base</th><th>Default</th></tr>
<tr><td colspan="3">MIC_CNTR</td><td colspan="2">2-wire serial</td><td>00h</td></tr>
<tr><td colspan="2" rowspan="2">Offset: 08h</td><td colspan="4">Negative Microphone Input Register</td></tr>
<tr><td colspan="4">Configures the gain for the negative microphone input and defines the microphone operation mode. This register is reset at POR.</td></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td>7</td><td>MIC_ON_N</td><td>0</td><td>R/W</td><td colspan="2">Second power up bit for the microphone preamplifier. This bit must be set together with MIC_ON_P bit for proper microphone operation.
0: Off
1: On</td></tr>
</table>

Table 16. MIC_R Register

<table>
<tr><th colspan="3">Name</th><th colspan="2">Base</th><th>Default</th></tr>
<tr><td colspan="3">MIC</td><td colspan="2">2-wire serial</td><td>00h</td></tr>
<tr><td colspan="2" rowspan="2">Offset: 09h</td><td colspan="4">Positive Microphone Input Register</td></tr>
<tr><td colspan="4">Configures the gain for the positive microphone input and enables register 08h & 09h. This register is reset at POR.</td></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td>7</td><td>MIC_REG_ON</td><td>0</td><td>R/W</td><td colspan="2">Defines which registers are used for the microphone settings.
0: settings of register 30h and 31h are used
1: settings of register 08h and 09h are used</td></tr>
<tr><td>6:0</td><td>MICP_VOL<6:0></td><td>000 0000</td><td>R/W</td><td colspan="2">Volume settings for positive microphone input, adjustable in 127 steps of 0.375dB.
00 0000: MUTE
00 0001: -5.625dB gain
00 0010: -5.25 dB gain
..
11 1110: 41.250dB gain
11 1111: 41.625 dB gain</td></tr>
</table>

Table 17. LINE_IN Register

<table>
<tr><th colspan="3">Name</th><th colspan="2">Base</th><th>Default</th></tr>
<tr><td colspan="3">LINE_IN</td><td colspan="2">2-wire serial</td><td>00h</td></tr>
<tr><td colspan="2" rowspan="2">Offset: 0Ah</td><td colspan="4">Line Input Register</td></tr>
<tr><td colspan="4">Configures the attenuation for the line input, defines the line input operation mode and enables register 0Ah. This register is reset at POR.</td></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td>7</td><td>LIN_REG_ON</td><td>0</td><td>R/W</td><td colspan="2">Defines which source is used for the line input settings.
0: settings of register 33h and VOL pin are used
1: register 0Ah is used</td></tr>
</table>

Table 17. LINE_IN Register

Name		Base		Default
LINE_IN		**2-wire serial**		**00h**
Offset: 0Ah		**Line Input Register**		
		Configures the attenuation for the line input, defines the line input operation mode and enables register 0Ah. This register is reset at POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6	LIN_ON_N	0	R/W	This bit is used to switch on the line input amplifier. It has to be set together with LIN_ON_P bit for proper operation of the line input. **0: off** 1: on
5:0	LIN_VOL<5:0>	00 0000	R/W	Volume settings for line input, adjustable in 63 steps of 0.75dB **00 0000: MUTE** 00 0001:-46.5dB gain 00 0010:-45.75dB gain .. 11 1110:-0.75dB gain 11 1111:.0 dB gain

Table 18. GP_OP_L Register

Name		Base		Default
GP_OP_2		**2-wire serial**		**00h**
Offset: 0Bh		**General Purpose Operational Amplifier Register**		
		Enables opamp 2 and sets the HP input multiplexer. This register is reset at POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	HP_MUX<1:0>	00	R/W	Multiplexes the analog audio signal to HP amp **00: MIC: selects QMIC output** 01: OP1: selects QOP1 outputs 10: - : do not use 11: open: no signal mixed together with the line input signal
0	OP2_ON	0	R/W	Enables OP 2 **0: OP2 is switched off** 1: OP2 is enabled

Table 19. GP_OP_R Register

Name		Base		Default
GP_OP_1		**2-wire serial**		**00h**
Offset: 0Ch		**General Purpose Operational Amplifier Register**		
		Enables opamp 1 stage and sets the HP mode. This register is reset at POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	OP_REG_ON	0	R/W	Defines which register is used for the opamp and HP settings. **0: settings of register 33h and 34h are used** 1: register 0B and 0Ch are used
6	HP_ON_N	0	R/W	Controls the inverting amplifier of the headphone amplifier **0: switches HP_N stage off** 1: switches HP_N stage on
0	OP1_ON	0	R/W	Enables OP 1 **0: OP1 is switched off** 1: OP1 is enabled

Table 20. SYSTEM Register

Name			Base	Default
SYSTEM			**2-wire serial**	**31h**
Offset: 20h				**SYSTEM Register** This register is reset at a POR.
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Design_Version<3:0>	0100	R	AFE number to identify the design version 0100: for chip version 1v0
3	TESTREG_ON	0	R/W	0: normal operation 1: enables writing to test register 3Eh & 3Fh to configure the OTP and set the access mode.
2	MONITOR_ON	0	R/W	Enables the monitor mode **0: normal operation** 1: monitor mode enabled
1	CONT_PWRUP	0	R/W	Continues the automatic power-up sequence when using the I2C mode **0: chip stops the power-up sequence after the supplies are stable, switching on individual blocks has to be done via I2C commands** 1: automatic power-up sequence is continued
0	PWR_HOLD	1	R/W	0: power up hold is cleared and AFE will power down **1: is automatically set to on after power on**

Table 21. PWR_SET Register

Name			Base	Default
PWR_SET			**2-wire serial**	**0x11 1111b (stand alone mode)** **0x00 0000b (I2C mode)**
Offset: 21h				**Power Setting Register** Please be aware that writing to this register will enable/disable the corresponding blocks, while reading gets the actual status. This register is reset at POR.
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PWR_REG_ON	0	R/W	Defines which register is used for the power settings. **0: all blocks stay on as defined in the start-up sequence** 1: register 21h is used
6	LOW_BAT	x	R	VBAT supervisor status **0: VBAT is above brown out level** 1: BVDD has reached brown out level
5	PWRUP_COMPLETE	x	R	Power-Up sequencer status **0: power-up sequence incomplete** 1: power-up sequence completed
4	HP_ON_P	0	W	**0: switches HP_P stage off** 1: switches HP_P stage on
		x	R	**0: HP stage not powered** 1: normal operation
3	MIC_ON_P	0	W	**0: switches microphone stage off** 1: switches microphone stage on
		x	R	**0: microphone stage not powered** 1: normal operation
2	LIN_ON_P	0	W	**0: switches line input stage off** 1: switches line input stage on
		x	R	**0: line input stage not powered** 1: normal operation

Table 21. PWR_SET Register

Name			Base	Default
PWR_SET			**2-wire serial**	**0x11 1111b (stand alone mode) 0x00 0000b (I2C mode)**
Offset: 21h		**Power Setting Register** Please be aware that writing to this register will enable/disable the corresponding blocks, while reading gets the actual status. This register is reset at POR.		

Bit	Bit Name	Default	Access	Bit Description
1	EN_PWR_SAVE_1	0	W	It is recommended to enable to power save mode 1 for operation of the device. **0: power save mode disabled** 1: power save mode enabled (recommended setting)
			R	**0: power save mode disabled** 1: power save mode enabled (recommended setting)
0	EN_PWR_SAVE_2	0	W	It is recommended to enable to power save mode 2 for operation of the device. **0: power save mode disabled** 1: power save mode enabled (recommended setting)
		x	R	**0: power save mode disabled** 1: power save mode enabled (recommended setting)

Table 22. ANC_L2 Register

Name		Base		Default
ANC_N2		**2-wire serial**		**80h (OTP)**
Offset: 10h		**Negative OTP Microphone Input Register (2nd OTP option)**		
		Configures the gain for the negative microphone input. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	TEST_BIT_5	1	R	for testing purpose only
6:0	MICL_VOL_OTP2 <6:0>	000 0000	R/W	Volume settings for negative microphone input, adjustable in 127 steps of 0.375dB **00 0000: MUTE** 00 0001: -5.625dB gain 00 0010: -5.25 dB gain .. 11 1110: 41.250dB gain 11 1111: 41.625 dB gain

Table 23. ANC_R2 Register

Name		Base		Default
ANC_P2		**2-wire serial**		**00h (OTP)**
Offset: 11h		**Positive OTP Microphone Input Register (2nd OTP option)**		
		Configures the gain for the positive microphone input. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ALT1_LOCK	0	R/W	**0: additional bits can be fused inside register 10h & 11h** 1: OTP fusing for register 10h & 11h gets locked, no more changes can be done.
6:0	MICR_VOL_OTP2 <6:0>	000 0000	R/W	Volume settings for positive microphone input, adjustable in 127 steps of 0.375dB **00 0000: MUTE** 00 0001: -5.625dB gain 00 0010: -5.25 dB gain .. 11 1110: 41.250dB gain 11 1111: 41.625 dB gain

Table 24. ANC_L3 Register

Name			Base	Default
ANC_N3			**2-wire serial**	**80h (OTP)**
Offset: 12h		**Negative OTP Microphone Input Register (3rd OTP option)**		
		Configures the gain for the negative microphone input. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	TEST_BIT_6	1	R	for testing purpose only
6:0	MICN_VOL_OTP3 <6:0>	000 0000	R/W	Volume settings for negative microphone input, adjustable in 127 steps of 0.375dB **00 0000: MUTE** 00 0001: -5.625dB gain 00 0010: -5.25 dB gain .. 11 1110: 41.250dB gain 11 1111: 41.625 dB gain

Table 25. ANC_R3 Register

Name			Base	Default
ANC_P3			**2-wire serial**	**00h (OTP)**
Offset: 13h		**Positive OTP Microphone Input Register (3rd OTP option)**		
		Configures the gain for the positive microphone input. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ALT2_LOCK	0	R/W	**0: additional bits can be fused inside register 12h & 13h** 1: OTP fusing for register 12h & 13h gets locked, no more changes can be done.
6:0	MICP_VOL_OTP3 <6:0>	000 0000	R/W	Volume settings for positive microphone input, adjustable in 127 steps of 0.375dB **00 0000: MUTE** 00 0001: -5.625dB gain 00 0010: -5.25 dB gain .. 11 1110: 41.250dB gain 11 1111: 41.625 dB gain

Table 26. ANC_L4 Register

Name		Base		Default
ANC_N4		**2-wire serial**		**80h (OTP)**
Offset: 14h		**Negative OTP Microphone Input Register (4th OTP option)**		
		Configures the gain for the negative microphone input. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	TEST_BIT_7	1	R	for testing purpose only
6:0	MICL_VOL_OTP4 <6:0>	000 0000	R/W	Volume settings for negative microphone input, adjustable in 127 steps of 0.375dB **00 0000: MUTE** 00 0001: -5.625dB gain 00 0010: -5.25 dB gain .. 11 1110: 41.250dB gain 11 1111: 41.625 dB gain

Table 27. ANC_R4 Register

Name		Base		Default
ANC_P4		**2-wire serial**		**00h (OTP)**
Offset: 15h		**Positive OTP Microphone Input Register (4th OTP option)**		
		Configures the gain for the positive microphone input. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ALT3_LOCK	0	R/W	**0: additional bits can be fused inside register 14h & 15h** 1: OTP fusing for register 14h & 15h gets locked, no more changes can be done.
6:0	MICP_VOL_OTP4 <6:0>	000 0000	R/W	Volume settings for positive microphone input, adjustable in 127 steps of 0.375dB **00 0000: MUTE** 00 0001: -5.625dB gain 00 0010: -5.25 dB gain .. 11 1110: 41.250dB gain 11 1111: 41.625 dB gain

Table 28. PWRUP_CNTR Register

Name	Base	Default
PWRUP_CNTR	**2-wire serial**	**00h (OTP)**

Offset: 17h	**PowerUp Control Register** Configures chip start-up speed. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.

Bit	Bit Name	Default	Access	Bit Description
7	SEQ_LOCK	0	R/W	**0: additional bits can be fused inside register 16h & 17h** 1: OTP fusing for register 16h & 17h gets locked, no more changes can be done.
6:2	FAST_START <4:0>	0 0000	R/W	**0h: ~900ms start-up time** 0Eh: ~600ms start-up time
1	LIN_AGC_OFF	0	R/W	**0: Line Input AGC enabled** 1: Line Input AGC switched off
0	MIC_AGC_OFF	0	R/W	**0:Microphone Input AGC enabled** 1: Microphone Input AGC switched off

Table 29. ANC_MIC Register

Name				Base	Default
ANC_MIC				**2-wire serial**	**80h (OTP)**
Offset: 31h		**Positive OTP Microphone Input Register**			
		Configures the gain for the microphone input. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7	TEST_BIT_2	1	R	for testing purpose only	
6:0	MIC_VOL_OTP <6:0>	000 0000	R/W	Volume settings for microphone input, adjustable in 127 steps of 0.375dB. **00 0000: MUTE** 00 0001: -5.625dB gain 00 0010: -5.25 dB gain .. 11 1110: 41.250dB gain 11 1111: 41.625 dB gain	

Table 30. MIC_MON Register

Name				Base	Default
MIC_MON				**2-wire serial**	**00h (OTP)**
Offset: 32h		**OPT Microphone Monitor Mode Register**			
		Configures the gain for the microphone input in monitor mode. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7	MON_MODE	0	R/W	**0: monitor mode is working with fixed microphone gain** 1: monitor mode uses adjustable gain via the VOL pin	
6:0	MIC_MON_OTP <6:0>	000 0000	R/W	Volume settings for microphone input during monitor mode, adjustable in 127 steps of 0.375dB. If MON_MODE bit is set to 1 the gain can be further adjusted via the VOL pin. **00 0000: MUTE** 00 0001: -5.625dB gain 00 0010: -5.25 dB gain .. 11 1110: 41.250dB gain 11 1111: 41.625 dB gain	

Table 31. AUDIO_SET Register

Name				Base	Default
AUDIO_SET				**2-wire serial**	**00h (OTP)**
Offset: 33h				**OPT Audio Setting Register**	
				Configures the audio settings. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.	
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7	VOL_PIN_OFF	0	R/W	**0: VOL pin is enabled** 1: line in volume settings can only be done via I2C. VOL_PIN_MODE has to be set to 1 in this mode.	
6	VOL_PIN_MODE	0	R/W	**0: VOL pin is in potentiometer mode** 1: VOL pin is in up/down button mode	
5	LIN_EN_OTP	0	R/W	**0: line input disabled** 1: line input enabled	
4	MIC_EN_OTP	0	R/W	**0: microphone input stage disabled** 1: normal operating in mono balanced	
3	HP_ON_OTP	0	R/W	This bit must always be enabled for proper operation of the headphone amplifier. **0: headphone stage not powered** 1: headphone stage powered	
2:0	LIN_MON_ATTEN <6:0>	000	R/W	Volume settings for line input during monitor mode, adjustable in 7 steps of 6dB and mute. **000: 0dB gain** 001: -6dB gain .. 110: -36dB gain 111: MUTE	

Table 32. GP_OP Register

Name	Base	Default
GP_OP	**2-wire serial**	**00h (OTP)**

Offset	Description
Offset: 34h	**OTP General Purpose Operational Amplifier Register** Enables the opamp stages, defines opamp 2 mode and gain and sets the HP input multiplexer. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.

Bit	Bit Name	Default	Access	Bit Description
7:6	HP_MUX_OTP<1:0>	00	R/W	Multiplexes the analog audio signal to HP amp **00: MIC: selects QMIC output** 01:OP1: selects QOP1 output 10: - : do not use 11: open: no signal mixed together with the line input signal
0	OP_ON	0	R/W	**0: OP1 and OP2 are switched off** 1: OP1 and OP2 are enabled

Table 33. OTP_SYS Register

Name	Base	Default
OTP_SYS	**2-wire serial**	**40h (OTP)**

Offset	Description
Offset: 35h	**OTP System Settings Register** Defines several system settings for OTP operation. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.

Bit	Bit Name	Default	Access	Bit Description
7	MAIN_LOCK	0	R/W	**0: additional bits can be fused inside the OTP** 1: OTP fusing gets locked, no more changes can be done
6	TEST_BIT_3	1	R	for testing purpose only
5:4	MON_HP_MUX <1:0>	00	R/W	Multiplexes the analog audio signal to HP amp in monitor mode **00: MIC: selects QMICL/R output** 01: OP1: selects QOP1L/R outputs 10: - : do not use 11: open: no signal mixed together with the line input signal
1	EN_PWR_SAVE_OTP	0	R/W	This bit must be set to ‘1’ for power savings. **0: Power savings disabled** 1: Power savings enabled (This setting must be used)
0	I2C	0	R/W	**0: I2C and stand alone mode start-up possible** 1: chip starts-up in I2C mode only

Table 34. CONFIG_1 Register

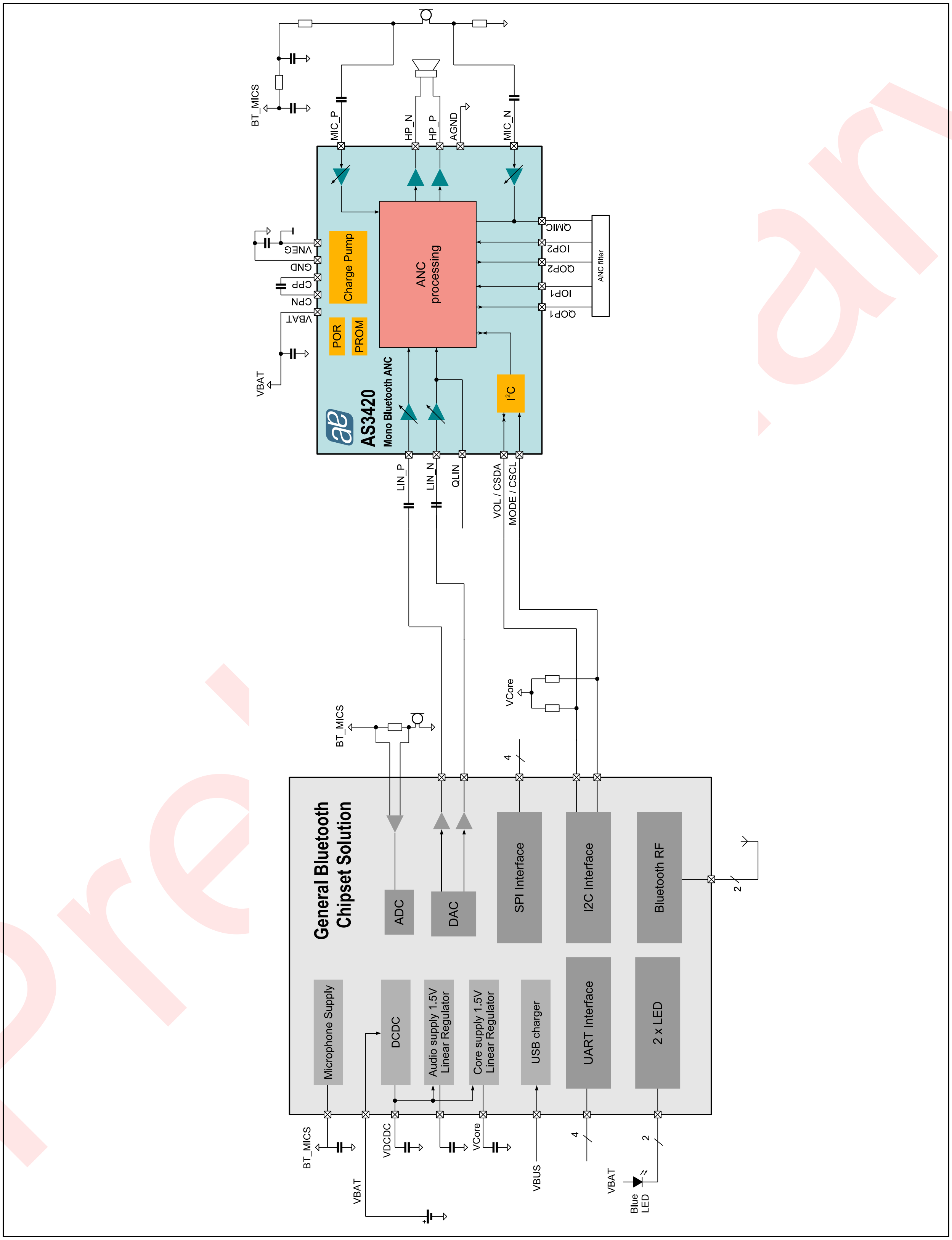
Name		Base	Default	
CONFIG_1		**2-wire serial**	**00h**	
Offset: 3Eh		**OTP Configuration Register** Controls the clock configuration. This is a special register, writing needs to be enabled by writing 9h to Reg 20h first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	-	0000	n/a	
3	EXTBURNCLK	0	n/a	**0: ext. clock for OTP burning disabled** 1: ext. clock for OTP burning enabled
2:0	-	000	n/a	

Table 35. CONFIG_2 Register

Name		Base	Default	
CONFIG_2		**2-wire serial**	**00h**	
Offset: 3Fh		**OTP Access Configuration Register** Controls the OTP access. This is a special register, writing needs to be enabled by writing 9h to Reg 20h first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	-	000	n/a	
5	TM34	0	n/a	This Register defines the Register bank selection for Register TM_REG34-35 and TMREG30-33. Depending on TM34 you can select either between Register bank 14h-17h and 10h-13h enabled or 30h-33h and 34h-37h enabled. **0: test mode Registers 14h-17h and 10h-13h disabled** **test mode Registers 30h-33h and 34h-37h enabled** 1: test mode Registers 14h-17h and 10h-13h enabled test mode Registers 30h-33h and 34h-37h disabled
4	BURNSW	0	n/a	**0: BURN switch from LINL to VNEG is disabled** 1: BURN switch from LINL to VNEG is enabled
3	TM_REG34-35	0	n/a	**0: test mode for Register 34h-35h disabled** **test mode for Register 14h-17h disabled** 1: test mode for Register 34h-35h enabled test mode for Register 14h-17h enabled
2	TM_REG30-33	0	n/a	**0: test mode for Register 30h-33h disabled** **test mode for Register 10h-13h disabled** 1: test mode for Register 30h-33h enabled test mode for Register 10h-13h enabled
1:0	OTP_MODE<1:0>	00	R/W	Controls the OTP access **00: READ** 01: LOAD 10: WRITE 11: BURN

10 Application Information

Figure 30. AS3420 Mono Bluetooth Feed Forward Application Example



11 Package Drawings and Marking

Figure 31. QFN Marking

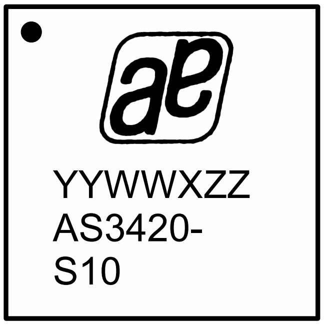
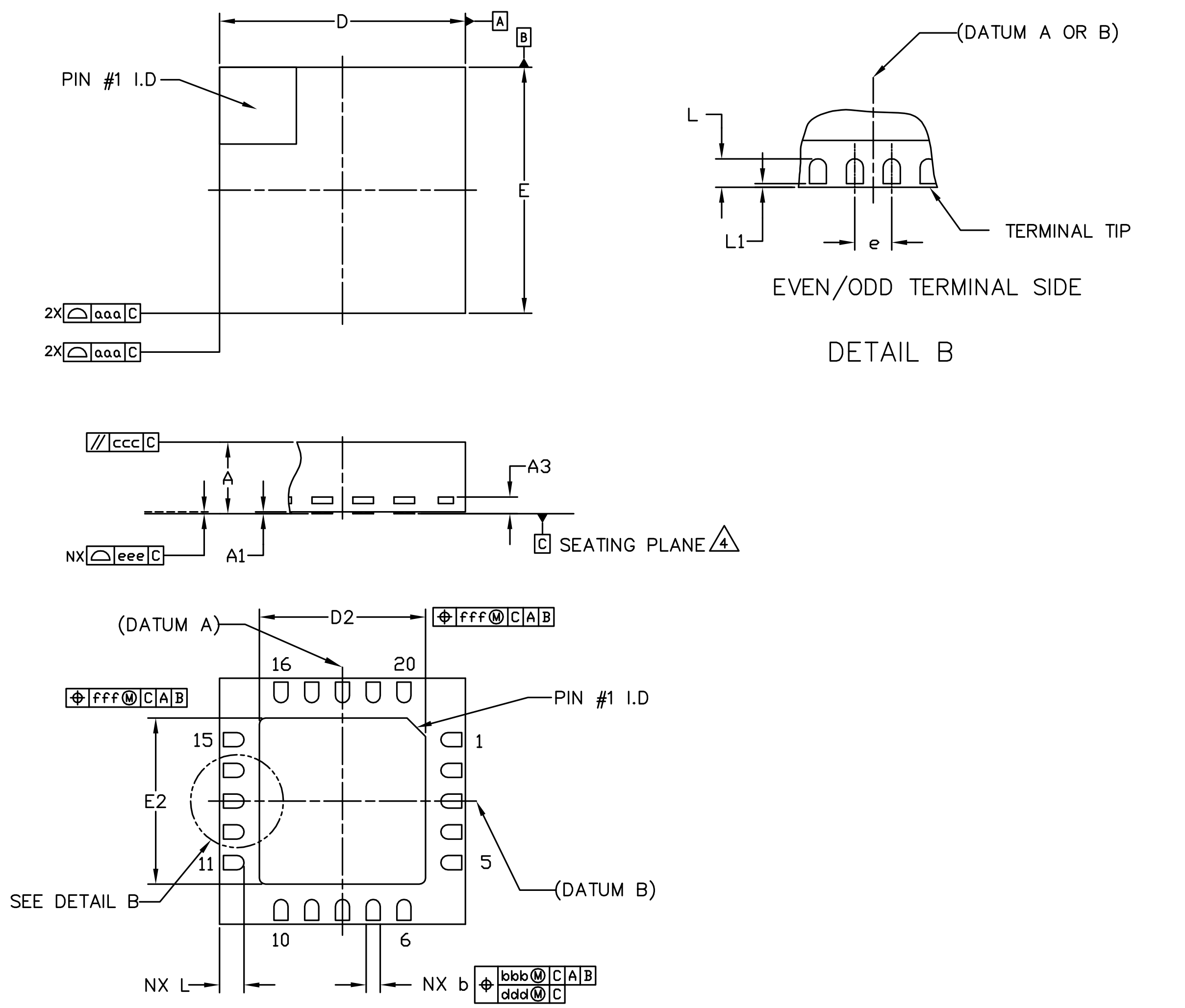


Table 36. Package Code YYWWIZZ

YY	WW	X	ZZ
last two digits of the year	manufacturing week	plant identifier	free choice / traceability code

Figure 32. AS3420 20-pin QFN (4x4mm) 0.5mm Pitch



REF.	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20 REF	
L	0.35	0.40	0.45
L1	0	–	0.15
b	0.18	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
aaa	–	0.15	–
bbb	–	0.10	–
ccc	–	0.10	–
ddd	–	0.05	–
eee	–	0.08	–
fff	–	0.10	–
N		20	

NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.15mm IS ACCEPTABLE.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
5. RADIUS ON TERMINAL IS OPTIONAL.
6. N IS THE TOTAL NUMBER OF TERMINALS.

Revision History

Revision	Date	Owner	Description
0.1	09.2.2011	hgt	initial release
0.2	10.10.2011	hgt	updated audio measurements

Note: Typos may not be explicitly mentioned under revision history.

12 Ordering Information

The devices are available as the standard products shown in Table 37.

Table 37. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS3420-EQFP	Mono Bluetooth Noise-Cancelling Speaker Driver	Tape & Reel dry pack	QFN 20 [4.0x4.0x0.9mm] 0.5mm pitch
AS3420-EQFP-500	Mono Bluetooth Noise-Cancelling Speaker Driver	Tape & Reel dry pack	QFN 20 [4.0x4.0x0.9mm] 0.5mm pitch

Note: All products are RoHS compliant and austriamicrosystems green.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

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or find your local distributor at http://www.austriamicrosystems.com/distributor

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