



## 256K X 8 BIT LOW POWER CMOS SRAM

**FEATURES**

- Fast access time : 55ns
- Low power consumption:  
Operating current : 20/18mA (TYP.)  
Standby current : 2μA (TYP.)
- Single 2.7V ~ 5.5V power supply
- All outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Lead free and green package available**
- Package : 32-pin 8mm x 20mm TSOP-I  
32-pin 8mm x 13.4mm STSOP  
32-pin 450 mil SOP  
32-pin 600 mil P-DIP  
36-ball 6mm x 8mm TFBGA

**GENERAL DESCRIPTION**

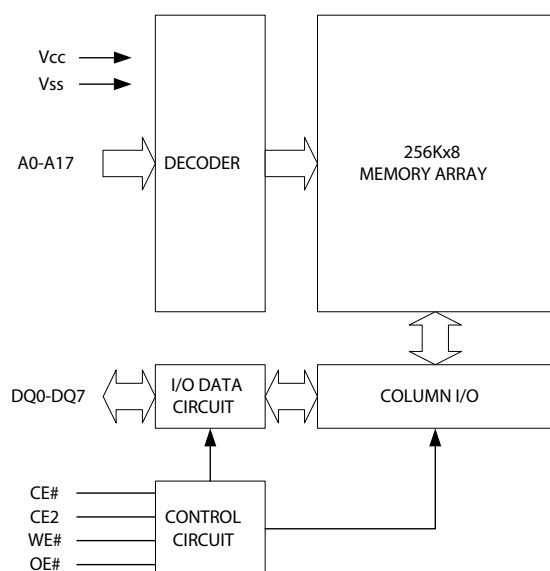
The AS6C2008A is a 2,097,152-bit low power CMOS static random access memory organized as 262,144 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C2008A is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C2008A operates from a single power supply of 2.7V ~ 5.5V and all outputs are fully TTL compatible

**PRODUCT FAMILY**

| Product Family | Operating Temperature | Vcc Range  | Speed | Power Dissipation  |                     |
|----------------|-----------------------|------------|-------|--------------------|---------------------|
|                |                       |            |       | Standby(Isb1,TYP.) | Operating(Icc,TYP.) |
| AS6C2008A(LLI) | -40 ~ 85°C            | 2.7 ~ 5.5V | 55ns  | 2μA(LL)            | 20/18mA             |

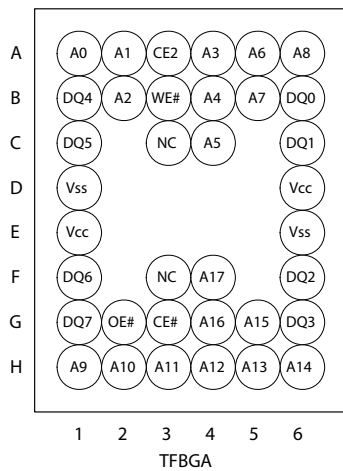
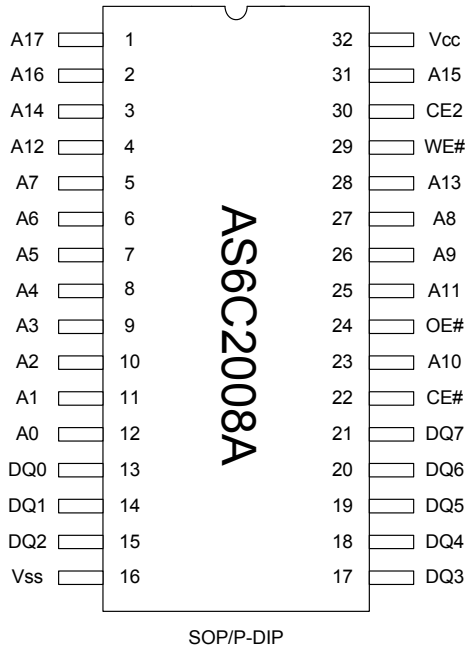
**FUNCTIONAL BLOCK DIAGRAM****PIN DESCRIPTION**

| SYMBOL    | DESCRIPTION         |
|-----------|---------------------|
| A0 - A17  | Address Inputs      |
| DQ0 – DQ7 | Data Inputs/Outputs |
| CE#, CE2  | Chip Enable Inputs  |
| WE#       | Write Enable Input  |
| OE#       | Output Enable Input |
| Vcc       | Power Supply        |
| Vss       | Ground              |
| NC        | No Connection       |



## 256K X 8 BIT LOW POWER CMOS SRAM

## PIN CONFIGURATION





## 256K X 8 BIT LOW POWER CMOS SRAM

**ABSOLUTE MAXIMUM RATINGS\***

| PARAMETER                                              | SYMBOL              | RATING                       | UNIT |
|--------------------------------------------------------|---------------------|------------------------------|------|
| Voltage on V <sub>CC</sub> relative to V <sub>SS</sub> | V <sub>T1</sub>     | -0.5 to 6.5                  | V    |
| Voltage on any other pin relative to V <sub>SS</sub>   | V <sub>T2</sub>     | -0.5 to V <sub>CC</sub> +0.5 | V    |
| Operating Temperature                                  | T <sub>A</sub>      | -40 to 85(I grade)           | °C   |
| Storage Temperature                                    | T <sub>STG</sub>    | -65 to 150                   | °C   |
| Power Dissipation                                      | P <sub>D</sub>      | 1                            | W    |
| DC Output Current                                      | I <sub>OUT</sub>    | 50                           | mA   |
| Soldering Temperature (under 10 sec)                   | T <sub>SOLDER</sub> | 260                          | °C   |

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

| MODE           | CE# | CE2 | OE# | WE# | I/O OPERATION    | SUPPLY CURRENT                     |
|----------------|-----|-----|-----|-----|------------------|------------------------------------|
| Standby        | H   | X   | X   | X   | High-Z           | I <sub>SB1</sub>                   |
|                | X   | L   | X   | X   | High-Z           | I <sub>SB1</sub>                   |
| Output Disable | L   | H   | H   | H   | High-Z           | I <sub>CC</sub> , I <sub>CC1</sub> |
| Read           | L   | H   | L   | H   | D <sub>OUT</sub> | I <sub>CC</sub> , I <sub>CC1</sub> |
| Write          | L   | H   | X   | L   | D <sub>IN</sub>  | I <sub>CC</sub> , I <sub>CC1</sub> |

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.



## 256K X 8 BIT LOW POWER CMOS SRAM

**DC ELECTRICAL CHARACTERISTICS**

| PARAMETER                              | SYMBOL                       | TEST CONDITION                                                                                                                         | MIN.                 | TYP. <sup>4</sup> | MAX.                 | UNIT |
|----------------------------------------|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|----------------------|-------------------|----------------------|------|
| Supply Voltage                         | V <sub>CC</sub>              |                                                                                                                                        | 2.7                  | 3.0               | 5.5                  | V    |
| Input High Voltage                     | V <sub>IH</sub> <sup>1</sup> |                                                                                                                                        | 0.7* V <sub>CC</sub> | -                 | V <sub>CC</sub> +0.3 | V    |
| Input Low Voltage                      | V <sub>IL</sub> <sup>2</sup> |                                                                                                                                        | - 0.2                | -                 | 0.6                  | V    |
| Input Leakage Current                  | I <sub>LI</sub>              | V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>                                                                                    | - 1                  | -                 | 1                    | μA   |
| Output Leakage Current                 | I <sub>LO</sub>              | V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> ,<br>Output Disabled                                                              | - 1                  | -                 | 1                    | μA   |
| Output High Voltage                    | V <sub>OH</sub>              | I <sub>OH</sub> = -1mA                                                                                                                 | 2.4                  | 2.7               | -                    | V    |
| Output Low Voltage                     | V <sub>OL</sub>              | I <sub>OL</sub> = 2mA                                                                                                                  | -                    | -                 | 0.4                  | V    |
| Average Operating Power supply Current | I <sub>CC</sub>              | Cycle time = Min., I <sub>I/O</sub> = 0mA<br>CE# = 0.2V and CE2 = V <sub>CC</sub> -0.2V<br>other pins at 0.2V or V <sub>CC</sub> -0.2V | - 55                 | 20                | 60                   | mA   |
|                                        |                              |                                                                                                                                        | - 70                 | 18                | 50                   | mA   |
|                                        | I <sub>CC1</sub>             | Cycle time = 1μs, I <sub>I/O</sub> = 0mA<br>CE# ≤ 0.2V and CE2 ≥ V <sub>CC</sub> -0.2V,<br>other pins at 0.2V or V <sub>CC</sub> -0.2V | -                    | 4                 | 10                   | mA   |
| Standby Power Supply Current           | I <sub>SB1</sub>             | CE# ≥ V <sub>CC</sub> -0.2V<br>or CE2 ≤ 0.2V<br>other pins at 0.2V or V <sub>CC</sub> -0.2V                                            | -                    | 2                 | 50                   | μA   |

Notes:

1. V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
2. V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C

**CAPACITANCE (T<sub>A</sub> = 25°C f = 1.0MHz)**

| PARAMETER                | SYMBOL           | MIN. | MAX | UNIT |
|--------------------------|------------------|------|-----|------|
| Input Capacitance        | C <sub>IN</sub>  | -    | 6   | pF   |
| Input/Output Capacitance | C <sub>I/O</sub> | -    | 8   | pF   |

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

|                                          |                                                                           |
|------------------------------------------|---------------------------------------------------------------------------|
| Input Pulse Levels                       | 0.2V to V <sub>CC</sub> - 0.2V                                            |
| Input Rise and Fall Times                | 3ns                                                                       |
| Input and Output Timing Reference Levels | 1.5V                                                                      |
| Output Load                              | C <sub>L</sub> = 30pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> = -2mA/4mA |



## 256K X 8 BIT LOW POWER CMOS SRAM

**AC ELECTRICAL CHARACTERISTICS****(1) READ CYCLE**

| PARAMETER                          | SYM.               | AS6C2008A-55 |      | UNIT |
|------------------------------------|--------------------|--------------|------|------|
|                                    |                    | MIN.         | MAX. |      |
| Read Cycle Time                    | t <sub>RC</sub>    | 55           | -    | ns   |
| Address Access Time                | t <sub>AA</sub>    | -            | 55   | ns   |
| Chip Enable Access Time            | t <sub>ACE</sub>   | -            | 55   | ns   |
| Output Enable Access Time          | t <sub>OE</sub>    | -            | 30   | ns   |
| Chip Enable to Output in Low-Z     | t <sub>CLZ</sub> * | 10           | -    | ns   |
| Output Enable to Output in Low-Z   | t <sub>OLZ</sub> * | 5            | -    | ns   |
| Chip Disable to Output in High-Z   | t <sub>CHZ</sub> * | -            | 20   | ns   |
| Output Disable to Output in High-Z | t <sub>OHZ</sub> * | -            | 20   | ns   |
| Output Hold from Address Change    | t <sub>OH</sub>    | 10           | -    | ns   |

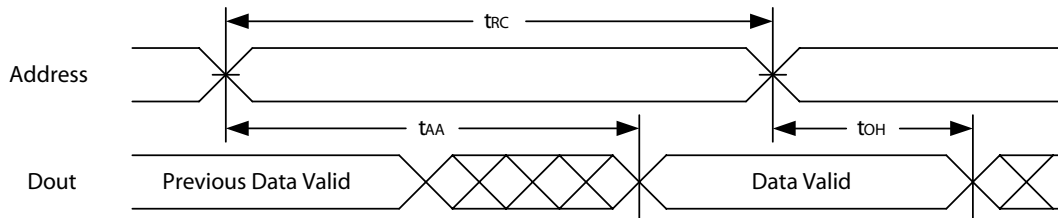
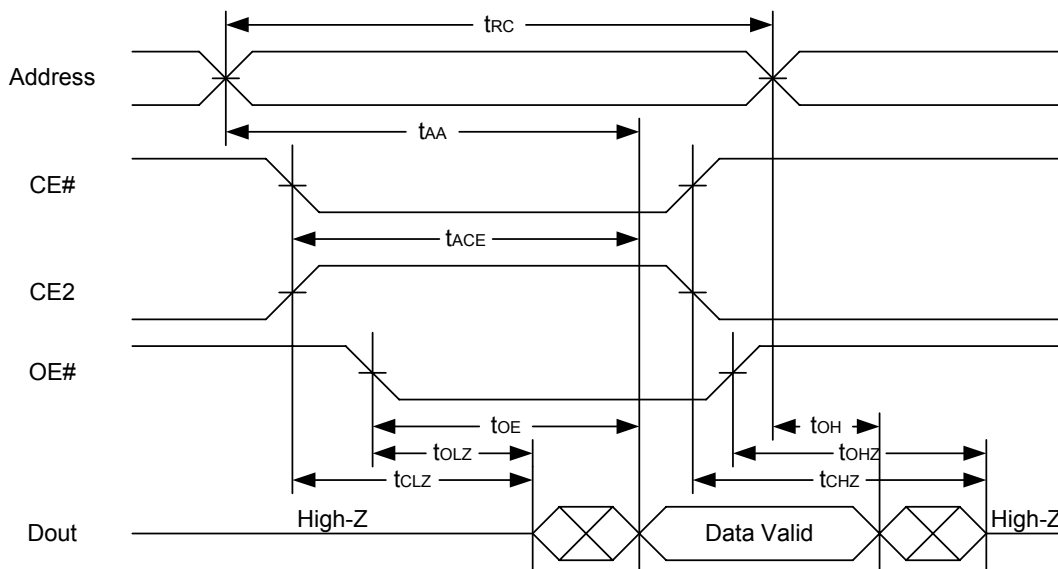
**(2) WRITE CYCLE**

| PARAMETER                        | SYM.               | AS6C2008A-55 |      | UNIT |
|----------------------------------|--------------------|--------------|------|------|
|                                  |                    | MIN.         | MAX. |      |
| Write Cycle Time                 | t <sub>WC</sub>    | 55           | -    | ns   |
| Address Valid to End of Write    | t <sub>AW</sub>    | 50           | -    | ns   |
| Chip Enable to End of Write      | t <sub>CW</sub>    | 50           | -    | ns   |
| Address Set-up Time              | t <sub>AS</sub>    | 0            | -    | ns   |
| Write Pulse Width                | t <sub>WP</sub>    | 45           | -    | ns   |
| Write Recovery Time              | t <sub>WR</sub>    | 0            | -    | ns   |
| Data to Write Time Overlap       | t <sub>DW</sub>    | 25           | -    | ns   |
| Data Hold from End of Write Time | t <sub>DH</sub>    | 0            | -    | ns   |
| Output Active from End of Write  | t <sub>OW</sub> *  | 5            | -    | ns   |
| Write to Output in High-Z        | t <sub>WHZ</sub> * | -            | 20   | ns   |

\*These parameters are guaranteed by device characterization, but not production tested.



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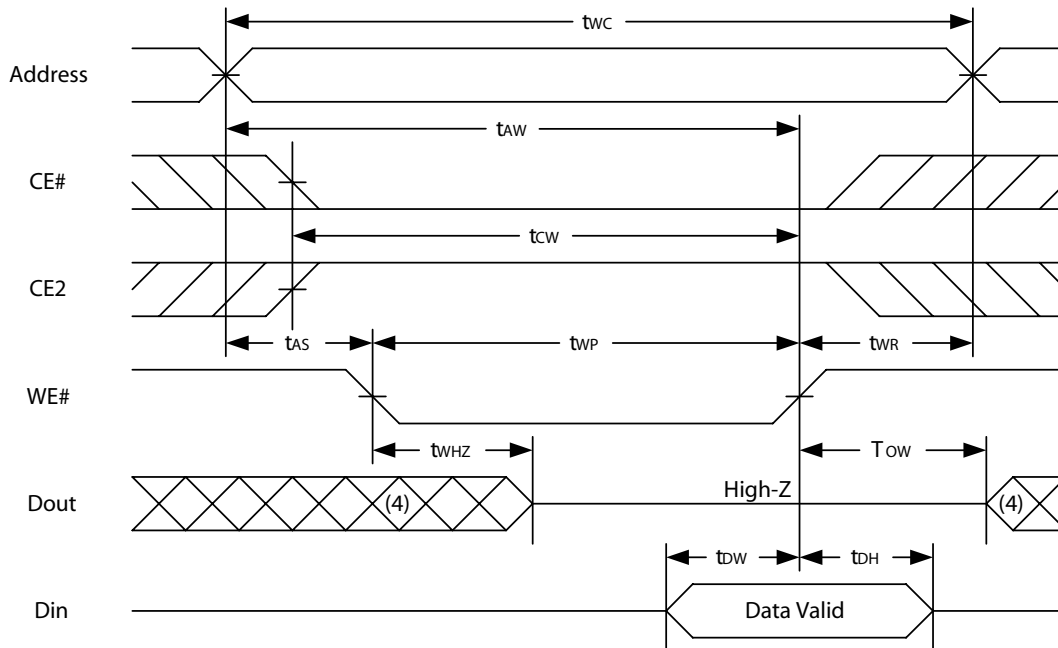
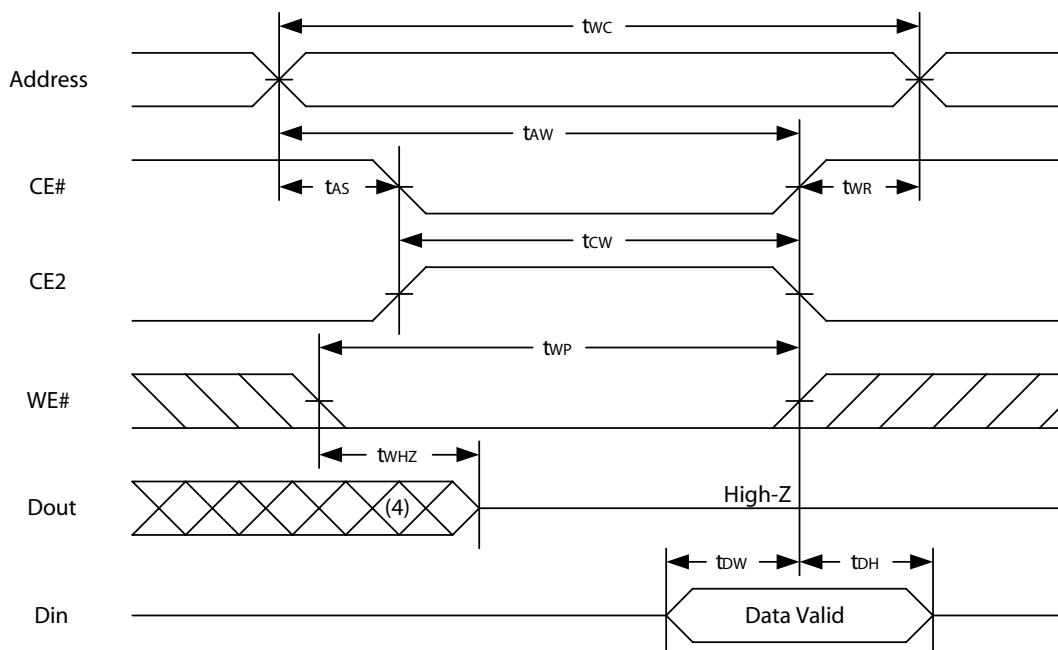
**TIMING WAVEFORMS****READ CYCLE 1 (Address Controlled) (1,2)****READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)**

## Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise tAA is the limiting parameter.
4. tCLZ, tOLZ, tCHZ and tOHZ are specified with  $C_L = 5\text{pF}$ . Transition is measured  $\pm 500\text{mV}$  from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tOHZ is less than tOLZ.



## 256K X 8 BIT LOW POWER CMOS SRAM

**WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)****WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)****Notes :**

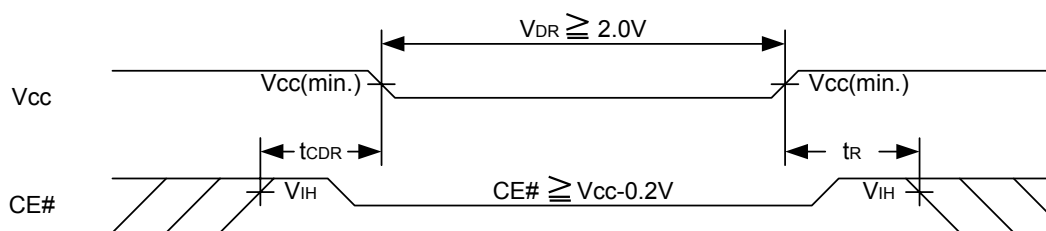
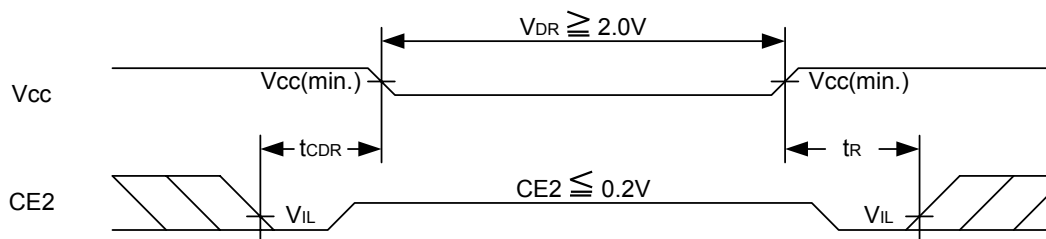
1. WE#, CE# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#.
3. During a WE#-controlled write cycle with OE# low,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{DW}$  to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.



## 256K X 8 BIT LOW POWER CMOS SRAM

**DATA RETENTION CHARACTERISTICS**

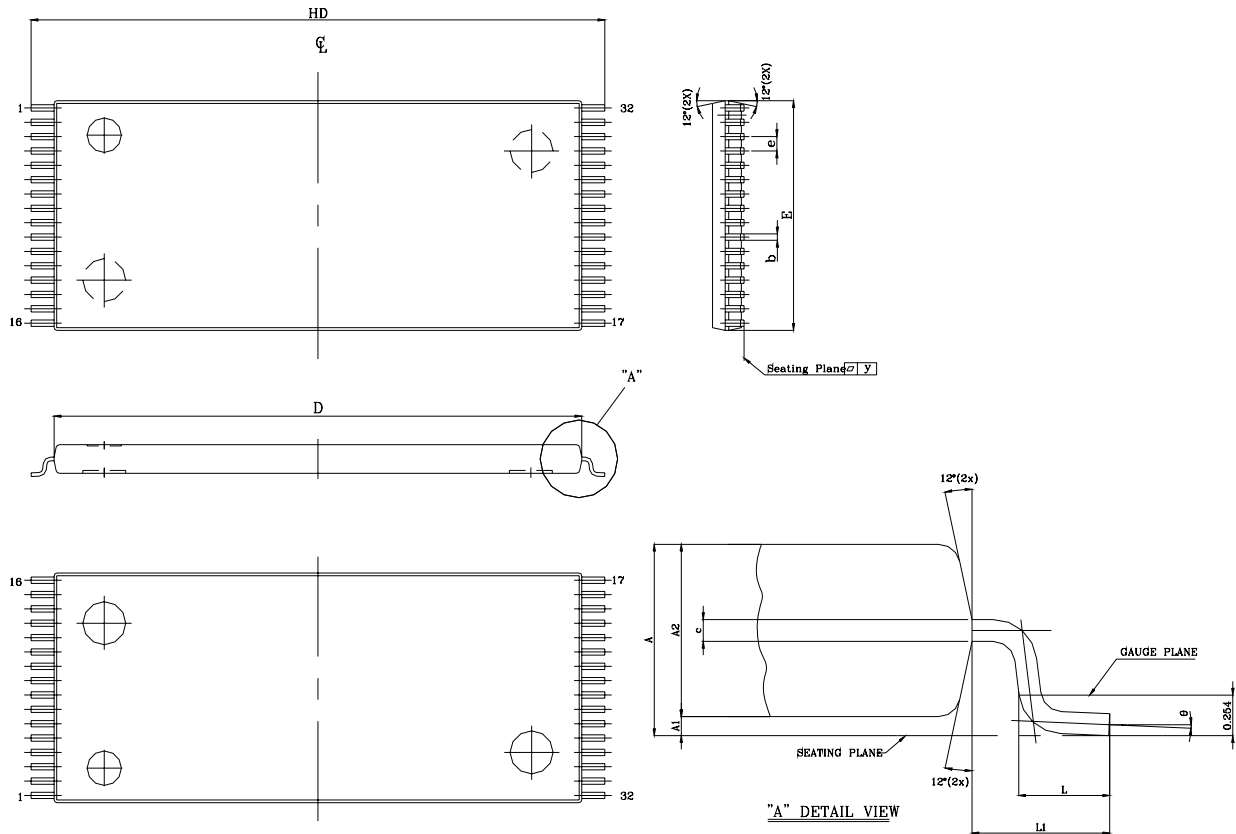
| PARAMETER                           | SYMBOL           | TEST CONDITION                                                                                                                   | MIN.             | TYP. | MAX. | UNIT    |
|-------------------------------------|------------------|----------------------------------------------------------------------------------------------------------------------------------|------------------|------|------|---------|
| V <sub>CC</sub> for Data Retention  | V <sub>DR</sub>  | CE# $\geq$ V <sub>CC</sub> - 0.2V<br>or CE2 $\leq$ 0.2V                                                                          | 2.0              | -    | 5.5  | V       |
| Data Retention Current              | I <sub>DR</sub>  | V <sub>CC</sub> = 2.0V<br>CE# $\geq$ V <sub>CC</sub> - 0.2V<br>or CE2 $\leq$ 0.2V<br>other pins at 0.2V or V <sub>CC</sub> -0.2V | -                | 0.5  | 20   | $\mu$ A |
| Chip Disable to Data Retention Time | t <sub>CDR</sub> | See Data Retention Waveforms (below)                                                                                             | 0                | -    | -    | ns      |
| Recovery Time                       | t <sub>R</sub>   |                                                                                                                                  | t <sub>RC*</sub> | -    | -    | ns      |

t<sub>RC\*</sub> = Read Cycle Time**DATA RETENTION WAVEFORM****Low V<sub>CC</sub> Data Retention Waveform (1)** (CE# controlled)**Low V<sub>CC</sub> Data Retention Waveform (2)** (CE2 controlled)





## 256K X 8 BIT LOW POWER CMOS SRAM

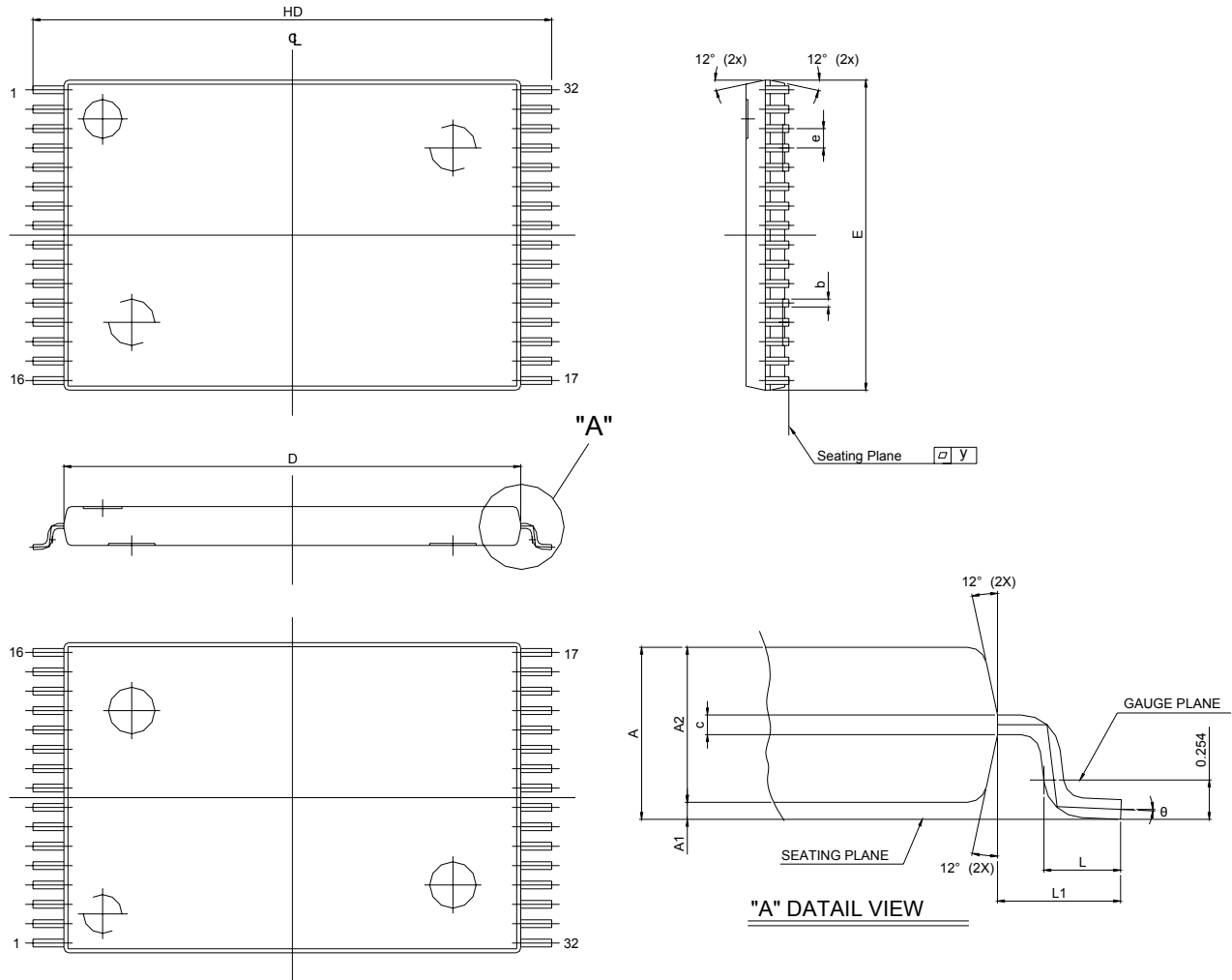
**PACKAGE OUTLINE DIMENSION****32 pin 8mm x 20mm TSOP-I Package Outline Dimension**

| SYM.     | UNIT | INCH(BASE)               | MM(REF)               |
|----------|------|--------------------------|-----------------------|
| A        |      | 0.047 (MAX)              | 1.20 (MAX)            |
| A1       |      | 0.004 $\pm$ 0.002        | 0.10 $\pm$ 0.05       |
| A2       |      | 0.039 $\pm$ 0.002        | 1.00 $\pm$ 0.05       |
| b        |      | 0.008 + 0.002<br>- 0.001 | 0.20 + 0.05<br>- 0.03 |
| c        |      | 0.005 (TYP)              | 0.127 (TYP)           |
| D        |      | 0.724 $\pm$ 0.004        | 18.40 $\pm$ 0.10      |
| E        |      | 0.315 $\pm$ 0.004        | 8.00 $\pm$ 0.10       |
| e        |      | 0.020 (TYP)              | 0.50 (TYP)            |
| HD       |      | 0.787 $\pm$ 0.008        | 20.00 $\pm$ 0.20      |
| L        |      | 0.0197 $\pm$ 0.004       | 0.50 $\pm$ 0.10       |
| L1       |      | 0.0315 $\pm$ 0.004       | 0.08 $\pm$ 0.10       |
| y        |      | 0.003 (MAX)              | 0.076 (MAX)           |
| $\theta$ |      | 0° ~ 5°                  | 0° ~ 5°               |



## 256K X 8 BIT LOW POWER CMOS SRAM

## 32 pin 8mm x 13.4mm STSOP Package Outline Dimension

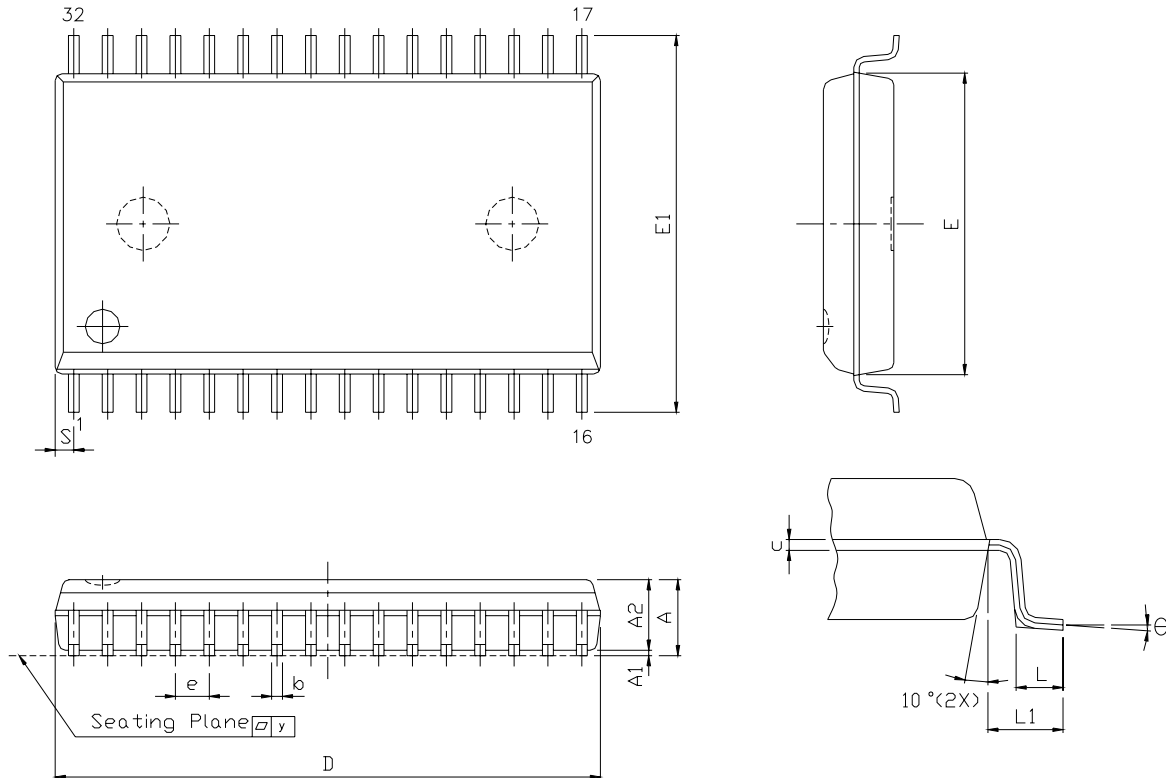


| SYM. \ UNIT | INCH(BASE)    | MM(REF)      |
|-------------|---------------|--------------|
| A           | 0.049 (MAX)   | 1.25 (MAX)   |
| A1          | 0.005 ±0.002  | 0.130 ±0.05  |
| A2          | 0.039 ±0.002  | 1.00 ±0.05   |
| b           | 0.008 ±0.01   | 0.20±0.025   |
| c           | 0.005 (TYP)   | 0.127 (TYP)  |
| D           | 0.465 ±0.004  | 11.80 ±0.10  |
| E           | 0.315 ±0.004  | 8.00 ±0.10   |
| e           | 0.020 (TYP)   | 0.50 (TYP)   |
| HD          | 0.528±0.008   | 13.40 ±0.20. |
| L           | 0.0197 ±0.004 | 0.50 ±0.10   |
| L1          | 0.0315 ±0.004 | 0.8 ±0.10    |
| y           | 0.003 (MAX)   | 0.076 (MAX)  |
| θ           | 0°~5°         | 0°~5°        |



## 256K X 8 BIT LOW POWER CMOS SRAM

## 32 pin 450 mil SOP Package Outline Dimension

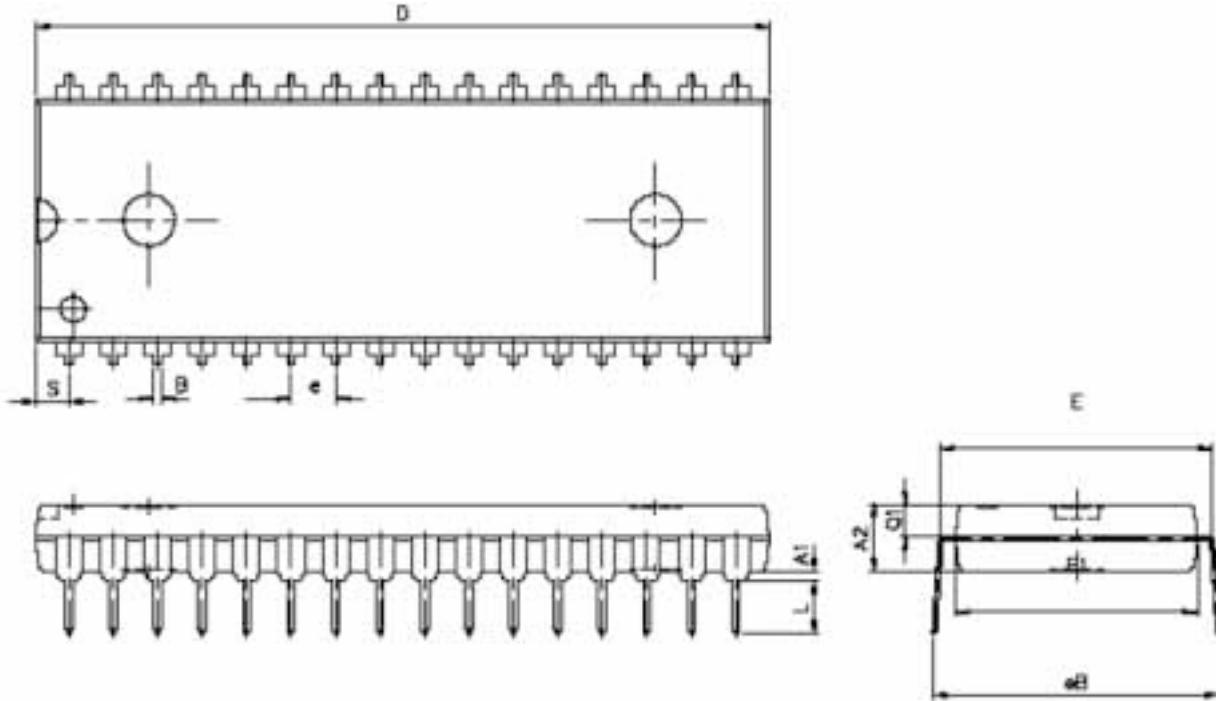


| SYM. \ UNIT | INCH.(BASE)        | MM(REF)            |
|-------------|--------------------|--------------------|
| A           | 0.118 (MAX)        | 2.997 (MAX)        |
| A1          | 0.004(MIN)         | 0.102(MIN)         |
| A2          | 0.111(MAX)         | 2.82(MAX)          |
| b           | 0.016(TYP)         | 0.406(TYP)         |
| c           | 0.008(TYP)         | 0.203(TYP)         |
| D           | 0.817(MAX)         | 20.75(MAX)         |
| E           | 0.445 $\pm$ 0.005  | 11.303 $\pm$ 0.127 |
| E1          | 0.555 $\pm$ 0.012  | 14.097 $\pm$ 0.305 |
| e           | 0.050(TYP)         | 1.270(TYP)         |
| L           | 0.0347 $\pm$ 0.008 | 0.881 $\pm$ 0.203  |
| L1          | 0.055 $\pm$ 0.008  | 1.397 $\pm$ 0.203  |
| S           | 0.026(MAX)         | 0.660 (MAX)        |
| y           | 0.004(MAX)         | 0.101(MAX)         |
| $\theta$    | 0° -10°            | 0° -10°            |



## 256K X 8 BIT LOW POWER CMOS SRAM

## 32 pin 600 mil P-DIP Package Outline Dimension



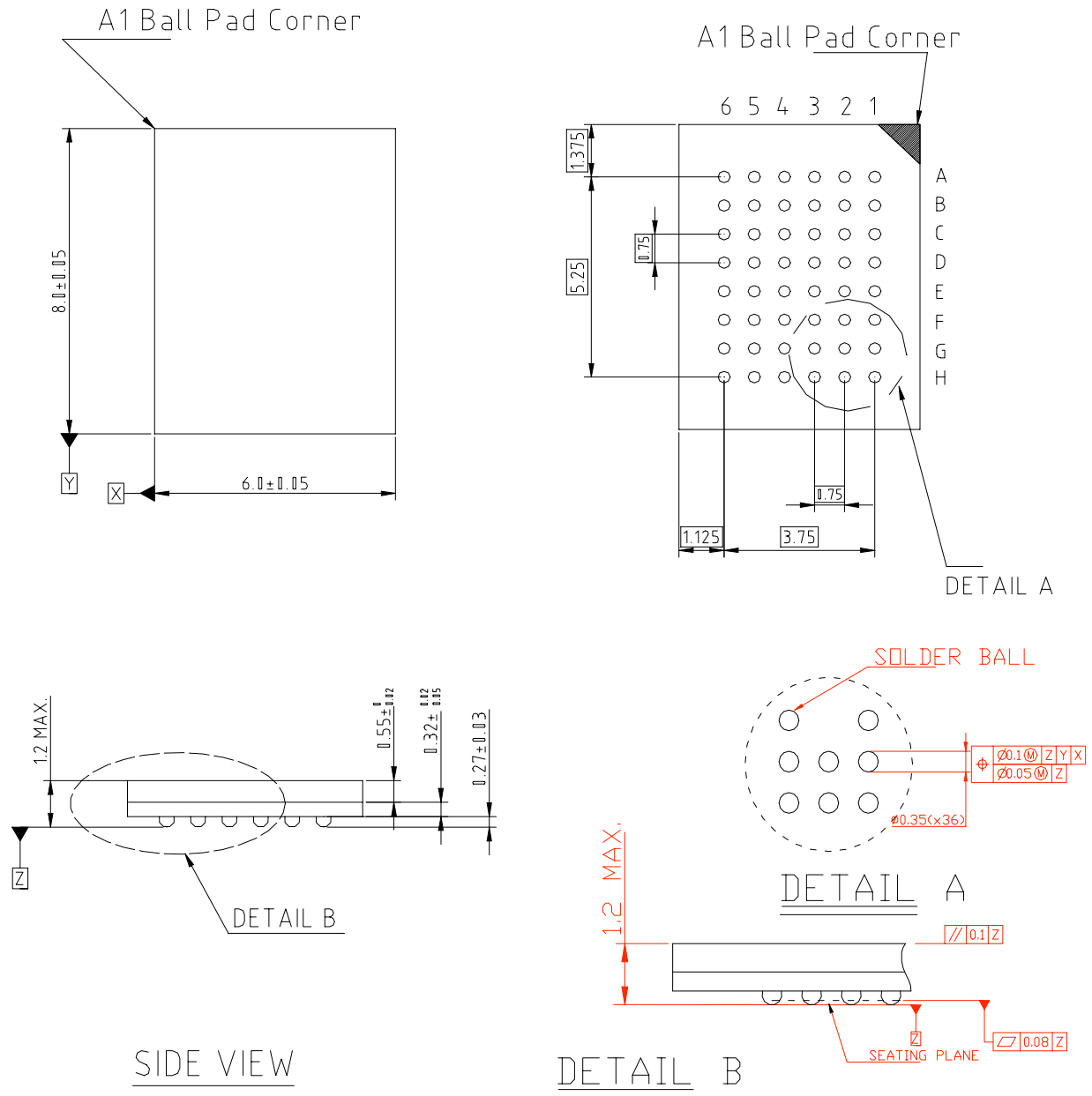
| SYM. \ UNIT | INCH(BASE)    | MM(REF)         |
|-------------|---------------|-----------------|
| A1          | 0.001 (MIN)   | 0.254 (MIN)     |
| A2          | 0.150 ± 0.005 | 3.810 ± 0.127   |
| B           | 0.018 ± 0.005 | 0.457 ± 0.127   |
| D           | 1.650 ± 0.005 | 41.910 ± 0.127  |
| E           | 0.600 ± 0.010 | 15.240 ± 0.254  |
| E1          | 0.544 ± 0.004 | 13.818 ± 0.102  |
| e           | 0.100 (TYP)   | 2.540 (TYP)     |
| eB          | 0.640 ± 0.020 | 16.256 ± 0.508. |
| L           | 0.130 ± 0.010 | 3.302 ± 0.254   |
| S           | 0.075 ± 0.010 | 1.905 ± 0.254   |
| Q1          | 0.070 ± 0.005 | 1.778 ± 0.127   |

Note : D/E1/S dimension do not include mold flash.



## 256K X 8 BIT LOW POWER CMOS SRAM

## 36 ball 6mm x 8mm TFBGA Package Outline Dimension





## 256K X 8 BIT LOW POWER CMOS SRAM

**ORDERING INFORMATION**

| Alliance         | Organization | VCC Range  | Package                  | Operating Temp            | Speed ns |
|------------------|--------------|------------|--------------------------|---------------------------|----------|
| AS6C2008A-55SIN  | 256K x 8     | 2.7 - 5.5V | 32pin 450mil SOP         | Industrial ~ -40 F - 85 F | 55       |
| AS6C2008A-55STIN | 256K x 8     | 2.7 - 5.5V | 32pin sTSOP(8 x 13.4mm)  | Industrial ~ -40 F - 85 F | 55       |
| AS6C2008A-55TIN  | 256K x 8     | 2.7 - 5.5V | 32pin TSOP- 1(8 x 20 mm) | Industrial ~ -40 F - 85 F | 55       |
| AS6C2008A-55BIN  | 256K x 8     | 2.7 - 5.5V | 36ball TFBGA(6 x 8mm)    | Industrial ~ -40 F - 85 F | 55       |

**PART NUMBERING SYSTEM**

| AS6C                     | 2008                                   | -55            | X                                                                                                     | X                                                         | N                                       |
|--------------------------|----------------------------------------|----------------|-------------------------------------------------------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------|
| low power<br>SRAM prefix | Device<br>Number<br>20 = 2M<br>08 = x8 | Access<br>Time | Package Option<br>S = 32pin 450 mil SOP<br>ST = 32pin sTSOP(8 x 13.4)<br>T = 32pin TSOP - 1(8 x 20mm) | Temperature<br>Range<br>I = Industrial<br>(-40 to + 85 C) | N = Lead Free<br>RoHS<br>compliant part |

256K X 8 BIT LOW POWER CMOS SRAM

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Alliance Memory, Inc  
511 Taylor Way,  
San Carlos, CA 94070, USA  
Phone: 650-610-6800  
Fax: 650-620-9211

[www.alliancememory.com](http://www.alliancememory.com)

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