



**512K x 36, 1M x 18  
2.5V Synchronous ZBT™ SRAMs  
2.5V I/O, Burst Counter  
Pipelined Outputs**

**AS8C163631  
AS8C161831**

## Features

- ◆ 512K x 36, 1M x 18 memory configurations
- ◆ Supports high performance system speed - 200 MHz (3.2 ns Clock-to-Data Access)
- ◆ ZBT™ Feature - No dead cycles between write and read cycles
- ◆ Internally synchronized output buffer enable eliminates the need to control OE
- ◆ Single R/W (READ/WRITE) control pin
- ◆ Positive clock-edge triggered address, data, and control signal registers for fully pipelined applications
- ◆ 4-word burst capability (interleaved or linear)
- ◆ Individual byte write (BW1 - BW4) control (May tie active)
- ◆ Three chip enables for simple depth expansion
- ◆ 2.5V power supply (±5%)
- ◆ 2.5V I/O Supply (VDDQ)
- ◆ Power down controlled by ZZ input
- ◆ Boundary Scan JTAG Interface (IEEE 1149.1 Compliant)
- ◆ Packaged in a JEDEC standard 100-pin plastic thin quad flatpack (TQFP)

## Description

The AS8C163631/1831 are 2.5V high-speed 18,874,368-bit (18 Megabit) synchronous SRAMs. They are designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus, they have been given the name ZBT™, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later the associated data cycle occurs, be it read or write.

The AS8C163631/1831 contain data I/O, address and control signal registers. Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable CEN pin allows operation of the AS8C163631/1831 to be suspended as long as necessary. All synchronous inputs are ignored when CEN is high and the internal device registers will hold their previous values.

There are three chip enable pins (CE1, CE2, CE2) that allow the user to deselect the device when desired. If any one of these three is not asserted when ADV/LD is low, no new memory operation can be initiated.

## Pin Description Summary

|                           |                                          |        |              |
|---------------------------|------------------------------------------|--------|--------------|
| A0-A19                    | Address Inputs                           | Input  | Synchronous  |
| CE1, CE2, CE2             | Chip Enables                             | Input  | Synchronous  |
| OE                        | Output Enable                            | Input  | Asynchronous |
| R/W                       | Read/Write Signal                        | Input  | Synchronous  |
| CEN                       | Clock Enable                             | Input  | Synchronous  |
| BW1, BW2, BW3, BW4        | Individual Byte Write Selects            | Input  | Synchronous  |
| CLK                       | Clock                                    | Input  | N/A          |
| ADV/LD                    | Advance burst address / Load new address | Input  | Synchronous  |
| LBO                       | Linear / Interleaved Burst Order         | Input  | Static       |
| TMS                       | Test Mode Select                         | Input  | N/A          |
| TDI                       | Test Data Input                          | Input  | N/A          |
| TCK                       | Test Clock                               | Input  | N/A          |
| TDO                       | Test Data Input                          | Output | N/A          |
| TRST                      | JTAG Reset (Optional)                    | Input  | Asynchronous |
| ZZ                        | Sleep Mode                               | Input  | Synchronous  |
| I/O0-I/O31, I/O P1-I/O P4 | Data Input / Output                      | I/O    | Synchronous  |
| VDD, VDDQ                 | Core Power, I/O Power                    | Supply | Static       |
| VSS                       | Ground                                   | Supply | Static       |

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**Description (cont.)**

However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state two cycles after the chip is deselected or a write is initiated.

The AS8C163631/1831 have an on-chip burst counter. In the burst mode, the AS8C163631/1831 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the  $\overline{\text{LBO}}$  input pin. The  $\overline{\text{LBO}}$  pin selects between linear and

interleaved burst sequence. The  $\text{ADV}/\overline{\text{LD}}$  signal is used to load a new external address ( $\text{ADV}/\overline{\text{LD}} = \text{LOW}$ ) or increment the internal burst counter ( $\text{ADV}/\overline{\text{LD}} = \text{HIGH}$ ).

The AS8C163631/1831 SRAMs utilize Alliance's latest high-performance 2.5V CMOS process, and are packaged in a JEDEC Standard 14mm x 20mm 100pin thin plastic quad flatpack (TQFP).

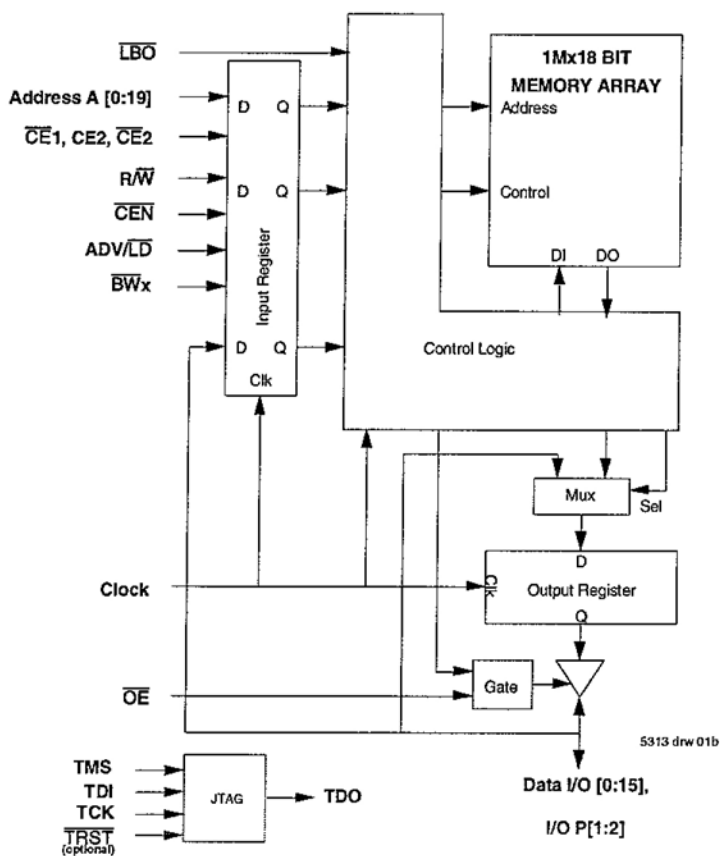
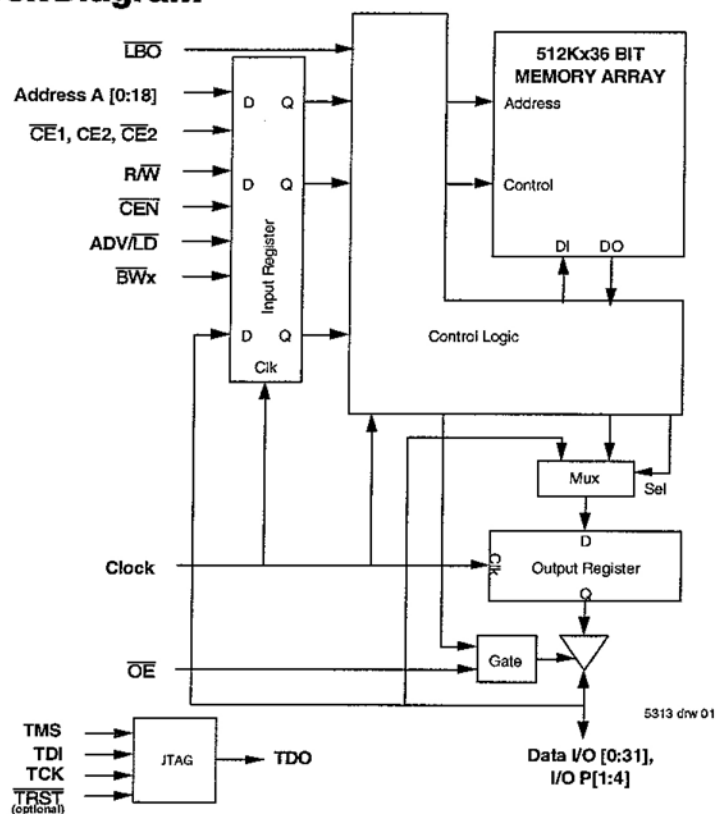
**Pin Definitions<sup>(1)</sup>**

| Symbol                                                                              | Pin Function                  | I/O | Active | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------------------------------------------------------------------------------------|-------------------------------|-----|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A0-A19                                                                              | Address Inputs                | I   | N/A    | Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, $\text{ADV}/\overline{\text{LD}}$ low, $\overline{\text{CEN}}$ low, and true chip enables.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| $\text{ADV}/\overline{\text{LD}}$                                                   | Advance / Load                | I   | N/A    | $\text{ADV}/\overline{\text{LD}}$ is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When $\text{ADV}/\overline{\text{LD}}$ is low with the chip deselected, any burst in progress is terminated. When $\text{ADV}/\overline{\text{LD}}$ is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when $\text{ADV}/\overline{\text{LD}}$ is sampled high.                                                                                                                         |
| R/ $\overline{\text{W}}$                                                            | Read / Write                  | I   | N/A    | $\overline{\text{R}}/\overline{\text{W}}$ signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place two clock cycles later.                                                                                                                                                                                                                                                                                                                                                                                                                     |
| $\overline{\text{CEN}}$                                                             | Clock Enable                  | I   | LOW    | Synchronous Clock Enable Input. When $\overline{\text{CEN}}$ is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of $\overline{\text{CEN}}$ sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, $\overline{\text{CEN}}$ must be sampled low at rising edge of clock.                                                                                                                                                                                                                                                                                  |
| $\overline{\text{BW}}_1\text{--}\overline{\text{BW}}_4$                             | Individual Byte Write Enables | I   | LOW    | Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (when R/ $\overline{\text{W}}$ and $\text{ADV}/\overline{\text{LD}}$ are sampled low) the appropriate byte write signal ( $\overline{\text{BW}}_1\text{--}\overline{\text{BW}}_4$ ) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/ $\overline{\text{W}}$ is sampled high. The appropriate byte(s) of data are written into the device two cycles later. $\overline{\text{BW}}_1\text{--}\overline{\text{BW}}_4$ can all be tied low if always doing write to the entire 36-bit word. |
| $\overline{\text{CE}}_1$ , $\overline{\text{CE}}_2$                                 | Chip Enables                  | I   | LOW    | Synchronous active low chip enable. $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ are used with $\overline{\text{CE}}_2$ to enable the AS8C163631/1831 ( $\overline{\text{CE}}_1$ or $\overline{\text{CE}}_2$ sampled high or $\overline{\text{CE}}_2$ sampled low) and $\text{ADV}/\overline{\text{LD}}$ low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a two cycle deselect, i.e., the data bus will tri-state two clock cycles after deselect is initiated.                                                                                                                                                                                   |
| $\text{CE}_2$                                                                       | Chip Enable                   | I   | HIGH   | Synchronous active high chip enable. $\text{CE}_2$ is used with $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ to enable the chip. $\text{CE}_2$ has inverted polarity but otherwise identical to $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ .                                                                                                                                                                                                                                                                                                                                                                                                                    |
| CLK                                                                                 | Clock                         | I   | N/A    | This is the clock input to the AS8C163631/1831. Except for $\overline{\text{OE}}$ , all timing references for the device are made with respect to the rising edge of CLK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| $\text{I/O}_0\text{--}\text{I/O}_{31}$<br>$\text{I/O}_{P1}\text{--}\text{I/O}_{P4}$ | Data Input/Output             | I/O | N/A    | Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| $\overline{\text{LBO}}$                                                             | Linear Burst Order            | I   | LOW    | Burst order selection input. When $\overline{\text{LBO}}$ is high the interleaved burst sequence is selected. When $\overline{\text{LBO}}$ is low the Linear burst sequence is selected. $\overline{\text{LBO}}$ is a static input and it must not change during device operation.                                                                                                                                                                                                                                                                                                                                                                                                  |
| $\overline{\text{OE}}$                                                              | Output Enable                 | I   | LOW    | Asynchronous output enable. $\overline{\text{OE}}$ must be low to read data from the AS8C163631/1831. When $\overline{\text{OE}}$ is high the I/O pins are in a high-impedance state. $\overline{\text{OE}}$ does not need to be actively controlled for read and write cycles. In normal operation, $\overline{\text{OE}}$ can be tied low.                                                                                                                                                                                                                                                                                                                                        |
| TMS                                                                                 | Test Mode Select              | I   | N/A    | Gives input command for TAP controller. Sampled on rising edge of TCK. This pin has an internal pullup.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| TDI                                                                                 | Test Data Input               | I   | N/A    | Serial input of registers placed between TDI and TDO. Sampled on rising edge of TCK. This pin has an internal pullup.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| TCK                                                                                 | Test Clock                    | I   | N/A    | Clock input of TAP controller. Each TAP event is clocked. Test inputs are captured on rising edge of TCK while test outputs are driven from the falling edge of TCK. This pin has an internal pullup.                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| TDO                                                                                 | Test Data Output              | O   | N/A    | Serial output of registers placed between TDI and TDO. This output is active depending on the state of the TAP controller.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| TRST                                                                                | JTAG Reset (Optional)         | I   | LOW    | Optional asynchronous JTAG reset. Can be used to reset the TAP controller, but not required. JTAG reset occurs automatically at power up and also resets using TMS and TCK per IEEE 1149.1. If not used TRST can be left floating. This pin has an internal pullup. Only available in BGA package.                                                                                                                                                                                                                                                                                                                                                                                  |
| ZZ                                                                                  | Sleep Mode                    | I   | HIGH   | Synchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the AS8C163631/1831 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode. This pin has an internal pulldown.                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| VDD                                                                                 | Power Supply                  | N/A | N/A    | 2.5V core power supply.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| VDDQ                                                                                | Power Supply                  | N/A | N/A    | 2.5V I/O Supply.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| VSS                                                                                 | Ground                        | N/A | N/A    | Ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

**NOTE:**

- 1 All synchronous inputs must meet specified setup and hold times with respect to CLK.

## Functional Block Diagram



## Recommended DC Operating Conditions

| Symbol           | Parameter                   | Min                 | Typ | Max                    | Unit |
|------------------|-----------------------------|---------------------|-----|------------------------|------|
| V <sub>DD</sub>  | Core Supply Voltage         | 2.375               | 2.5 | 2.625                  | V    |
| V <sub>DDQ</sub> | I/O Supply Voltage          | 2.375               | 2.5 | 2.625                  | V    |
| V <sub>SS</sub>  | Ground                      | 0                   | 0   | 0                      | V    |
| V <sub>IH</sub>  | Input High Voltage - Inputs | 1.7                 | —   | V <sub>DD</sub> + 0.3  | V    |
| V <sub>IH</sub>  | Input High Voltage - I/O    | 1.7                 | —   | V <sub>DDQ</sub> + 0.3 | V    |
| V <sub>IL</sub>  | Input Low Voltage           | -0.3 <sup>(1)</sup> | —   | 0.7                    | V    |

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### NOTE:

1 V<sub>IL</sub> (min) = -0.8V for pulse width less than tcvc/2, once per cycle

## Recommended Operating Temperature and Supply Voltage

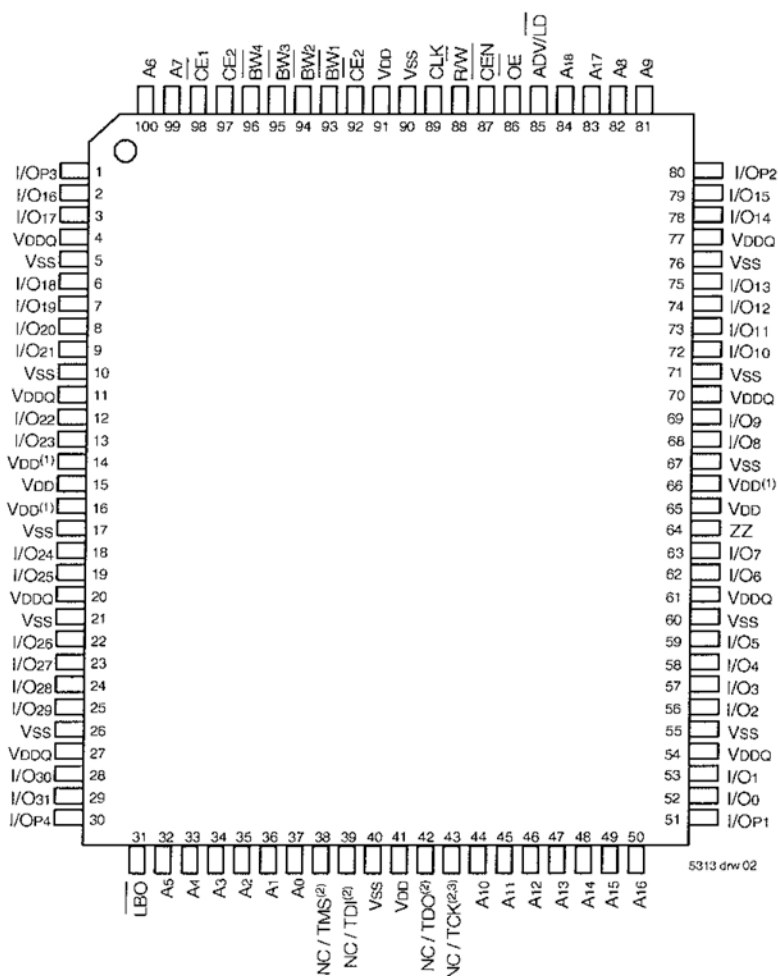
| Grade      | Ambient Temperature <sup>(1)</sup> | V <sub>SS</sub> | V <sub>DD</sub> | V <sub>DDQ</sub> |
|------------|------------------------------------|-----------------|-----------------|------------------|
| Commercial | 0° C to +70° C                     | OV              | 2.5V ± 5%       | 2.5V ± 5%        |
| Industrial | -40° C to +85° C                   | OV              | 2.5V ± 5%       | 2.5V ± 5%        |

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### NOTE:

1 During production testing the case temperature equals the ambient temperature

## Pin Configuration — 512K x 36



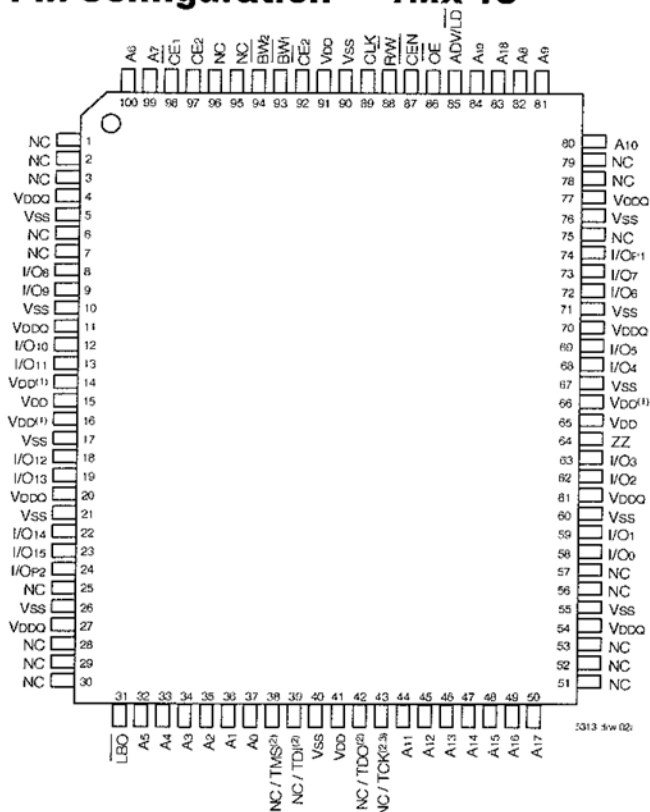
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## Top View 100 TQFP

### NOTES:

- Pins 14, 16, and 66 do not have to be connected directly to V<sub>DD</sub> as long as the input voltage is ≥ V<sub>IH</sub>.
- Pins 38, 39, and 43 will be pulled internally to V<sub>DD</sub> if not actively driven. To disable the TAP controller without interfering with normal operation, several settings are possible. Pins 38, 39, and 43 could be tied to V<sub>DD</sub> or V<sub>SS</sub> and pin 42 should be left unconnected. Or all JTAG inputs (TMS, TDI, and TCK) pins 38, 39, and 43 could be left unconnected. "NC" and the JTAG circuit will remain disabled from power up.
- Pin 43 is reserved for the 36M address. JTAG is not offered in the 100-pin TQFP package for the 36M ZBT device.

## Pin Configuration — 1Mx 18



**Top View  
100 TQFP**

### NOTES:

- Pins 14, 16, and 66 do not have to be connected directly to VDD as long as the input voltage is  $\geq V_{IH}$
- Pins 38, 39 and 43 will be pulled internally to VDD if not actively driven. To disable the TAP controller without interfering with normal operation, several settings are possible. Pins 38, 39 and 43 could be tied to VDD or VSS and pin 42 should be left unconnected. Or all JTAG inputs (TMS, TDI and TCK) pins 38, 39 and 43 could be left unconnected "NC" and the JTAG circuit will remain disabled from power up.
- Pin 43 is reserved for the 36M address. JTAG is not offered in the 100-pin TQFP package for the 36M ZBT device.

## 100-Pin TQFP Capacitance

( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ )

| Symbol          | Parameter <sup>(1)</sup> | Conditions             | Max. | Unit |
|-----------------|--------------------------|------------------------|------|------|
| C <sub>IN</sub> | Input Capacitance        | V <sub>IN</sub> = 3dV  | 5    | pF   |
| C <sub>VO</sub> | I/O Capacitance          | V <sub>OUT</sub> = 3dV | 7    | pF   |

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## Absolute Maximum Ratings<sup>(1)</sup>

| Symbol                             | Rating                               | Commercial                    | Industrial                    | Unit |
|------------------------------------|--------------------------------------|-------------------------------|-------------------------------|------|
| V <sub>TERM</sub> <sup>(2)</sup>   | Terminal Voltage with Respect to GND | -0.5 to +3.6                  | -0.5 to +3.6                  | V    |
| V <sub>TERM</sub> <sup>(3,8)</sup> | Terminal Voltage with Respect to GND | -0.5 to V <sub>DD</sub>       | -0.5 to V <sub>DD</sub>       | V    |
| V <sub>TERM</sub> <sup>(4,6)</sup> | Terminal Voltage with Respect to GND | -0.5 to V <sub>DD</sub> +0.5  | -0.5 to V <sub>DD</sub> +0.5  | V    |
| V <sub>TERM</sub> <sup>(5,6)</sup> | Terminal Voltage with Respect to GND | -0.5 to V <sub>DDQ</sub> +0.5 | -0.5 to V <sub>DDQ</sub> +0.5 | V    |
| T <sub>A</sub> <sup>(7)</sup>      | Operating Ambient Temperature        | 0 to +70                      | -40 to +85                    | °C   |
| T <sub>BIAS</sub>                  | Temperature Under Bias               | -55 to +125                   | -55 to +125                   | °C   |
| T <sub>STG</sub>                   | Storage Temperature                  | -55 to +125                   | -55 to +125                   | °C   |
| P <sub>T</sub>                     | Power Dissipation                    | 2.0                           | 2.0                           | W    |
| I <sub>OUT</sub>                   | DC Output Current                    | 50                            | 50                            | mA   |

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### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>DD</sub> terminals only.
- V<sub>DDQ</sub> terminals only.
- Input terminals only.
- I/O terminals only.
- This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V<sub>DDQ</sub> during power supply ramp up.
- During production testing, the case temperature equals T<sub>A</sub>.

**Synchronous Truth Table<sup>(1)</sup>**

| CEN | R/W | Chip <sup>(5)</sup><br>Enable | ADV/LD | BWx   | ADDRESS<br>USED | PREVIOUS CYCLE              | CURRENT CYCLE                                         | I/O<br>(2 cycles later) |
|-----|-----|-------------------------------|--------|-------|-----------------|-----------------------------|-------------------------------------------------------|-------------------------|
| L   | L   | Select                        | L      | Valid | External        | X                           | LOAD WRITE                                            | D <sup>(7)</sup>        |
| L   | H   | Select                        | L      | X     | External        | X                           | LOAD READ                                             | Q <sup>(7)</sup>        |
| L   | X   | X                             | H      | Valid | Internal        | LOAD WRITE /<br>BURST WRITE | BURST WRITE<br>(Advance burst counter) <sup>(2)</sup> | D <sup>(7)</sup>        |
| L   | X   | X                             | H      | X     | Internal        | LOAD READ /<br>BURST READ   | BURST READ<br>(Advance burst counter) <sup>(2)</sup>  | Q <sup>(7)</sup>        |
| L   | X   | Deselect                      | L      | X     | X               | X                           | DESELECT or STOP <sup>(6)</sup>                       | HiZ                     |
| L   | X   | X                             | H      | X     | X               | DESELECT / NOOP             | NOOP                                                  | HiZ                     |
| H   | X   | X                             | X      | X     | X               | X                           | SUSPEND <sup>(4)</sup>                                | Previous Value          |

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**NOTES:**

- 1 L = V<sub>IL</sub>, H = V<sub>IH</sub>, X = Don't Care
- 2 When ADV/LD signal is sampled high, the internal burst counter is incremented. The R/W signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/W signal when the first address is loaded at the beginning of the burst cycle.
- 3 Deselect cycle is initiated when either  $\overline{CE}_1$  or  $\overline{CE}_2$  is sampled high or CE<sub>2</sub> is sampled low) and ADV/LD is sampled low at rising edge of clock. The data bus will tri-state two cycles after deselect is initiated.
- 4 When CEN is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers and the I/Os remains unchanged.
- 5 To select the chip requires  $\overline{CE}_1 = L$ ,  $\overline{CE}_2 = L$ , CE<sub>2</sub> = H on these chip enables. Chip is deselected if any one of the chip enables is false.
- 6 Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.
- 7 Q - Data read from the device. D - data written to the device.

**Partial Truth Table for Writes<sup>(1)</sup>**

| OPERATION                                                      | R/W | BW <sub>1</sub> | BW <sub>2</sub> | BW <sub>3</sub> <sup>(3)</sup> | BW <sub>4</sub> <sup>(3)</sup> |
|----------------------------------------------------------------|-----|-----------------|-----------------|--------------------------------|--------------------------------|
| READ                                                           | H   | X               | X               | X                              | X                              |
| WRITE ALL BYTES                                                | L   | L               | L               | L                              | L                              |
| WRITE BYTE 1 (I/O[0:7], I/OP <sub>1</sub> ) <sup>(2)</sup>     | L   | L               | H               | H                              | H                              |
| WRITE BYTE 2 (I/O[8:15], I/OP <sub>2</sub> ) <sup>(2)</sup>    | L   | H               | L               | H                              | H                              |
| WRITE BYTE 3 (I/O[16:23], I/OP <sub>3</sub> ) <sup>(2,3)</sup> | L   | H               | H               | L                              | H                              |
| WRITE BYTE 4 (I/O[24:31], I/OP <sub>4</sub> ) <sup>(2,3)</sup> | L   | H               | H               | H                              | L                              |
| NO WRITE                                                       | L   | H               | H               | H                              | H                              |

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**NOTES:**

- 1 L = V<sub>IL</sub>, H = V<sub>IH</sub>, X = Don't Care
- 2 Multiple bytes may be selected during the same cycle.
- 3 N/A for X18 configuration.

## Interleaved Burst Sequence Table ( $\overline{\text{LBO}}=\text{VDD}$ )

|                               | Sequence 1 |    | Sequence 2 |    | Sequence 3 |    | Sequence 4 |    |
|-------------------------------|------------|----|------------|----|------------|----|------------|----|
|                               | A1         | A0 | A1         | A0 | A1         | A0 | A1         | A0 |
| First Address                 | 0          | 0  | 0          | 1  | 1          | 0  | 1          | 1  |
| Second Address                | 0          | 1  | 0          | 0  | 1          | 1  | 1          | 0  |
| Third Address                 | 1          | 0  | 1          | 1  | 0          | 0  | 0          | 1  |
| Fourth Address <sup>(1)</sup> | 1          | 1  | 1          | 0  | 0          | 1  | 0          | 0  |

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### NOTE:

- 1 Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting

## Linear Burst Sequence Table ( $\overline{\text{LBO}}=\text{Vss}$ )

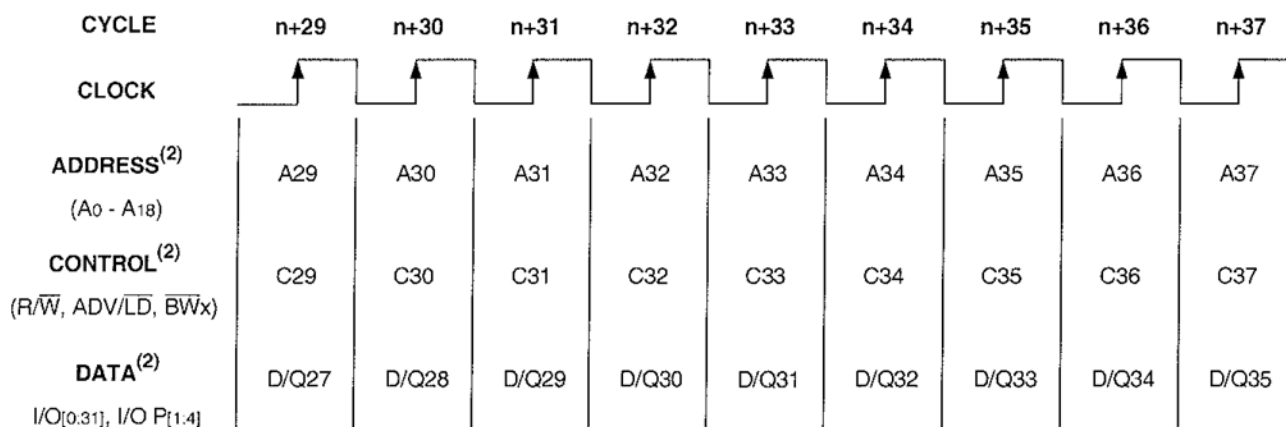
|                               | Sequence 1 |    | Sequence 2 |    | Sequence 3 |    | Sequence 4 |    |
|-------------------------------|------------|----|------------|----|------------|----|------------|----|
|                               | A1         | A0 | A1         | A0 | A1         | A0 | A1         | A0 |
| First Address                 | 0          | 0  | 0          | 1  | 1          | 0  | 1          | 1  |
| Second Address                | 0          | 1  | 1          | 0  | 1          | 1  | 0          | 0  |
| Third Address                 | 1          | 0  | 1          | 1  | 0          | 0  | 0          | 1  |
| Fourth Address <sup>(1)</sup> | 1          | 1  | 0          | 0  | 0          | 1  | 1          | 0  |

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### NOTE:

- 1 Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting

## Functional Timing Diagram<sup>(1)</sup>



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### NOTES:

- 1 This assumes  $\overline{\text{CEN}}$ ,  $\overline{\text{CE1}}$ ,  $\overline{\text{CE2}}$ ,  $\overline{\text{CE2}}$  are all true
- 2 All Address, Control and Data\_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data\_Out is valid after a clock-to-data delay from the rising edge of clock

## Device Operation - Showing Mixed Load, Burst, Deselect and NOOP Cycles<sup>(2)</sup>

| Cycle | Address        | R/ $\overline{W}$ | ADV/ $\overline{LD}$ | $\overline{CE}^{(1)}$ | $\overline{CEN}$ | $\overline{BWx}$ | $\overline{OE}$ | I/O              | Comments         |
|-------|----------------|-------------------|----------------------|-----------------------|------------------|------------------|-----------------|------------------|------------------|
| n     | A <sub>0</sub> | H                 | L                    | L                     | L                | X                | X               | X                | Load read        |
| n+1   | X              | X                 | H                    | X                     | L                | X                | X               | X                | Burst read       |
| n+2   | A <sub>1</sub> | H                 | L                    | L                     | L                | X                | L               | Q <sub>0</sub>   | Load read        |
| n+3   | X              | X                 | L                    | H                     | L                | X                | L               | Q <sub>0+1</sub> | Deselect or STOP |
| n+4   | X              | X                 | H                    | X                     | L                | X                | L               | Q <sub>1</sub>   | NOOP             |
| n+5   | A <sub>2</sub> | H                 | L                    | L                     | L                | X                | X               | Z                | Load read        |
| n+6   | X              | X                 | H                    | X                     | L                | X                | X               | Z                | Burst read       |
| n+7   | X              | X                 | L                    | H                     | L                | X                | L               | Q <sub>2</sub>   | Deselect or STOP |
| n+8   | A <sub>3</sub> | L                 | L                    | L                     | L                | L                | L               | Q <sub>2+1</sub> | Load write       |
| n+9   | X              | X                 | H                    | X                     | L                | L                | X               | Z                | Burst write      |
| n+10  | A <sub>4</sub> | L                 | L                    | L                     | L                | L                | X               | D <sub>3</sub>   | Load write       |
| n+11  | X              | X                 | L                    | H                     | L                | X                | X               | D <sub>3+1</sub> | Deselect or STOP |
| n+12  | X              | X                 | H                    | X                     | L                | X                | X               | D <sub>4</sub>   | NOOP             |
| n+13  | A <sub>5</sub> | L                 | L                    | L                     | L                | L                | X               | Z                | Load write       |
| n+14  | A <sub>6</sub> | H                 | L                    | L                     | L                | X                | X               | Z                | Load read        |
| n+15  | A <sub>7</sub> | L                 | L                    | L                     | L                | L                | X               | D <sub>5</sub>   | Load write       |
| n+16  | X              | X                 | H                    | X                     | L                | L                | L               | Q <sub>6</sub>   | Burst write      |
| n+17  | A <sub>8</sub> | H                 | L                    | L                     | L                | X                | X               | D <sub>7</sub>   | Load read        |
| n+18  | X              | X                 | H                    | X                     | L                | X                | X               | D <sub>7+1</sub> | Burst read       |
| n+19  | A <sub>9</sub> | L                 | L                    | L                     | L                | L                | L               | Q <sub>8</sub>   | Load write       |

### NOTES:

- $\overline{CE} = L$  is defined as  $\overline{CE}_1 = L$ ,  $\overline{CE}_2 = L$  and  $CE_2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE}_1 = H$ ,  $\overline{CE}_2 = H$  or  $CE_2 = L$ .
- H = High; L = Low; X = Don't Care; Z = High Impedance

5313 tbl 12

## Read Operation<sup>(1)</sup>

| Cycle | Address        | R/ $\overline{W}$ | ADV/ $\overline{LD}$ | $\overline{CE}^{(2)}$ | $\overline{CEN}$ | $\overline{BWx}$ | $\overline{OE}$ | I/O            | Comments                                    |
|-------|----------------|-------------------|----------------------|-----------------------|------------------|------------------|-----------------|----------------|---------------------------------------------|
| n     | A <sub>0</sub> | H                 | L                    | L                     | L                | X                | X               | X              | Address and Control meet setup              |
| n+1   | X              | X                 | X                    | X                     | L                | X                | X               | X              | Clock Setup Valid                           |
| n+2   | X              | X                 | X                    | X                     | X                | X                | L               | Q <sub>0</sub> | Contents of Address A <sub>0</sub> Read Out |

### NOTES:

- H = High; L = Low; X = Don't Care; Z = High Impedance
- $\overline{CE} = L$  is defined as  $CE_1 = L$ ,  $\overline{CE}_2 = L$  and  $CE_2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE}_1 = H$ ,  $\overline{CE}_2 = H$  or  $CE_2 = L$ .

5313 tbl 13

**Burst Read Operation<sup>(1)</sup>**

| Cycle | Address        | R/W | ADV/LD | $\overline{CE}^{(2)}$ | $\overline{CEN}$ | $\overline{BWx}$ | $\overline{OE}$ | I/O              | Comments                                               |
|-------|----------------|-----|--------|-----------------------|------------------|------------------|-----------------|------------------|--------------------------------------------------------|
| n     | A <sub>0</sub> | H   | L      | L                     | L                | X                | X               | X                | Address and Control meet setup                         |
| n+1   | X              | X   | H      | X                     | L                | X                | X               | X                | Clock Setup Valid, Advance Counter                     |
| n+2   | X              | X   | H      | X                     | L                | X                | L               | Q <sub>0</sub>   | Address A <sub>0</sub> Read Out, Inc. Count            |
| n+3   | X              | X   | H      | X                     | L                | X                | L               | Q <sub>0+1</sub> | Address A <sub>0+1</sub> Read Out, Inc. Count          |
| n+4   | X              | X   | H      | X                     | L                | X                | L               | Q <sub>0+2</sub> | Address A <sub>0+2</sub> Read Out, Inc. Count          |
| n+5   | A <sub>1</sub> | H   | L      | L                     | L                | X                | L               | Q <sub>0+3</sub> | Address A <sub>0+3</sub> Read Out, Load A <sub>1</sub> |
| n+6   | X              | X   | H      | X                     | L                | X                | L               | Q <sub>0</sub>   | Address A <sub>0</sub> Read Out, Inc. Count            |
| n+7   | X              | X   | H      | X                     | L                | X                | L               | Q <sub>1</sub>   | Address A <sub>1</sub> Read Out, Inc. Count            |
| n+8   | A <sub>2</sub> | H   | L      | L                     | L                | X                | L               | Q <sub>1+1</sub> | Address A <sub>1+1</sub> Read Out, Load A <sub>2</sub> |

5313 tbl 14

**NOTES:**

1 H = High; L = Low; X = Don't Care; Z = High Impedance

2  $\overline{CE} = L$  is defined as  $\overline{CE}_1 = L$ ,  $\overline{CE}_2 = L$  and  $CE_2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE}_1 = H$ ,  $\overline{CE}_2 = H$  or  $CE_2 = L$ .**Write Operation<sup>(1)</sup>**

| Cycle | Address        | R/W | ADV/LD | $\overline{CE}^{(2)}$ | $\overline{CEN}$ | $\overline{BWx}$ | $\overline{OE}$ | I/O            | Comments                        |
|-------|----------------|-----|--------|-----------------------|------------------|------------------|-----------------|----------------|---------------------------------|
| n     | A <sub>0</sub> | L   | L      | L                     | L                | L                | X               | X              | Address and Control meet setup  |
| n+1   | X              | X   | X      | X                     | L                | X                | X               | X              | Clock Setup Valid               |
| n+2   | X              | X   | X      | X                     | L                | X                | X               | D <sub>0</sub> | Write to Address A <sub>0</sub> |

5313 tbl 15

**NOTES:**

1 H = High; L = Low; X = Don't Care; Z = High Impedance

2  $\overline{CE} = L$  is defined as  $\overline{CE}_1 = L$ ,  $\overline{CE}_2 = L$  and  $CE_2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE}_1 = H$ ,  $\overline{CE}_2 = H$  or  $CE_2 = L$ .**Burst Write Operation<sup>(1)</sup>**

| Cycle | Address        | R/W | ADV/LD | $\overline{CE}^{(2)}$ | $\overline{CEN}$ | $\overline{BWx}$ | $\overline{OE}$ | I/O              | Comments                                            |
|-------|----------------|-----|--------|-----------------------|------------------|------------------|-----------------|------------------|-----------------------------------------------------|
| n     | A <sub>0</sub> | L   | L      | L                     | L                | L                | X               | X                | Address and Control meet setup                      |
| n+1   | X              | X   | H      | X                     | L                | L                | X               | X                | Clock Setup Valid, Inc. Count                       |
| n+2   | X              | X   | H      | X                     | L                | L                | X               | D <sub>0</sub>   | Address A <sub>0</sub> Write, Inc. Count            |
| n+3   | X              | X   | H      | X                     | L                | L                | X               | D <sub>0+1</sub> | Address A <sub>0+1</sub> Write, Inc. Count          |
| n+4   | X              | X   | H      | X                     | L                | L                | X               | D <sub>0+2</sub> | Address A <sub>0+2</sub> Write, Inc. Count          |
| n+5   | A <sub>1</sub> | L   | L      | L                     | L                | L                | X               | D <sub>0+3</sub> | Address A <sub>0+3</sub> Write, Load A <sub>1</sub> |
| n+6   | X              | X   | H      | X                     | L                | L                | X               | D <sub>0</sub>   | Address A <sub>0</sub> Write, Inc. Count            |
| n+7   | X              | X   | H      | X                     | L                | L                | X               | D <sub>1</sub>   | Address A <sub>1</sub> Write, Inc. Count            |
| n+8   | A <sub>2</sub> | L   | L      | L                     | L                | L                | X               | D <sub>1+1</sub> | Address A <sub>1+1</sub> Write, Load A <sub>2</sub> |

5313 tbl 16

**NOTES:**

1 H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance

2  $\overline{CE} = L$  is defined as  $\overline{CE}_1 = L$ ,  $\overline{CE}_2 = L$  and  $CE_2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE}_1 = H$ ,  $\overline{CE}_2 = H$  or  $CE_2 = L$ .

**Read Operation with Clock Enable Used<sup>(1)</sup>**

| Cycle | Address        | R/W | ADV/LD | $\overline{CE}^{(2)}$ | $\overline{CEN}$ | $\overline{BWx}$ | $\overline{OE}$ | I/O            | Comments                                          |
|-------|----------------|-----|--------|-----------------------|------------------|------------------|-----------------|----------------|---------------------------------------------------|
| n     | A <sub>0</sub> | H   | L      | L                     | L                | X                | X               | X              | Address and Control meet setup                    |
| n+1   | X              | X   | X      | X                     | H                | X                | X               | X              | Clock n+1 Ignored                                 |
| n+2   | A <sub>1</sub> | H   | L      | L                     | L                | X                | X               | X              | Clock Valid                                       |
| n+3   | X              | X   | X      | X                     | H                | X                | L               | Q <sub>0</sub> | Clock Ignored. Data Q <sub>0</sub> is on the bus. |
| n+4   | X              | X   | X      | X                     | H                | X                | L               | Q <sub>0</sub> | Clock Ignored. Data Q <sub>0</sub> is on the bus. |
| n+5   | A <sub>2</sub> | H   | L      | L                     | L                | X                | L               | Q <sub>0</sub> | Address A <sub>0</sub> Read out (bus trans.)      |
| n+6   | A <sub>3</sub> | H   | L      | L                     | L                | X                | L               | Q <sub>1</sub> | Address A <sub>1</sub> Read out (bus trans.)      |
| n+7   | A <sub>4</sub> | H   | L      | L                     | L                | X                | L               | Q <sub>2</sub> | Address A <sub>2</sub> Read out (bus trans.)      |

5313 tbl 17

**NOTES:**

1 H = High; L = Low; X = Don't Care; Z = High Impedance.

2  $\overline{CE} = L$  is defined as  $\overline{CE}_1 = L$ ,  $\overline{CE}_2 = L$  and  $CE_2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE}_1 = H$ ,  $\overline{CE}_2 = H$  or  $CE_2 = L$ .**Write Operation with Clock Enable Used<sup>(1)</sup>**

| Cycle | Address        | R/W | ADV/LD | $\overline{CE}^{(2)}$ | $\overline{CEN}$ | $\overline{BWx}$ | $\overline{OE}$ | I/O            | Comments                        |
|-------|----------------|-----|--------|-----------------------|------------------|------------------|-----------------|----------------|---------------------------------|
| n     | A <sub>0</sub> | L   | L      | L                     | L                | L                | X               | X              | Address and Control meet setup. |
| n+1   | X              | X   | X      | X                     | H                | X                | X               | X              | Clock n+1 Ignored.              |
| n+2   | A <sub>1</sub> | L   | L      | L                     | L                | L                | X               | X              | Clock Valid.                    |
| n+3   | X              | X   | X      | X                     | H                | X                | X               | X              | Clock Ignored.                  |
| n+4   | X              | X   | X      | X                     | H                | X                | X               | X              | Clock Ignored.                  |
| n+5   | A <sub>2</sub> | L   | L      | L                     | L                | L                | X               | D <sub>0</sub> | Write Data D <sub>0</sub>       |
| n+6   | A <sub>3</sub> | L   | L      | L                     | L                | L                | X               | D <sub>1</sub> | Write Data D <sub>1</sub>       |
| n+7   | A <sub>4</sub> | L   | L      | L                     | L                | L                | X               | D <sub>2</sub> | Write Data D <sub>2</sub>       |

5313 tbl 18

**NOTES:**

1 H = High; L = Low; X = Don't Care; Z = High Impedance.

2  $\overline{CE} = L$  is defined as  $\overline{CE}_1 = L$ ,  $\overline{CE}_2 = L$  and  $CE_2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE}_1 = H$ ,  $\overline{CE}_2 = H$  or  $CE_2 = L$ .

**Read Operation with Chip Enable Used<sup>(1)</sup>**

| Cycle | Address        | R/W | ADV/LD | $\overline{CE}^{(2)}$ | $\overline{CEN}$ | $\overline{BWx}$ | $\overline{OE}$ | I/O <sup>(3)</sup> | Comments                                               |
|-------|----------------|-----|--------|-----------------------|------------------|------------------|-----------------|--------------------|--------------------------------------------------------|
| n     | X              | X   | L      | H                     | L                | X                | X               | ?                  | Deselected                                             |
| n+1   | X              | X   | L      | H                     | L                | X                | X               | ?                  | Deselected                                             |
| n+2   | A <sub>0</sub> | H   | L      | L                     | L                | X                | X               | Z                  | Address and Control meet setup.                        |
| n+3   | X              | X   | L      | H                     | L                | X                | X               | Z                  | Deselected or STOP.                                    |
| n+4   | A <sub>1</sub> | H   | L      | L                     | L                | X                | L               | Q <sub>0</sub>     | Address A <sub>0</sub> Read out. Load A <sub>1</sub> . |
| n+5   | X              | X   | L      | H                     | L                | X                | X               | Z                  | Deselected or STOP.                                    |
| n+6   | X              | X   | L      | H                     | L                | X                | L               | Q <sub>1</sub>     | Address A <sub>1</sub> Read out. Deselected.           |
| n+7   | A <sub>2</sub> | H   | L      | L                     | L                | X                | X               | Z                  | Address and control meet setup.                        |
| n+8   | X              | X   | L      | H                     | L                | X                | X               | Z                  | Deselected or STOP.                                    |
| n+9   | X              | X   | L      | H                     | L                | X                | L               | Q <sub>2</sub>     | Address A <sub>2</sub> Read out. Deselected.           |

5313 tbl 19

**NOTES:**

- 1 H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance
- 2  $\overline{CE} = L$  is defined as  $\overline{CE}_1 = L$   $\overline{CE}_2 = L$  and  $CE_2 = H$   $\overline{CE} = H$  is defined as  $\overline{CE}_1 = H$   $\overline{CE}_2 = H$  or  $CE_2 = L$
- 3 Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up

**Write Operation with Chip Enable Used<sup>(1)</sup>**

| Cycle | Address        | R/W | ADV/LD | $\overline{CE}^{(2)}$ | $\overline{CEN}$ | $\overline{BWx}$ | $\overline{OE}$ | I/O            | Comments                                               |
|-------|----------------|-----|--------|-----------------------|------------------|------------------|-----------------|----------------|--------------------------------------------------------|
| n     | X              | X   | L      | H                     | L                | X                | X               | ?              | Deselected.                                            |
| n+1   | X              | X   | L      | H                     | L                | X                | X               | ?              | Deselected.                                            |
| n+2   | A <sub>0</sub> | L   | L      | L                     | L                | L                | X               | Z              | Address and Control meet setup.                        |
| n+3   | X              | X   | L      | H                     | L                | X                | X               | Z              | Deselected or STOP.                                    |
| n+4   | A <sub>1</sub> | L   | L      | L                     | L                | L                | X               | D <sub>0</sub> | Address D <sub>0</sub> Write in. Load A <sub>1</sub> . |
| n+5   | X              | X   | L      | H                     | L                | X                | X               | Z              | Deselected or STOP.                                    |
| n+6   | X              | X   | L      | H                     | L                | X                | X               | D <sub>1</sub> | Address D <sub>1</sub> Write in. Deselected.           |
| n+7   | A <sub>2</sub> | L   | L      | L                     | L                | L                | X               | Z              | Address and control meet setup.                        |
| n+8   | X              | X   | L      | H                     | L                | X                | X               | Z              | Deselected or STOP.                                    |
| n+9   | X              | X   | L      | H                     | L                | X                | X               | D <sub>2</sub> | Address D <sub>2</sub> Write in. Deselected.           |

5313 tbl 20

**NOTES:**

- 1 H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance
- 2  $\overline{CE} = L$  is defined as  $\overline{CE}_1 = L$   $\overline{CE}_2 = L$  and  $CE_2 = H$   $\overline{CE} = H$  is defined as  $\overline{CE}_1 = H$   $\overline{CE}_2 = H$  or  $CE_2 = L$

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ( $V_{DD} = 2.5V \pm 5\%$ )

| Symbol     | Parameter                                                           | Test Conditions                                   | Min. | Max. | Unit    |
|------------|---------------------------------------------------------------------|---------------------------------------------------|------|------|---------|
| $ I_{IL} $ | Input Leakage Current                                               | $V_{DD} = \text{Max}$ , $V_{IN} = 0V$ to $V_{DD}$ | —    | 5    | $\mu A$ |
| $ I_{L} $  | $\overline{LBO}$ , JTAG and ZZ Input Leakage Current <sup>(1)</sup> | $V_{DD} = \text{Max}$ , $V_{IN} = 0V$ to $V_{DD}$ | —    | 30   | $\mu A$ |
| $ I_{LO} $ | Output Leakage Current                                              | $V_{OUT} = 0V$ to $V_{DD}$ , Device Deselected    | —    | 5    | $\mu A$ |
| $V_{OL}$   | Output Low Voltage                                                  | $I_{OL} = +6mA$ , $V_{DD} = \text{Min}$           | —    | 0.4  | V       |
| $V_{OH}$   | Output High Voltage                                                 | $I_{OH} = -6mA$ , $V_{DD} = \text{Min}$           | 2.0  | —    | V       |

## NOTE:

5313 tbl 21

1 The  $\overline{LBO}$ , TMS, TDI, TCK and  $\overline{TRST}$  pins will be internally pulled to  $V_{DD}$  and the ZZ pin will be internally pulled to  $V_{SS}$  if they are not actively driven in the application

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range <sup>(1)</sup> ( $V_{DD} = 2.5V \pm 5\%$ )

| Symbol    | Parameter                          | Test Conditions                                                                                                                                                            | 200MHz |     | 166MHz |     | 150MHz |     | 133MHz |     | 100MHz |     | Unit |
|-----------|------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|------|
|           |                                    |                                                                                                                                                                            | Com'l  | Ind | Com'l  | Ind | Com'l  | Ind | Com'l  | Ind | Com'l  | Ind |      |
| $I_{DD}$  | Operating Power Supply Current     | Device Selected, Outputs Open<br>$ADV/\overline{LD} = X$ , $V_{DD} = \text{Max}$<br>$V_{IN} \geq V_{IH}$ or $\leq V_{IL}$ , $f = f_{MAX}^{(2)}$                            | 275    | 295 | 245    | 265 | 215    | 235 | 195    | 215 | 175    | 195 | mA   |
| $I_{SB1}$ | CMOS Standby Power Supply Current  | Device Deselected, Outputs Open,<br>$V_{DD} = \text{Max}$ , $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$<br>$f = 0^{(2,3)}$                                                       | 40     | 60  | 40     | 60  | 40     | 60  | 40     | 60  | 40     | 60  | mA   |
| $I_{SB2}$ | Clock Running Power Supply Current | Device Deselected, Outputs Open<br>$V_{DD} = \text{Max}$ , $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$<br>$f = f_{MAX}^{(2,3)}$                                                  | 80     | 100 | 70     | 90  | 60     | 80  | 50     | 70  | 45     | 65  | mA   |
| $I_{SB3}$ | Idle Power Supply Current          | Device Selected, Outputs Open,<br>$\overline{CEN} \geq V_{IH}$ , $V_{DD} = \text{Max}$<br>$V_{IN} \geq V_{HD}$ or $\leq V_{LD}$ , $f = f_{MAX}^{(2,3)}$                    | 60     | 80  | 60     | 80  | 60     | 80  | 60     | 80  | 60     | 80  | mA   |
| $I_{ZZ}$  | Full Sleep Mode Supply Current     | Device Selected, Outputs Open,<br>$\overline{CEN} \leq V_{IH}$ , $V_{DD} = \text{Max}$<br>$V_{IN} \geq V_{HD}$ or $\leq V_{LD}$ , $f = f_{MAX}^{(2,3)}$ , $ZZ \geq V_{HD}$ | 40     | 60  | 40     | 60  | 40     | 60  | 40     | 60  | 40     | 60  | mA   |

## NOTES:

5313 tbl 22

1 All values are maximum guaranteed values

2 At  $f = f_{MAX}$  inputs are cycling at the maximum frequency of read cycles of 1/tcyc;  $f=0$  means no input lines are changing

3 For I/Os  $V_{HD} = V_{DD} - 0.2V$ ,  $V_{LD} = 0.2V$ . For other inputs  $V_{HD} = V_{DD} - 0.2V$ ,  $V_{LD} = 0.2V$

## AC Test Load

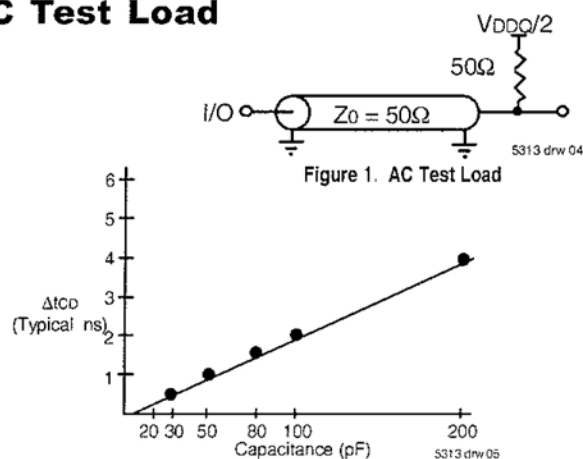


Figure 2. Lumped Capacitive Load, Typical Derating

## AC Test Conditions

|                                |               |
|--------------------------------|---------------|
| Input Pulse Levels             | 0 to 2.5V     |
| Input Rise/Fall Times          | 2ns           |
| Input Timing Reference Levels  | $(V_{DDQ}/2)$ |
| Output Timing Reference Levels | $(V_{DDQ}/2)$ |
| AC Test Load                   | See Figure 1  |

5313 tbl 23

**AC Electrical Characteristics (V<sub>DD</sub> = 2.5V +/-5%, Commercial and Industrial Temperature Ranges)**

| Symbol                              | Parameter                          | 200MHz |      | 166MHz |      | 150MHz |      | 133MHz |      | 100MHz |      | Unit |
|-------------------------------------|------------------------------------|--------|------|--------|------|--------|------|--------|------|--------|------|------|
|                                     |                                    | Min.   | Max. | Min.   | Max. | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| t <sub>CYC</sub>                    | Clock Cycle Time                   | 5      | —    | 6      | —    | 6.7    | —    | 7.5    | —    | 10     | —    | ns   |
| f <sub>clk</sub> <sup>(1)</sup>     | Clock Frequency                    | —      | 200  | —      | 166  | —      | 150  | —      | 133  | —      | 100  | MHz  |
| t <sub>CH</sub> <sup>(2)</sup>      | Clock High Pulse Width             | 1.8    | —    | 1.8    | —    | 2.0    | —    | 2.2    | —    | 3.2    | —    | ns   |
| t <sub>CL</sub> <sup>(2)</sup>      | Clock Low Pulse Width              | 1.8    | —    | 1.8    | —    | 2.0    | —    | 2.2    | —    | 3.2    | —    | ns   |
| <b>Output Parameters</b>            |                                    |        |      |        |      |        |      |        |      |        |      |      |
| t <sub>CD</sub>                     | Clock High to Valid Data           | —      | 3.2  | —      | 3.5  | —      | 3.8  | —      | 4.2  | —      | 5    | ns   |
| t <sub>DC</sub>                     | Clock High to Data Change          | 1.0    | —    | 1.0    | —    | 1.5    | —    | 1.5    | —    | 1.5    | —    | ns   |
| t <sub>CLZ</sub> <sup>(3,4,5)</sup> | Clock High to Output Active        | 1.0    | —    | 1.0    | —    | 1.5    | —    | 1.5    | —    | 1.5    | —    | ns   |
| t <sub>CHZ</sub> <sup>(3,4,5)</sup> | Clock High to Data High-Z          | 1.0    | 3    | 1.0    | 3    | 1.5    | 3    | 1.5    | 3    | 1.5    | 3.3  | ns   |
| t <sub>OE</sub>                     | Output Enable Access Time          | —      | 3.2  | —      | 3.5  | —      | 3.8  | —      | 4.2  | —      | 5    | ns   |
| t <sub>OLZ</sub> <sup>(3,4)</sup>   | Output Enable Low to Data Active   | 0      | —    | 0      | —    | 0      | —    | 0      | —    | 0      | —    | ns   |
| t <sub>OHZ</sub> <sup>(3,4)</sup>   | Output Enable High to Data High-Z  | —      | 3.2  | —      | 3.5  | —      | 3.8  | —      | 4.2  | —      | 5    | ns   |
| <b>Set Up Times</b>                 |                                    |        |      |        |      |        |      |        |      |        |      |      |
| t <sub>SE</sub>                     | Clock Enable Setup Time            | 1.4    | —    | 1.5    | —    | 1.5    | —    | 1.7    | —    | 2.0    | —    | ns   |
| t <sub>SA</sub>                     | Address Setup Time                 | 1.4    | —    | 1.5    | —    | 1.5    | —    | 1.7    | —    | 2.0    | —    | ns   |
| t <sub>SD</sub>                     | Data In Setup Time                 | 1.4    | —    | 1.5    | —    | 1.5    | —    | 1.7    | —    | 2.0    | —    | ns   |
| t <sub>SW</sub>                     | Read/Write (R/W) Setup Time        | 1.4    | —    | 1.5    | —    | 1.5    | —    | 1.7    | —    | 2.0    | —    | ns   |
| t <sub>ADV</sub>                    | Advance/Load (ADV/LD) Setup Time   | 1.4    | —    | 1.5    | —    | 1.5    | —    | 1.7    | —    | 2.0    | —    | ns   |
| t <sub>SC</sub>                     | Chip Enable/Select Setup Time      | 1.4    | —    | 1.5    | —    | 1.5    | —    | 1.7    | —    | 2.0    | —    | ns   |
| t <sub>SB</sub>                     | Byte Write Enable (BWx) Setup Time | 1.4    | —    | 1.5    | —    | 1.5    | —    | 1.7    | —    | 2.0    | —    | ns   |
| <b>Hold Times</b>                   |                                    |        |      |        |      |        |      |        |      |        |      |      |
| t <sub>HE</sub>                     | Clock Enable Hold Time             | 0.4    | —    | 0.5    | —    | 0.5    | —    | 0.5    | —    | 0.5    | —    | ns   |
| t <sub>HA</sub>                     | Address Hold Time                  | 0.4    | —    | 0.5    | —    | 0.5    | —    | 0.5    | —    | 0.5    | —    | ns   |
| t <sub>HD</sub>                     | Data In Hold Time                  | 0.4    | —    | 0.5    | —    | 0.5    | —    | 0.5    | —    | 0.5    | —    | ns   |
| t <sub>HW</sub>                     | Read/Write (R/W) Hold Time         | 0.4    | —    | 0.5    | —    | 0.5    | —    | 0.5    | —    | 0.5    | —    | ns   |
| t <sub>HADV</sub>                   | Advance/Load (ADV/LD) Hold Time    | 0.4    | —    | 0.5    | —    | 0.5    | —    | 0.5    | —    | 0.5    | —    | ns   |
| t <sub>HC</sub>                     | Chip Enable/Select Hold Time       | 0.4    | —    | 0.5    | —    | 0.5    | —    | 0.5    | —    | 0.5    | —    | ns   |
| t <sub>HB</sub>                     | Byte Write Enable (BWx) Hold Time  | 0.4    | —    | 0.5    | —    | 0.5    | —    | 0.5    | —    | 0.5    | —    | ns   |

**NOTES:**

5313 tbl 24

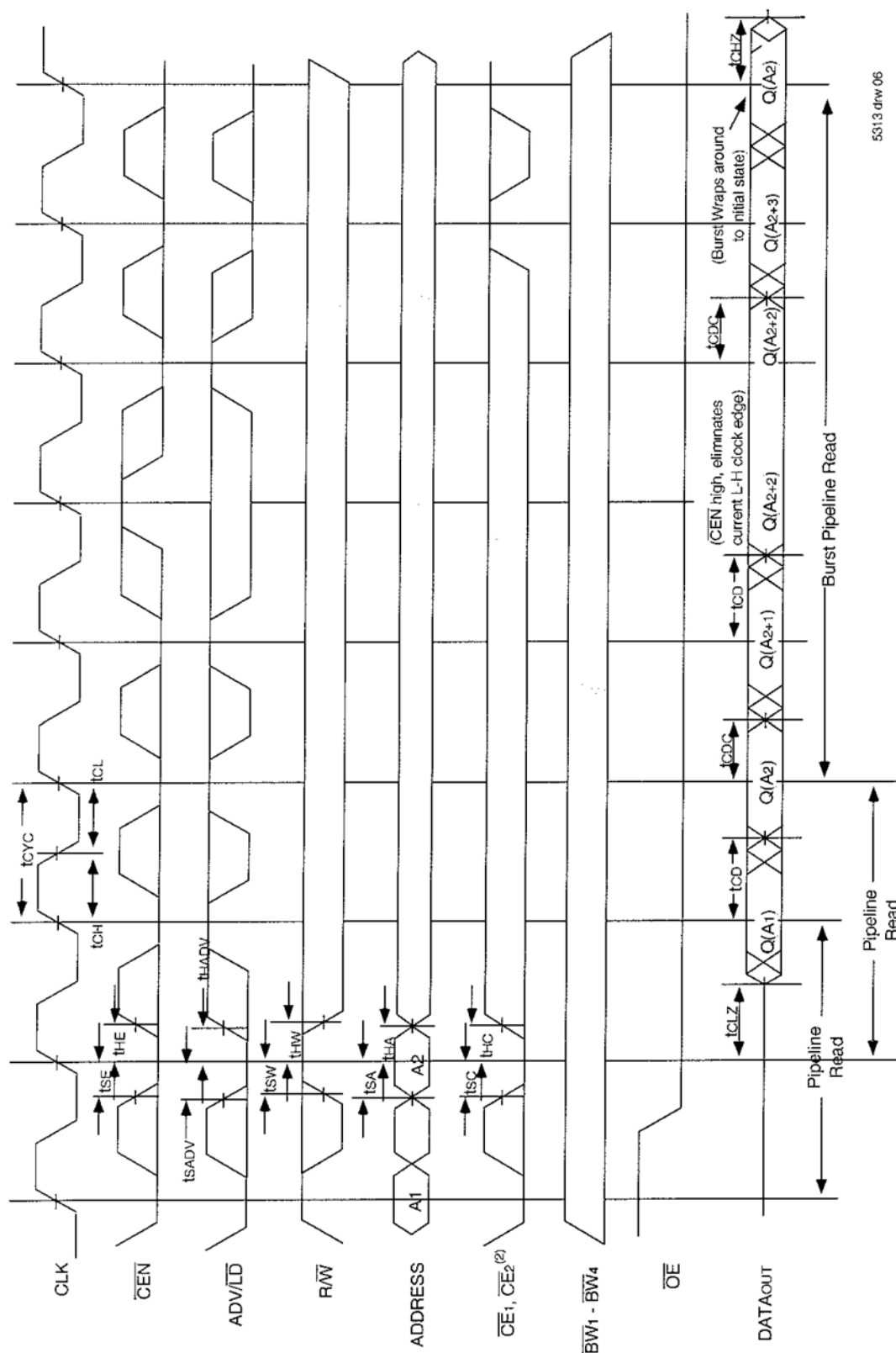
1 t<sub>F</sub> = 1/t<sub>CYC</sub>2 Measured as HIGH above 0.6V<sub>DD</sub> and LOW below 0.4V<sub>DD</sub>.

3 Transition is measured ±200mV from steady-state

4 These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.

5 To avoid bus contention, the output buffers are designed such that t<sub>CHZ</sub> (device turn-off) is faster than t<sub>CLZ</sub> (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because t<sub>CLZ</sub> is a Min. parameter that is worse case at totally different test conditions (0 deg C, 2.625V) than t<sub>CHZ</sub> which is a Max. parameter (worse case at 70 deg C, 2.375V).

# Timing Waveform of Read Cycle<sup>(1,2,3,4)</sup>



5313 drw 06

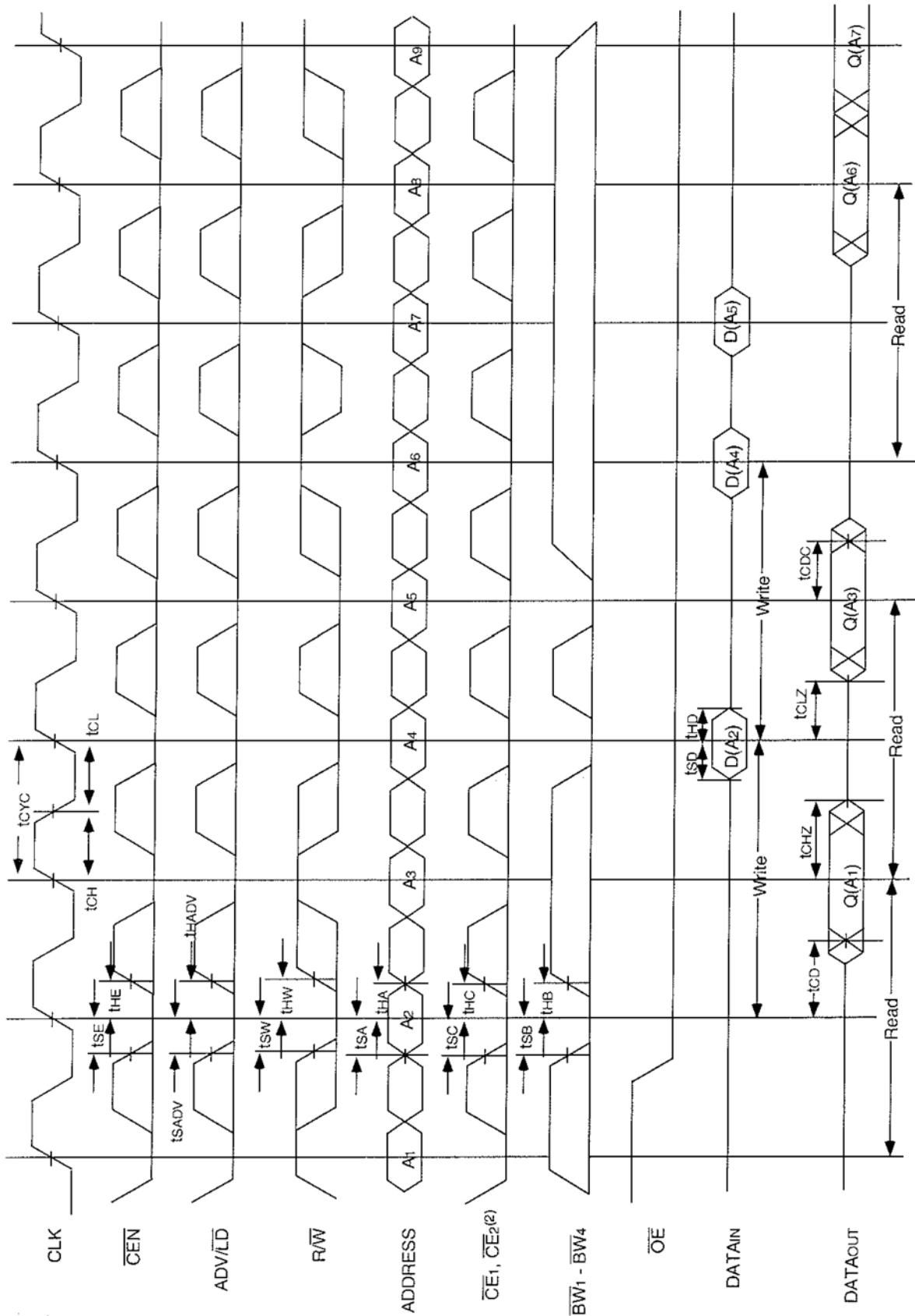
## NOTES:

1. Q(A1) represents the first output from the external address A1. Q(A2) represents the first output from the external address A2; Q(A2+1) represents the next output data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. CE2 timing transitions are identical but inverted to the CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD LOW.
4. R/W is don't care when the SRAM is bursting (ADV/LD sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/W signal when new address and control are loaded into the SRAM.

Timing diagram for burst pipeline write operation. The diagram shows signals CLK, CEN, ADVLD, RW, ADDRESS (A1, A2), CE1, CE2<sup>(2)</sup>, BW1-BW4, OE, and DATIN. It illustrates the sequence of events for a burst write, including address strobes, data strobes, and pipeline write operations. Key timing parameters like tCYC, tCH, tSE, tAE, tSA, tSC, tSW, tSH, tSA, tSC, tSB, tSH, tHD, tSD, and tHLD are indicated. The diagram is divided into two sections: Pipeline Write and Burst Pipeline Write. The Burst Pipeline Write section shows a sequence of data writes D(A1), D(A2), D(A2+1), D(A2+2), and D(A2+3) with wrap-around from the initial state.

1. D (A1) represents the first input to the external address A1. D (A2) represents the first input to the external address A2; D (A2+1) represents the next input data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. CE2 timing transitions are identical but inverted to the  $\overline{\text{CE1}}$  and  $\overline{\text{CE2}}$  signals. For example, when  $\overline{\text{CE1}}$  and  $\overline{\text{CE2}}$  are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD LOW.
4.  $\overline{\text{RW}}$  is don't care when the SRAM is bursting (ADV/LD sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the  $\overline{\text{RW}}$  signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals ( $\overline{\text{BWx}}$ ) must be valid on all write and burst-write cycles. A write cycle is initiated when  $\overline{\text{RW}}$  signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

## Timing Waveform of Combined Read and Write Cycles<sup>(1,2,3)</sup>

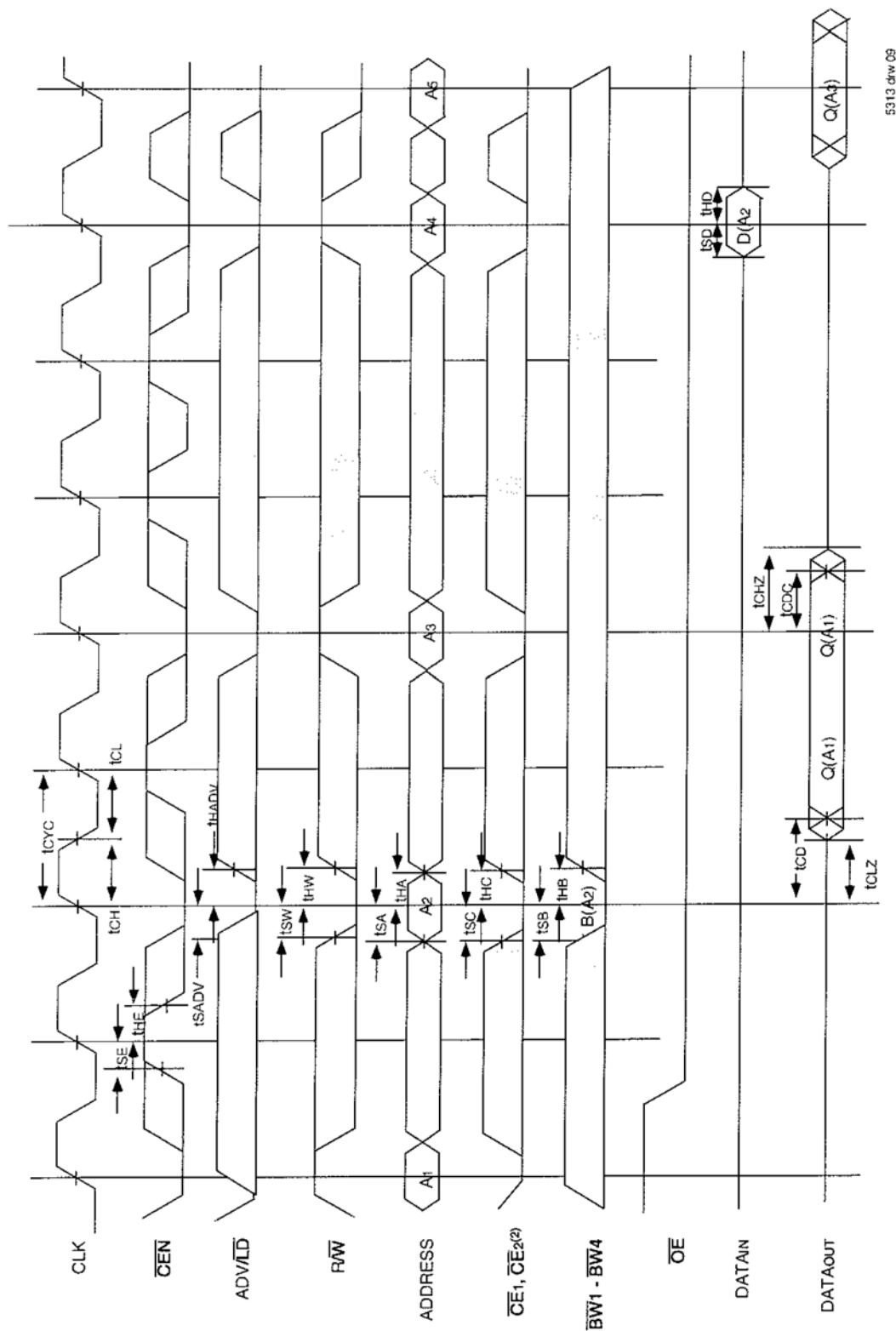


5313 drw 08

### NOTES:

1. Q(A1) represents the first output from the external address A1. D(A2) represents the input data to the SRAM corresponding to address A2.
2. CE2 timing transitions are identical but inverted to the CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE2 is HIGH.
3. Individual Byte Write signals (BWx) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

## Timing Waveform of $\overline{\text{CEN}}$ Operation<sup>(1,2,3,4)</sup>

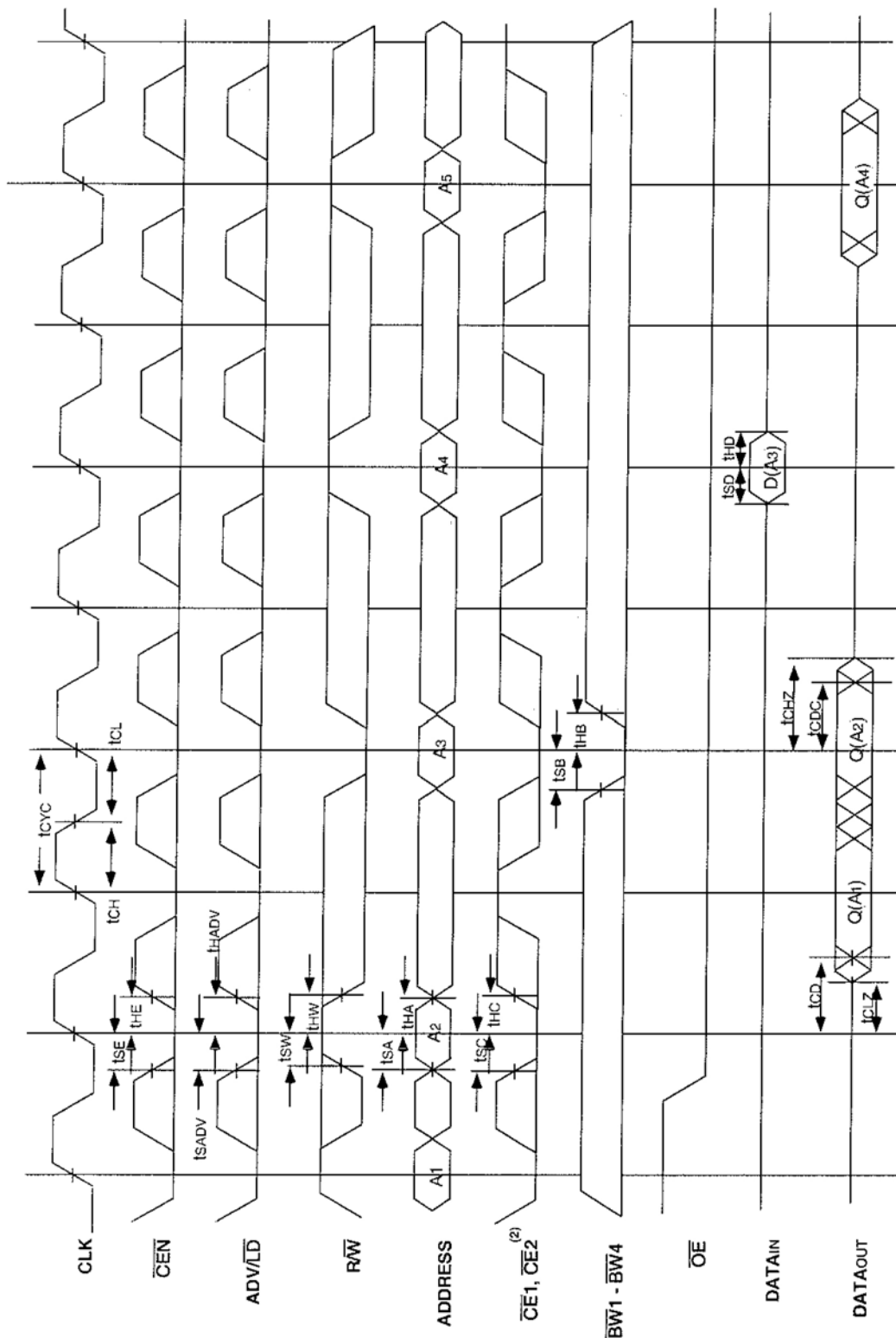


5313 drw 09

### NOTES:

1. Q(A1) represents the first output from the external address A1. D(A2) represents the input data to the SRAM corresponding to address A2.
2.  $\overline{\text{CE1}}$  and  $\overline{\text{CE2}}$  timing transitions are identical but inverted to the  $\overline{\text{CE1}}$  and  $\overline{\text{CE2}}$  signals. For example, when  $\overline{\text{CE1}}$  and  $\overline{\text{CE2}}$  are LOW on this waveform,  $\overline{\text{CE2}}$  is HIGH.
3.  $\overline{\text{CEN}}$  when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ( $\overline{\text{BWx}}$ ) must be valid on all write and burst-write cycles. A write cycle is initiated when  $\overline{\text{RW}}$  signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

## Timing Waveform of $\overline{CS}$ Operation<sup>(1,2,3,4)</sup>

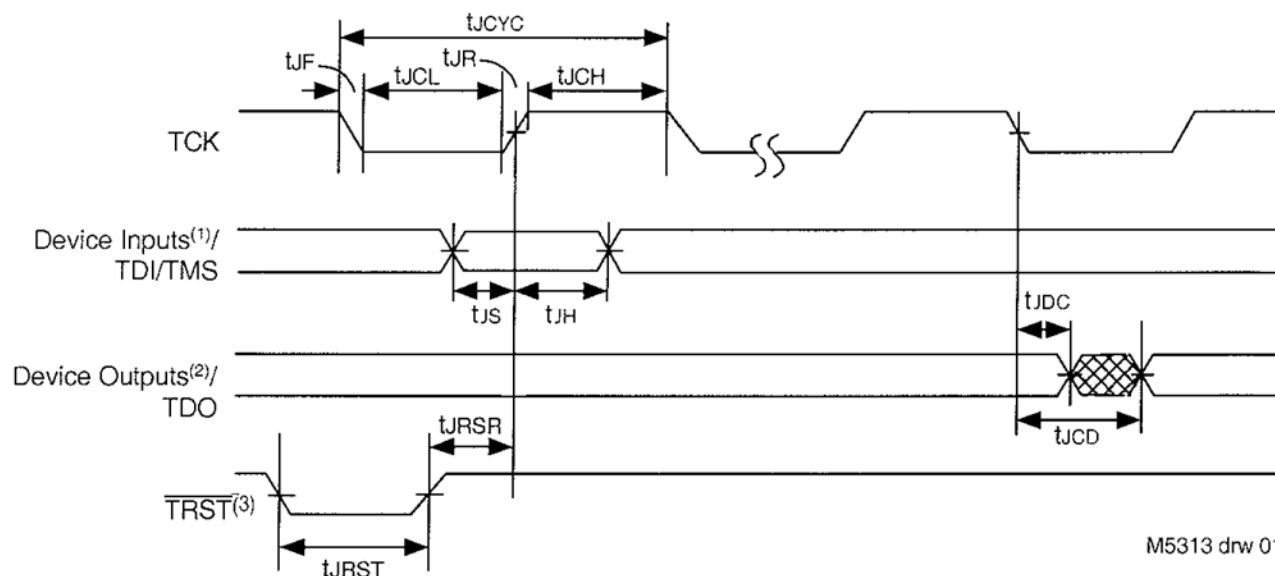


5313 d/w 10

### NOTES:

1. Q(A1) represents the first output from the external address A1. D(A3) represents the input data to the SRAM corresponding to address A3.
2. CE2 timing transitions are identical but inverted to the CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE2 is HIGH.
3. CEN when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals (BWx) must be valid on all write and burst-write cycles. A write cycle is initiated when RW signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

## JTAG Interface Specification



### NOTES:

- 1 Device inputs = All device inputs except TDI, TMS and  $\overline{\text{TRST}}$
- 2 Device outputs = All device outputs except TDO
- 3 During power up,  $\overline{\text{TRST}}$  could be driven low or not be used since the JTAG circuit resets automatically.  $\overline{\text{TRST}}$  is an optional JTAG reset.

## JTAG AC Electrical Characteristics<sup>(1,2,3,4)</sup>

| Symbol            | Parameter               |      |                  |       |
|-------------------|-------------------------|------|------------------|-------|
|                   |                         | Min. | Max.             | Units |
| t <sub>JCYC</sub> | JTAG Clock Input Period | 100  | —                | ns    |
| t <sub>JCH</sub>  | JTAG Clock HIGH         | 40   | —                | ns    |
| t <sub>JCL</sub>  | JTAG Clock Low          | 40   | —                | ns    |
| t <sub>JR</sub>   | JTAG Clock Rise Time    | —    | 5 <sup>(1)</sup> | ns    |
| t <sub>JF</sub>   | JTAG Clock Fall Time    | —    | 5 <sup>(1)</sup> | ns    |
| t <sub>JRST</sub> | JTAG Reset              | 50   | —                | ns    |
| t <sub>JRSR</sub> | JTAG Reset Recovery     | 50   | —                | ns    |
| t <sub>JCD</sub>  | JTAG Data Output        | —    | 20               | ns    |
| t <sub>JDC</sub>  | JTAG Data Output Hold   | 0    | —                | ns    |
| t <sub>JS</sub>   | JTAG Setup              | 25   | —                | ns    |
| t <sub>JH</sub>   | JTAG Hold               | 25   | —                | ns    |

M5313 tbl 01

## Scan Register Sizes

| Register Name              | Bit Size |
|----------------------------|----------|
| Instruction (IR)           | 4        |
| Bypass (BYR)               | 1        |
| JTAG Identification (JIDR) | 32       |
| Boundary Scan (BSR)        | Note (1) |

M5313 tbl 03

### NOTE:

- 1 The Boundary Scan Descriptive Language (BSDL) file for this device is available.

### NOTES:

- 1 Guaranteed by design
- 2 AC Test Load (Fig. 1) on external output signals
- 3 Refer to AC Test Conditions stated earlier in this document
- 4 JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet

## JTAG Identification Register Definitions

| Instruction Field                 | Value        | Description                                                 |
|-----------------------------------|--------------|-------------------------------------------------------------|
| Revision Number (31:28)           | 0x2          | Reserved for version number.                                |
| IDT Device ID (27:12)             | 0x220, 0x222 | Defines part number AS8C163631 and AS8C161831, respectively |
| IDT JEDEC ID (11:1)               | 0x33         | Allows unique identification of device vendor               |
| ID Register Indicator Bit (Bit 0) | 1            | Indicates the presence of an ID register                    |

5313 tbl 02

## Available JTAG Instructions

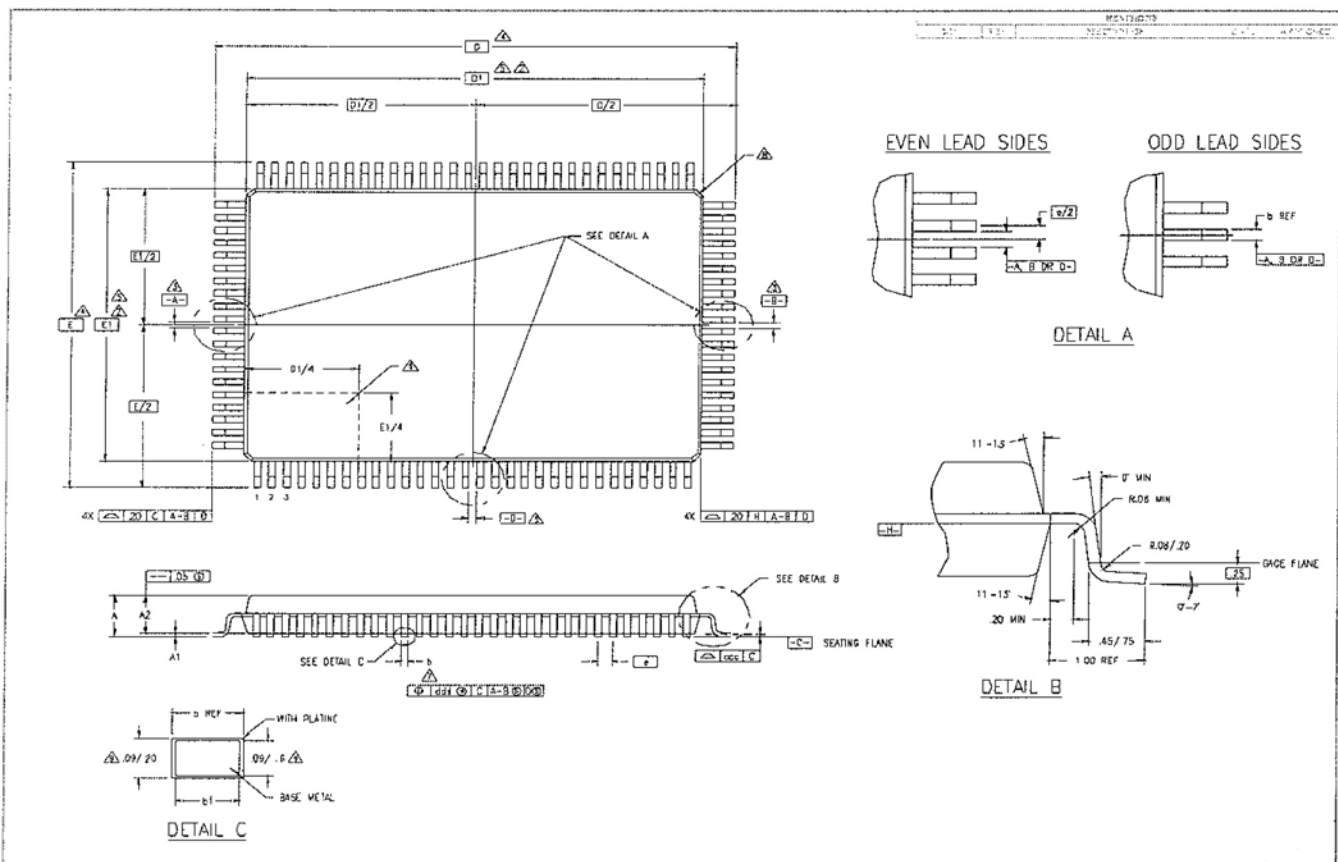
| Instruction    | Description                                                                                                                                                                                                                                                                                                 | OPCODE |
|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|
| EXTEST         | Forces contents of the boundary scan cells onto the device outputs <sup>(1)</sup><br>Places the boundary scan register (BSR) between TDI and TDO                                                                                                                                                            | 0000   |
| SAMPLE/PRELOAD | Places the boundary scan register (BSR) between TDI and TDO<br>SAMPLE allows data from device inputs <sup>(2)</sup> and outputs <sup>(1)</sup> to be captured in the boundary scan cells and shifted serially through TDO PRELOAD allows data to be input serially into the boundary scan cells via the TDI | 0001   |
| DEVICE_ID      | Loads the JTAG ID register (JIDR) with the vendor ID code and places the register between TDI and TDO                                                                                                                                                                                                       | 0010   |
| HIGHZ          | Places the bypass register (BYR) between TDI and TDO Forces all device output drivers to a High-Z state                                                                                                                                                                                                     | 0011   |
| RESERVED       | Several combinations are reserved. Do not use codes other than those identified for EXTEST, SAMPLE/PRELOAD, DEVICE_ID, HIGHZ, CLAMP, VALIDATE and BYPASS instructions                                                                                                                                       | 0100   |
| RESERVED       |                                                                                                                                                                                                                                                                                                             | 0101   |
| RESERVED       |                                                                                                                                                                                                                                                                                                             | 0110   |
| RESERVED       |                                                                                                                                                                                                                                                                                                             | 0111   |
| CLAMP          | Uses BYR Forces contents of the boundary scan cells onto the device outputs Places the bypass register (BYR) between TDI and TDO                                                                                                                                                                            | 1000   |
| RESERVED       | Same as above                                                                                                                                                                                                                                                                                               | 1001   |
| RESERVED       |                                                                                                                                                                                                                                                                                                             | 1010   |
| RESERVED       |                                                                                                                                                                                                                                                                                                             | 1011   |
| RESERVED       |                                                                                                                                                                                                                                                                                                             | 1100   |
| VALIDATE       | Automatically loaded into the instruction register whenever the TAP controller passes through the CAPTURE-IR state. The lower two bits '01' are mandated by the IEEE std 1149.1 specification                                                                                                               | 1101   |
| RESERVED       | Same as above                                                                                                                                                                                                                                                                                               | 1110   |
| BYPASS         | The BYPASS instruction is used to truncate the boundary scan register as a single bit in length                                                                                                                                                                                                             | 1111   |

5313 tbl 04

### NOTES:

- 1 Device outputs = All device outputs except TDO
- 2 Device inputs = All device inputs except TDI TMS and TRST

## 100-Pin Thin Quad Flatpack (TQFP) Package Diagram Outline

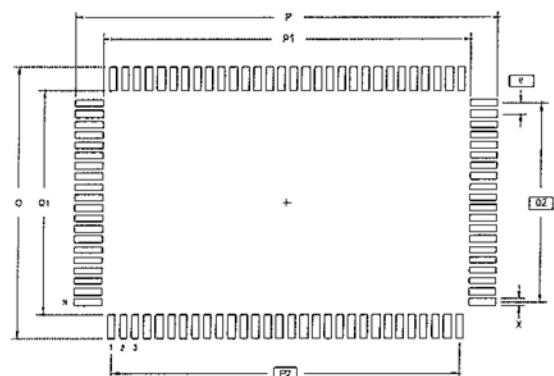


| SYMBOL | JEDEC VARIATION |      |      | PITCH |
|--------|-----------------|------|------|-------|
|        | MIN             | NOM  | MAX  |       |
| A      | —               | —    | 1.60 |       |
| A1     | .05             | .10  | .15  |       |
| A2     | 1.35            | 1.40 | 1.45 |       |
| D      | 22.00 BSC       |      |      | 4     |
| D1     | 20.00 BSC       |      |      | 5.2   |
| E      | 16.00 BSC       |      |      | 4     |
| E1     | 14.00 BSC       |      |      | 5.2   |
| N      | 100             |      |      |       |
| N0     | 30              |      |      |       |
| NE     | 20              |      |      |       |
| e      | .65 BSC         |      |      |       |
| b      | .22             | .32  | .38  | 7     |
| b1     | .22             | .30  | .35  |       |
| ccc    | —               | —    | .10  |       |
| ddd    | —               | —    | 1.3  |       |

### NOTES:

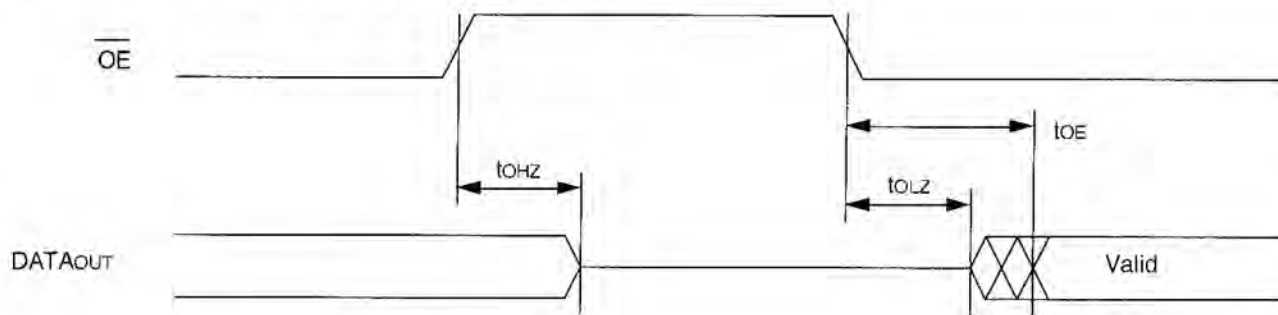
- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- 2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
- 3 DATUMS [A-B] AND [D-E] TO BE DETERMINED AT DATUM PLANE [H-I]
- 4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [C-E]
- 5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD VENTHATCH
- 6 DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- 7 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADII OR THE FOOT.
- 8 EXACT SHAPE OF EACH CORNER IS OPTIONAL
- 9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- 10 ALL DIMENSIONS ARE IN MILLIMETERS
- 11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-135 VARIATION QJ AND BX

### LAND PATTERN DIMENSIONS



|    | MIN       | MAX   |
|----|-----------|-------|
| P  | 22.80     | 23.00 |
| P1 | 19.80     | 20.00 |
| P2 | 18.65 BSC |       |
| Q  | 16.80     | 17.00 |
| Q1 | 13.80     | 14.00 |
| Q2 | 12.35 BSC |       |
| X  | .30       | .50   |
| e  | .65 BSC   |       |
| N  | 100       |       |

## Timing Waveform of $\overline{OE}$ Operation<sup>(1)</sup>



5313 drw 11

**NOTE:**
<sup>1</sup> A read operation is assumed to be in progress

## ORDERING INFORMATION

| Alliance          | Organization | VCC Range  | Package      | Operating Temp     | Speed Mhz |
|-------------------|--------------|------------|--------------|--------------------|-----------|
| AS8C163631-QC166N | 512K x 36    | 2.3 - 2.6V | 100 pin TQFP | Comercial: 0 - 70C | 166       |
| AS8C161831-QC166N | 1M x 18      | 2.3 - 2.6V | 100 pin TQFP | Comercial: 0 - 70C | 166       |

## PART NUMBERING SYSTEM

| AS8C                 | Device   | Conf.               | Mode                                                                 | Package          | Operating Temp | Speed  | N           |
|----------------------|----------|---------------------|----------------------------------------------------------------------|------------------|----------------|--------|-------------|
| Sync.<br>SRAM prefix | 16 = 16M | 18= x18<br>36 = x36 | 01= ZBT<br>00 = Pipelined<br>25 = Flow- Thru<br>31 = ZBT (Pipelined) | Q = 100 Pin TQFP | 0 ~ 70C        | 166MHz | N= Leadfree |



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