

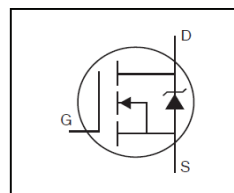
## Features

- Advanced Process Technology
- Ultra Low On-Resistance
- Logic Level Gate Drive
- 150°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to  $T_{jmax}$
- Lead-Free, RoHS Compliant
- Automotive Qualified \*

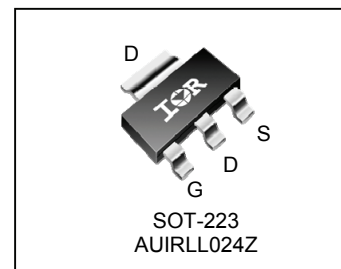
## Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

## HEXFET® Power MOSFET



$V_{DSS}$	<b>55V</b>
$R_{DS(on)}$ typ.	<b>48mΩ</b>
max.	<b>60mΩ</b>
$I_D$	<b>5.0A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRLL024Z	SOT-223	Tape and Reel	2500	AUIRLL024ZTR

## Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature ( $T_A$ ) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ⑦	5.0	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ⑦	4.0	
$I_{DM}$	Pulsed Drain Current ①	40	
$P_D @ T_A = 25^\circ\text{C}$	Maximum Power Dissipation (PCB Mount) ⑦	2.8	W
$P_D @ T_A = 25^\circ\text{C}$	Maximum Power Dissipation (PCB Mount) ⑧	1.0	
	Linear Derating Factor (PCB Mount) ⑦	0.02	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 16	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ②	21	mJ
$E_{AS} \text{ (Tested)}$	Single Pulse Avalanche Energy (Tested Value) ⑥	38	
$I_{AR}$	Avalanche Current ①	See Fig. 12a, 12b, 15, 16	A
$E_{AR}$	Repetitive Avalanche Energy ⑤		mJ
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		

## Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑦	—	45	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑧	—	120	

HEXFET® is a registered trademark of Infineon.

\*Qualification standards can be found at [www.infineon.com](http://www.infineon.com)

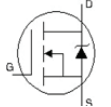
**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.049	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	48	60	m $\Omega$	$V_{GS} = 10V, I_D = 3.0A$ ③
		—	—	80		$V_{GS} = 5.0V, I_D = 3.0A$ ③
		—	—	100		$V_{GS} = 4.5V, I_D = 3.0A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Trans conductance	7.5	—	—	S	$V_{DS} = 25V, I_D = 3.0A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 55V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -16V$

**Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

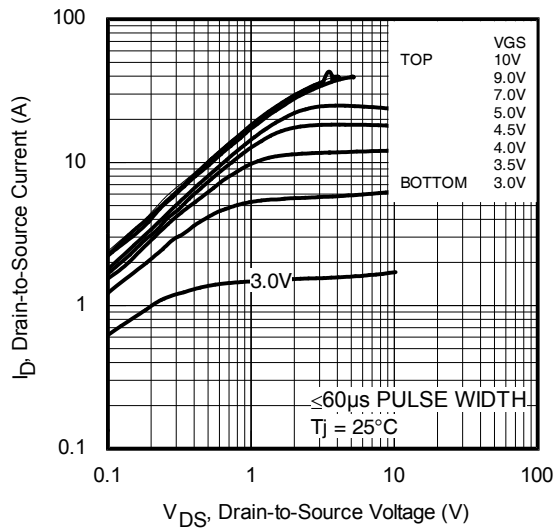
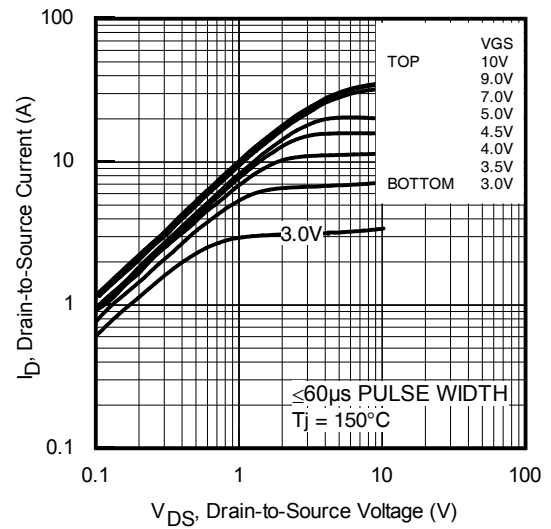
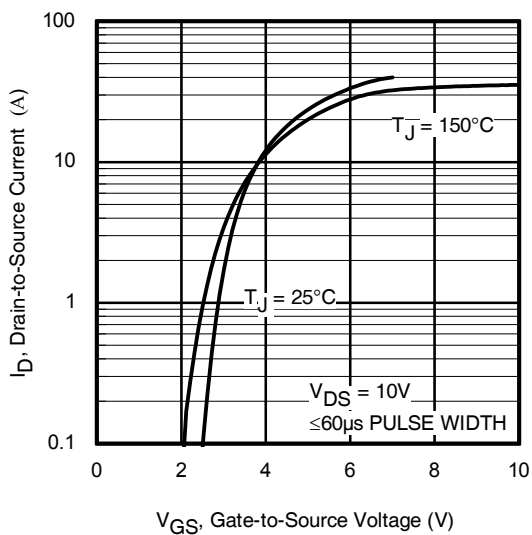
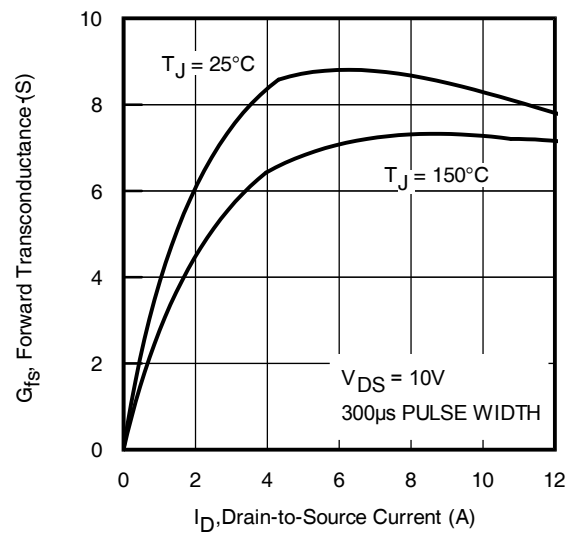
$Q_g$	Total Gate Charge	—	7.0	11	nC	$I_D = 3.0A$
$Q_{gs}$	Gate-to-Source Charge	—	1.5	—		$V_{DS} = 44V$
$Q_{gd}$	Gate-to-Drain Charge	—	4.0	—		$V_{GS} = 5.0V$ ③
$t_{d(on)}$	Turn-On Delay Time	—	8.6	—	ns	$V_{DD} = 28V$
$t_r$	Rise Time	—	33	—		$I_D = 3.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	20	—		$R_G = 56\Omega$
$t_f$	Fall Time	—	15	—		$V_{GS} = 5.0V$ ③
$C_{iss}$	Input Capacitance	—	380	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	66	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	36	—		$f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	220	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	53	—		$V_{GS} = 0V, V_{DS} = 44V, f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	93	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 44V$ ④

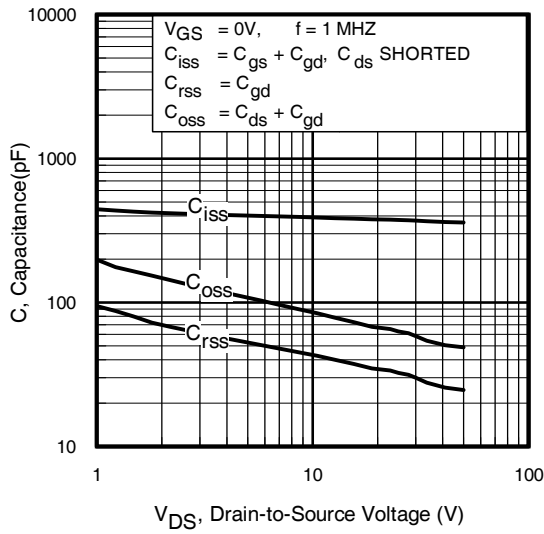
**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	5.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	40		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 3.0A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	15	23	ns	$T_J = 25^\circ\text{C}, I_F = 3.0A, V_{DD} = 28V$
$Q_{rr}$	Reverse Recovery Charge	—	9.1	14	nC	$di/dt = 100A/\mu s$ ③
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

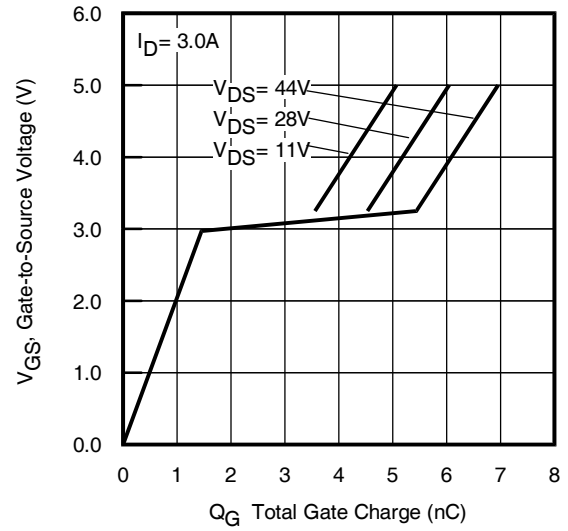
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Limited by  $T_{Jmax}$ , Starting  $T_J = 25^\circ\text{C}$ ,  $L = 4.8\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 3.0A$ ,  $V_{GS} = 10V$ . Part not recommended for use above this value.
- ③ Pulse width  $\leq 1.0\text{ms}$ ; duty cycle  $\leq 2\%$ .
- ④  $C_{oss \text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑤ Limited by  $T_{Jmax}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population, starting  $T_J = 25^\circ\text{C}$ ,  $L = 4.8\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 3.0A$ ,  $V_{GS} = 10V$ .
- ⑦ When mounted on 1 inch square copper board.
- ⑧ When mounted on FR-4 board using minimum recommended footprint.

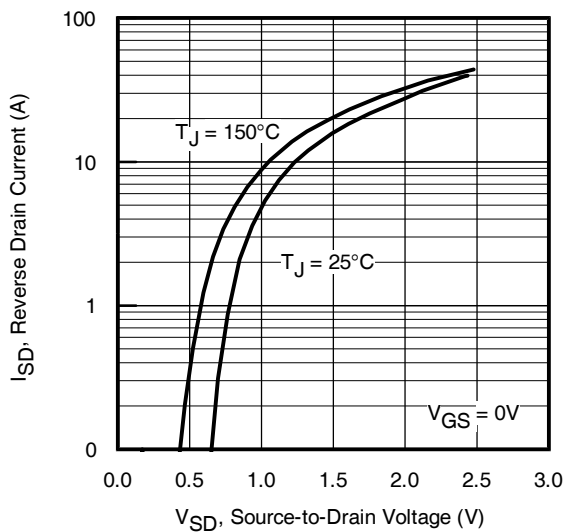

**Fig. 1** Typical Output Characteristics

**Fig. 2** Typical Output Characteristics

**Fig. 3** Typical Transfer Characteristics

**Fig. 4** Typical Forward Trans conductance vs. Drain Current



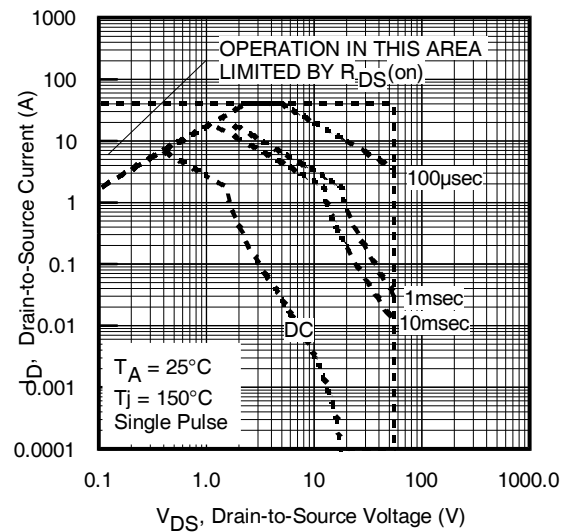
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



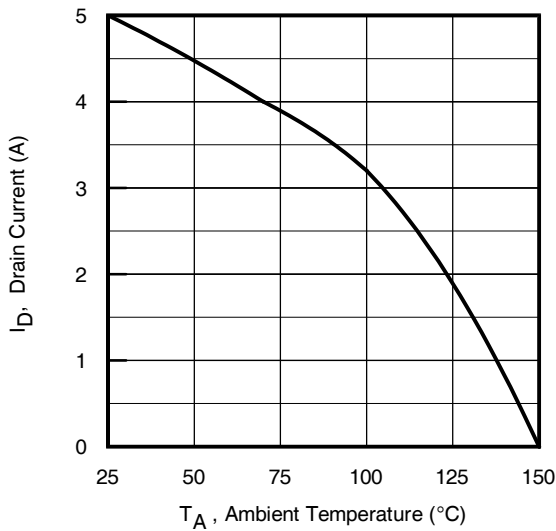
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



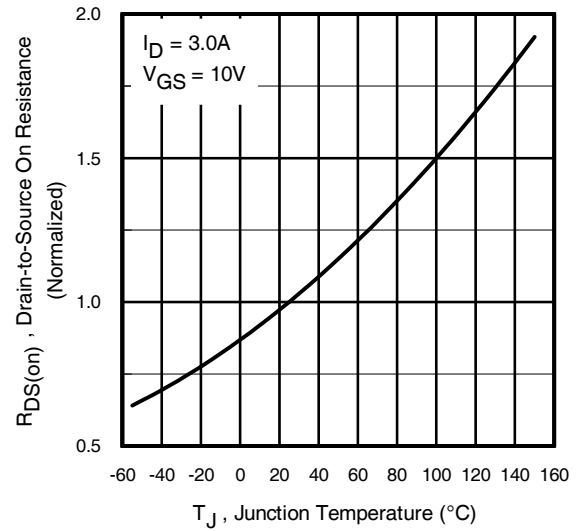
**Fig. 7** Typical Source-to-Drain Diode Forward Voltage



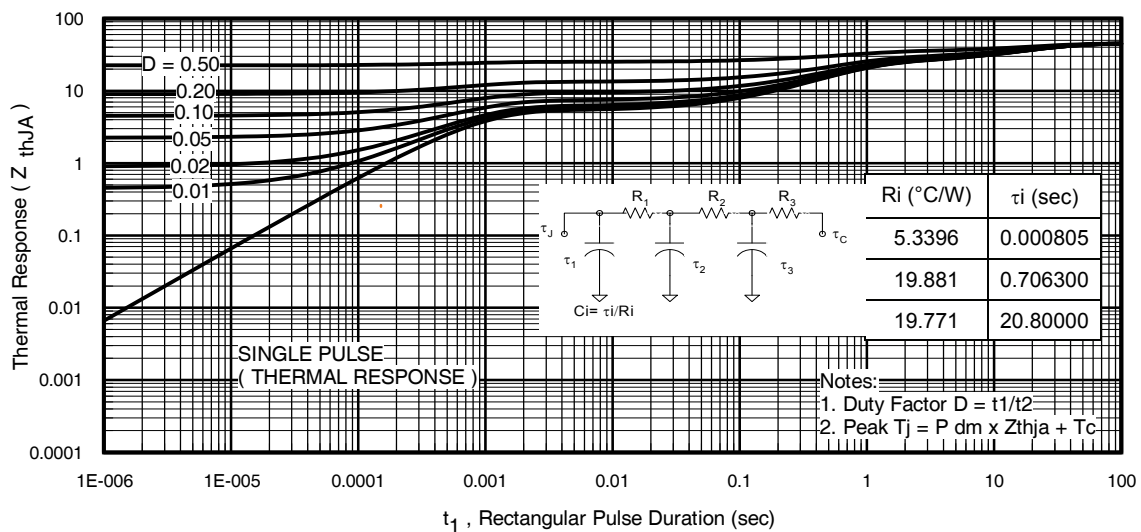
**Fig 8.** Maximum Safe Operating Area



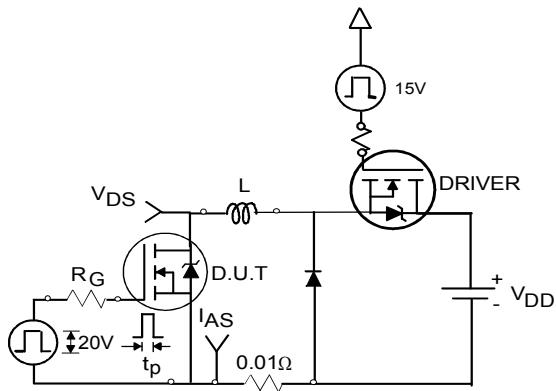
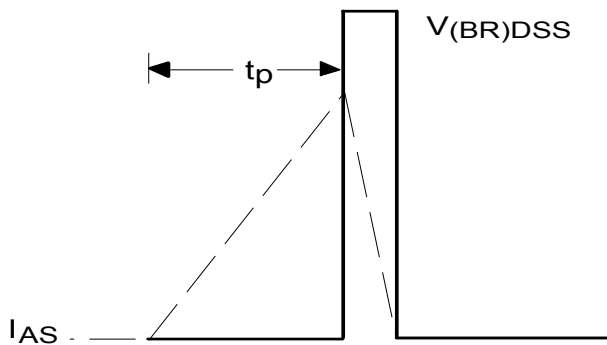
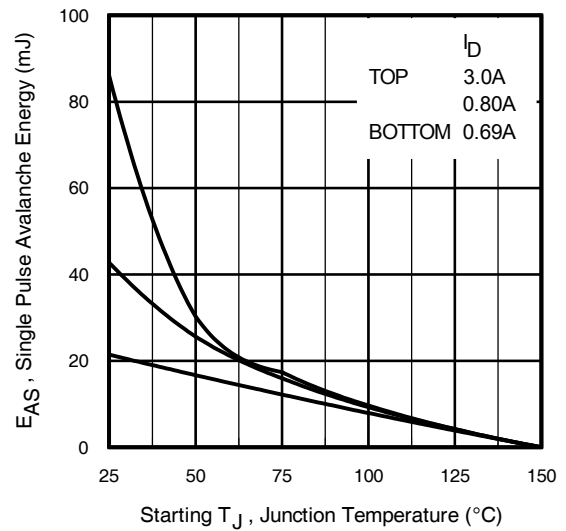
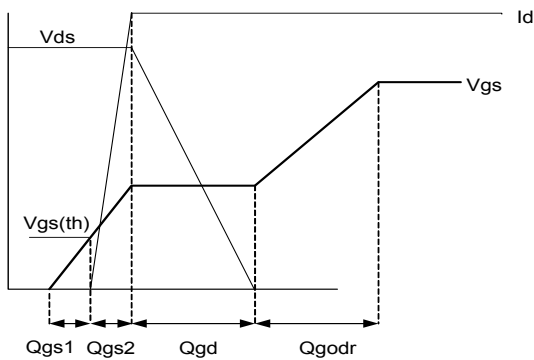
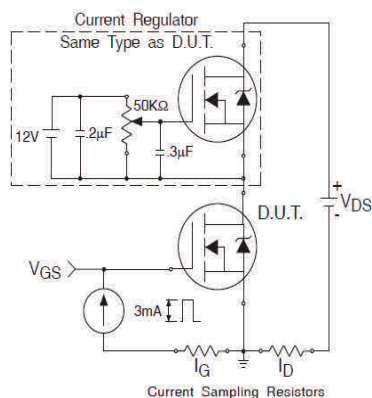
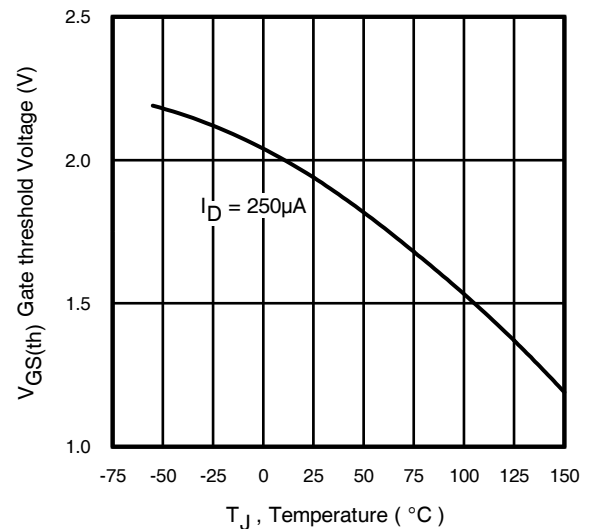
**Fig 9.** Maximum Drain Current Vs. Ambient Temperature

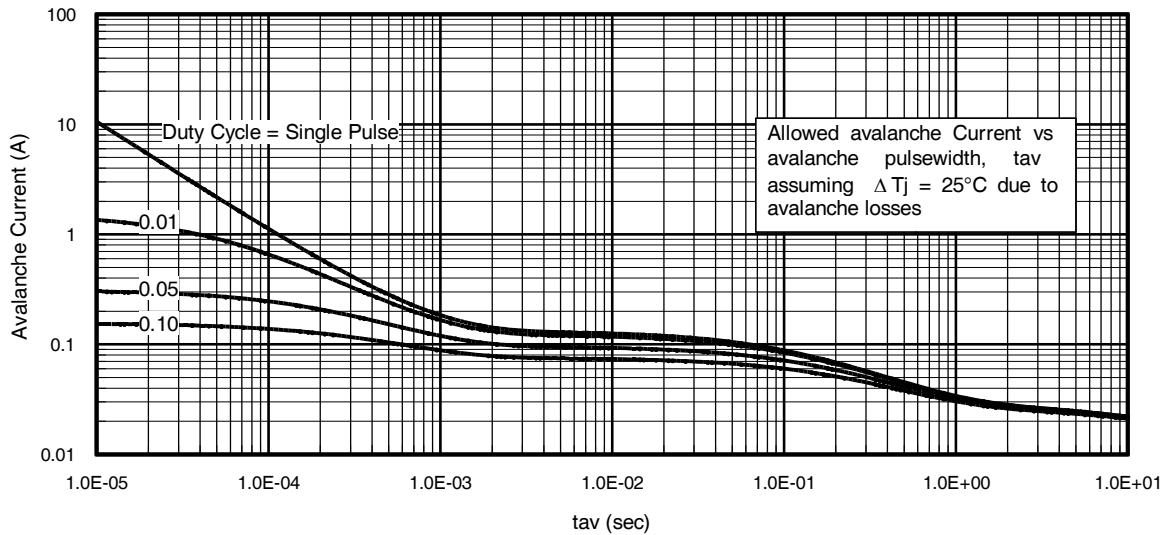


**Fig 10.** Normalized On-Resistance vs. Temperature

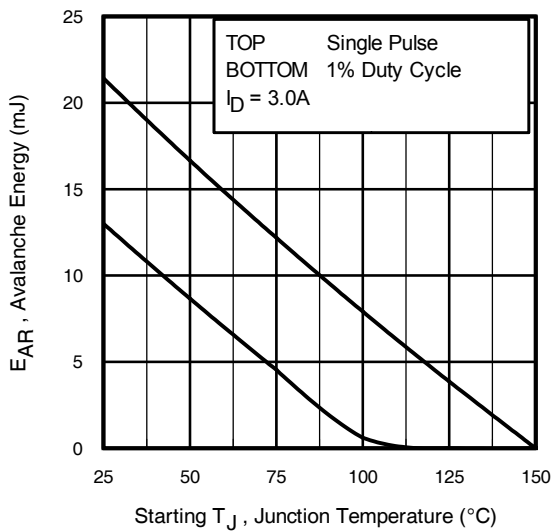


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient


**Fig 12a.** Unclamped Inductive Test Circuit

**Fig 12b.** Unclamped Inductive Waveforms

**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

**Fig 13a.** Basic Gate Charge Waveform

**Fig 13b.** Gate Charge Test Circuit

**Fig 14.** Threshold Voltage vs. Temperature



**Fig 15.** Typical Avalanche Current vs. Pulse width



**Fig 16.** Maximum Avalanche Energy vs. Temperature

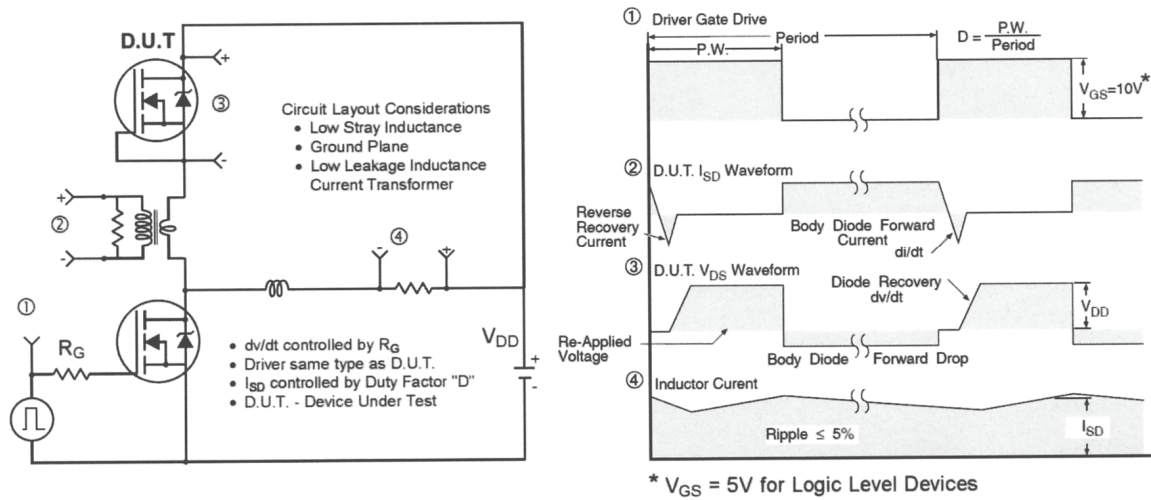
**Notes on Repetitive Avalanche Curves , Figures 15, 16:**  
(For further info, see AN-1005 at [www.infineon.com](http://www.infineon.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

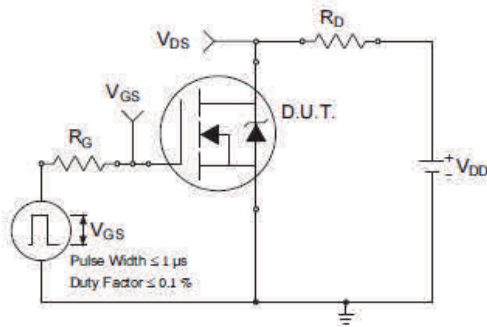
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

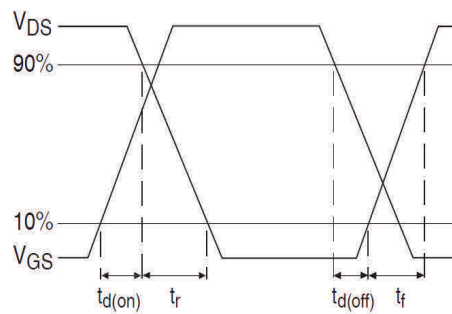
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



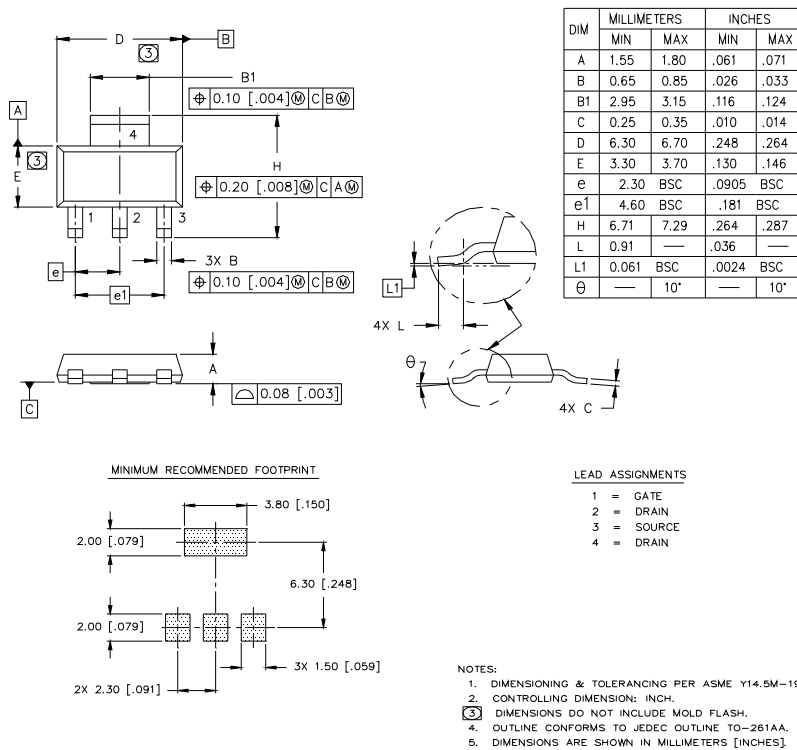
**Fig 18a.** Switching Time Test Circuit



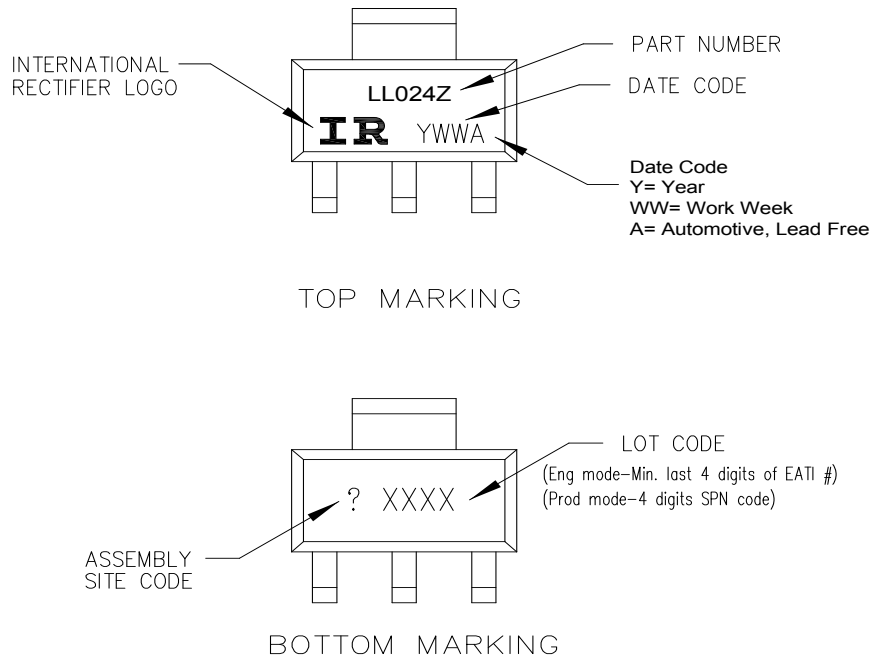
**Fig 18b.** Switching Time Waveforms



# SOT-223 (TO-261AA) Package Outline (Dimensions are shown in millimeters (inches))

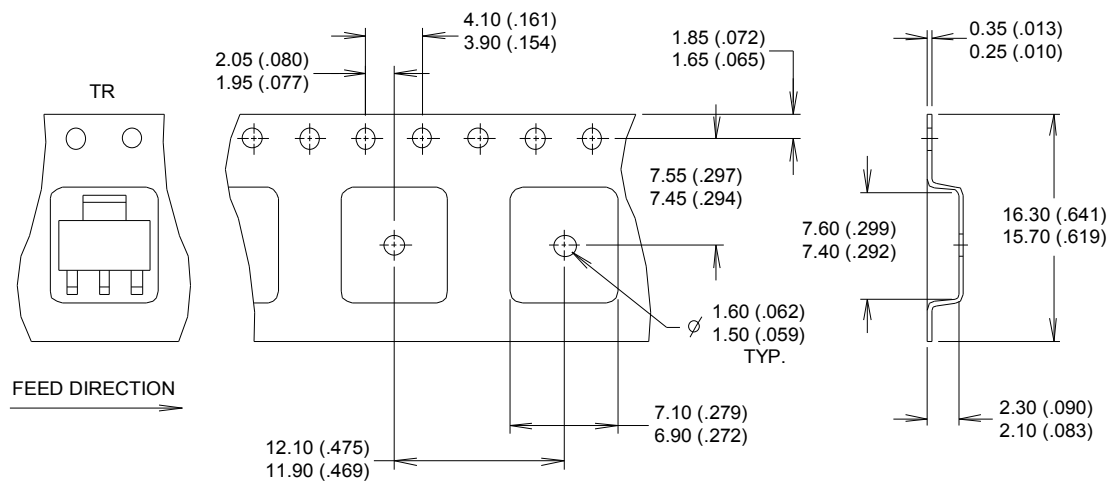


## SOT-223(TO-261AA) Part Marking Information



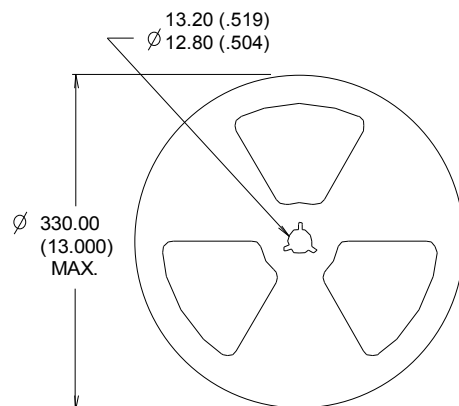
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**SOT-223(TO-261AA) Tape and Reel** (Dimensions are shown in millimeters (inches))



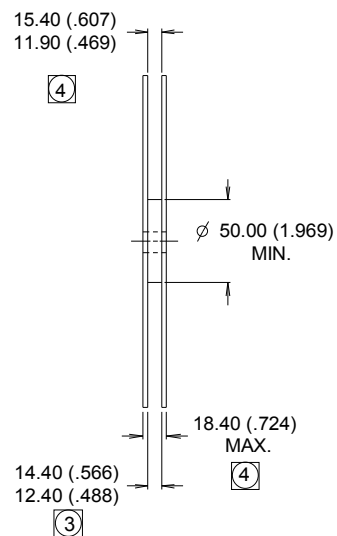
NOTES :

1. CONTROLLING DIMENSION: MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.
3. EACH 0330.00 (13.00) REEL CONTAINS 2,500 DEVICES.



NOTES :

1. OUTLINE COMFORMS TO EIA-418-1.
2. CONTROLLING DIMENSION: MILLIMETER..
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information**

<b>Qualification Level</b>		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		SOT-223	MSL1
<b>ESD</b>	Machine Model	Class M1B (+/- 100V) <sup>†</sup> AEC-Q101-002	
	Human Body Model	Class H0 (+/- 250V) <sup>†</sup> AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 1125V) <sup>†</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

† Highest passing voltage.

**Revision History**

Date	Comments
3/26/2014	<ul style="list-style-type: none"> <li>Added "Logic Level Gate Drive" bullet in the features section on page 1</li> <li>Updated part marking on page 9</li> <li>Updated data sheet with new IR corporate template</li> </ul>
10/29/2015	<ul style="list-style-type: none"> <li>Updated datasheet with corporate template</li> <li>Corrected ordering table on page 1.</li> </ul>

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