AWT6651

High Efficiency ProEficient™
UMTS2100 (Band 1)
LTE/WCDMA/TD-SCDMA Linear PAM
DATA SHEET - Rev 2.2

FEATURES

- WCDMA/HSPA, LTE and TD-SCDMA Compliant
- High Efficiency (R99 waveform):
  - 48% @ POUT = +28.5 dBm
  - 25% @ POUT = +17 dBm in LPM, without DC/DC Converter
- Simple Calibration with only 2 Bias Modes
- Optimized for SMPS Supply
- Low Leakage Current in Shutdown Mode: <5 μA
- Internal Voltage Regulator
- Integrated "daisy chainable" directional couplers with CPLIN and CPLOUT Ports
- Optimized for a 50 Ω System
- Internal DC blocks on IN/OUT RF ports
- 1.8 V Control Logic
- RoHS Compliant Package, 260 °C MSL-3

10 Pin 3 mm x 3 mm x 0.9 mm Surface Mount Module

APPLICATIONS

- Wireless Handsets and Data Devices for:
  - WCDMA/HSPA/LTE IMT-Band
  - TD-SCDMA 1.8/2.0 GHz Band

PRODUCT DESCRIPTION

The AWT6651 PA is designed to provide highly linear output for WCDMA, LTE and TD-SCDMA handsets and data devices with high efficiency at both high and low power modes. This ProEficient™ PA can be used with an external switch mode power supply (SMPS) to improve its efficiency and reduce current consumption further at medium and low output powers. The device is manufactured on an advanced InGaP HBT MMIC technology offering state-of-the-art reliability, temperature stability, and ruggedness. There are two selectable bias modes that optimize efficiency for different output power levels, and a shutdown mode with low leakage current, which increases handset talk and standby time. The self-contained 3 mm x 3 mm x 0.9 mm surface mount package incorporates matching networks optimized for output power, efficiency, and linearity in a 50 Ω system.

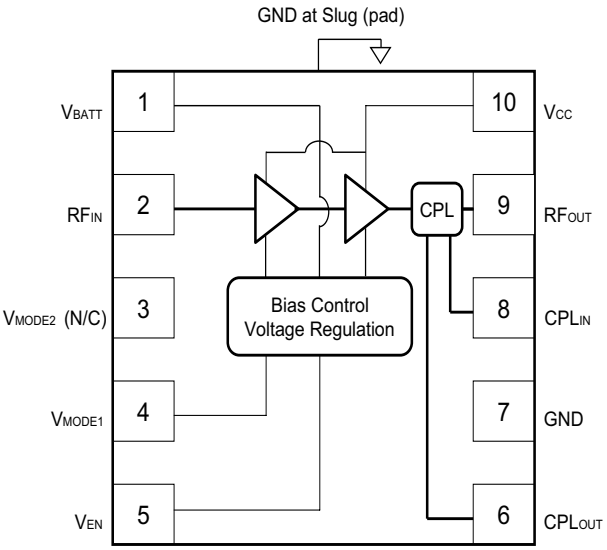


Figure 1: Block Diagram

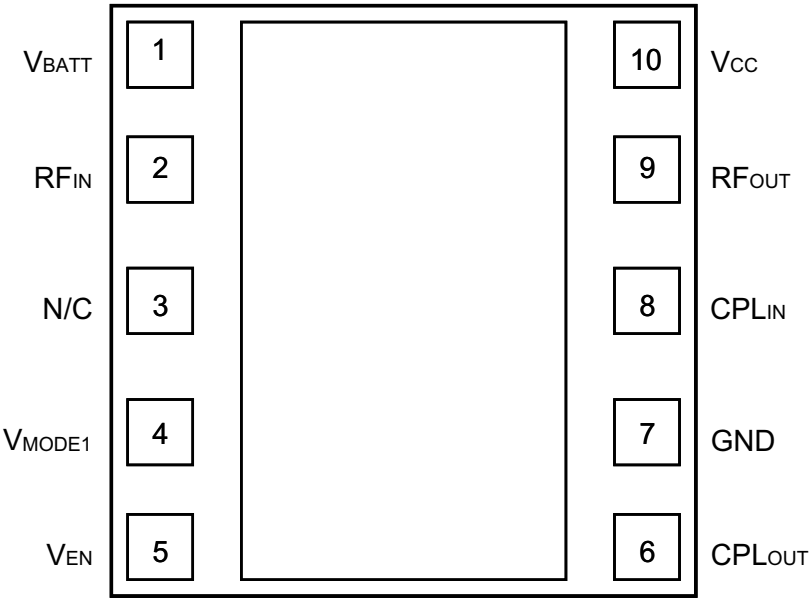


Figure 2: Pinout (X-ray Top View)

Table 1: Pin Description

PIN	NAME	DESCRIPTION
1	V_{BATT}	Battery Voltage
2	RF_{IN}	RF Input
3	N/C	No Connection
4	V_{MODE1}	Mode Control Voltage 1
5	V_{EN}	PA Enable Voltage
6	CPL_{OUT}	Coupler Output
7	GND	Ground
8	CPL_{IN}	Coupler Input
9	RF_{OUT}	RF Output
10	V_{CC}	Supply Voltage

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	TYP	MAX	UNIT
RF Input (P_{IN})	-	0	10	dBm
V_{CC}	0	3.4	5	V
V_{BATT}	0	3.4	6	V
Control Voltage (V_{ENABLE}, V_{MODE})	0	1.8	3.5	V
Storage Temperature ($T_{STORAGE}$)	-40	25	150	°C

Functional operation to the specified performance is not implied under these conditions. Operation of any single parameter in excess of the absolute ratings may cause permanent damage. No damage occurs if one parameter is set at the limit while all other parameters are set within normal operating ranges.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (f)	1920 1880 2010	- - -	1980 1920 2025	MHz	UMTS Band 1 TD-SCDMA Band TD-SCDMA Band
Supply Voltage (V_{CC})	+0.5	+3.4	+4.4	V	$P_{OUT} \leq$ +28.5 dBm
Battery Voltage (V_{BATT})	+3.1	+3.4	+4.4	V	$P_{OUT} \leq$ +28.5 dBm
Enable Voltage (V_{ENABLE})	+1.35 0	+1.8 0	+3.1 +0.5	V	PA “on” PA “shut down”
Mode Control Voltage (V_{MODE1})	+1.35 0	+1.8 0	+3.1 +0.5	V	Low Bias Mode High Bias Mode
RF Output Power (P_{OUT}) [1] R99 WCDMA, HPM HSPA (MPR = 0), HPM LTE, HPM R99 WCDMA, LPM HSPA (MPR = 0), LPM LTE, LPM	 27.7 26.45 26.45 16.2 15.2 15.2	 28.5 27.25 27.25 17 16 16	 28.5 27.25 27.25 17 16 16	 dBm	 3GPP TS 34.121-1, Rel 8 Table C.11.1.3, for WCDMA Subtest 1 TS 36.101 Rel 8 for LTE
RF Output Power (P_{OUT}) [1] TD-SCDMA (HPM) TD-SCDMA (LPM)	 26.7 15.7	 27.5 16.5	 27.5 16.5	 dBm	 3GPP TS 25.62 Section 6.2.1
Case Temperature (T_C)	-30	-	+90	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Notes:

(1) For operation at V_{CC} = +3.1 V, P_{OUT} is derated by 0.8 dB.

Table 4: Electrical Specifications - WCDMA Operation (R99 waveform)
(T_C = +25 °C, V_{CC} = V_{BATT} = +3.4 V, V_{EN} = +1.8 V, 50 Ω system, unless otherwise specified)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					P_{OUT}	V_{CC}	V_{MODE1}
Gain	24.5 - 12	27 20 15	30 - 17.5	dB	+28.5 dBm +17 dBm +17 dBm	3.4 V 1.5 V 3.4 V	0 V 0 V 1.8 V
ACLR1 at 5 MHz offset (1)	- - -	-40 -40 -42	-36 -36 -36	dBc	+28.5 dBm +17 dBm +17 dBm	3.4 V 1.5 V 3.4 V	0 V 0 V 1.8 V
ACLR2 at 10 MHz offset (1)	- - -	-52 -55 -55	-47 -47 -47	dBc	+28.5 dBm +17 dBm +17 dBm	3.4 V 1.5 V 3.4 V	0 V 0 V 1.8 V
Power-Added Efficiency (1)	43 20 17	48 25 23	- - -	%	+28.5 dBm +17 dBm +17 dBm	3.4 V 1.5 V 3.4 V	0 V 0 V 1.8 V
Quiescent Current (Icq) Low Bias Mode	-	17	-	mA	through V_{CC} pin, V_{MODE1} = +1.8 V		
Mode Control Current	-	0.1	-	mA	through V_{MODE} pin, V_{MODE1} = 1.8 V		
Enable Current	-	0.1	-	mA	through V_{ENABLE} pin		
BATT Current	-	2.5	-	mA	through V_{BATT} pin, V_{MODE1} = +1.8 V		
Leakage Current	-	4	10	µA	V_{BATT} = +4.4 V, V_{CC} = +4.4 V V_{ENABLE} = 0 V, V_{MODE1} = 0 V		
Noise in Receive Band (2)	- -	-135 -140	- -	dBm/Hz	P_{OUT} < +28.5 dBm, V_{MODE1} = 0 V P_{OUT} < 17 dBm, V_{MODE1} = +1.8 V		
Harmonics 2f_O 3f_O, 4f_O	- -	-43 -55	- -	dBc	P_{OUT} < +28.5 dBm		
Input Impedance	-	-	2:1	VSWR			
Coupling Factor	18	20	23	dB			
Directivity	-	20	-	dB			
Coupler IN-OUT Daisy Chain Insertion Loss	-	<0.25	-	dB	698 to 2620 MHz Pin 8 to 6 Shutdown Mode		
Spurious Output Level (all suprious outputs)	-	-	-70	dBc	$P_{OUT} \leq$ +28.5 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating conditions		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range		
Phase Delta (HPM-LPM)	-	10	-	Deg			

Notes:
(1) ACLR and Efficiency measured at 1950 MHz.
(2) Noise measured at 2110 MHz to 2170 MHz.

Table 5: Electrical Specifications - LTE Operation (RB = 12, START = 0, QPSK)
(T_C = +25 °C, V_{CC} = V_{BATT} = +3.4 V, V_{EN} = +1.8 V, 50 Ω system, unless otherwise specified)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					P_{OUT}	V_{CC}	V_{MODE1}
Gain	24.5 - 12	27 20 15	38 - 17.5	dB	+27.25 dBm +16 dBm +16 dBm	3.4 V 1.5 V 3.4 V	0 V 0 V 1.8 V
ACLR E-UTRA [1] at ± 10 MHz offset	- - -	-38 -38 -38	-34 -34 -34	dBc	+27.25 dBm +16 dBm +16 dBm	3.4 V 1.5 V 3.4 V	0 V 0 V 1.8 V
ACLR1 UTRA [1] at ± 7.5 MHz offset	- - -	-39 -39 -39	-36 -36 -36	dBc	+27.25 dBm +16 dBm +16 dBm	3.4 V 1.5 V 3.4 V	0 V 0 V 1.8 V
ACLR2 UTRA [1] at ± 12.5 MHz offset	- - -	-60 -60 -60	-48 -48 -48	dBc	+27.25 dBm +16 dBm +16 dBm	3.4 V 1.5 V 3.4 V	0 V 0 V 1.8 V
Power-Added Efficiency [1]	- - -	41 20 19	- - -	%	+27.25 dBm +16 dBm +16 dBm	3.4 V 1.5 V 3.4 V	0 V 0 V 1.8 V
Noise emissions B34	-	-38	-	dBm/MHz	2010 - 2025 MHz, 100 RB QPSK LTE signal centered at 1970 MHz at LTE max power		
LTE NS_05 PHS emissions	-	-48	-	dBm/ 300 kHz	1884.5 - 1919.6 MHz		
Spurious Output Level (all spurious outputs)	-	-	<-70	dBc	$P_{OUT} \leq$ +27.25 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating conditions		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range		

Notes:
(1) ACLR and Efficiency measured at 1950 MHz.

Table 6: Electrical Specifications - TD-SCDMA Operation
(T_C = +25 °C, V_{CC} = V_{BATT} = +3.4 V, V_{EN} = +1.8 V, 50 Ω system, unless otherwise specified)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					P_{OUT}	V_{CC}	V_{MODE1}
Gain	24.5 - 12	27 20 15	30 - 17.5	dB	+27.5 dBm +16.5 dBm +16.5 dBm	3.4 V 1.5 V 3.4 V	0 V 0 V 1.8 V
ACLR1 at 1.6 MHz offset	- - -	-42 -42 -46	-36 -36 -36	dBc	+27.5 dBm +16.5 dBm +16.5 dBm	3.4 V 1.5 V 3.4 V	0 V 0 V 1.8 V
ACLR2 at 3.2 MHz offset	- - -	-55 -55 -64	-48 -48 -48	dBc	+27.5 dBm +16.5 dBm +16.5 dBm	3.4 V 1.5 V 3.4 V	0 V 0 V 1.8 V
Power-Added Efficiency	35 15 15	42 20 19	- - -	%	+27.5 dBm +16.5 dBm +16.5 dBm	3.4 V 1.5 V 3.4 V	0 V 0 V 1.8 V
Quiescent Current (Icq) Low Bias Mode	-	20	-	mA	V_{MODE1} = +1.8 V		
Mode Control Current	-	0.1	-	mA	through V_{MODE} pin, V_{MODE1} = +1.8 V		
Enable Current	-	0.1	-	mA	through V_{ENABLE} pin, V_{EN} = +1.8 V		
BATT Current	-	2.5	-	mA	through V_{BATT} pin, V_{MODE1} = +1.8 V		
Leakage Current	-	<5	10	µA	V_{BATT} = +4.4 V, V_{CC} = +4.4 V, V_{ENABLE} = 0 V, V_{MODE1} = 0 V		
Harmonics $2f_O$ $3f_O$, $4f_O$	 - -	 -43 -55	 - -	dBc	P_{OUT} < +27.5 dBm		
Input Impedance	-	-	2:1	VSWR			
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range		

APPLICATION INFORMATION

To ensure proper performance, refer to all related Application Notes on the ANADIGICS web site: http://www.anadigics.com

Shutdown Mode

The power amplifier may be placed in a shutdown mode by applying logic low levels (see Operating Ranges table) to the V_{ENABLE} and V_{MODE1} voltages.

Bias Modes

The power amplifier may be placed in either a Low Bias mode or a High Bias mode by applying the appropriate logic level (see Operating Ranges table) to V_{MODE1}. The Bias Control table lists the recommended modes of operation for various applications. V_{MODE2} is not necessary for this PA.

Two operating modes are available to optimize current consumption. High Bias/High Power operating mode is for P_{OUT} levels ≥ 16 dBm. At around 17 dBm output power, the PA should be "Mode Switched" to Low power mode for lowest quiescent current consumption.

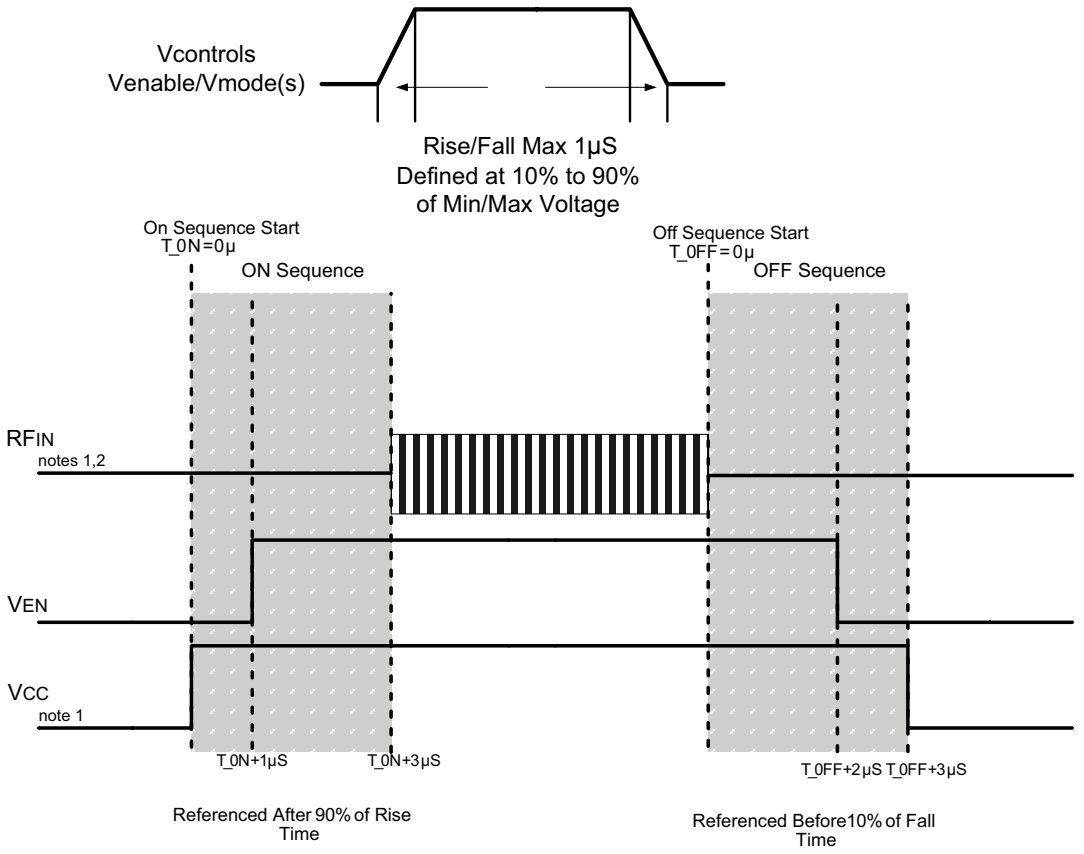


Figure 3: Recommended ON/OFF Timing Sequence

Notes:
(1) Level might be changed after RF is ON.
(2) RF OFF defined as P_{IN} ≤ -30 dBm.
(3) Switching simultaneously between V_{MODE} and V_{EN} is not recommended.

Table 7: Bias Control (WCDMA and LTE)

APPLICATION	P_{OUT} LEVELS	BIAS MODE	V_{ENABLE}	V_{MODE1}	V_{CC}	V_{BATT}
High power (High Bias Mode)	> +16 dBm	High	+1.8 V	0 V	1.5 - 4.35 V	> 3.1 V
Med/low power (Low Bias Mode)	≤ +17 dBm	Low	+1.8 V	+1.8 V	0.5 - 4.35 V	> 3.1 V
Shutdown	-	Shutdown	0 V	0 V	0.5 - 4.35 V	> 3.1 V

Table 8: Bias Control (TD-SCDMA)

APPLICATION	P_{OUT} LEVELS	BIAS MODE	V_{ENABLE}	V_{MODE1}	V_{CC}	V_{BATT}
TD-SCDMA - high power (High Bias Mode)	> +15 dBm	High	+1.8 V	0 V	1.5 - 4.35 V	> 3.1 V
TD-SCDMA - med/low power (Low Bias Mode)	≤ +16 dBm	Low	+1.8 V	+1.8 V	0.5 - 4.35 V	> 3.1 V
Shutdown	-	Shutdown	0 V	0 V	0.5 - 4.35 V	> 3.1 V

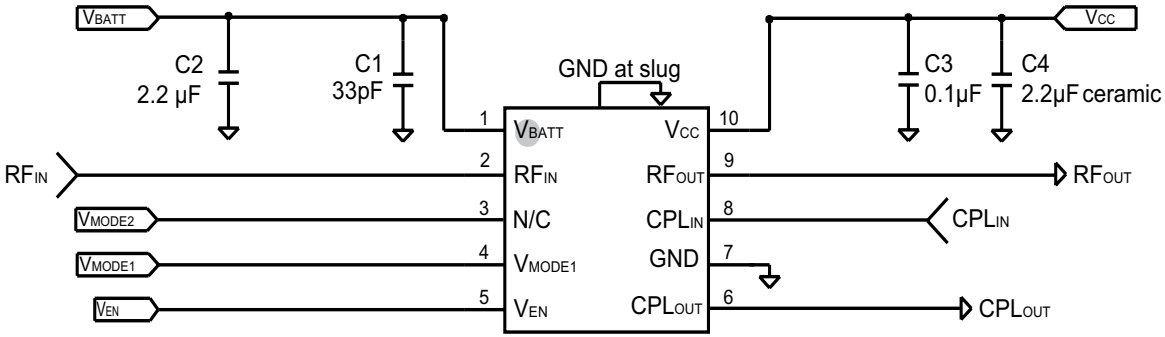


Figure 4: Evaluation Board Schematic

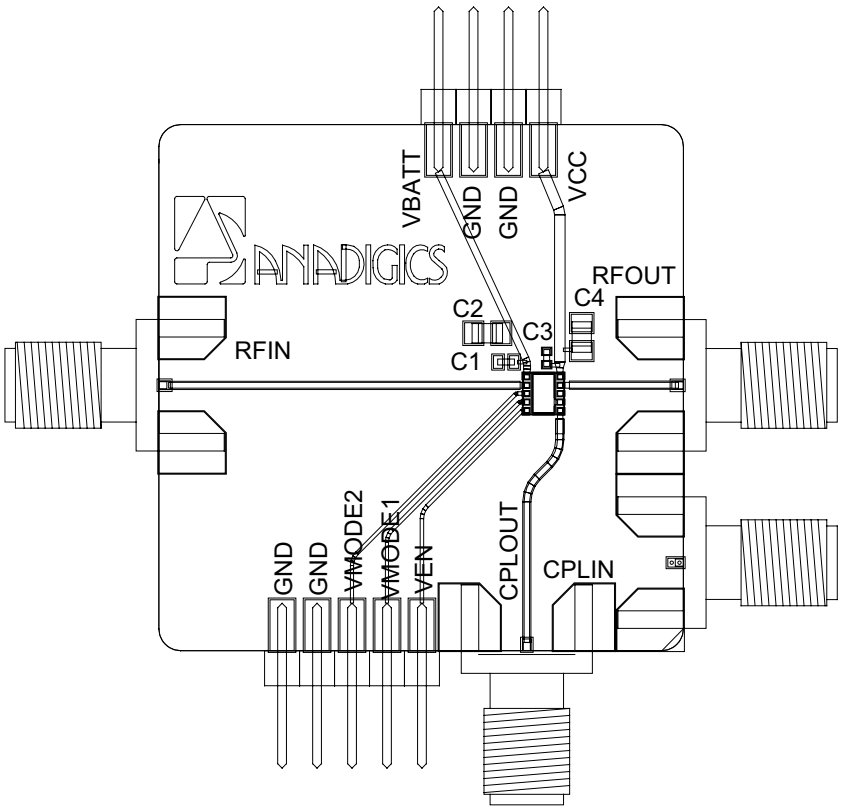


Figure 5: Evaluation Board Layout

ProEficient™

The AWT6651 power amplifier module is based on ANADIGICS proprietary ProEficient™ technology. The PA is designed to operate up to 17 dBm in the low power mode, thus eliminating the need for three gain states, while still maintaining low quiescent current and high efficiency in low and medium power levels. Average weighted efficiency can be increased by using an external switch mode power supply (SMPS) or DC/DC converter to reduce V_{CC}.

The directional "daisy chainable" coupler is integrated within the PA module, therefore there is no need for external couplers.

The AWT6651 has an integrated voltage regulator, which eliminates the need for an external constant voltage source. The PA is turn on/off is controlled by V_{EN} pin. A single V_{MODE} control logic (V_{MODE1}) is needed to operate this device. AWT6651 requires only two calibration sweeps for system calibration, thus saving calibration time.

Figure 6 shows one application example on mobile board. C1, C2 and C4 are RF bypass caps and should be placed nearby pin 1 and pin 10. RF Bypassing is used to optimize unwanted out of band (OOB) emissions and reduce OOB gain.

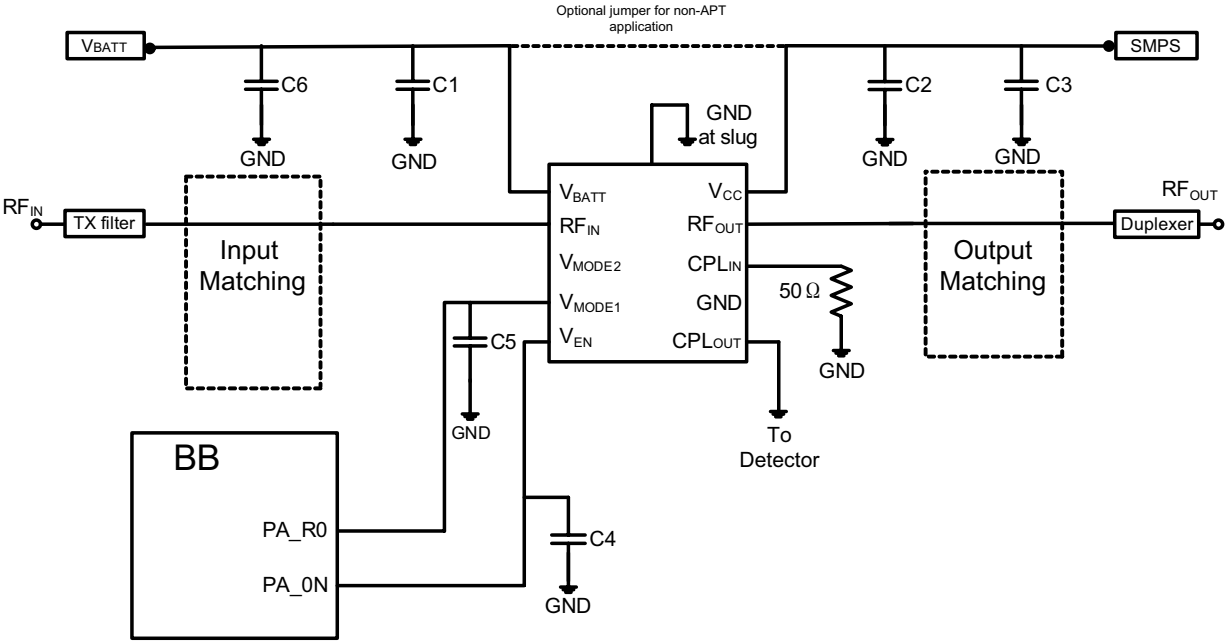
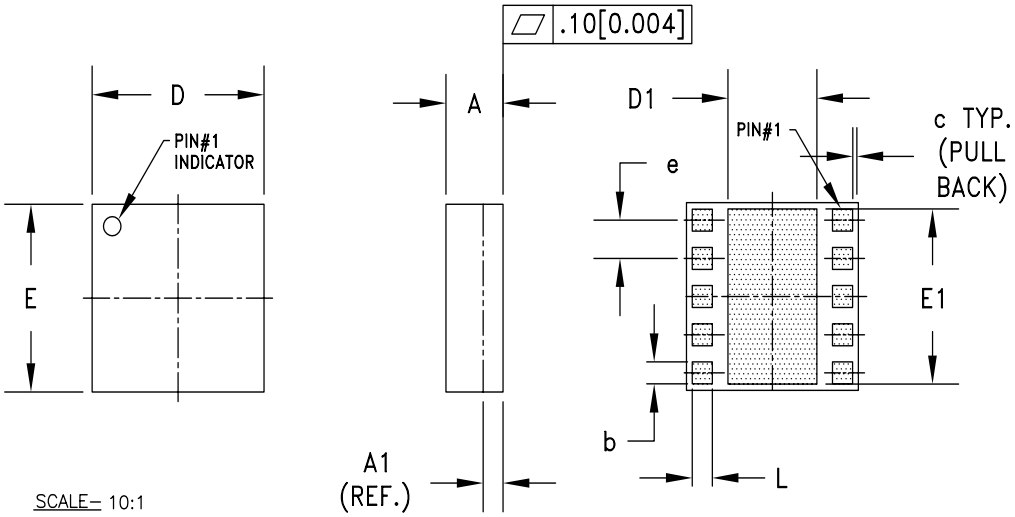


Figure 6: Typical Application Circuit

PACKAGE OUTLINE



SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.874	0.904	0.994	0.034	0.036	0.039	–
A1	PLEASE REFER TO LAMINATE CONTROL DRAWING						–
b	0.32	0.35	0.40	0.013	0.014	0.016	3
c	–	0.10	–	–	0.004	–	–
D	2.88	3.00	3.12	0.113	0.118	0.123	–
D1	1.45	1.50	1.57	0.057	0.059	0.062	3
E	2.88	3.00	3.12	0.113	0.118	0.123	–
E1	2.70	2.75	2.85	0.106	0.108	0.112	3
e	0.60			0.024			3
L	0.32	0.35	0.40	0.013	0.014	0.016	3

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. PADS (INCLUDING CENTER) SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL PAD SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO SPECIFIC LAMINATE DESIGN.
4. UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
5. LAMINATE CONTROL DRAWING SPECIFIED BY PART NUMBER.

Figure 7: Package Outline - 10 Pin 3 mm x 3 mm x 0.9 mm Surface Mount Module

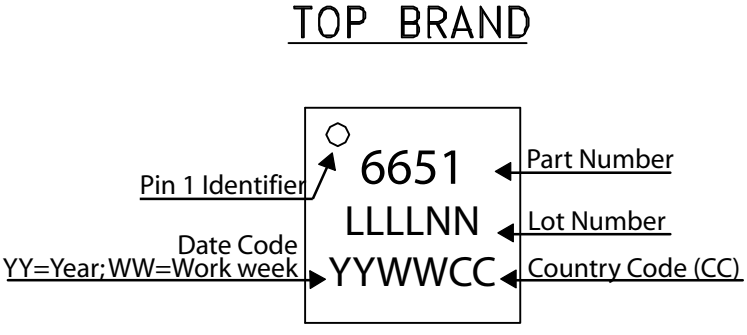
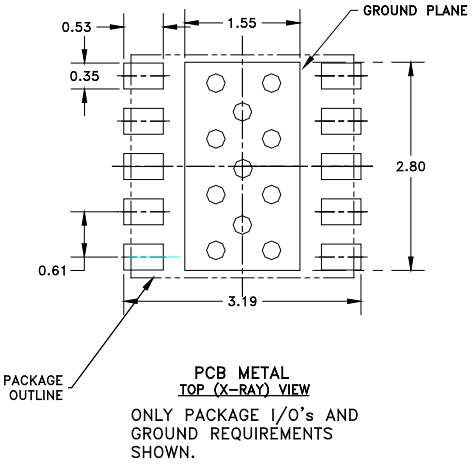


Figure 8: Branding Specification

PCB AND STENCIL DESIGN GUIDELINE



NOTES:

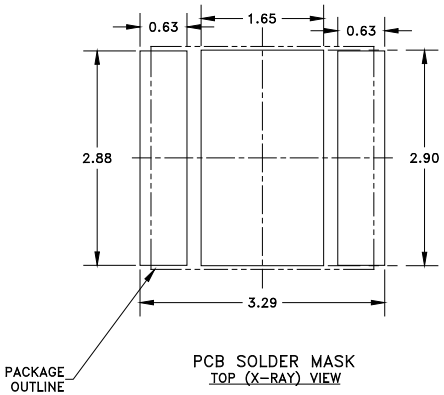
(1) OUTLINE DRAWING REFERENCE: P8002478_E

(2) UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.

(3) DIMENSIONS IN MILLIMETERS.

(4) VIAS SHOWN IN PCB METAL VIEW ARE FOR REFERENCE ONLY. NUMBER & SIZE OF THERMAL VIAS REQUIRED DEPENDENT ON HEAT DISSIPATION REQUIREMENT AND THE PCB PROCESS CAPABILITY.

(5) RECOMMENDED STENCIL THICKNESS: APPROX. 0.150mm (6 Mils)



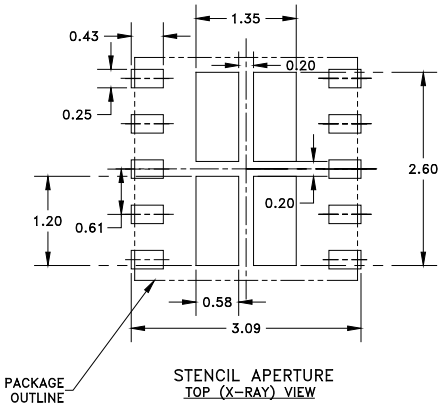
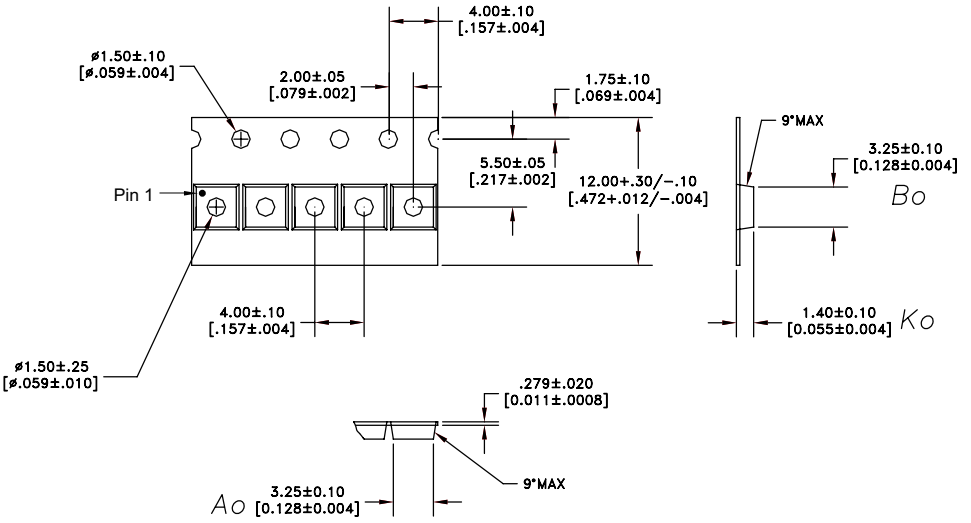


Figure 9: Recommended PCB Layout Information

COMPONENT PACKAGING



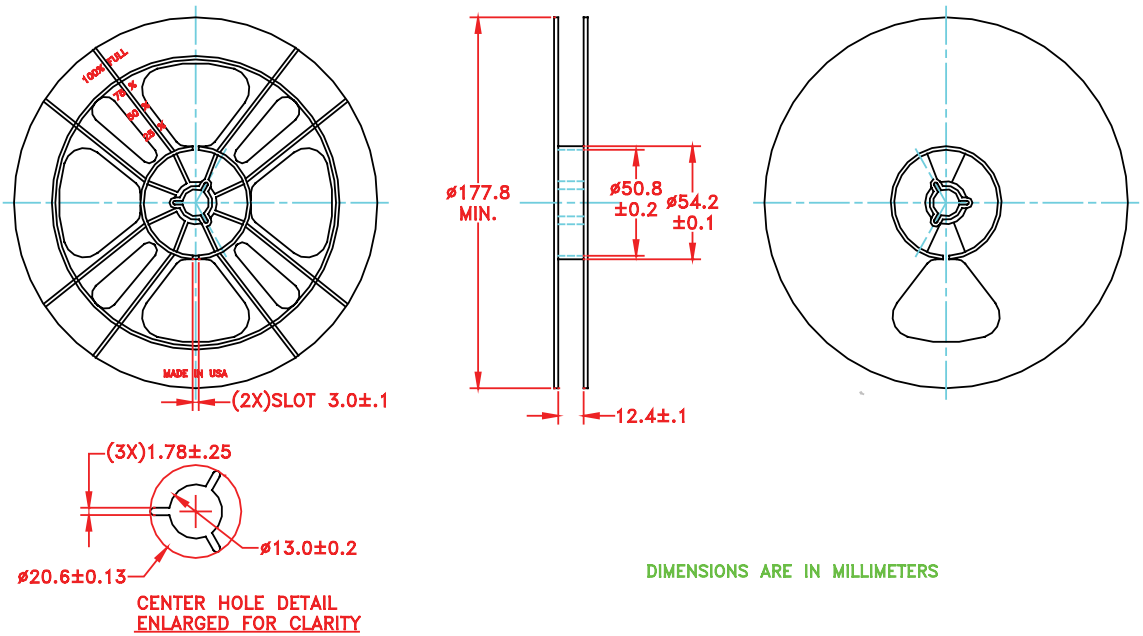
NOTES:

1. MATERIAL: 3000 (CARBON FILLED POLYCARBONATE)
100% RECYCLABLE.

DIMENSIONS ARE IN MILLIMETERS [INCHES]

DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

Figure 10: Carrier Tape



DIMENSIONS ARE IN MILLIMETERS

NOTES:

1. MATERIAL: BLACK CARBON POLYSTYRENE
SURFACE RESISTIVITY: $1X10^4$ TO $1X10^8$ ohms/square

DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

Figure 11: Reel

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
AWT6651Q7	-30 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 0.9 mm Surface Mount Module	Tape and Reel, 2500 pieces per Reel
AWT6651P9	-30 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 0.9 mm Surface Mount Module	Partial Tape and Reel

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URL: http://www.anadigics.com