



**Motor Drivers for MDs** 

**BD6641KUT/BD6643KN** 

# **Sensorless** 4ch PWM System **Motor Driver for MDs**





# Description

1chip system spindle motor driver IC for playback in portable player drive. Supports spindle, sled, focus, and tracking functions.

The driver incorporates a charge pump, direct PWM soft switching drive for spindle, low ON resistance power DMOS driver, reducing power consumption and suppressing spindle motor driving noise.

The driver is has small, thin package making it idea for use in portable players.

#### Features

- 1) Operates at low power supply voltage (2.1V min.)
- 2) Power DMOS output with low ON resistance ( $0.8\Omega$  typ.)
- 3) Incorporates a charge pump circuit for VG boost
- 4) 3-phase full-wave PWM soft switching sensorless driver for spindle motor.
- 5) 3-level control 3-phase driver for sled (Built-in comparator for BEMF voltage detection)
- 6) 2ch, 3-level control H-bridges for focus/tracking

# Applications

Recording and playback MD

### ●Product lineup

Parameter	BD6641KUT	BD6643KN
VCC operating power supply voltage range	2.1~6.5V	2.1~6.5V
VM operating power supply voltage range	0~3V	0~3V
Operating temperature range	-25∼+75℃	-25~+75℃
Output current	500mA	500mA
Rotation speed	~5000rpm (typ.)	~2300rpm (typ.)
Package	TQFP64U	UQFN48
Spindle/brake input	H: Brake ON	L: Brake ON

Ver.B Oct.2005

# ● Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
Power supply voltage for control circuit	VCC	7	٧
Power supply voltage for driver block	VM	7	٧
Power supply voltage for pre-driver	VG	14	٧
Output current	Iomax	*500	mA
Dower discinction	Pd	**1375 (BD6641KUT)	mW
Power dissipation	Pu	***760 (BD6643KN)	IIIVV
Operating temperature range	Topr	-25~+75	Ç
Storage temperature range	Tstg	-55 <b>∼</b> +150	Ç
Junction temperature	Tjmax	+150	°C

<sup>\*</sup> Must not exceed Pd or ASO.

# Operating conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit
	VCC	2.1	2.2	6.5	V
Power supply voltage	VM	_	_	3.0	V
	VG	3	6.5	13	V

#### ●Electrical characteristics

(Unless otherwise specified, Ta=25°C, VCC=2.2V, VM=1.0V, fin=176kHz)

Description	O b I		Limit		1.1	Conditions	
Parameter	Symbol	Min.	Тур.	Max.	Unit		
0: ''	ICC		4.0	7.0	mA	at operation in all blocks	
Circuit current	IST	-	1	10	μA	at stop in all blocks	
STBY H level input voltage	VSTH	VCC-0.4	-	VCC	V	at operation in all blocks	
STBY L level input voltage	VSTL	0	-	0.4	V	at stop in all blocks	
STBY H level input current	ISTH	-	220	310	μA		
STBY L level input current	ISTL	-1	-	-	μA		
Output ON resistance	RON	_	0.8	1.2	Ω	upper and lower ON resistance in total	
~Boost circuit~							
	VG1	5.5	6.5	6.7	V	each input L	
Output voltage	VG2	4.4	5.2	-	V	at operation in all blocks	

<sup>\* \*</sup> Reduced by 11 mW/°C over 25°C, when mounted on a glass epoxy board (70mm×70 mm×1.6mm).

<sup>\* \* \*</sup> Reduced by 7.6mW/°C over Ta=25°C, when mounted on a glass epoxy board (70mm×70mm×1.6mm).

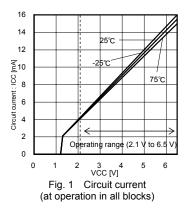
# ● Electrical characteristics

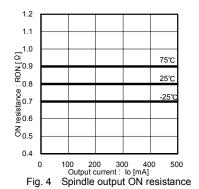
(Unless otherwise specified, Ta=25 $^{\circ}$ C, VCC=2.2V, VM=1.0V, fin=176kHz)

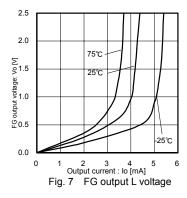
Sylindia   Type   Max   Orth   Conditions	Darameter	Cumbal		Limit		Linit	Conditions	
Position detection comparator injust range   VSD   0	Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions	
Position detection comparator input range   VSD   0   - VCC-1.0   V	$\sim$ Spindle (3-phase full-wave sensorless driv	∼Spindle (3-phase full-wave sensorless driver)∼						
Position detection comparator   ISH   -   -   2	Position detection comparator offset	VSOFS	-10	-	10	mV		
Input current H	Position detection comparator input range	VSD	0	-	VCC-1.0	V		
Input current H	Position detection comparator	IQH			2		input=VCC	
Input current L   ISL   -2   -	input current H	1011	-		2	μΛ	input=vcc	
Input current   ISLO	Position detection comparator	ISI	2				input=0\/	
SLOPE discharge current   ISLI   6.5   9.4   12.5   μA	input current L	IGE	-2		-	μΛ	input=0 v	
SLOPE clamp H level   VSLH   0.5   0.8   1.1   V	SLOPE charge current	ISLO	-12.8	-9.8	-6.8	μΑ		
SLOPE clamp L level   VSLL   0.3   0.46   0.6   V	SLOPE discharge current	ISLI	6.5	9.4	12.5	μΑ		
OSC oscillating frequency	SLOPE clamp H level	VSLH	0.5	8.0	1.1	V		
OSC charge current   OSCO	SLOPE clamp L level	VSLL	0.3	0.46	0.6	V		
OSC discharge current	OSC oscillating frequency	fOSC	70	100	130	kHz	OSC=200pF ISET=50kΩ	
OSC H level   VOSCH   0.5   0.75   1.0   V	OSC charge current	IOSCO	-12.5	-9.65	-6.5	μA		
OSC L level   VOSC	OSC discharge current	IOSCI	6.5	9.56	12.5	μA		
SET voltage	•	VOSCH	0.5	0.75	1.0	V		
ISET voltage	OSC L level	VOSCL	0.35	0.53	0.70	V		
PWM level input voltage	ISET voltage		350		650	mV	ISET=50kΩ	
PWM H level input voltage	<u> </u>	f PWM	60	132	200	kHz		
PWM L level input voltage   VPWL   0   -   0.4   V		VPWH						
PWM H level input current   IPWH   -   -   1								
PWM L level input current   IPWL   -1   -   -   μA   PWM=0V	· • • • • • • • • • • • • • • • • • • •		_				PWM=VCC	
BLAKE H level input voltage   VBKH   VCC-0.4   - VCC   V   Brake OF (BD6641KUT)   Brake OFF (BD6643KN)	<u>'</u>		-1	-				
BLAKE L level input voltage   VBKH   VCC-0.4   - VCC   V   Brake OFF (BD6643KN)	1 WWW E level input durient	***				μπ		
BLAKE L level input voltage   VBKL   0   -   0.4   V   Brake OFF (BD6641KUT) Brake ON (BD6643KN)	BLAKE H level input voltage	VBKH	VCC-0.4	-	VCC	V		
BLAKE L level input voltage   VBKL   0   -   0.4   V   Brake ON (BD6643KN)							· · · · · · · · · · · · · · · · · · ·	
BLAKE H level input current   BKH   -   -   1	BLAKE L level input voltage	VBKL	0	-	0.4	V		
BLAKE L level input current   BKL   -1   -   -   μA   BRAKE=0V   FG H level output voltage   VFGH   VCC-0.4   -   VCC   V   lo=-500μA   FG L level output voltage   VFGL   0   -   0.4   V   lo=500μA    ~Sled, focus, tracking (stepping, H-bridge × 2ch)~  H level input voltage   VINH   VCC-0.4   -   VCC   V   L level input voltage   VINL   0   -   0.4   V   H level input current   IINH   -   -   1   μA   VIN=VCC   L level input current   IINH   -1   -   μA   VIN=VCC   L level input current   IINL   -1   -   μA   VIN=VCC   L level input current   IINL   -1   -   μA   VIN=VCC   L level input current   IINL   -1   -   μA   VIN=VCC   L level input current   IINL   -1   -   μA   VIN=VCC   L level input current   IINL   -1   -   μA   VIN=VCC   L level input current   IINL   -1   -   μA   VIN=VCC   L level input current   IINL   -1   -   μA   VIN=VCC   L level input current   IINL   -1   0.7   μs    Short pulse input response (H-bridge)   tmin   120   -   -   ns   Input pulse width 200 ns    ~Sled, position detection comparator ~  Position detection comparator input range   VAD   0   -   VCC-1.0   V    Position detection comparator input range   VAD   0   -   VCC-1.0   V    Position detection comparator   IAH   -   -   2   μA    Position detection comparator   IAL   -2   -   -   μA    Position detection comparator   VAOL   -   0.2   0.3   V    Position detection comparator output voltage L   Position detection comparator output   Position detection comparator output   Position detection comparator output   Position detection comparator o	RLAKE H level input current	IBKH			1	пΛ	· · · · · · · · · · · · · · · · · · ·	
FG H level output voltage	,							
FG L level output voltage   VFGL   0   -   0.4   V   lo=500μA	·					•		
~Sled, focus, tracking (stepping, H-bridge × 2ch)~  H level input voltage	·						•	
H level input voltage VINH VCC-0.4 - VCC V L level input voltage VINL 0 - 0.4 V H level input current IINH 1			U		0.4	v	10-300μΑ	
Lievel input voltage			\/00 0 4		1,00			
H level input current								
Lievel input current   IINL   -1   -   -   μA   VIN=0V				-				
TRISE - 0.2 1 μs  TFALL - 0.1 0.7 μs  Short pulse input response (H-bridge) tmin 120 ns Input pulse width 200 ns  ~Sled, position detection comparator ~  Position detection comparator offset VAOFS -10 - 10 mV  Position detection comparator input range VAD 0 - VCC-1.0 V  Position detection comparator input range IAH 2 μA  Position detection comparator input current H  Position detection comparator input current L  Position detection com	•					•		
TFALL - 0.1 0.7 μs  Short pulse input response (H-bridge) tmin 120 ns Input pulse width 200 ns  ~Sled, position detection comparator ~  Position detection comparator offset VAOFS -10 - 10 mV  Position detection comparator input range VAD 0 - VCC-1.0 V  Position detection comparator input current H  Position detection comparator input current L  Position detection comparator output VAOL - 0.2 0.3 V Io=300μA	L level input current		-1		-		VIN=0V	
Short pulse input response (H-bridge)  Thin  Th	I/O propagation delay time (H-bridge)		-					
~Sled, position detection comparator ~  Position detection comparator offset VAOFS -10 - 10 mV  Position detection comparator input range VAD 0 - VCC-1.0 V  Position detection comparator input current H  Position detection comparator input current L  Position detection comparator input current L  Position detection comparator input current L  Position detection comparator output VAOL - 0.2 0.3 V Io=300μA  Position detection comparator output ROA 10 20 30 kΩ	,	TFALL	-	0.1	0.7	μs		
~Sled, position detection comparator ~  Position detection comparator offset VAOFS -10 - 10 mV  Position detection comparator input range VAD 0 - VCC-1.0 V  Position detection comparator input current H  Position detection comparator input current L  Position detection comparator input current L  Position detection comparator input current L  Position detection comparator output VAOL - 0.2 0.3 V Io=300μA  Position detection comparator output ROA 10 20 30 kΩ	Short pulse input response (H-bridge)	tmin	120	_	_	ns	Input pulse width 200 ns	
Position detection comparator offset VAOFS -10 - 10 mV  Position detection comparator input range VAD 0 - VCC-1.0 V  Position detection comparator input current H  Position detection comparator input current L  Position detection comparator input current L  Position detection comparator output VAOL - 0.2 0.3 V  Position detection comparator output ROA 10 20 30 kΩ	Chart paled input responds (it shage)	a i i i i	120			110	mpat paide Width 200 He	
Position detection comparator input range VAD 0 - VCC-1.0 V Position detection comparator input current H	$\sim$ Sled, position detection comparator $\sim$							
Position detection comparator input range VAD 0 - VCC-1.0 V Position detection comparator input current H	Position detection comparator offset	VAOFS	-10	-	10	mV		
Position detection comparator input current H  Position detection comparator input current L  Position detection comparator input current L  Position detection comparator output voltage L  Position detection comparator output  Position detection comparator output  ROA  10  20  μA  10  10  10  10  10  10  10  10  10  1		VAD		-	VCC-1.0	V		
input current H  Position detection comparator input current L  Position detection comparator output voltage L  Position detection comparator output  ROA  IAH  2 μA  μA  μA  Io=300μA  V  Io=300μA								
Position detection comparator input current L  Position detection comparator output voltage L  Position detection comparator output  Position detection comparator output  ROA  10  20  30  kΩ	input current H	IAH	-	-	2	μA		
input current L  Position detection comparator output VAOL  Position detection comparator output  Position detection comparator output  ROA  10  20  30  kΩ	,							
Position detection comparator output VAOL - 0.2 0.3 V Io=300μA output voltage L  Position detection comparator output ROA 10 20 30 kΩ	•	IAL	-2	-	-	μA		
output voltage L  Position detection comparator output  ROA 10 20 30 kQ	•						Io=300μA	
Position detection comparator output ROA 10 20 30 kQ	'	VAOL	-	0.2	0.3	V		
ROA   10   20   30   KΩ	· · · · · · · · · · · · · · · · · · ·							
		ROA	10	20	30	kΩ		

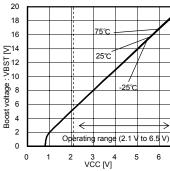
 $<sup>\</sup>bigcirc \mathsf{This}\;\mathsf{IC}$  is not designed to be radiation-resistant.

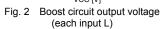
#### ●Reference data

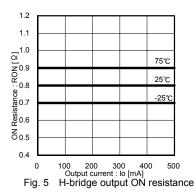












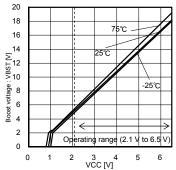
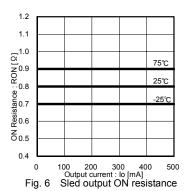
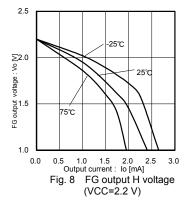
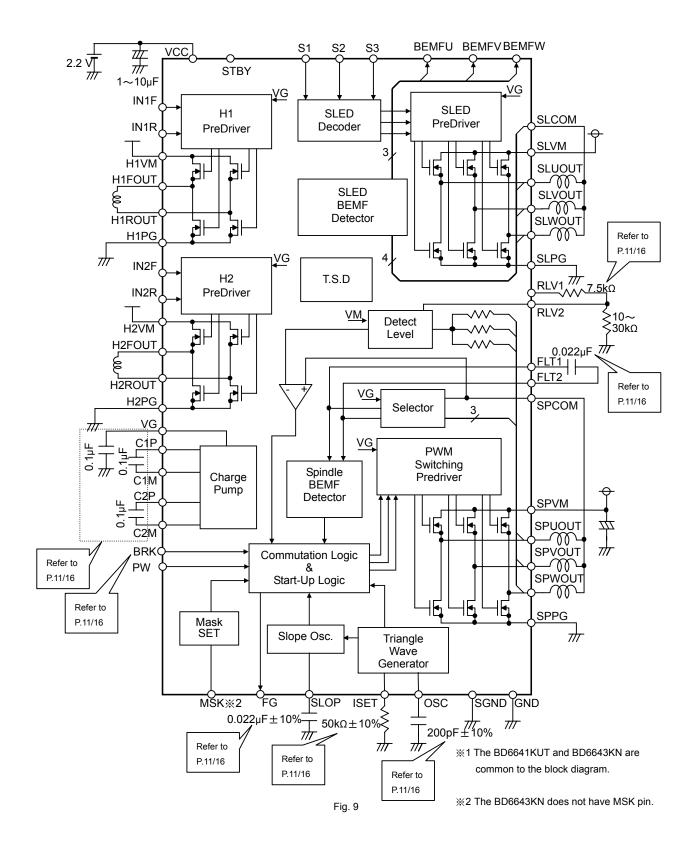


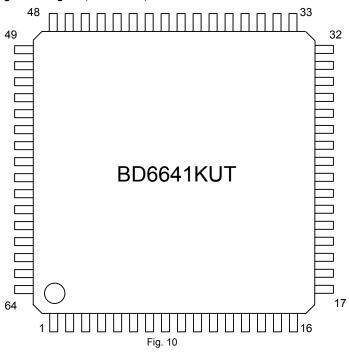
Fig. 3 Boost circuit output voltage (at operation in all blocks)



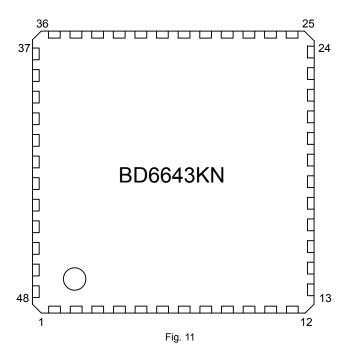




# ●Pin assignment table / Pin arrangement diagram (BD6641KUT)



NO.	Pin name	Pin function	NO.	Pin name	Pin function
1	S2	Stepping decoder 2 input pin		BRK	Brake signal input pin
2	S3	Stepping decoder 3 input pin		SPCOM	Spindle motor coil neutral point input pin
3	VG	Charge pump output pin	35	SLOPE	Slope capacitor connection pin
4	N.C		36	N.C	
5	H2VM	H-bridge 2 power block power supply pin	37	SPVM	Spindle power block power supply pin
6	N.C		38	MSK	Mask time setting pin
7	C2M	Charge pump capacitor 2 connection pin -	39	ISET	OSC/SLOPE charge/discharge current setting pin
8	C2P	Charge pump capacitor 2 connection pin +	40	VCC	Power supply pin for small signal block
9	GND	Small signal block GND pin	41	N.C	
10	C1M	Charge pump capacitor 1 connection pin -	42	OSC	OSC capacitor connection pin
11	N.C		43	N.C	
12	H1VM	H-bridge 1 power block power supply pin	44	SLVM	Stepping power block power supply pin
13	N.C		45	FG	FG output pin
14	C1P	Charge pump capacitor 1 connection pin +	46	FLT1	Filter capacitor connection pin 1
15	BEMFU	Stepping detection comparator output (phase U)	47	FLT2	Filter capacitor connection pin 2
16	BEMFV	Stepping detection comparator output (phase V)	48	RLV2	Rotor position detection level setting pin 2
17	BEMFW	Stepping detection comparator output (phase W)	49	SGND	Substrate GND pin
18	IN1F	H-bridge 1 forward input pin	50	RLV1	Rotor position detection level setting pin 1
19	IN1R	H-bridge 1 reverse input pin	51	SLCOM	Stepping motor coil midpoint input pin
20	H1FOUT	H-bridge 1 forward output pin	52	SLUOUT	Stepping motor output (phase U)
21	H1PG	H-bridge1 power block GND	53	SLPG	Stepping power block GND pin
22	H1ROUT	H-bridge 1 reverse output pin	54	SLVOUT	Stepping motor output (phase V)
23	N.C		55	N.C	
24	N.C		56	SLWOUT	Stepping motor output (phase W)
25	SPUOUT	Spindle motor output pin (phase U)	57	N.C	
26	N.C		58	N.C	
27	SPVOUT	Spindle motor output pin (phase V)	59	H2FOUT	H-bridge 2 forward output pin
28	SPPG	Spindle power block GND pin	60	H2PG	H-bridge 2 power block GND
29	SPWOUT	Spindle motor output pin (phase W)	61	H2ROUT	H-bridge 2 reverse output pin
30	N.C		62	IN2F	H-bridge 2 forward input pin
31	PWM	PWM input pin	63	IN2R	H-bridge 2 reverse input pin
32	STBY	Standby pin	64	S1	Stepping decoder 1 input pin



⊚Pin function table

NO.	Pin name	Pin function	NO.	Pin name	Pin function
1	S2	Stepping decoder 2 input pin	25	BRK	Brake signal input pin
2	S3	Stepping decoder 3 input pin	26	SPCOM	Spindle motor coil neutral point input pin
3	VG	Charge pump output pin	27	SLOPE	Slope capacitor connection pin
4	H2VM	H-bridge 2 power block power supply pin	28	SPVM	Spindle power block power supply pin
5	C2M	Charge pump capacitor 2 connection pin -	29	ISET	OSC/SLOPE charge/discharge current setting pin
6	C2P	Charge pump capacitor 2 connection pin +	30	VCC	Power supply pin for small signal block
7	GND	Small-signal block GND pin	31	OSC	OSC capacitor connection pin
8	C1M	Charge pump capacitor 1 connection pin -	32	SLVM	Stepping power block power supply pin
9	H1VM	H-bridge 1 power block power supply pin	33	FG	FG output pin
10	C1P	Charge pump capacitor 1 connection pin +	34	FLT1	Filter capacitor connection pin 1
11	BEMFU	Stepping detection comparator output (phase U)	35	FLT2	Filter capacitor connection pin 2
12	BEMFV	Stepping detection comparator output (phase V)	36	RLV2	Rotor position detection level setting pin 2
13	BEMFW	Stepping detection comparator output (phase W)	37	RLV1	Rotor position detection level setting pin 1
14	IN1F	H-bridge 1 forward input pin	38	SLCOM	Stepping motor coil neutral point input pin
15	IN1R	H-bridge 1 reverse input pin	39	SLUOUT	Stepping motor output (phase U)
16	H1FOUT	H-bridge 1 forward output pin	40	SLPG	Stepping power block GND pin
17	H1PG	H-bridge 1 power block GND	41	SLVOUT	Stepping motor output (phase V)
18	H1ROUT	H-bridge 1 reverse output pin	42	SLWOUT	Stepping motor output (phase W)
19	SPUOUT	Spindle motor output pin (phase U)	43	H2FOUT	H-bridge 2 forward output pin
20	SPVOUT	Spindle motor output pin (phase V)	44	H2PG	H-bridge 2 power block GND
21	SPPG	Spindle power block GND pin	45	H2ROUT	H-bridge 2 reverse output pin
22	SPWOUT	Spindle motor output pin (phase W)	46	IN2F	H-bridge 2 forward input pin
23	PWM	PWM input pin	47	IN2R	H-bridge 2 reverse input pin
24	STBY	Standby pin	48	S1	Stepping decoder 1 input pin

#### Description of each block operation

Spindle BEMF Detector (spindle)

Comparator to detect BEMF voltage generated in rotating motor coil.

· Commutation Logic & Start-up Logic (spindle)

This logic generates the motor startup sequence and motor driving waveforms.

Operates based on the CLK (100kHz typ.) generated by the Triangle Wave Generator.

Generates soft switching drive waveforms with the OSC triangle waveform and SLOPE waveform.

Control the motor's rotation speed external PWM signal input. The brake (deceleration) ON/OFF can be switched by external BRK signal input.

· Mask Set (BD6641KUT/spindle)

The FG maximum frequency can be set to 700Hz/1090Hz/1515Hz by setting the MSK pin to OPEN/GND/VCC. (The setting maximum frequency may not be reached for some motors.)

Triangle Wave Generator (spindle)

Generates a triangle waveform (100kHz) that is used in generating the logic CLK and soft switching waveforms, as well as for the Charge Pump clock. The triangle waveform frequency is set with the ISET resistor ( $50k\Omega$  typ.) and the OSC capacity (200pF typ.). It is not recommended to use values other than the typ. because this waveform is used as the CLK for the entire IC system (100kHz typ.). It is recommended to use the ISET resistor and the OSC capacity network with low temperature characteristics.

· Slope OSC (spindle)

Generates the slope waveform which is used in generating the soft switching drive waveform.

Charge Pump (common to all blocks)

Boost circuit for each block's power output pre-driver VG power supply. The generated VG voltage is three times the VCC. Therefore, use caution when using a VCC that exceeds the standard.

· SLED BEMF Detector (Sled)

Comparator to detect the BEMF voltage generated in rotating motor coil.

Negative input pins are connected in common (SLCOM), and positive input pins are connected to each output (SLUOUT, SLVOUT, SLWOUT).

· TSD (common to all blocks)

Thermal shutdown circuit. Turns off all driver output when the chip temperature Tj reaches approximately 175°C (typ.). The circuit returns to normal operation at approximately 20°C of hysteresis.

#### · H-bridge/Sled truth table

H-bridge block for focus and tracking motor

STBY	IN1,2F	IN1,2R	H1,2FOUT	H1,2ROUT
Н	L	L	L	L
Н	н	L	н	L
Н	L	Н	L	Н
Н	Н	Н	L	L
L	Х	Х	Z	Z

Z: High-Impedance, X: Don't care

Stepping block for sled motor

STBY	S3	S2	S1	SLUOUT	SLVOUT	SLWOUT
Н	L	L	L	Н	L	Z
Н	L	L	Н	Н	Z	L
Н	L	Н	L	Z	Н	L
Н	L	Н	Н	L	Н	Z
Н	Н	L	L	L	Z	Н
Н	Н	L	Н	Z	L	Н
Н	Н	Н	Х	Z	Z	Z
L	Х	Х	Х	Z	Z	Z

Z: High-Impedance, X: Don't care

Description of basic spindle driver operation

#### 1) Startup from the stop condition of the motor

Generally, the appropriate motor driving logic is unclear because no BEMF voltage is generated in the stopping motor coil. For the BD6641KVT/BD6643KN, appropriate driving logic can be obtained by input of a driving waveform, (as shown in Fig. 12) to the motor, allowing the motor to be started up efficiently (Fig. 13).

Although the FG edge usually switches each time a zero cross is detected, the first 4 to 5 FG edges are cancelled only at startup, as unstable FG edge is not output immediately after startup.

If no zero cross detection occurs during 300ms (typ.), the driving logic is forced to move forward to vibrate the motor and detect a zero cross. In this case, the motor may startup after vibrating briefly in the reverse direction.

This vibration occurs because the driving logic has been forcefully inputted without regard to the rotor position.

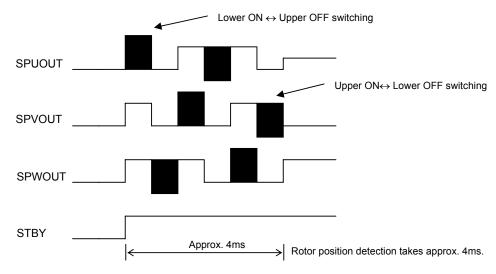
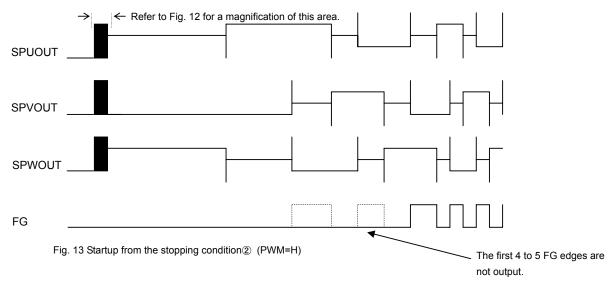


Fig. 12 Startup from the stopping condition (PWM=H)



# 2) Operation at normal rotation (Fig. 14)

For a sensorless system, the rotor position detection (zero cross detection) is performed by comparing the BEMF voltage generated in the Hi-Impedance (upper and lower Tr are off) phase to the coil's neutral point voltage with a comparator and the driving waveform of the motor is composed.

In soft switching operation, the waveform generated by comparing the SLOPE pin waveform and the OSC pin triangle waveform with a comparator is overlaid on each output waveform. This causes the output current to rise and fall gently, reducing drive noise.

When the PWM pin is H (full torque) or L (output OFF), zero cross detection is timed using the internal CLK (the peaks of the OSC triangle waveform). At PWM control, zero cross detection is timed to the PWM falling edge.

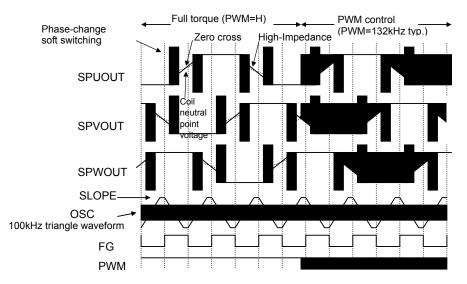


Fig. 14 Each pin waveform at normal rotation (Full Torque & PWM)

#### 3) Brake operation (Fig. 15)

Brake operation applies a reverse torque to the motor by setting the output phases from H to L and L to H. The zero cross detection during brake operation is performed as in normal rotation. A strong brake is applied by continuously keeping reverse torque according to the rotor position. Although most motors will not rotate in reverse, some motors may do so. In brake operation at high speed rotation, some motors may generate a significant BEMF voltage, causing the logic to malfunction.

Because the SLOPE waveform is rising during brake operation, brake driving noise may become noticeable. This serves to prevent the error zero cross detection during brake operation. To reduce brake driving noise, limit the output current by PWM control.

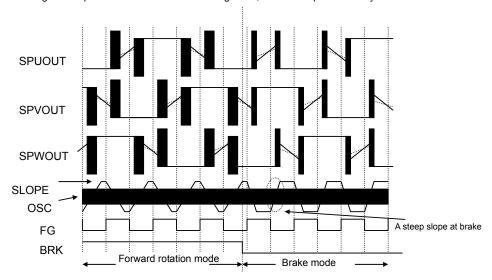


Fig. 15 Each pin waveform at brake (Same as at PWM.)

%Fig. 15 shows the waveforms for the BD6643KN. In BD6641KUT, only BRK signal is reversing.

### 4) FG signal output

FG signal is set by zero cross signal EX-OR composition. It has the width of electrical angle 60°. There is an edge in zero cross timing which can be used in servo systems as a rotation speed signal of the motor. When the motor is off, it is H and frequency that is in proportion to the rotation speed and is always output during braking. Therefore, it can be used in the same way as FG signal of external FG pattern. The edge chattering is removed by logic. Therefore, stable edge can be provided in case of unstable BEMF voltage, such as at low speed rotation. Furthermore, there is no need for an external filter.

Design method	Design evernals
Design method  1. Spindle block: SLOPE capacity	Design example  Set the following values as a standard.
Smoothly set the slope of output current to reduce the motor's	BD6641KUT
driving noise. A large capacitance can cause slope time noise	MSK pin=OPEN⇒0.022µF±10%
and may cause malfunction.	MSK pin=GND⇒0.014µF±10%
A small capacitance results in a steep output current slope,	MSK pin=VCC⇒0.010µF±10%
increasing motor noise.	, , , , , , , , , , , , , , , , , , ,
	- BD6643KN
	$0.022 \mu F \pm 10\%$
2. Spindle block: ISET resistor	Set the IC's system CLK (100kHz). The optimum value is
Set the charge and discharge current of the capacitor	50kΩ±10%.
connected to the OSC pin.	
ISET voltage = Charge and discharge current ISET resistor	
ISET resistor	
3. Spindle block: OSC capacitor	Set the IC's system CLK (100kHz). Therefore, the optimum
Generate a triangle waveform (100kHz) using the charge and	value is 200pF±10%.
discharge current set by the ISET resistor.	
4. Spindle block: FLT capacity C <sub>FLT</sub>	When C <sub>FLT</sub> =0.022μF,
Comprise the filter for the noise elimination of BEMF	fc=1/(2× $\pi$ ×0.022 $\mu$ F×5.5k $\Omega$ )
comparator input signal with an internal input resistor (5k $\Omega$	=1.315kHz
typ.).	Set fc=approx. several to several 10kHz.
317	Setting too large value of C <sub>FLT</sub> and too low value of fc may
The cutoff frequency fc is given by the following formula:	cause a deviation between the motor's rotor position and BEMF
$fc=1/(2 \times \pi \times C_{FLT} \times 5.5 k\Omega)$	comparator detection timing, and may affect efficiency and
	driving noise.
5. Spindle block: R <sub>LV</sub> resistor	Set the resistor between the RLV1 and RLV2 pins to $7.5k\Omega$ and
Detect the rotor position and startup the motor at approximately	the resistor between the RLV2 and GND pins from $10k\Omega$ to
4ms after rising STBY pin.	30kΩ to startup well. Some motors may rotate in the reverse
Set the rotor position detection level (sensitivity) by the resistor	direction at startup.
connected to RLV1 and RLV2 pins.	
6 Charge numn	The optimum capacitance is 0.1μF.
6. Charge pump  Boost to up three times the VCC voltage. Therefore, set the	тно оринин сарасканое в оттре.
VCC voltage within a range where the VG does not exceed the	
rating. If the VG is input externally, without using an internal	
charge pump, disconnect the capacitor between the C1P and	
C1M, C2P and C2M.	
7. Brake	BD6641KUT: Brake ON at BRK pin voltage>VCC-0.4V.
Set on reverse torque brake and decelerate the spindle motor.	BD6643KN: Brake ON at BRK pin voltage<0.4V.
Do not apply on the brake to a stopping motor as some motors	
may rotate in the reverse direction	
may rotate in the reverse direction	

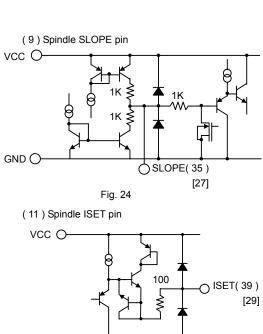
<sup>\*\*</sup>The setting values of the data above are reference values. Board layout, wiring, and types of components to be used may cause characteristic variations in actual setting. Verify the setting in the actual application.

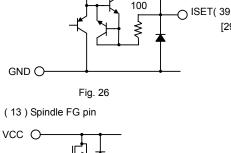
#### ●I/O equivalent circuit diagrams

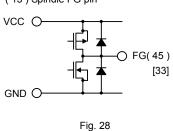
(1) Logic input (2) Standby input S1(64)[48] VCC O VCC O S2(1)[1] S3(2)[2] IN1F(18)[14] IN1R( 19 ) [15] 10K 10K STBY( 32 )( IN2F( 62 ) [46] W [24] IN2R(63)[47] PWM(31)[23] 10K BRK(-) [25] GND O GND O Fig. 16 Fig. 17 (3) Charge pump (4) Sled BEMF detection comparator output C1P(14) C2P(8) [10] [6] vcc O OVG(3)[3] vccC 20K BEMFU(15)[11] BEMFV( 16 ) [12] vcc0 BEMFW(17)[13] GND () OC2M(7)[5] Fig. 19 **GNDO** C1M(10)[8] Fig. 18 (5) H-bridge 2 output (6) H-bridge 1 output H2VM( 5 ) H1VM( 12 ) H1ROUT(22) H1FOUT( 20 ) [4] [9] H2ROUT(61) [48] H2FOUT( 59 ) [45] [43] H2PG( 60 ) H1PG( 21 )O [44] [17] Fig. 21 Fig. 20 (8) Spindle BEMF detection comparator (7) Spindle output SPUOUT(25) SPVOUT(27) SPWOUT(29) VCC O  $Q_{[19]}$  $Q_{[20]}$ [22] SPVM(37)O FLT1(46) [25] SPCOM( 34 ) -Ŏ FLT2( 47 ) [26] 200 SPPG( 28 )O [35] GND O [21]

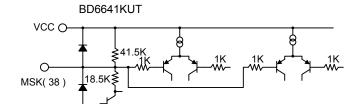
Fig. 23

Fig. 22



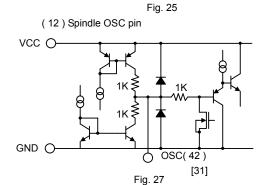




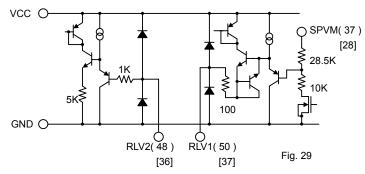


(10) Spindle MSK pin

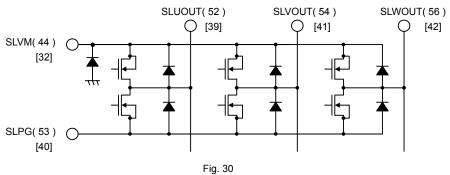
GND C



( 14 ) Spindle rotor position detection level setting pin



(15) Sled output



(16 ) Sled BEMF detection comparator

VCC

10K

10K

10K

10K

10K

SLVOUT(54 ) SLWOUT(56 )

[39]

[41]

#### ●Notes on the use

#### 1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

#### 2) Reverse polarity connection of the power supply

Connecting the of power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

#### 3) Power supply lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, note that capacitance characteristic values are reduced at low temperatures.

#### 4) GND voltage

Ground-GND potential should maintain at the minimum ground voltage level. Furthermore, no terminals should be lower than the GND potential voltage including an electric transients.

#### 5) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

#### 6) Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if positive and ground power supply terminals are reversed. The IC may also be damaged if pins are shorted together or are shorted to other circuit's power lines.

#### 7) Operation in a strong magnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

#### 8) ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

# 9) Thermal shutdown circuit (TSD)

When the chip temperature (Tj) becomes 175°C (Typ.), thermal shutdown circuit (TSD circuit) operates and makes the coil output to motor open. There is a temperature hysteresis of approx. 20°C (Typ.). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

#### 10) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to, or removing it from a jig or fixture, during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting and storing the IC.

#### 11) Regarding input pin of the IC

This monolithic IC contains  $P^+$  isolation and P substrate layers between adjacent elements to keep them isolated. P–N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic diode and transistor.

Parasitic elements can occur inevitably in the structure of the IC. The operation of parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

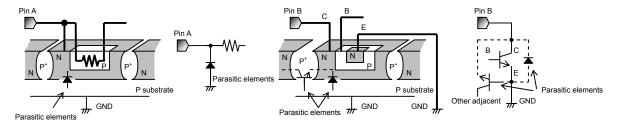
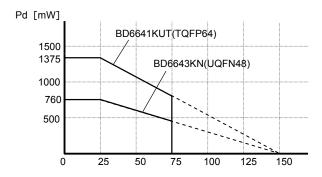


Fig.32 Example of a simple IC structure

#### 12) Ground wiring patterns

The power supply and ground lines must be as short and thick as possible to reduce line impedance. Fluctuating voltage on the power ground line may damage the device.

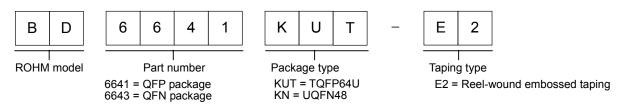
#### Power dissipation characteristics



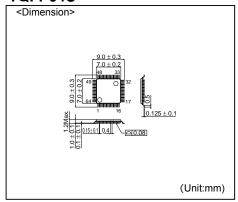
\*Reduced by 11mW/°C (BD6641KUT) and by 7.6mW/°C (BD6643KN) over Ta=25°C, when mounted on a glass epoxy board (70mm×70mm×1.6mm).

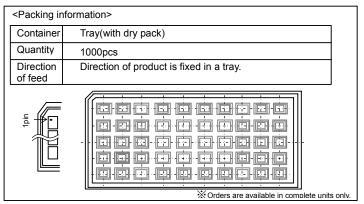
Fig. 33

#### Selecting a Model Name When Ordering

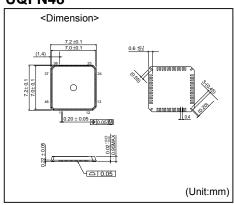


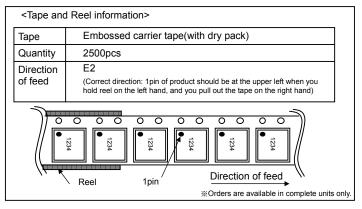
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