

4ch System Motor Driver IC

BD8229EFV

General Description

BD8229EFV is a 5-input, 4-output, BTL driver developed for driving Spindle motor, Sled/Loading motor and actuator coil. The hysteresis comparator for reset is built-in, so the number of parts can be reduced when designing a set.

Features

- 4CH BTL Driver
- Wide dynamic range
($V_{PREVCC}=V_{POWVCC}=8V, R_L=8\Omega, 6.0V$ (Typ))
- Built-in thermal shut down circuit
- Separate VCC into Pre and Power (Power divides into CH1/2 and CH3/4), which can improve power efficiency
- Switches CH2 input by Control input terminal (CNT)
- Incorporates mute function by CNT terminal and MUTE terminal
- Built in hysteresis comparator for reset

Applications

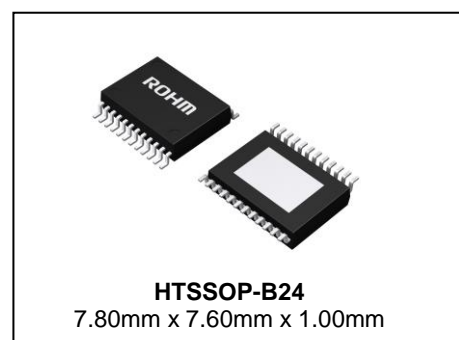
Car Audio

Key Specifications

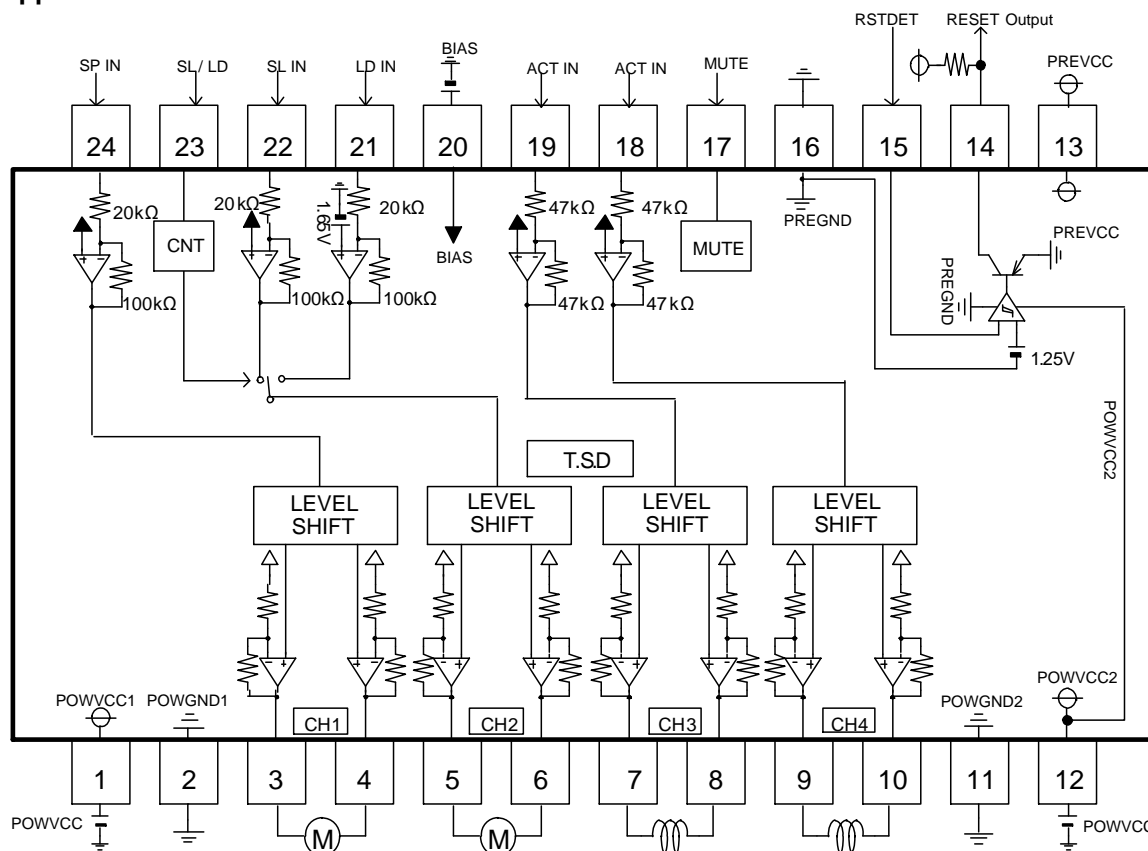
- PRE Part Power Supply Range: 4.5V to 14V
- DC Motor System Power Supply Range: 4.5V to V_{PREVCC} V
- Actuator System Power Supply Range: 4.5V to V_{PREVCC} V
- Operating Temperature Range: -40°C to +85°C

Package

W(Typ) x D(Typ) x H(Max)

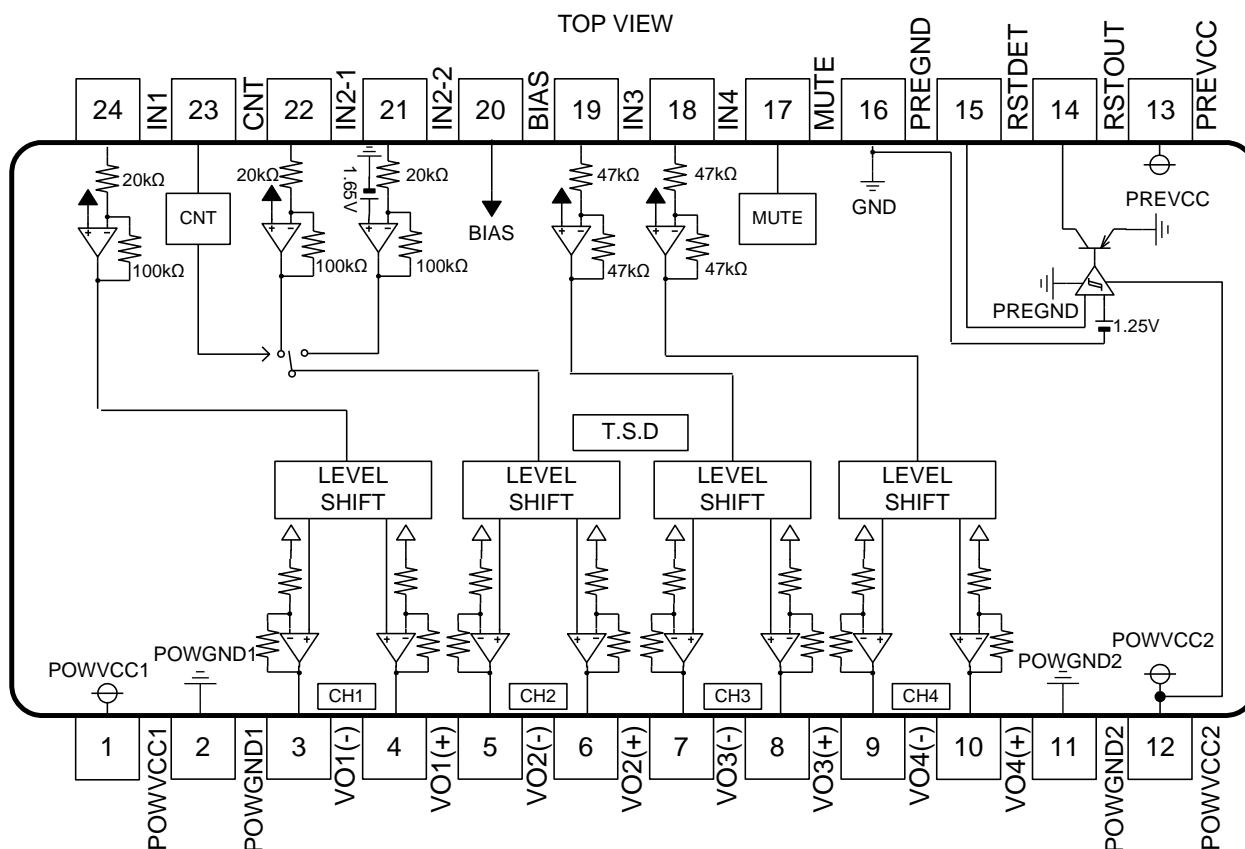


Typical Application Circuit



TSD : Thermal Shut-Down

Block Diagram and Pin Configuration



Pin Descriptions

No.	Symbol	Description	No.	Symbol	Description
1	POWVCC1	CH1,2 power supply terminal	13	PREVCC	PRE, RESET power supply terminal
2	POWGND1	Power GND1	14	RSTOUT	Reset output
3	VO1(-)	Driver CH1 negative output	15	RSTDET	Reset detection comparator input
4	VO1(+)	Driver CH1 positive output	16	PREGND	PRE, RESET Block GND
5	VO2(-)	Driver CH2 negative output	17	MUTE	MUTE terminal
6	VO2(+)	Driver CH2 positive output	18	IN4	CH4 input
7	VO3(-)	Driver CH3 negative output	19	IN3	CH3 input
8	VO3(+)	Driver CH3 positive output	20	BIAS	BIAS input terminal
9	VO4(-)	Driver CH4 negative output	21	IN2-2	CH2-2 input
10	VO4(+)	Driver CH4 positive output	22	IN2-1	CH2-1 input
11	POWGND2	Power GND2	23	CNT	Control input terminal
12	POWVCC2	CH3,4 power supply terminal	24	IN1	IN1 input

Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
Power Supply Voltage	$V_{PREVCC}, V_{POWVCC1}, V_{POWVCC2}$	15	V
Input Terminal Voltage 1	V_{IN1} (Note 1)	V_{PREVCC}	V
Input Terminal Voltage 2	V_{IN2} (Note 2)	$V_{POWVCC2}$	V
Power Dissipation	Pd	1.1 (Note 3)	W
		4.0 (Note 4)	
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	+150	°C

(Note 1) IN1 Application terminal : IN1, CNT, IN2-1, IN2-2, BIAS, IN3, IN4, MUTE

(Note 2) IN2 Application terminal : RSTDET

(Note 3) 70mm x 70mm x 1.6mm, 1 layer substrate, (copper foil 0mm x 0mm).

Reduce power dissipation capability by 8.8mW for each degree above 25°C.

(Note 4) 70mm x 70mm x 1.6mm, 4 layer substrate, (copper foil 70mm x 70mm)

Reduce power dissipation capability by 32.0mW for each degree above 25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Limit			Unit
		MIN	TYP	MAX	
PRE Part Power Supply (Note 1)	V_{PREVCC}	4.5	8	14	V
DC Motor System Power Supply (Note 1)	$V_{POWVCC1}$	4.5	8	V_{PREVCC}	V
Actuator System Power Supply (Note 1)	$V_{POWVCC2}$	4.5	8	V_{PREVCC}	V

(Note 1) Take into consideration the allowable power dissipation when setting the power supply voltage.

Electrical Characteristics

(Unless otherwise noted, Ta=25°C, $V_{PREVCC}=V_{POWVCC1}=V_{POWVCC2}=8V$, $V_{BIAS}=1.65V$, $R_L=8\Omega$)

Parameter	Symbol	Limit			Unit	Conditions
		MIN	TYP	MAX		
Quiescent Dissipation Current	I_Q	-	30	45	mA	At no-load
< Driver >						
Output Offset Voltage (CH1,2)	V_{OOF12}	-100	0	+100	mV	
Output Offset Voltage (CH3,4)	V_{OOF34}	-50	0	+50	mV	
Maximum Output Amplitude (CH1,2)	V_{OM12}	5.4	6.0	-	V	
Maximum Output Amplitude (CH3,4)	V_{OM34}	4.7	5.3	-	V	
Closed Circuit Voltage Gain (CH1,2)	G_{V12}	24.0	25.7	27.4	dB	
Closed Circuit Voltage Gain (CH3,4)	G_{V34}	15.5	17.5	19.5	dB	
MUTE Terminal Low Level Input Voltage	V_{ML}	-	-	0.5	V	
MUTE Terminal High Level Input Voltage	V_{MH}	2.0	-	-	V	
CNT Terminal Low Level Input Voltage	V_{CNTL}	-	-	0.5	V	
CNT Terminal High Level Input Voltage	V_{CNTH}	2.0	-	-	V	
LDIN Terminal Voltage (SLED input)	V_{LDIN}	-	0.1	0.3	V	CNT='L'
Internal Bias Voltage	V_{BIN}	1.53	1.65	1.77	V	CNT='H'
< Reset >						
Reset Release Voltage	V_{DET}	1.19	1.25	1.31	V	
Hysteresis Voltage	V_{HYS}	5	25	55	mV	
Detection Terminal Outflow Current	I_{CMP}	-	50	150	nA	
RSTOUT Output Low Voltage	V_{RSTOUT}	-	0.1	0.3	V	3.3V pull-up (10kΩ)

Application Information

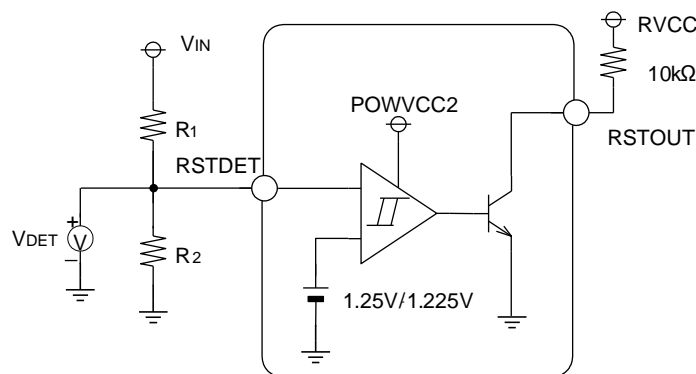
1. Functional Description

- (1) The driver is put on mute by switching the MUTE terminal and the CNT terminal to High level and Low level respectively. The table below shows the logic.

INPUT		OUTPUT	
MUTE	CNT	CH1,3,4	CH2
H	H	ACTIVE	LD ON
H	L	ACTIVE	SL ON
L	H	MUTE	LD ON
L	L	MUTE	MUTE

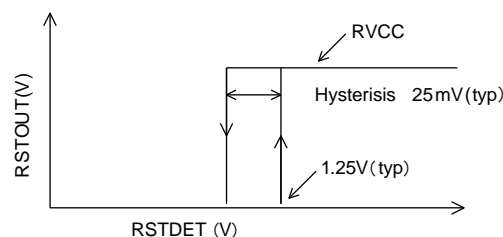
SL : SLED LD : Loading

- (2) The mute works when the bias terminal (Pin 20) becomes 0.7V (Typ) or less. Please set it to 1.3V or higher to put outputs in ACTIVE state. (However, the mute doesn't work for CH2 at CNT='H'.)
- (3) When the power-supply voltage becomes 3.8V (Typ) or less, the output terminal will be in MUTE state. When the power-supply voltage rises up to 4.0V again, the driver part circuit starts up.
- (4) The threshold voltage of POWVCC2 reset can be calculated by the following expressions.



$$V_{IN} = \frac{R_1 + R_2}{R_2} \times V_{DET}$$

- (a) The threshold voltage of POWVCC2 reset can be changed by external resistors R_1 and R_2 . The recommended resistance value of R_1 and R_2 is 100kΩ or less.
- (b) Please make the voltage of the RSTOUT output terminal that is pulled-up to RVCC lower than the voltage of POWVCC2 (Pin12).
- (c) The characteristic chart of RSTDET and RSTOUT is as follows.



2. The Picture of Application Board Wire Connection (Reference for BD8229EFV)

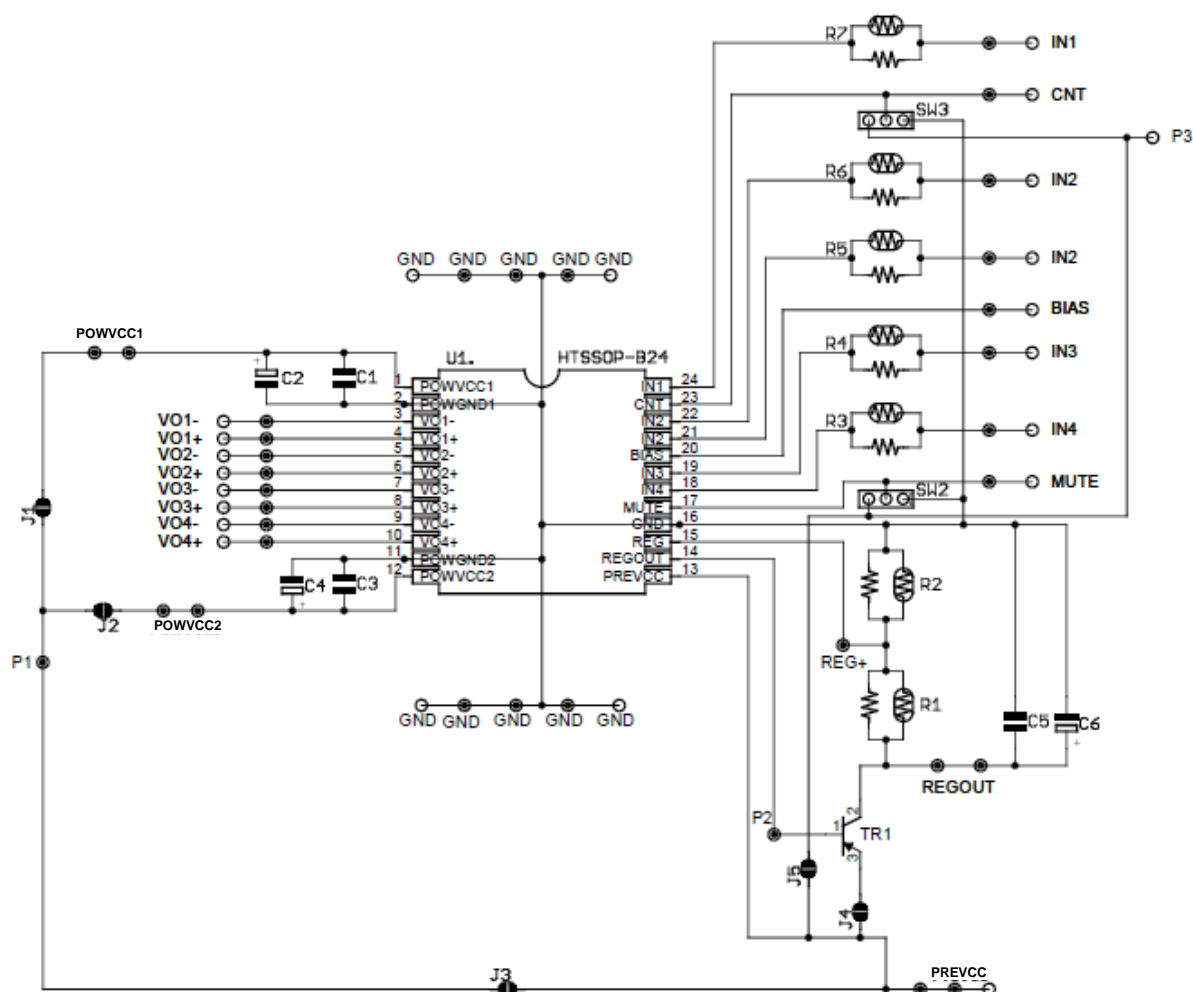
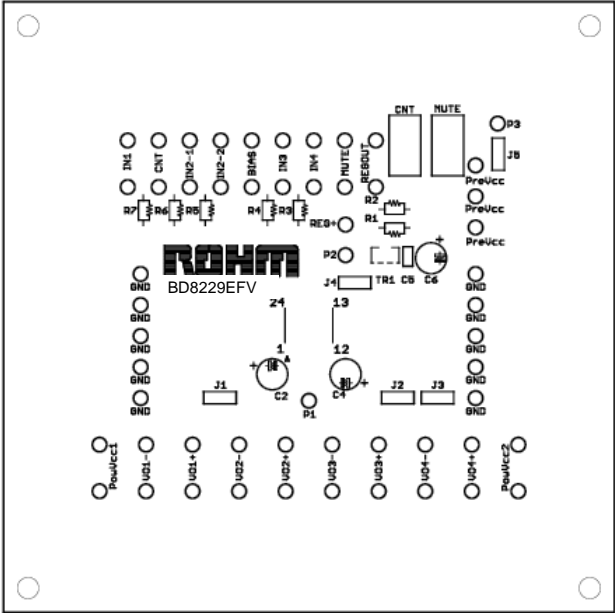
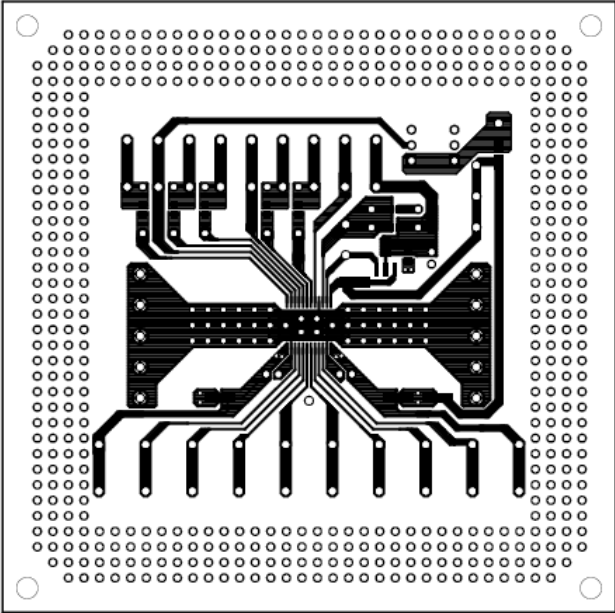


Figure 1. Application Board Wire Connection

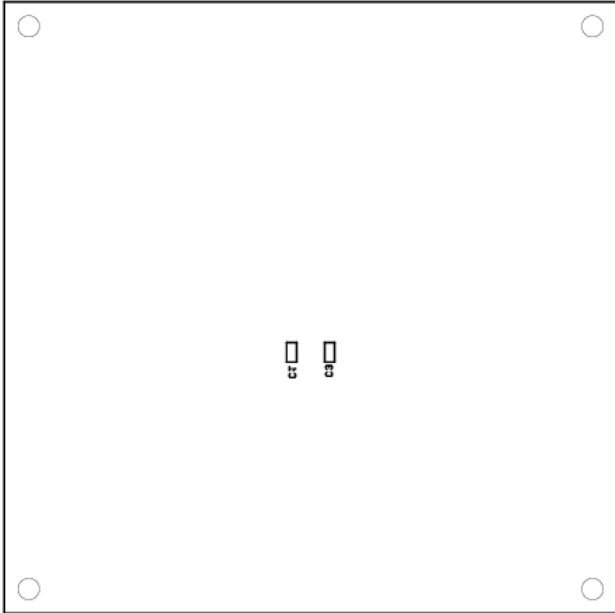
3. The Picture of Application Board PCB Pattern (Reference for BD8229EFV)



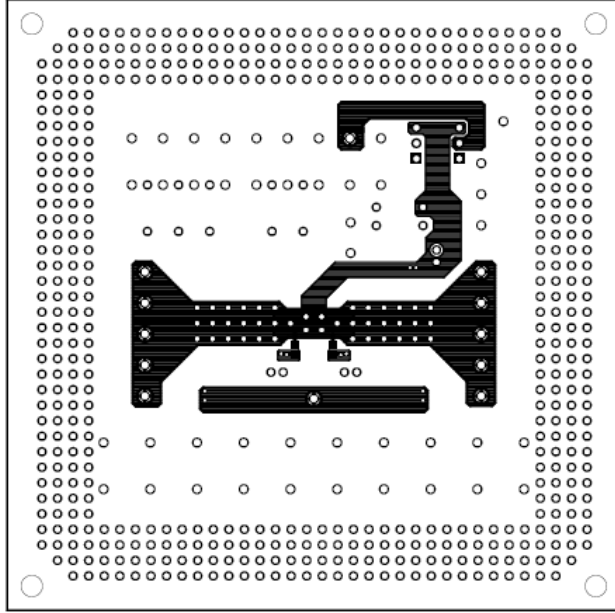
Top Silkscreen Overlay



Top Layer

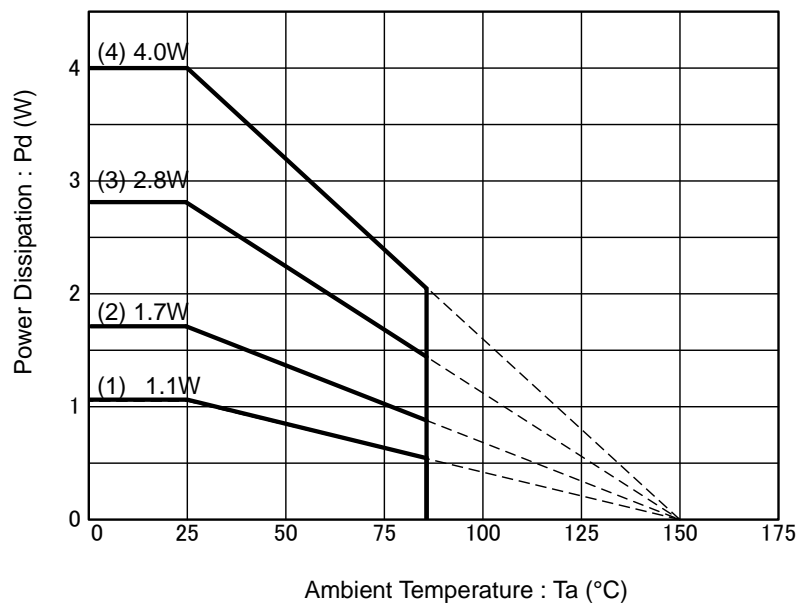


Bottom Silkscreen Overlay



Bottom Layer

Power Dissipation



<Conditions>

- 70mm x 70mm x 1.6mm glass epoxy substrate
(power dissipation changes with the layer number and the copper foil density of the board.)
- The board and the IC's bottom thermal plate are solder-connected.

Board(1) : 1 –layer board (copper foil 0mm x 0mm)
 Board(2) : 2 –layer board (copper foil 15mm x 15mm)
 Board(3) : 2 –layer board (copper foil 70mm x 70mm)
 Board(4) : 4 –layer board (copper foil 70mm x 70mm)

Board(1) : $\theta_{ja}=113.6^{\circ}\text{C/W}$
 Board(2) : $\theta_{ja}=73.5^{\circ}\text{C/W}$
 Board(3) : $\theta_{ja}=44.6^{\circ}\text{C/W}$
 Board(4) : $\theta_{ja}=31.3^{\circ}\text{C/W}$

I/O Equivalent Circuits

Bias terminal		Input terminal	
Driver output		Input terminal	
Mute		Input terminal	
Control		Input terminal	
Driver output		Input terminal	
Reset output		Reset detection Comparator input	

(Note) Resistance in the above-mentioned terminal equivalent circuit chart are typical values at T=25°C.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin\ A$ and $GND > Pin\ B$, the P-N junction operates as a parasitic diode.

When $GND > Pin\ B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

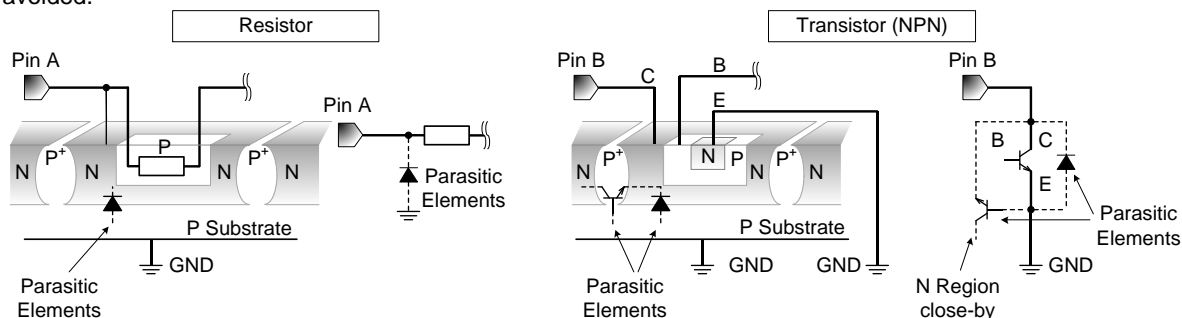


Figure 2. Example of monolithic IC structure

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF all output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

TSD ON temperature [°C] (typ)	Hysteresis temperature [°C] (typ)
175	25

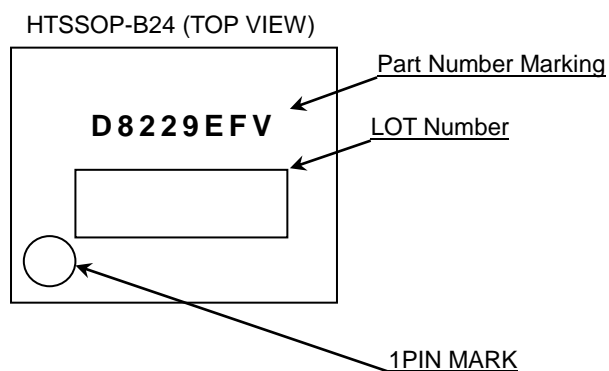
15. Capacitor Between Output and Ground

If a large capacitor is connected between the output pin and ground pin, current from the charged capacitor can flow into the output pin and may destroy the IC when the VCC or IN pin is shorted to ground or pulled down to 0V. Use a capacitor smaller than 0.1 μF between output and ground.

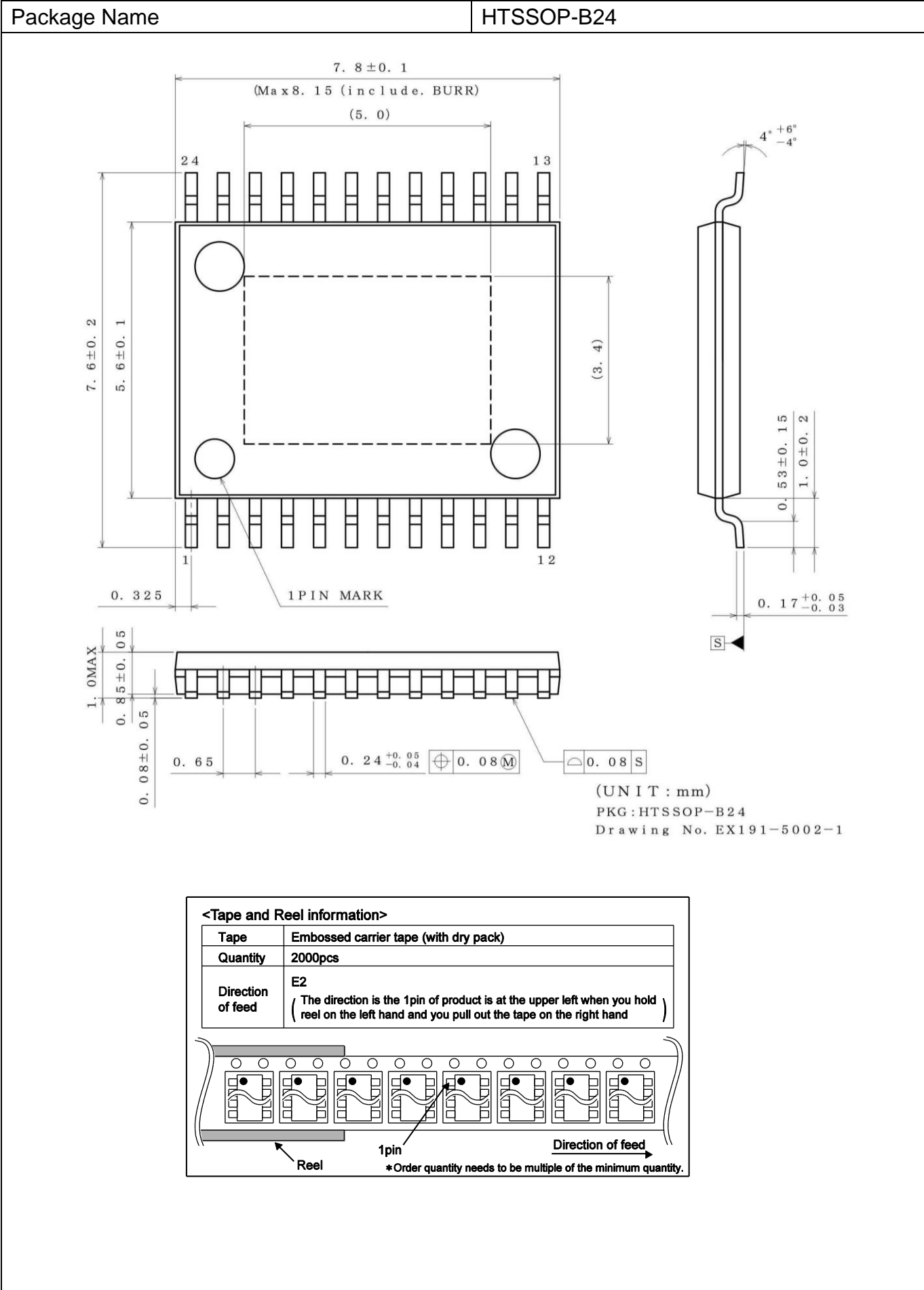
Ordering Information

B D 8 2 2 9 E F V									-	E 2	
Part number									Package EFV : HTSSOP-B24		Packaging and forming specification E2: Embossed tape and reel

Marking Diagram



Physical Dimension, Tape and Reel Information



Revision History

Date	Revision	Changes
04.Nov.2015	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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