

Constant Current LED Drivers

50V 500mA

1ch Source Driver for Automotive

BD8374HFP-M BD8374EFJ-M

General Description

BD8374HFP-M and BD8374EFJ-M are 50V-withstanding LED source drivers. Most suitably for Automotive LED driving, it can control light through PWM of constant current output.

Having LED open/short detective circuit and overvoltage mute functions integrated, it can deliver high reliability.

Also by utilizing our patented PBUS function, it is possible to turn OFF all LEDs in case where a row of LEDs are short/open-circuited if multiple rows of LEDs are driven through multiple number of the ICs.

Features

- AEC-Q100 Qualified
- Variable form Constant-Current Source Driver
- PWM Dimming Function
- CR Timer for PWM Dimming Function Integrated
- LED Open/Short detective Circuit Function Integrated
- Overvoltage Mute and Temperature Protection Functions Integrated
- Abnormal Output Detection and Output Functions (PBUS)

Application

- On-board Exterior Lamp
(Rear Lamp, Turn Lamp, DRL/Position Lamp, Fog Lamp, etc.)
- On-board Interior Lamp
(Air Conditioner Lamp, Interior Lamp, Cluster Light, etc.)

Basic Application Circuit

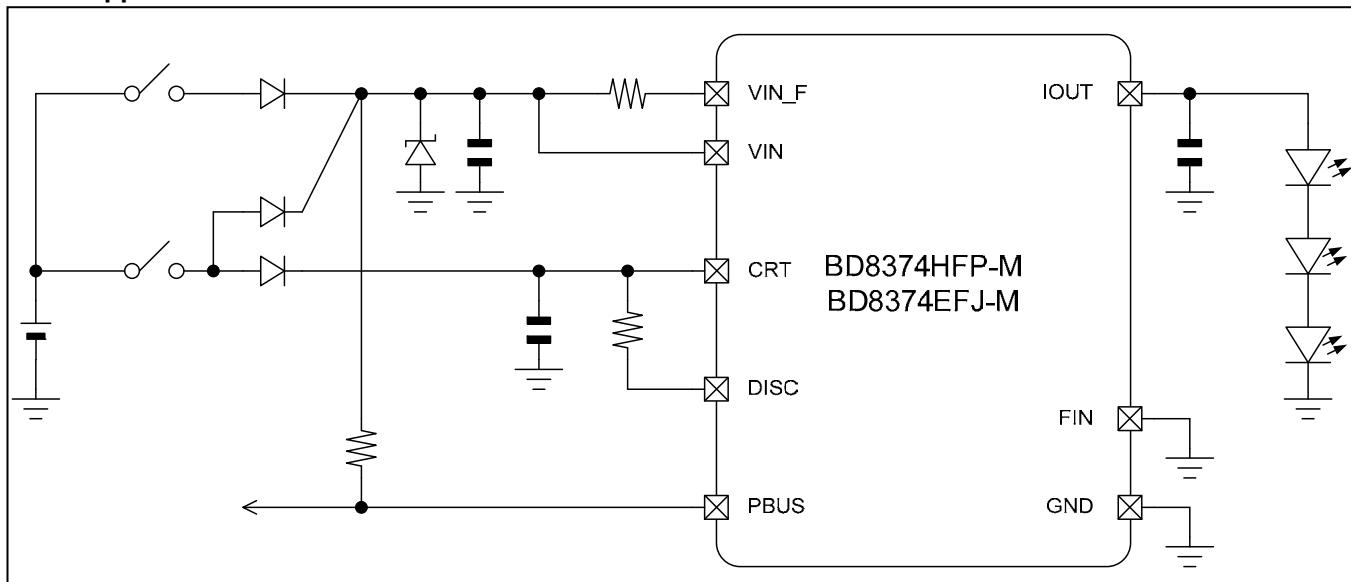


Figure 1. Typical Application Circuit

Product configuration: Silicon monolithic integrated circuit The product is not designed for radiation resistance.

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Pin Configurations

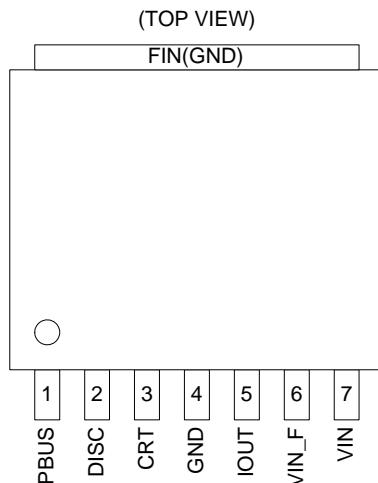


Figure 2. HRP7 Package Pin Configuration

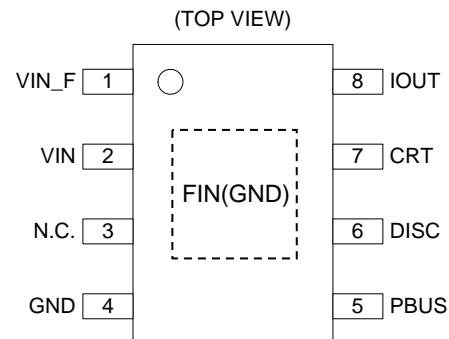


Figure 3. HTSOP-J8 Package Pin Configuration

Pin Descriptions

HRP7 Package

Pin No.	Pin Name	Function
1	PBUS	Error detection I/O
2	DISC	Discharge setting
3	CRT	PWM dimming timer setting
4	GND	GND
5	IOUT	Current output
6	VIN_F	Output current detection
7	VIN	Power supply input

HTSOP-J8 Package

Pin No.	Pin Name	Function
1	VIN_F	Output current detection
2	VIN	Power supply input
3	N.C.	N.C.
4	GND	GND
5	PBUS	Error detection I/O
6	DISC	Discharge setting
7	CRT	PWM dimming timer setting
8	IOUT	Current output

Block Diagram

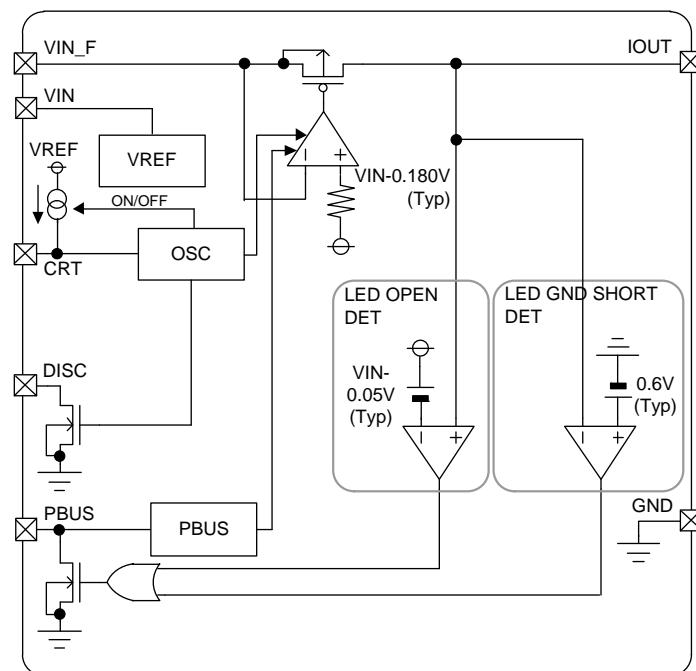


Figure 4. Block Diagram

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol		Rating	Unit
Supply Voltage	VIN		-0.3 ~ +50	V
VIN_F,CRT,DISC,IOUT,PBUS Terminal Voltage	VVIN_F,VCRT,VDISC,VOUT,VPBUS		-0.3 ~ VIN+0.3	V
Power Dissipation	Pd	HRP7	2.3 ^(Note1)	W
		HTSOP-J8	1.1 ^(Note2)	
Operating Temperature Range	Topr		-40~125	°C
Storage Temperature Range	Tstg		-55~150	°C
Junction Temperature	Tjmax		150	°C
IOUT Output Maximum Current	IOUT		500	mA

(Note1) HRP7
Derate by 18.4mW/°C when operating above Ta=25°C
(when mounted in ROHM's standard board(70mm×70mm×1.6mm) 2 layer copper foil(15mm×15mm)).

(Note2) HTSOP-J8
Derate by 8.8mW/°C when operating above Ta=25°C
(when mounted in ROHM's standard board(70mm×70mm×1.6mm) 2 layer copper foil(15mm×15mm)).

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage ^(Note1)	VIN	4.5~42.0	V
Operating Temperature Range	Topr	-40~125	°C
Current Setting Resistor	RVIN_F	0.36~3.6	Ω
Minimum capacitor connecting IOUT terminal	CiOUT_MIN	0.1	μF
CRTIMER Frequency Range	F_PWM	100~5000	Hz
PWM Minimum Pulse Width	TMIN	20	μs

(Note1) Pd, ASO should not be exceeded

Electrical Characteristics (Unless otherwise specified $T_a = -40 \sim 125^\circ C$, $V_{IN} = 13V$, $R_{VIN_F} = 0.47\Omega$, $R_{PBUS} = 10k\Omega$)

Parameter	Symbol	Min	Typ	Max	UNIT	Condition
Circuit Current	I_{VIN}	-	2.1	6.0	mA	
I _{OUT} Terminal Output Current Accuracy	I_{OUT}	373	383	393	mA	$T_a = 25^\circ C$
		364	383	402	mA	$T_a = -40^\circ C \sim 125^\circ C$
$V_{IN} - I_{OUT}$ Drop Voltage	V_{DR_IOUT}	-	0.45	1.0	V	$I_{OUT} = 383mA$
I _{OUT} Terminal OFF Current	I_{OUT_OFF}	-	-	1	μA	$V_{OUT} = 2V$, $V_{CRT} = 0.7V$ $T_a = 25^\circ C$
I _{OUT} Current at GND Short	I_{OUT_SHORT}	-	-	40	μA	$V_{OUT} = 0V$
V_{IN_F} Terminal Voltage	$V_{IN_F_REF}$	0.171	0.180	0.189	V	$V_{IN_F_REF} = V_{IN} - V_{IN_F}$
I _{OUT} Voltage at LED Open Detection	V_{OUT_OPEN}	$V_{IN} - 0.15$	$V_{IN} - 0.050$	$V_{IN} - 0.020$	V	
I _{OUT} Voltage at LED Open Detection Release	$V_{OUT_OPEN_RELEASE}$	$V_{IN} - 0.300$	$V_{IN} - 0.150$	$V_{IN} - 0.060$	V	
I _{OUT} Voltage at LED Short Detection	V_{OUT_SHORT}	0.2	0.6	1.0	V	
CRT Terminal Charge Current	I_{CRT_SO}	29.75	35.00	40.25	μA	$V_{CRT} = 0.9V$
CRT Terminal Charge Voltage	V_{CRT_CHA}	0.990	1.10	1.21	V	
CRT Terminal Discharge Voltage 1	V_{CRT_DIS1}	2.7	3.0	3.3	V	
CRT Terminal Discharge Voltage 2	V_{CRT_DIS2}	3.6	4.0	4.4	V	$R_{D1} \leftrightarrow R_{D2}$ ^(Note1)
CRT Terminal Charge Resistance	R_{CHA}	51.6	54.3	57.0	$k\Omega$	$R_{CHA} = (V_{CRT_DIS1} - V_{CRT_CHA}) / I_{CRT_SO}$
DISC Terminal Discharge Resistance 1	R_{D1}	-	50.0	100	Ω	$V_{CRT} = 3.4V$
DISC Terminal Discharge Resistance 2	R_{D2}	2.5	5.0	10	$k\Omega$	$V_{CRT} = 5V$
PBUS Terminal Input Voltage High	V_{IH_PBUS}	4.0	-	$V_{IN} + 0.20$	V	
PBUS Terminal Input Voltage Low	V_{IL_PBUS}	$GND - 0.20$	-	2.0	V	
PBUS Terminal Low Voltage	V_{OL_PBUS}	-	-	1.5	V	$I_{PBUS} = 2mA$
PBUS Terminal Input Current	I_{IN_PBUS}	-	38.0	100	μA	$V_{PBUS} = 13V$
Overvoltage Mute	$V_{IN_OVPMUTE}$	27	29	33	V	$V_{OUT} = 6V$

(Note) This product is not designed for use in radioactive environments.

(Note1) Refer to Functional Description

Typical Performance Curves (Reference Data)
(Unless otherwise specified $T_a=25^{\circ}\text{C}$, $V_{IN}=V_{IN_F}=13\text{V}$)

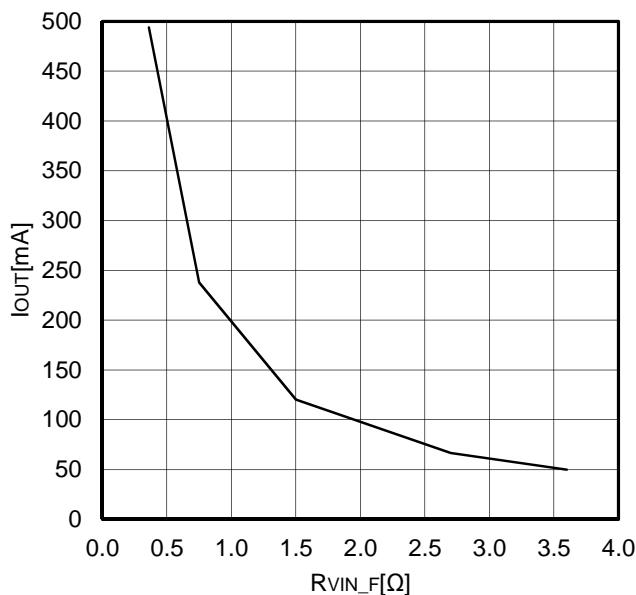


Figure 5. RVIN_F vs IOUT

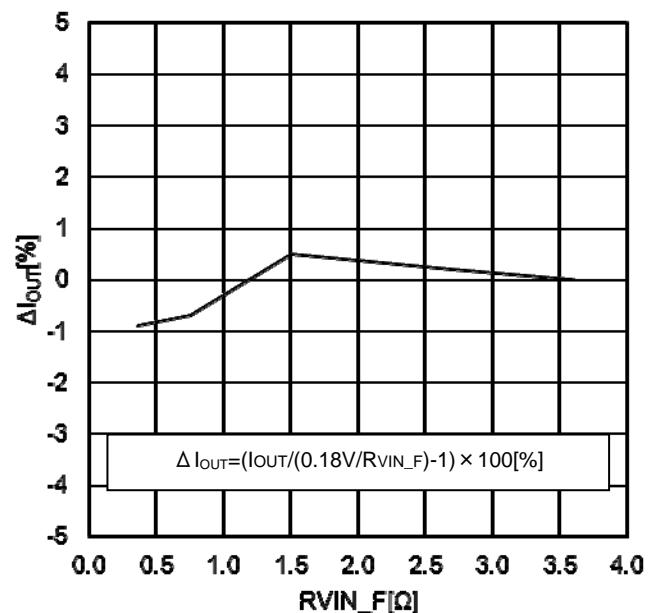


Figure 6. RVIN_F vs ΔIOUT

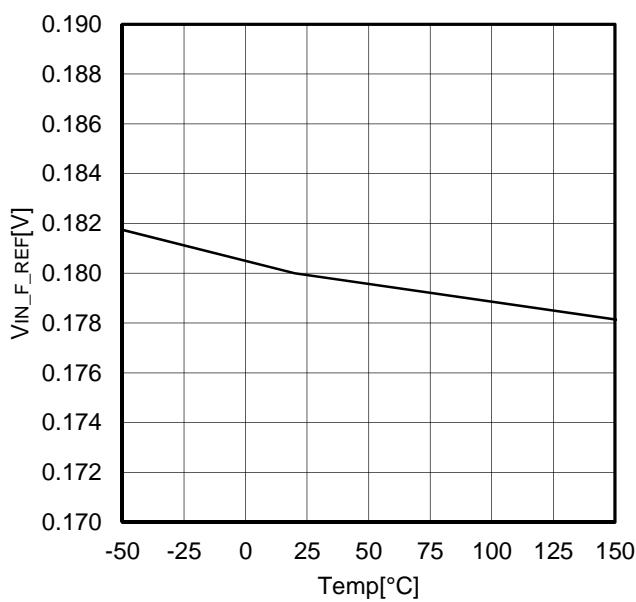


Figure 7. Temperature vs VIN_F_REF

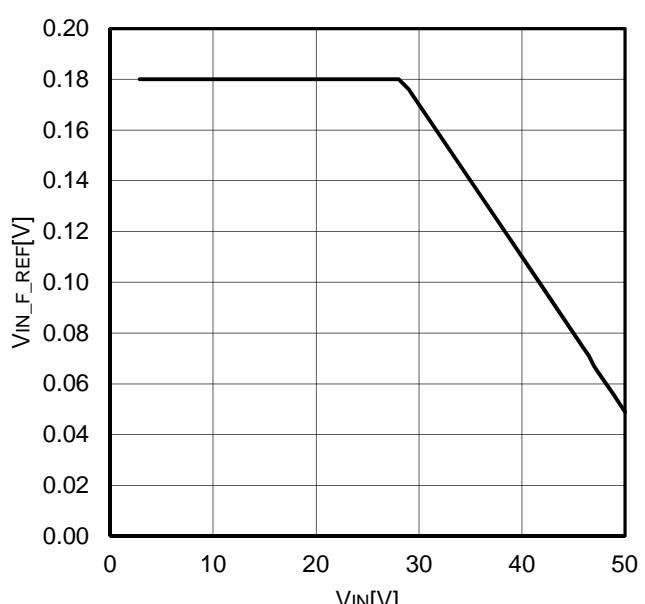


Figure 8. VIN vs VIN_F_REF

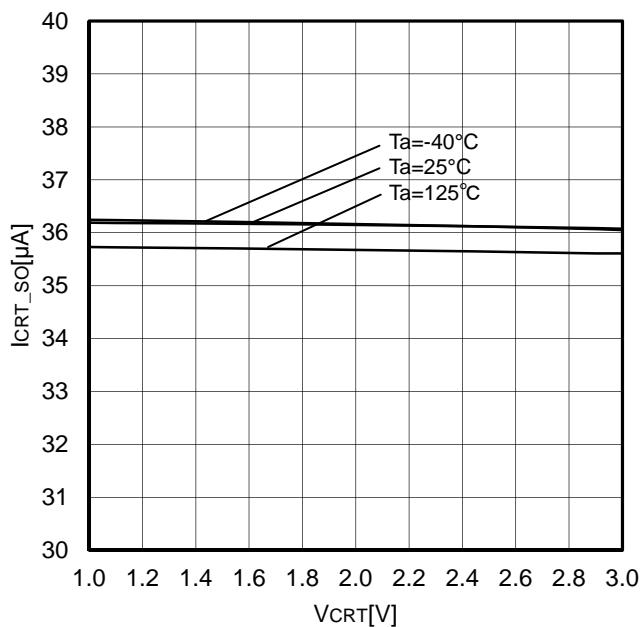


Figure 9. VCRT vs ICRT_SO
(VCRT:CRT Terminal Voltage)

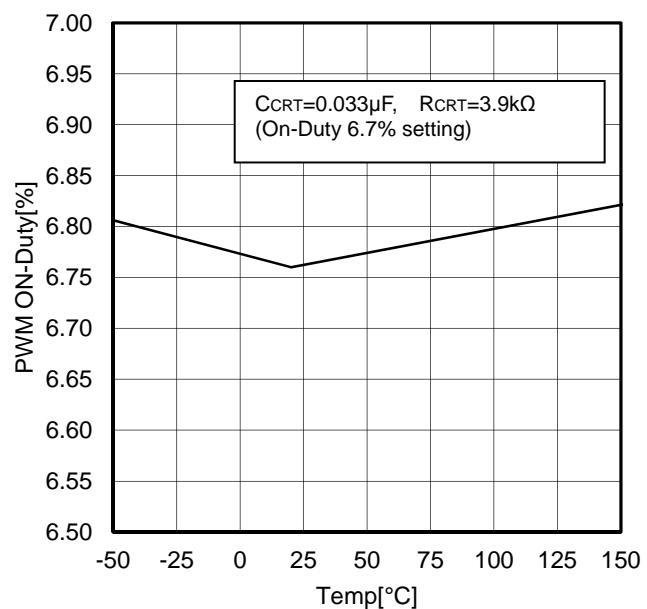


Figure 10. Temperature vs PWM ON Duty

Functional Description(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{IN}=13\text{V}$, $I_{OUT}=6\text{V}$ and $R_{VIN_F}=0.47\Omega$. Numbers are "Typical" values.)**1. Output Current Setting**LED Current I_{OUT} can be set as below depending on values of current setting resistance R_{VIN_F} .

$$I_{OUT} = \frac{(V_{IN} - V_{IN_F})}{R_{VIN_F}} = \frac{V_{IN_F_REF}}{R_{VIN_F}} [\text{A}]$$

where:

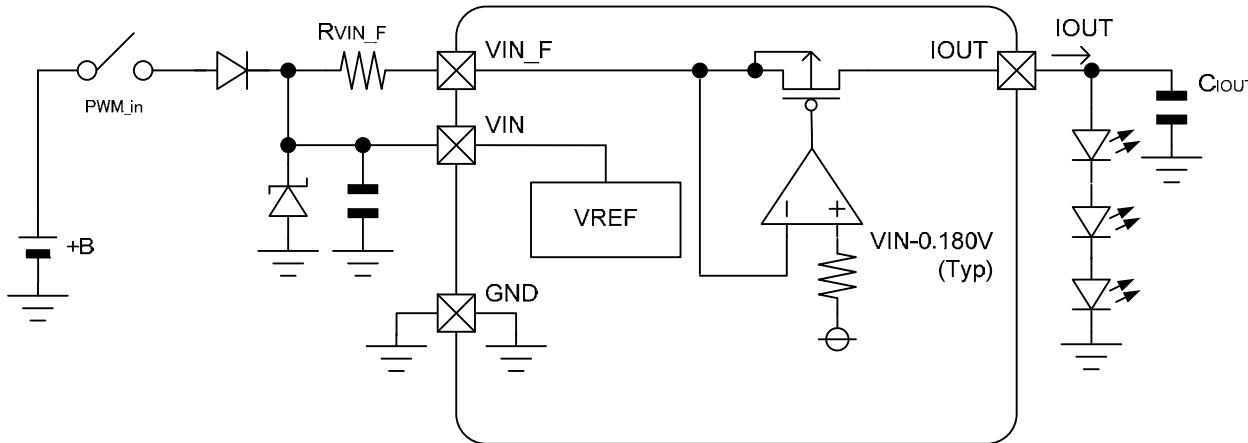
 $V_{IN_F_REF}$ is 0.18V (Typ)

Figure 11. Output Current Setting

2. Table of Operations

PWM dimming mode switches to linear control depending on CRT terminal voltage.

When CRT terminal voltage surpasses $V_{CRT_DIS2}(4.0\text{V}(\text{Typ}))$, Dimming mode turns to Linear Control, and discharge resistance of DISC terminal changes from $R_{D1}(50\Omega(\text{Typ}))$ to $R_{D2}(5\text{k}\Omega(\text{Typ}))$.

LED open/short-circuit protection is activated depending on IOUT terminal voltage status, and output current is turned OFF. Output current is also turned OFF when Low signal is input to PBUS terminal.

Operation Mode	CRT Terminal	IOUT Terminal Voltage (V_{IOUT})	Output Current (I_{OUT})	PBUS Terminal
Linear Control	$4.0\text{V}(\text{Typ}) \leq V_{CRT}$	-	$50\text{mA} \sim 500\text{mA}$	Hi-Z
PWM dimming	OPEN	-	See Features Description, 3. PWM Light Control Operation	Hi-Z
LED Open	-	$V_{IOUT} \geq V_{IN} - 0.050\text{V}(\text{Typ})$	$1\mu\text{A}(\text{Max})$	Low Output
LED Short	-	$V_{IOUT} \leq 0.6\text{V}(\text{Typ})$	$40\mu\text{A}(\text{Max})$	Low Output
PBUS Control OFF	-	-	$1\mu\text{A}(\text{Max})$	Low Input

3. PWM Dimming Operation

PWM Dimming is performed if CRT terminal is the following circuit. Dimming cycle and Duty width can be set through external resistance value and capacity.

CR timer function in IC is activated if CRT terminal turned OPEN. In order to perform PWM light control of LED current, triangular waveform is generated at CRT terminal. Output is controlled so that **LED current is turned OFF** while CRT voltage is ramping up, and **LED current is turned ON** while CRT voltage is ramping down.

Ramp up/down time of CRT voltage can be set by values of external components (**C_{CRT}**, **R_{CRT}**).

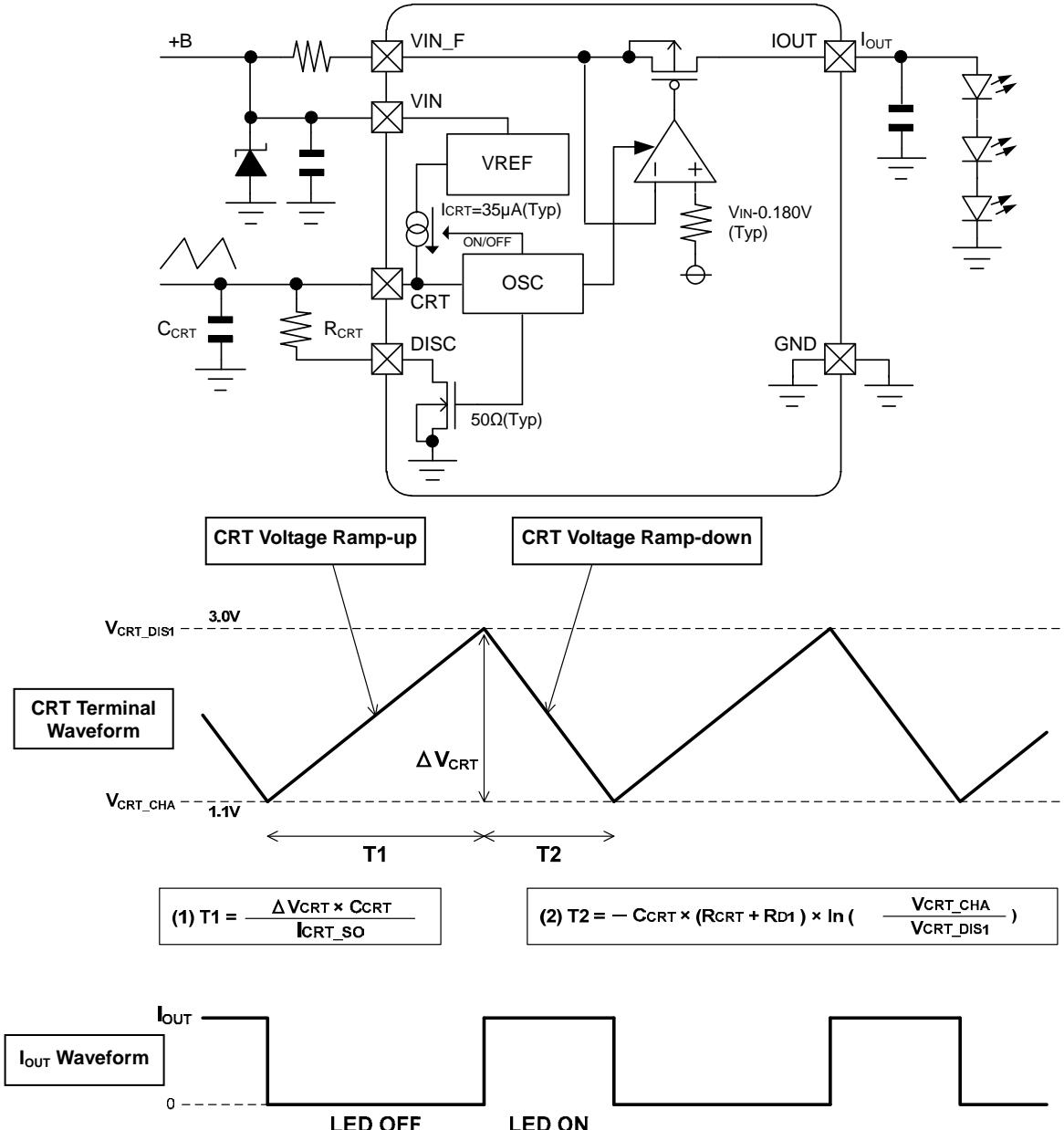


Figure 12. PWM Fimming Operation

(1) CRT Ramp up Time T1
CRT ramp up time can be obtained from the following equations:

$$T1 = \frac{\Delta V_{CRT} \times C_{CRT}}{I_{CRT_SO}} = R_{CHA} \times C_{CRT} [s]$$

where:

I_{CRT_SO} is the CRT Terminal Charge Current 35µA (Typ)
R_{CHA} is the CRT Terminal Charge Resistance 54.3kΩ(Typ)

(2) CRT Ramp down Time T2

CRT ramp down time is defined by discharge period due to external capacity C_{CRT} and resistance ($R_{CRT} + R_{D1}$).
(CRT Terminal Charge Current is OFF at CRT ramp down)
Make sure that T2 is set at not smaller than Min. pulse width 20μs(Min).

$$T2 = -C_{CRT} \times (R_{CRT} + R_{D1}) \times \ln\left(\frac{V_{CRT_CHA}}{V_{CRT_DIS1}}\right) \text{ [s]}$$

where:

R_{D1} is the CRT Terminal Discharge Resistance 1 50Ω (Typ)
 V_{CRT_CHA} is the CRT Terminal Discharge ON Voltage 1.1V (Typ)
 V_{CRT_DIS1} is the CRT Terminal Discharge OFF Voltage 3.0V (Typ)

(3) Dimming Frequency fPWM

PWM frequency is defined by T1 and T2.

$$f_{PWM} = \frac{1}{T_1 + T_2} \text{ [Hz]}$$

(4) ON Duty (DON)

Like the above, PWM ON duty is defined by T1 and T2.

$$D_{ON} = \frac{T_2}{T_1 + T_2}$$

(Ex) In case of $f_{PWM} = 518\text{Hz}$ and 6.7% Duty (Typ),

From $f_{PWM}=518\text{Hz}$; $T_1 + T_2 = 1 / f_{PWM} = 1 / 518\text{Hz} = 1931\mu\text{s}$

From ON Duty = 6.7%; CRT ramp up time T1 is $T_1 = (T_1 + T_2) \times 0.933 = 1801.6\mu\text{s}$

External capacity C_{CRT} is;

$$C_{CRT} = T_1 \times (I_{CRT} / \Delta V_{CRT}) = 1800.7\mu\text{s} \times 35\mu\text{A} / 1.9\text{V} \doteq \underline{0.033\mu\text{F}}$$

CRT ramp down time T2 is; $T_2 = (T_1 + T_2) \times 0.067 = 129\mu\text{s}$

External resistance R_{CRT} is;

$$R_{CRT} = -T_2 / (C_{CRT} \times \ln(V_{CRT_CHA} / V_{CRT_DIS})) \quad R_{D1} = -129\mu\text{sec} / (0.033\mu\text{F} \times \ln(1.1 / 3.0) - 50\Omega) \doteq \underline{3.9\text{k}\Omega}$$

In case where PWM signal is applied from external;

It is possible to directly input PWM signal from external microcomputer for Dimming.

Input PWM signal to CRT terminal. In that case, 'High' level voltage of PWM signal should be equal to or higher than V_{CRT_DIS2} (4.4V(Max)) and 'Low' level voltage of PWM signal should be equal to or less than V_{CRT_CHA} (0.99V(Min)).

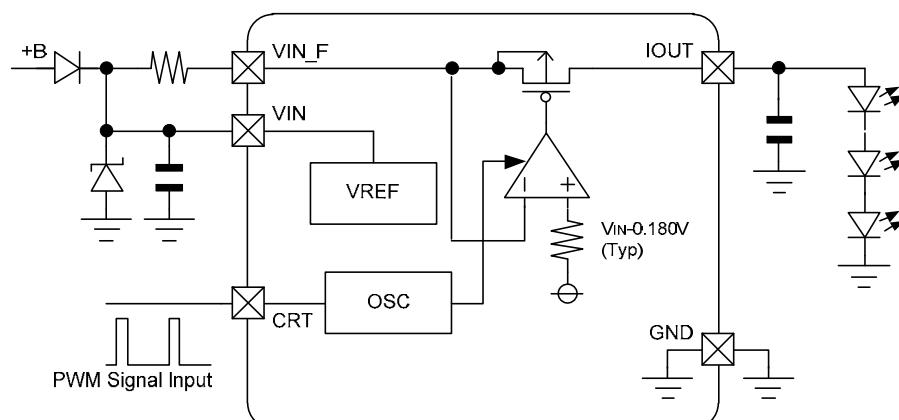


Figure 13. External Input of PWM Signal

4. LED Setting Range

Number of LED connections N should meet the following conditions:

$$V_{f_led} \times N \leq +B - V_{f_diode} - V_{IN_F_REF} - V_{DR_IOUT}$$

where:

+B is the Battery Voltage

V_{f_diode} is the Reverse Connection Preventing Diode Vf

$V_{IN_F_REF}$ is the V_{IN_F} Terminal Voltage ($V_{IN} - V_{IN_F}$)

V_{DR_IOUT} is the I_{OUT} Terminal Drop Voltage

V_{f_led} is the LED Vf

N is the Number of LED Levels

Ex) If you want to supply constant current to LED at 9V or higher Battery Voltage (+B) (Supposing that V_{f_diode} is 0.5V),

$$V_{f_led} \times N \leq +B - V_{f_diode} - V_{IN_F_REF} - V_{DR_IOUT} = 9V - 0.5V - 0.189V(\text{Max}) - 1.0V(\text{Max}) = 7.311V$$

(Sum of Vf of LED connected to I_{OUT} terminal is set to be 7.311V Max.)

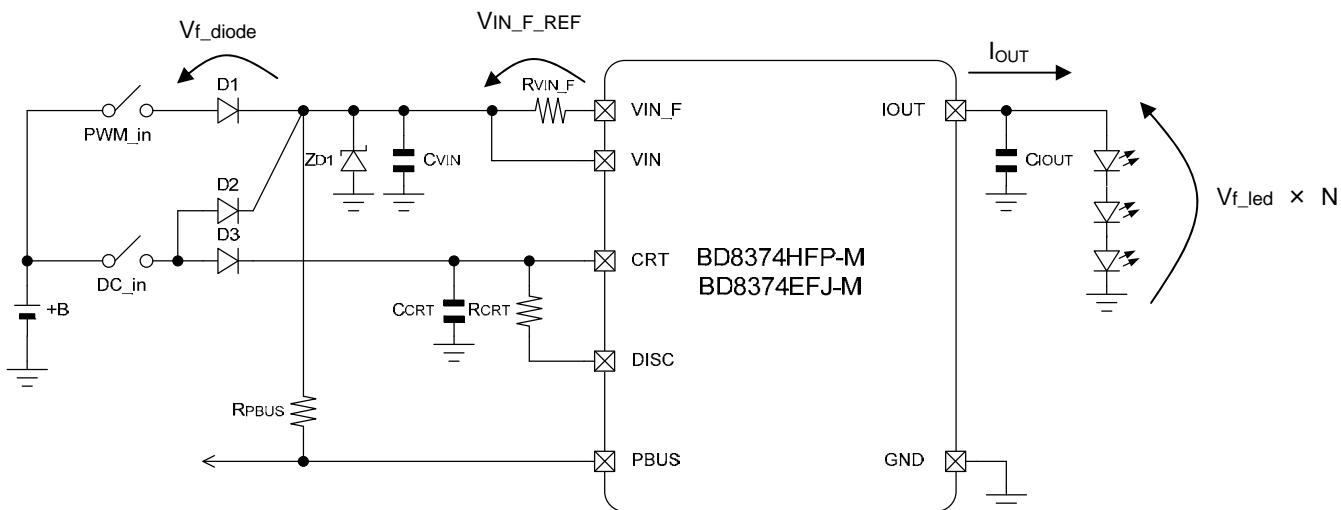


Figure 14. LED Setting Range Schematic

5. Overvoltage Mute

If $29V(\text{Typ}) \leq V_{IN}$, Overvoltage Mute is activated to restrict output current in order to suppress heat generated from IC. I_{OUT} attenuates by $3.2\% / V(\text{Typ})$.

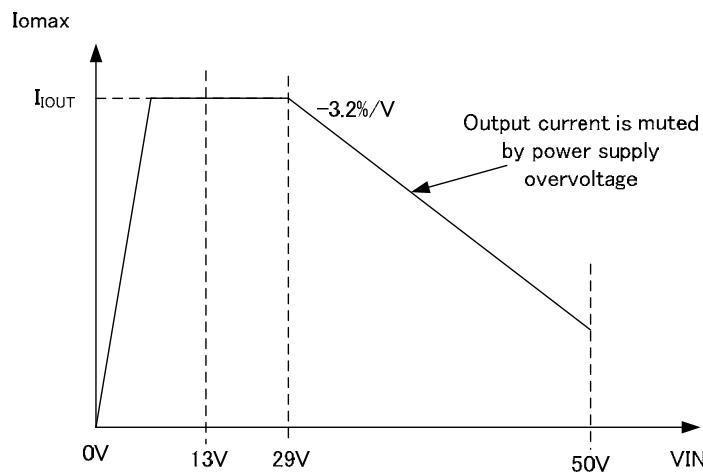


Figure 15. Overvoltage Mute Performance

6. Protective Function

In this IC integrated is a function for protection from short/open-circuit of external component, and it is possible to detect abnormal condition at PBUS terminal.

(1) LED Open Detective Function

In case where LED connected to IOUT terminal is open-circuited, it is detected due to overvoltage of IOUT terminal. During the detection, PBUS terminal is switched to Low to notify the trouble.

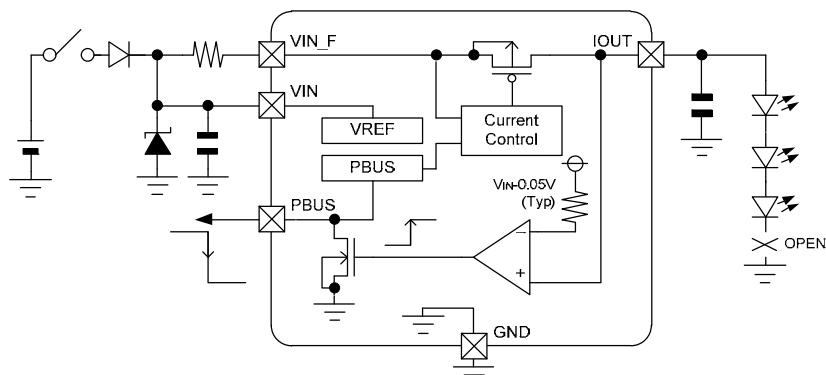


Figure 16. LED Open Detection

(2) LED Short-circuit Detective Function

In case where LED connected to IOUT terminal is short-circuited, it is detected due to low voltage of IOUT terminal. During the detection, output current is turned OFF to prevent thermal destruction of IC, and PBUS terminal is switched to Low to notify the trouble.

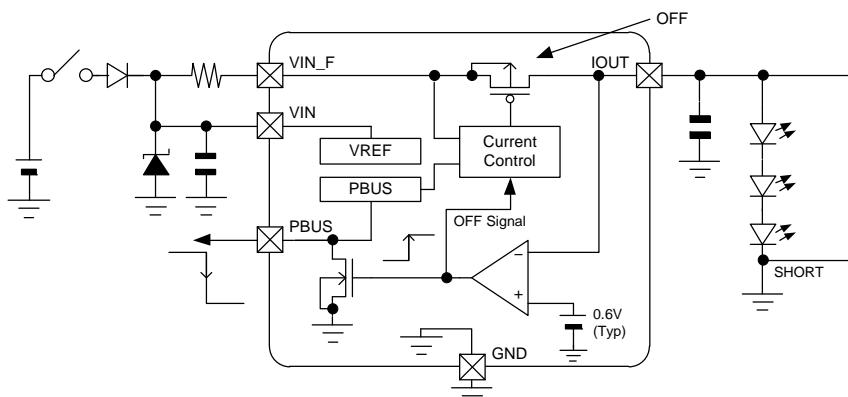


Figure 17. LED Short-circuit Detection

(3) I_{OUT} Current at GND Short (I_{OUT SHORT})

When V_{IOUT} is less than 1.4V(Typ), I_{OUT} Current at GND Short(I_{IOUT_SHORT}) flows from I_{OUT} terminal. It is varied due to I_{OUT} terminal Voltage.

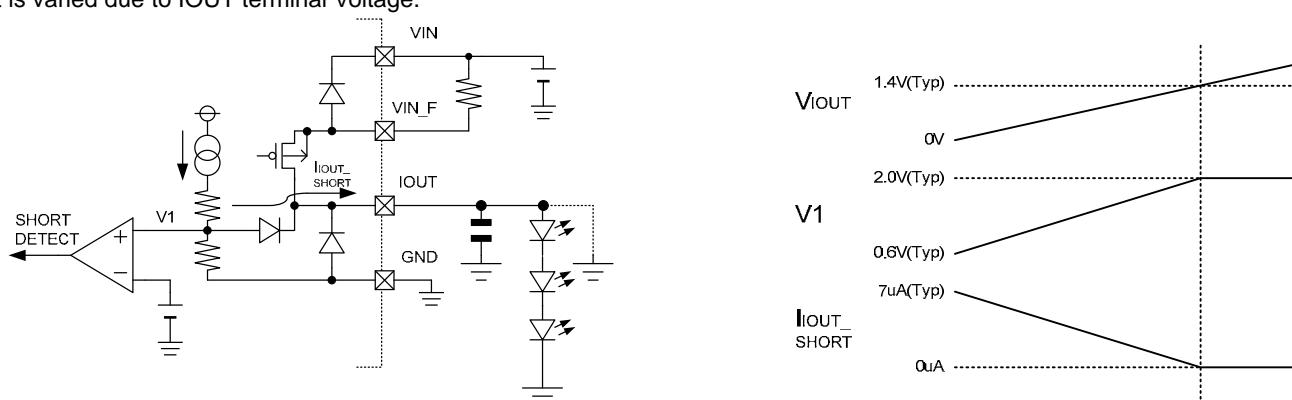


Figure 18. About I_{OUT} Current at GND Short

(4) About Active zone of LED Open Detective & LED Short Detective Function and IOUT Terminal Hi-Z zone

Active zone of LED Open Detective & LED Short Circuit Detective Function is different from Linear Control Mode and PWM dimming Mode.(Refer to Figure19.)

Linear Control Mode : Each function is active at All zone.

PWM dimming Mode : LED Open Detective Function is active only Fall time of V_{CRT}.
LED Short Circuit Detective Function is active at All zone.

There is **IOUT Terminal Hi-Z zone at PWM dimming Mode**.

To prevent Malfunction of LED Short Detective Function by noise^(Note1),

It is necessary to connect Capacitor(more than 0.1uF^(Note2))

between IOUT terminal and GND terminal nearby terminal

(ROHM Recommended Value : C_{OUT}=0.1μF GCM188R11H104KA42 murata)

(Note1) Conducted noise, Radiated noise, Interference of connector and PCB pattern etc...

(Note2) If connect more than 0.1uF, please evaluate the time of V_{IN} on to I_{OUT} on.

Linear Control Mode

V _{IN}	0V
V _{CRT}	0V
V _{OUT}	0V
I _{OUT}	0mA
IOUT Terminal Hi-Z zone	None
LED Open Detective Function	Active
LED Short Circuit Detective Function	Active

PWM dimming Mode

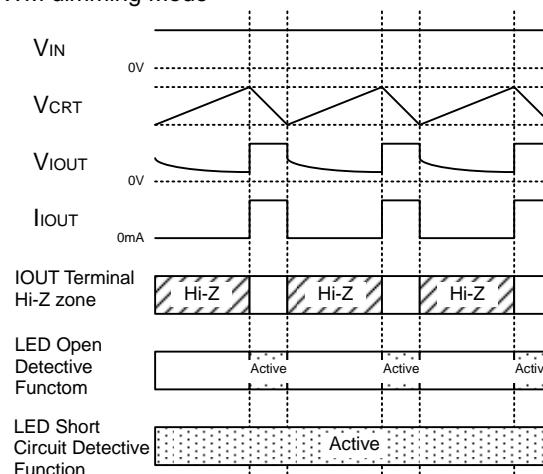


Figure 19. About Active zone of LED Open Detective & LED Short Detective Function and IOUT Terminal Hi-Z zone

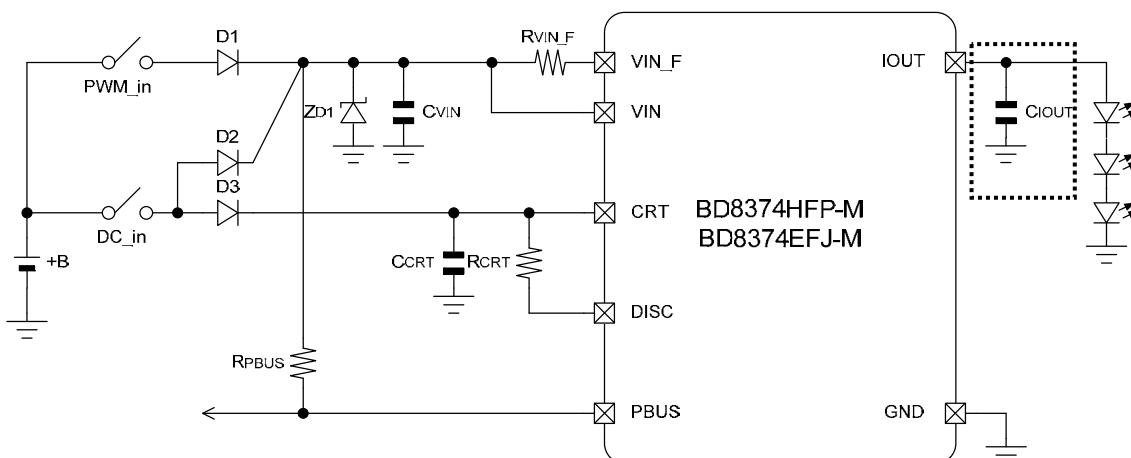
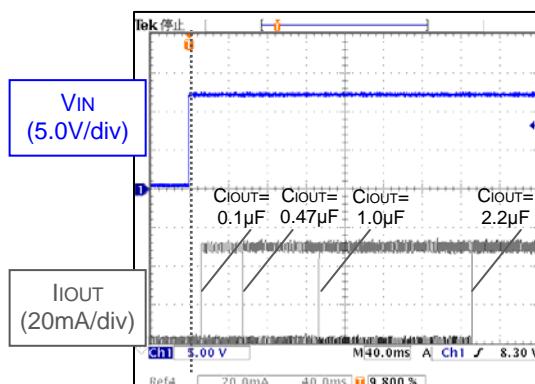


Figure 20. About the capacitor of connecting IOUT terminal

Evaluation example(The time of VIN on to IOUT on)

Condition : +B=13V
 Ta=25°C
 LED 3Strings
 VCRT=VIN
 DC Mode

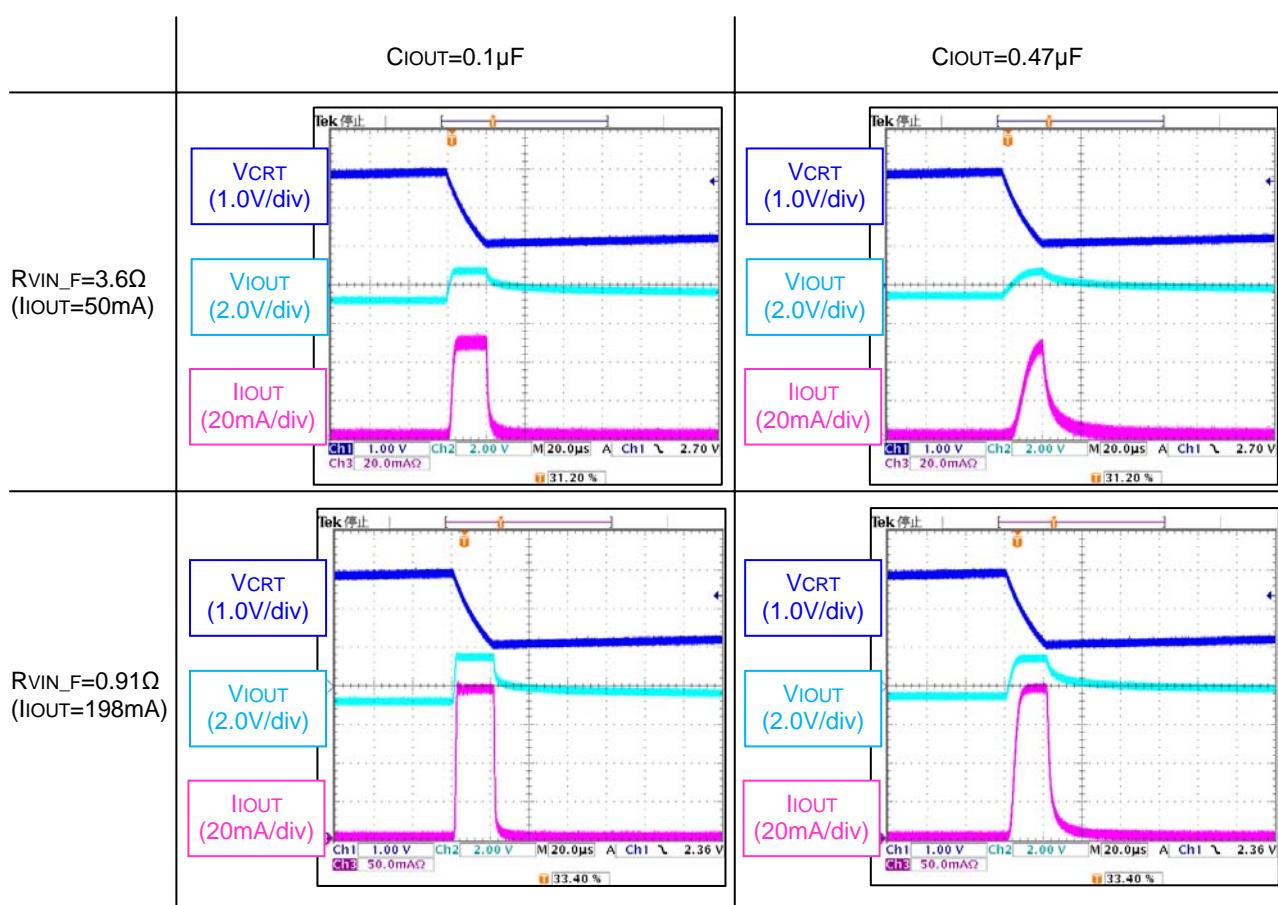


The time of VIN on to IOUT on

C_{OUT}=0.1μF : 11ms
 C_{OUT}=0.47μF : 51ms
 C_{OUT}=1.0μF : 130ms
 C_{OUT}=2.2μF : 290ms

Evaluation example(IOUT pulse width at PWM Dimming operation)

Condition : +B=13V
 Ta=25°C
 LED 3Strings
 RCRT=560Ω
 CCRT=0.033μF
 PWM Dimming Mode



7. PBUS Function

PBUS terminal is an input/output terminal for outputting trouble and inputting trouble detection.

In case where a trouble occurred due to open/short-circuit of external component, it is possible to notify the trouble outside by switching PBUS terminal output from High (Note1) to Low.

It is possible to turn OFF output current by externally controlling PBUS from High→Low.

(Note1) PBUS terminal is an open drain terminal. Even when used separately, please be pulled up($10k\Omega$) to power supply voltage.

In case where you use multiple number of this LSI to drive multiple LEDs, as shown in the drawing below, it is possible to turn off all rows of LEDs even if some LEDs are short/open-circuited by connecting PBUS terminal of each CH.

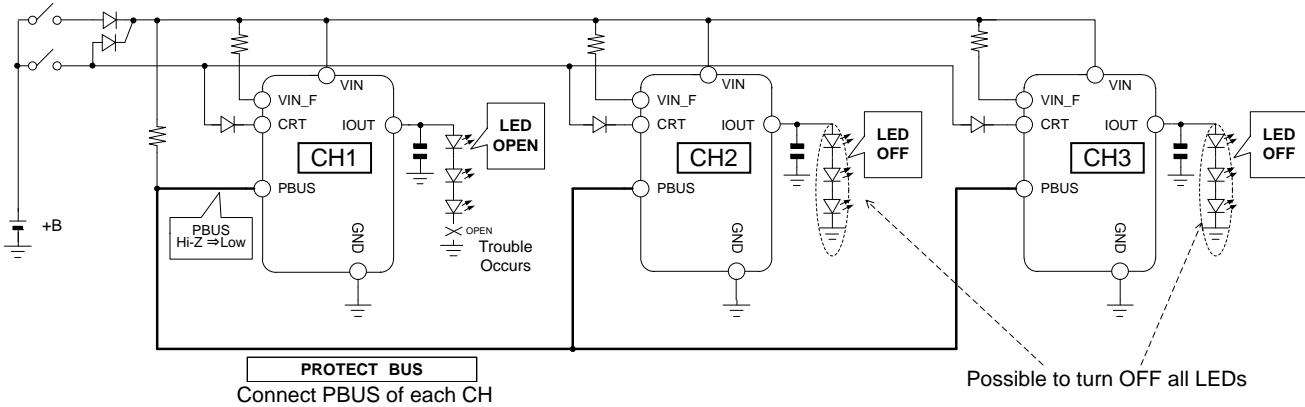


Figure 21. PBUS Function

▼ Example of Protective Operation by LED Open

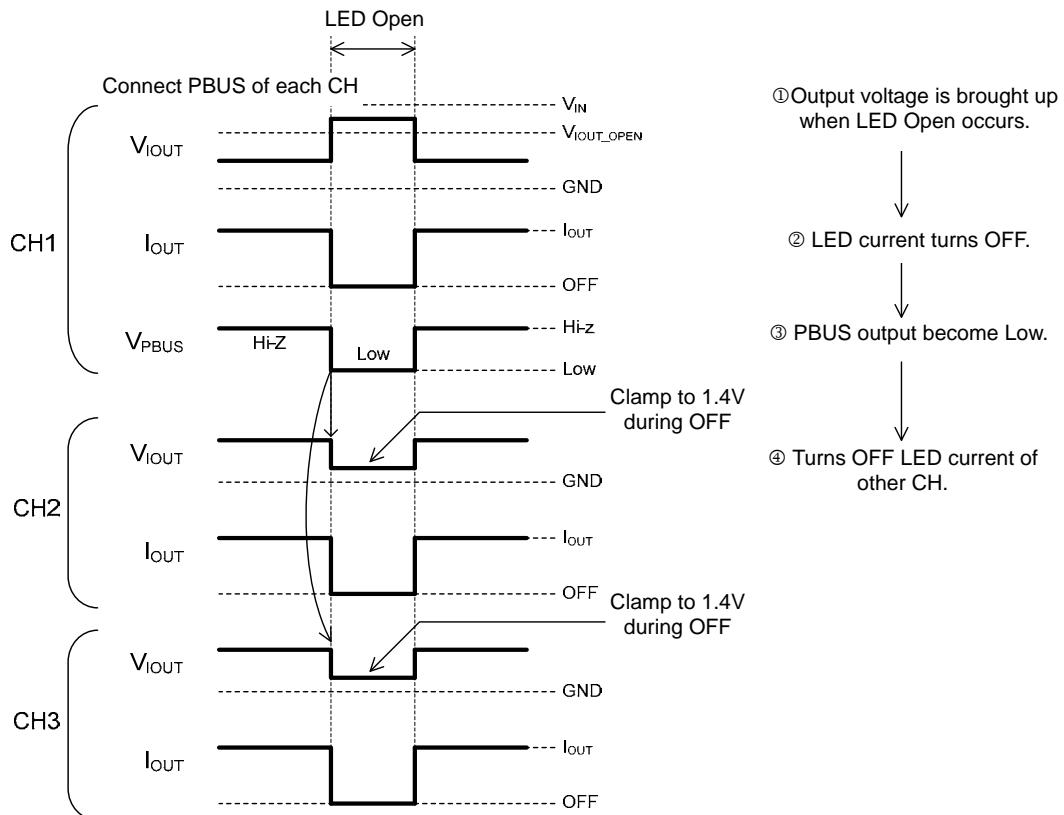


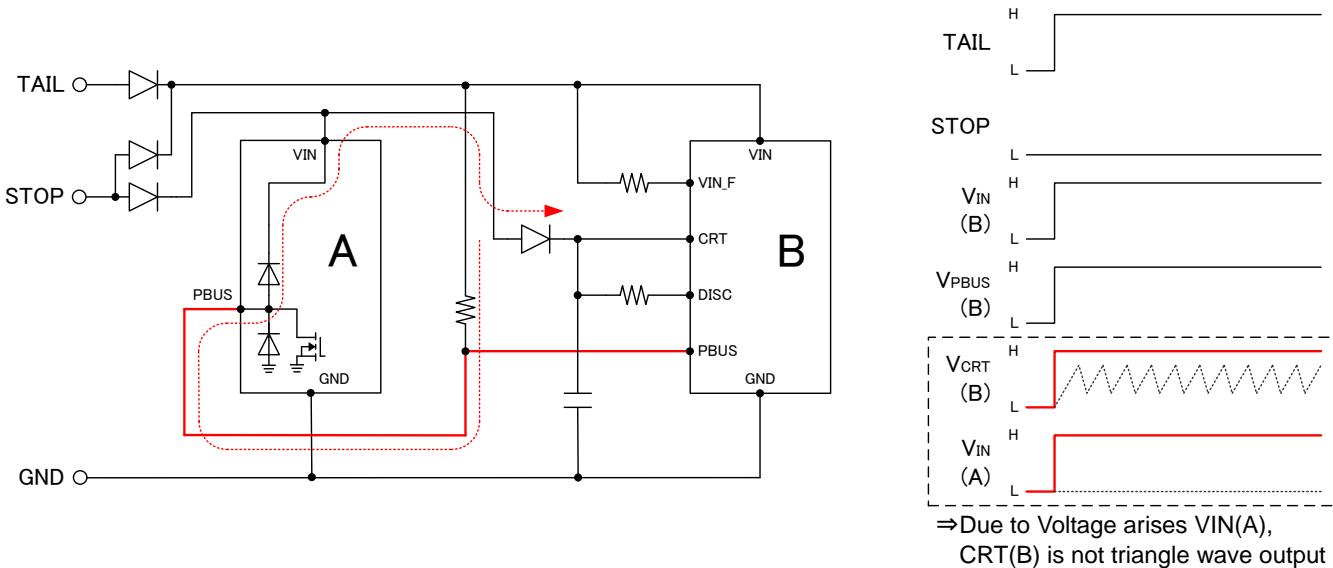
Figure 22. Example of Protective Operation

If LED OPEN occurs, PBUS of CH1 is switched from Hi-z to Low output. As PBUS becomes Low, LED drivers of other CH detect the trouble and turns OFF their own LEDs. VOUT clamps to 1.4V (Typ) during the OFF period, in order to prohibit ground fault detection.

8. Caution of driving IC used multi-power supply

Each Input terminal is built- in ESD protection diodes. (Refer to I/O equivalence circuits)
**If VIN terminal is not supplied voltage and Input terminal (without VIN) is supplied voltage,
 IC may occur malfunction(abnormal operation mode, abnormal LED lighting)
 due to arise VIN terminal voltage .**

The Application Example of accidental operation is below.



(Operational Explanation)

Only input Tail : Arise V_{IN} terminal voltage of IC A from ESD protection Diode between V_{IN} terminal and PBUS terminal of IC A.
 Due to connect V_{IN} terminal of IC A and CRT terminal of IC B across Diode, DC voltage inputs CRT terminal of IC B, so it is possible to operate ICB DC mode.

Timing Chart

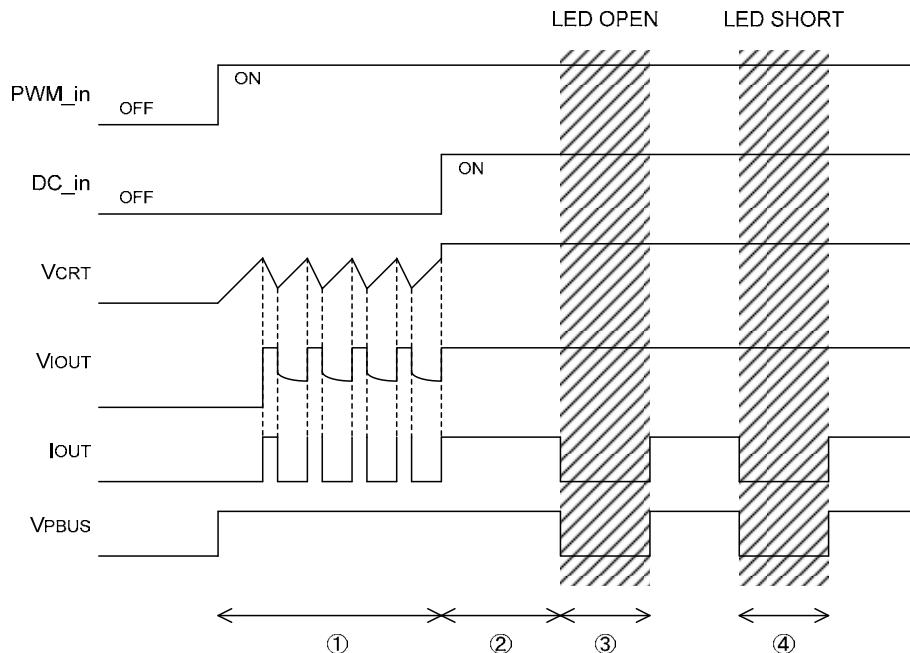
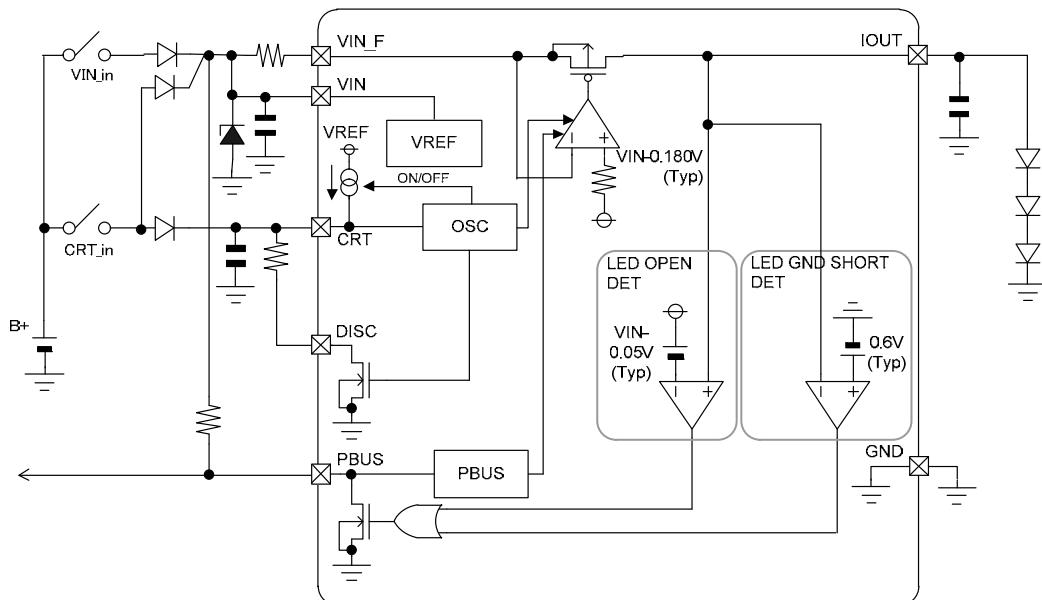


Figure 24. Timing Chart

- ① If PWM_in is switched ON, VCRT will start oscillation, and according to its waveform LED current IOUT is output. (PWM light control mode)
- ② If DC_in is switched ON, VCRT will be fixed at High (VIN-Vf). LED current IOUT will be continuously output. (Linear control mode)
- ③ If LED becomes OPEN, LED current IOUT will stop. At the same time, VPBUS falls to Low.
- ④ If LED is short-circuited to GND, LED current IOUT will stop. At the same time, VPBUS falls to Low.

Guaranteed Range of Current Accuracy and LED Open Detection Range

Guaranteed range of current accuracy and LED open detection range can be obtained from the following equation:

PBUS output becomes Low if IOUT terminal output (V_{IOUT}) is higher than the LED open detection range at the time of reduced V_{IN} terminal voltage.

Therefore, pay attention to respective setting range during power ON/OFF, and consider operating voltage range of the set.

Guaranteed Range of Current Accuracy

$$V_{IN} \geq V_{f_led} \times N + V_{IN_F_REF} + V_{DR_IOUT} [V]$$

Where:

V_{IN} is the V_{IN} Terminal Voltage

V_{f_diode} is the Reverse Connection Preventing Diode V_f

V_{f_led} is the LED V_f

N is the: Number of LED Levels

$V_{IN_F_REF}$ is the V_{IN_F} Terminal Voltage ($V_{IN} - V_{IN_F}$)

V_{DR_IOUT} is the $IOUT$ Terminal Drop Voltage

LED Open Detection Voltage

$$V_{IOUT} = V_{IN} - 50mV(\text{Typ})$$

LED Open Detection Release Voltage

$$V_{IOUT} = V_{IN} - 150mV(\text{Typ})$$

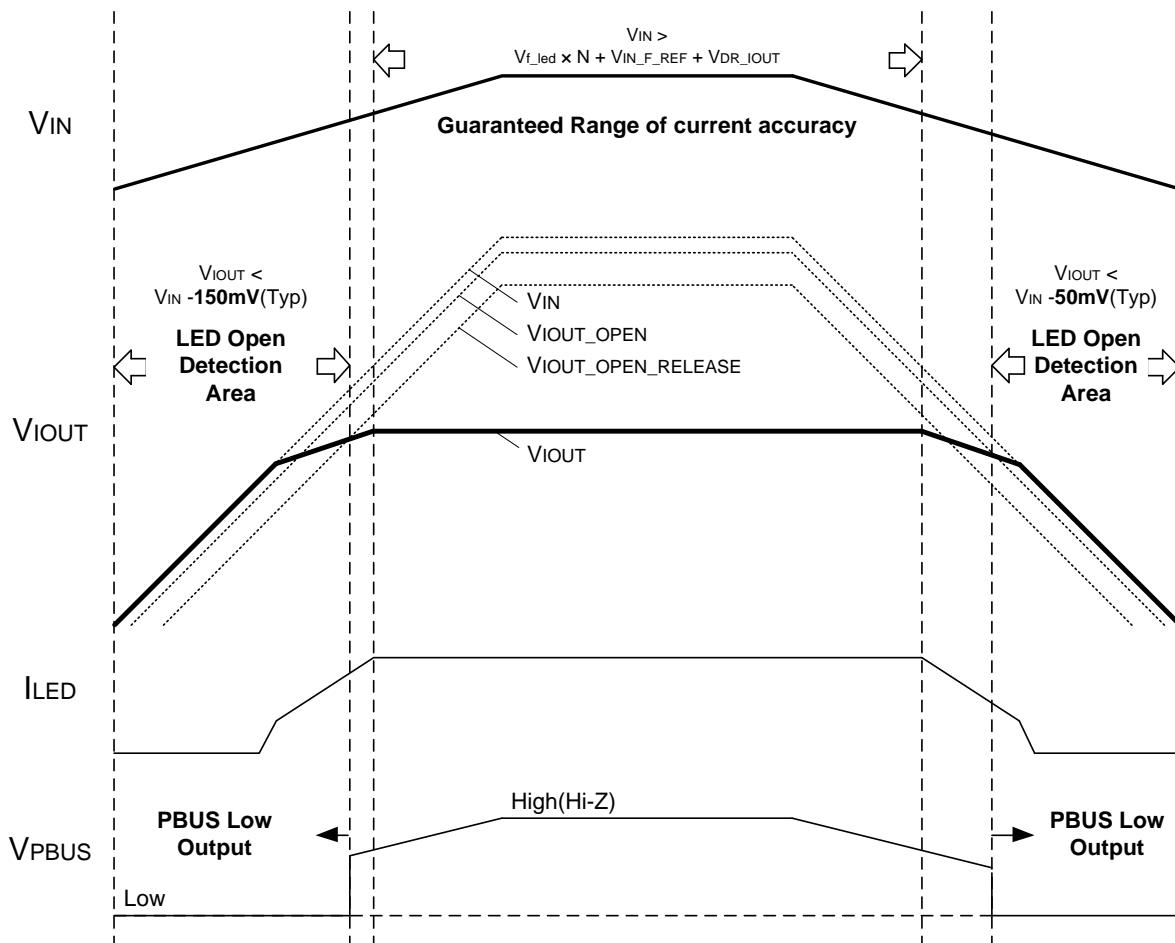


Figure 25. Guaranteed Range of Current Accuracy and LED Open Detection Range

How to Connect LED

In case of connected LED to IOUT terminal as shown in the following, note that protective detection becomes possible/impossible depending on connection patterns.

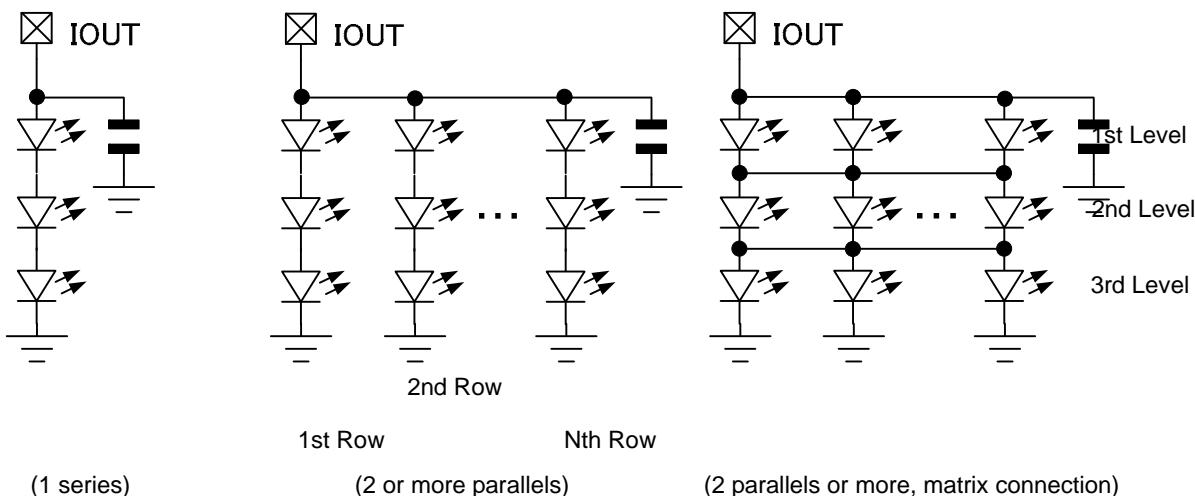


Figure 26. LED Connection Patterns

Connection Pattern	LED Short-circuit Detection (GND short of IOUT terminal)	LED OPEN detection
1 Series	Detectable	Detectable-
2 parallels or more	Detectable	Non-detectable ^(Note 1)
2 parallels or more (Matrix Connection)	Detectable	Non-detectable ^(Note 2)

(Note1) : Detectable only when one or more LEDs become open in all rows.

(Note2) : Detectable only when all LEDs on the same level become open.

Recommended Application Circuit

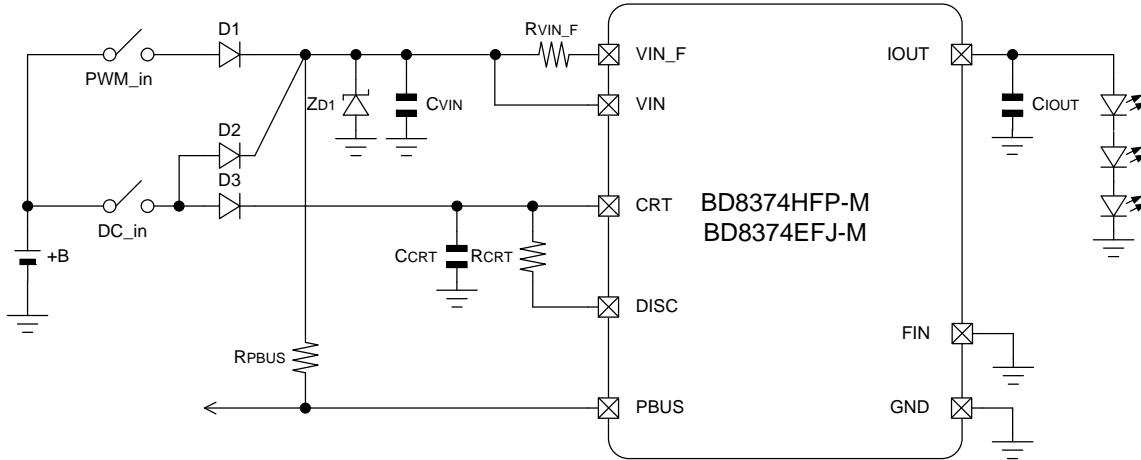


Figure 27. Recommended Application Circuit

▼Corresponding EMC Test Items

- ISO11425-2
- ISO11452-4
- ISO7637-2
(pulse1, pulse 2a,2b, pulse 3a,3b)

No.	Component Name	Component Value	Product Name	Company
1	D1	-	RF201L2S	ROHM
2	D2	-	RF201L2S	ROHM
3	D3	-	RF201L2S	ROHM
4	Z _{D1}	-	TNR12H-220K	NIPPON CHEMICON
5	C _{VIN}	4.7μF	GCM32ER71H475KA40	murata
6	R _{VIN_F}	0.91Ω	MCR10 Series	ROHM
7	R _{PBUS}	10kΩ	MCR03 Series	ROHM
8	C _{CRT}	0.033μF	GCM188R11H333KA40	murata
9	R _{CRT}	3.9kΩ	MCR03 Series	ROHM
10	C _{iOUT}	0.1μF	GCM188R11H104KA42	murata

Table 1. BOM List

PWM_in	DC_in	Mode
Low	Low	OFF
High	Low	PWM Dimming Mode ^(Note1,Note2) (14mA 6.7% ON duty@518Hz)
Low	High	Linear Control Mode ^(Note2) (200mA 100% ON duty)
High	High	Linear Control Mode ^(Note2) (200mA 100% ON duty)

(Note1) See Functional Description "3. PWM Dimming Operation."

(Note2) See Functional Description "2. Table of Operations."

Table 2. Table of Operations

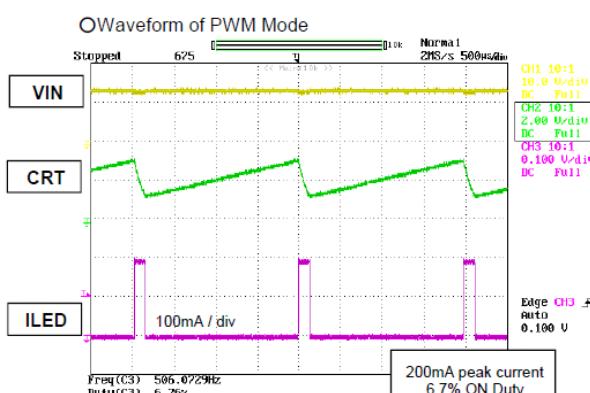


Figure 28. Example of Waveform Measurement

Thermal Loss

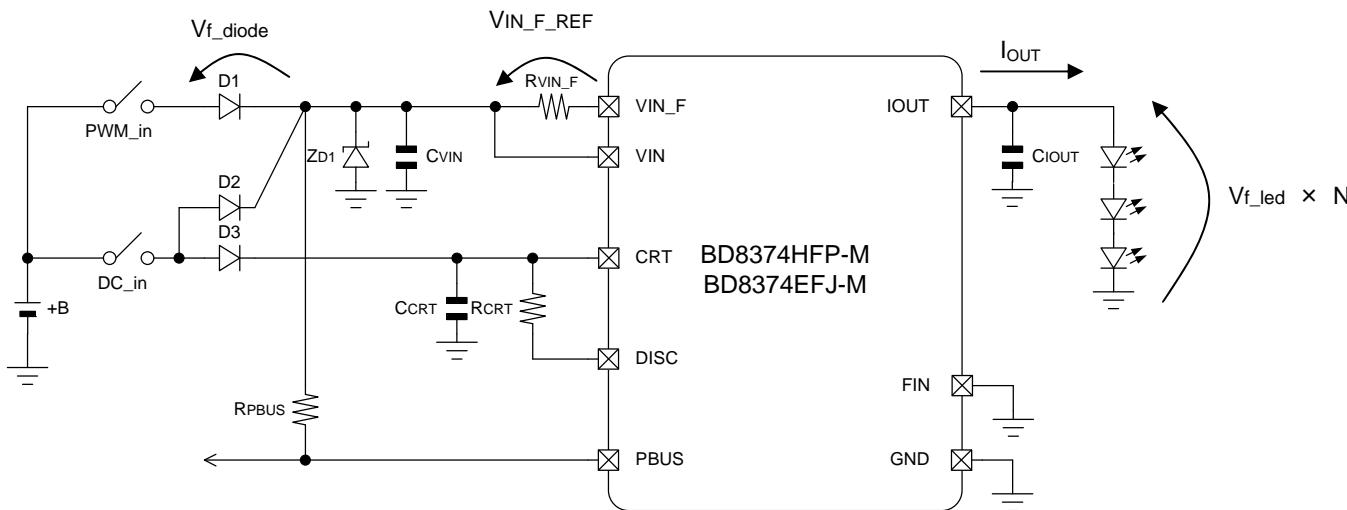


Figure 29. Application Circuit Diagram for Thermal Description

Thermal design should meet the following equation:

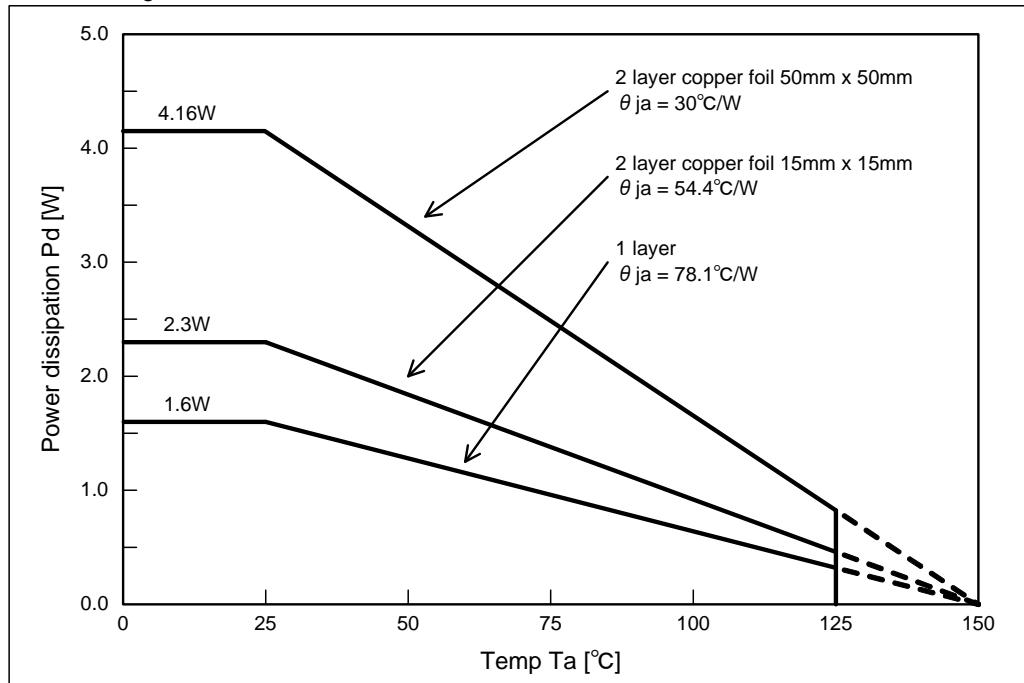
$$P_d > P_c = (+B - V_{f_diode} - V_{IN_F_REF} - V_{f_led \times N}) \times I_{OUT} + I_{VIN} \times V_{IN}$$

$$P_d = (1/\theta_{ja}) \times (T_{jmax} - T_a) \text{ or } (1/\theta_{jc}) \times (T_{jmax} - T_c)$$

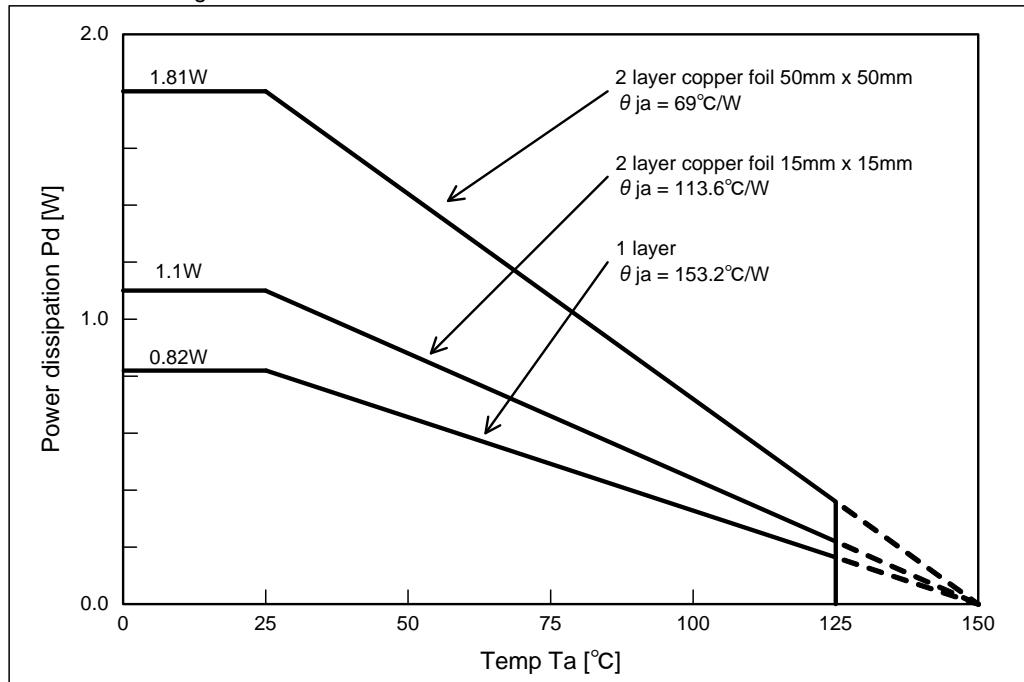
where:

P_d is the Power Dissipation
 P_c is the Power Consumption
 $+B$ is the Battery Voltage
 V_{f_diode} is the Reverse Connection Preventing Diode V_f
 $V_{IN_F_REF}$ is the V_{IN_F} Terminal Voltage ($V_{IN} - V_{IN_F}$)
 V_{f_led} is the LED V_f
 N is the Number of LED Levels
 I_{OUT} is the Output Current
 I_{VIN} is the Circuit Current
 V_{IN} is the Power Supply Voltage
 θ_{ja} is the Thermal Resistance between T_j and T_a
 θ_{jc} is the Thermal Resistance between T_j and T_c
 T_{jmax} is the Max Joint Temperature (150°C)
 T_a is the Ambient Temperature
 T_c is the Case Surface Temperature

HRP7 Package



HTSOP-J8 Package



(Caution1) When mounted with 70.0mm X 70.0mm X 1.6mm glass epoxy substrate.

(Caution2) Above copper foil area indicates backside copper foil area.

(Caution3) Value changes according to number of substrate layers and copper foil area. Note that this value is a measured value, not a guaranteed value.

Figure 30. Thermal Dissipation Curve

Thermal Design for Few Number of LED Lamps

If there are few LED lamps, insert resistance between IOUT terminal and LED to reduce heat generation from IC and dissipate heat.

(This does not apply where amperage is low.)

In that case, note that guaranteed range of current accuracy will be as shown in the following equation:

$$+B \geq V_{f_diode} + V_{f_led} \times N + V_{IN_F_REF} + V_{DR_IOUT} + I_{OUT} \times R_1$$

V_{f_diode} is the Reverse Connection Preventing Diode V_f

V_{f_led} is the LED V_f

N is the Number of LED Levels

$V_{IN_F_REF}$ is the V_{IN_F} Terminal Voltage ($V_{IN} - V_{IN_F}$)

V_{DR_IOUT} is the I_{OUT} Terminal Drop Voltage

I_{OUT} is the Output Current

R_1 is the Thermal Dissipation Resistance

Thermal design should meet the following equation when inserting thermal dissipation resistance:

$$P_d = (1/\theta_{ja}) \times (T_{jmax} - T_a) \text{ or } (1/\theta_{jc}) \times (T_{jmax} - T_c)$$

P_d is the Power Dissipation

P_c is the Power Consumption

$+B$ is the Battery Voltage

V_{f_diode} is the Reverse Connection Preventing Diode V_f

$V_{IN_F_REF}$ is the V_{IN_F} Terminal Voltage ($V_{IN} - V_{IN_F}$)

V_{f_led} is the LED V_f

N is the Number of LED Levels

I_{OUT} is the Output Current

R_1 is the Thermal Dissipation Resistance

I_{VIN} is the Circuit Current

V_{IN} is the Power Supply Voltage

θ_{ja} is the Thermal Resistance between T_j and T_a

θ_{jc} is the Thermal Resistance between T_j and T_c

T_{jmax} is the Max Joint Temperature (150°C)

T_a is the Ambient Temperature

T_c is the Case Surface Temperature

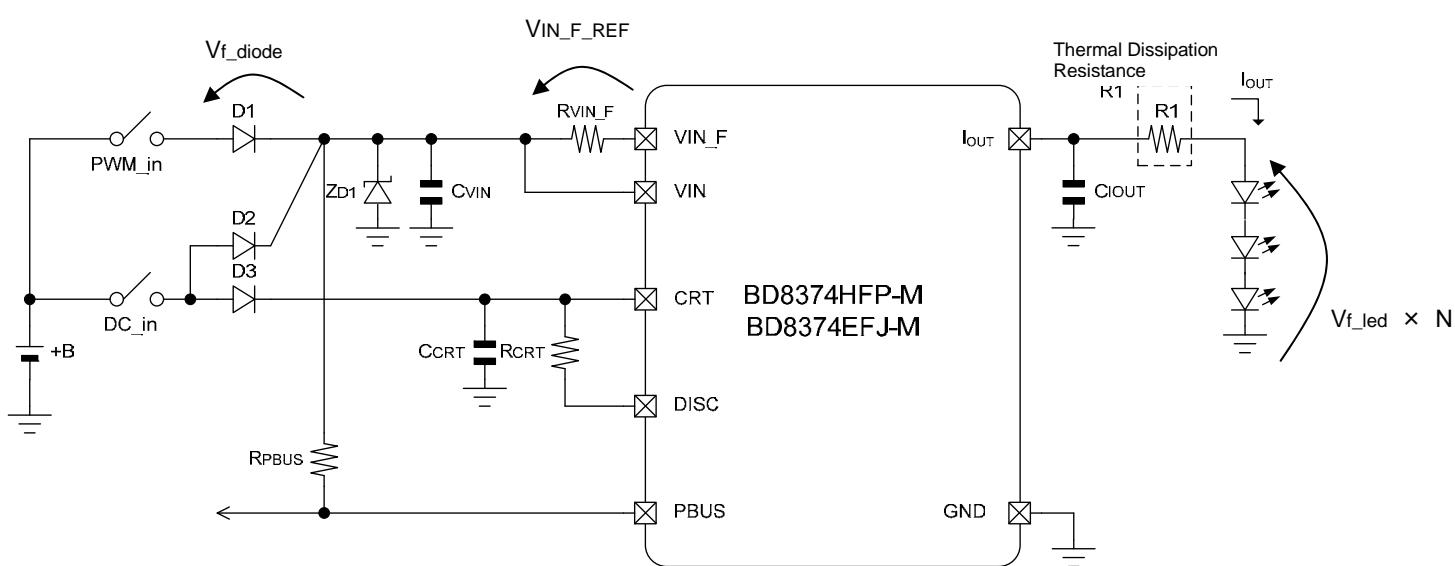
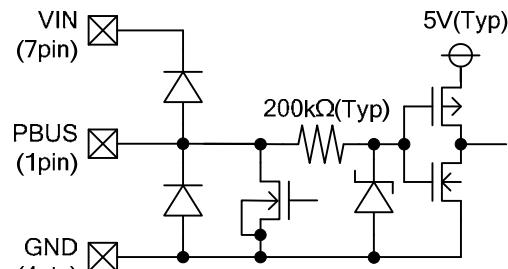
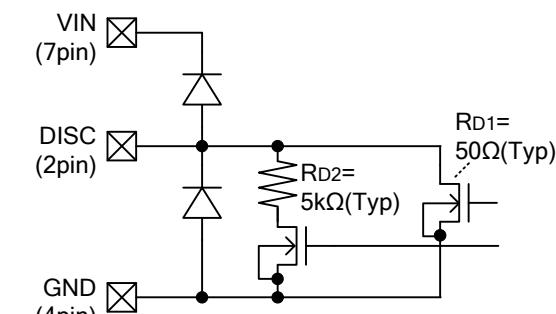
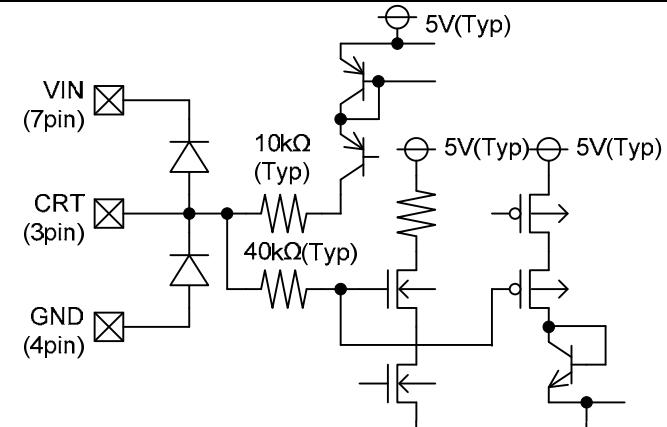
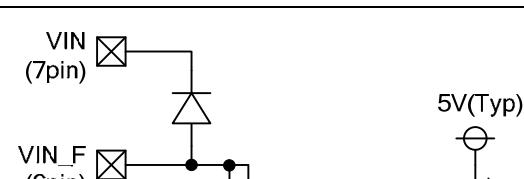
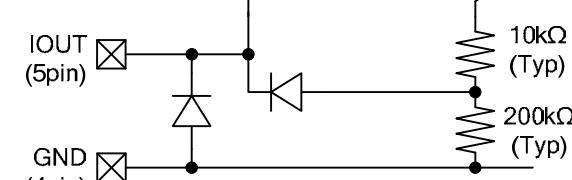


Figure 31. Example of How to Connect Thermal Dissipation Resistance

I/O equivalence circuits (HRP7 Package)

Number	Terminal Name	Equivalence Circuit
1	PBUS	
2	DISC	
3	CRT	
4	GND	-
5	IOUT	
6	VIN_F	
7	VIN	-

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Rush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

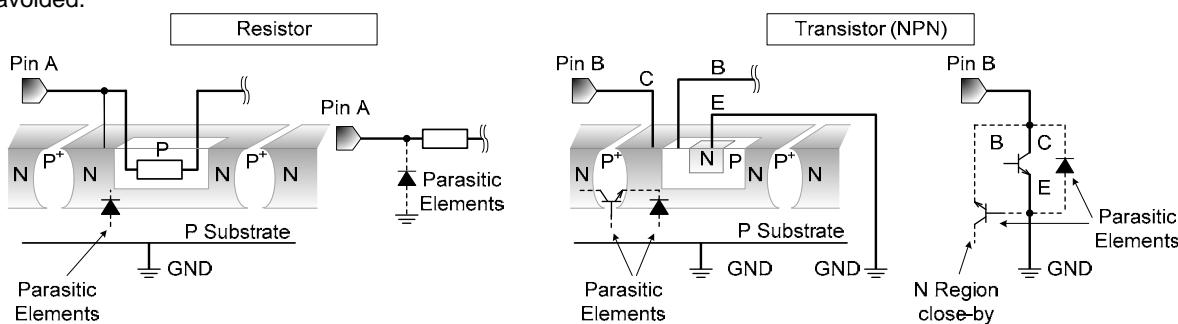


Figure 32. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

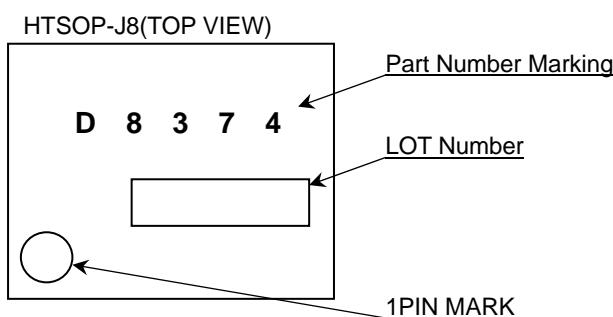
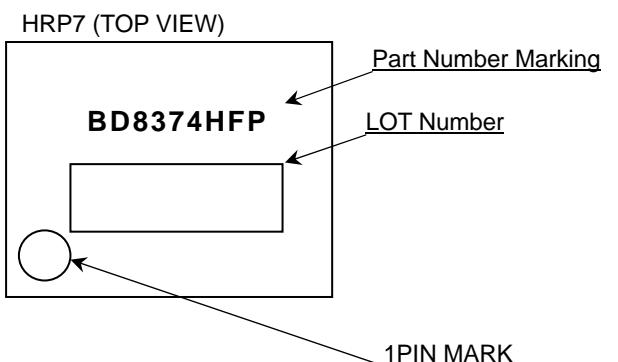
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF all output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

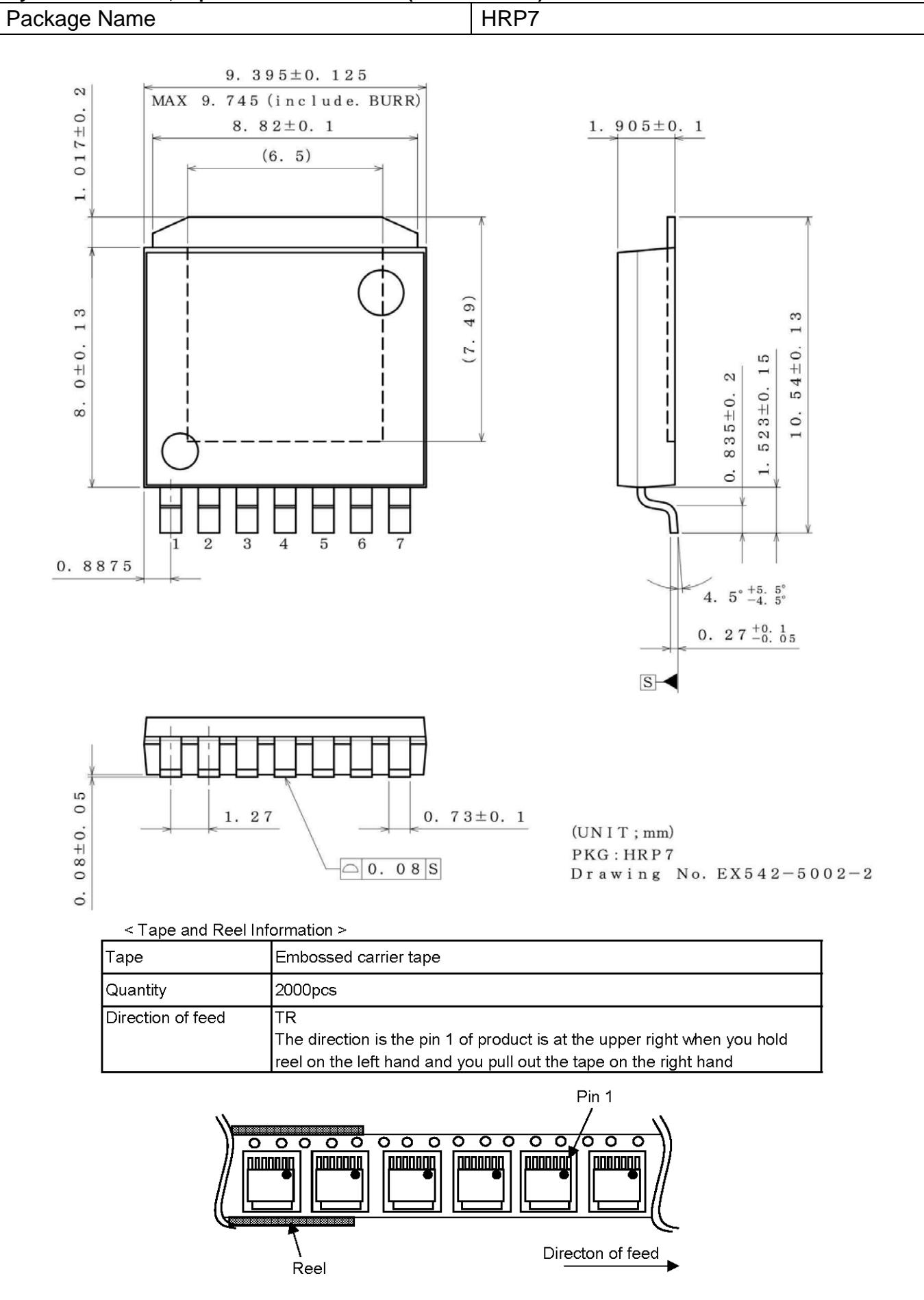
Ordering Information

B D 8 3 7 4 H F P	-	MTR
	Package HFP:HRP7	Packaging and forming specification M: High Reliability Design TR: Embossed tape and reel (HRP7)
B D 8 3 7 4 E F J	-	ME2
	Package EFJ:HTSOP-J8	Packaging and forming specification M: High Reliability Design E2: Embossed tape and reel (HTSOP-J8)

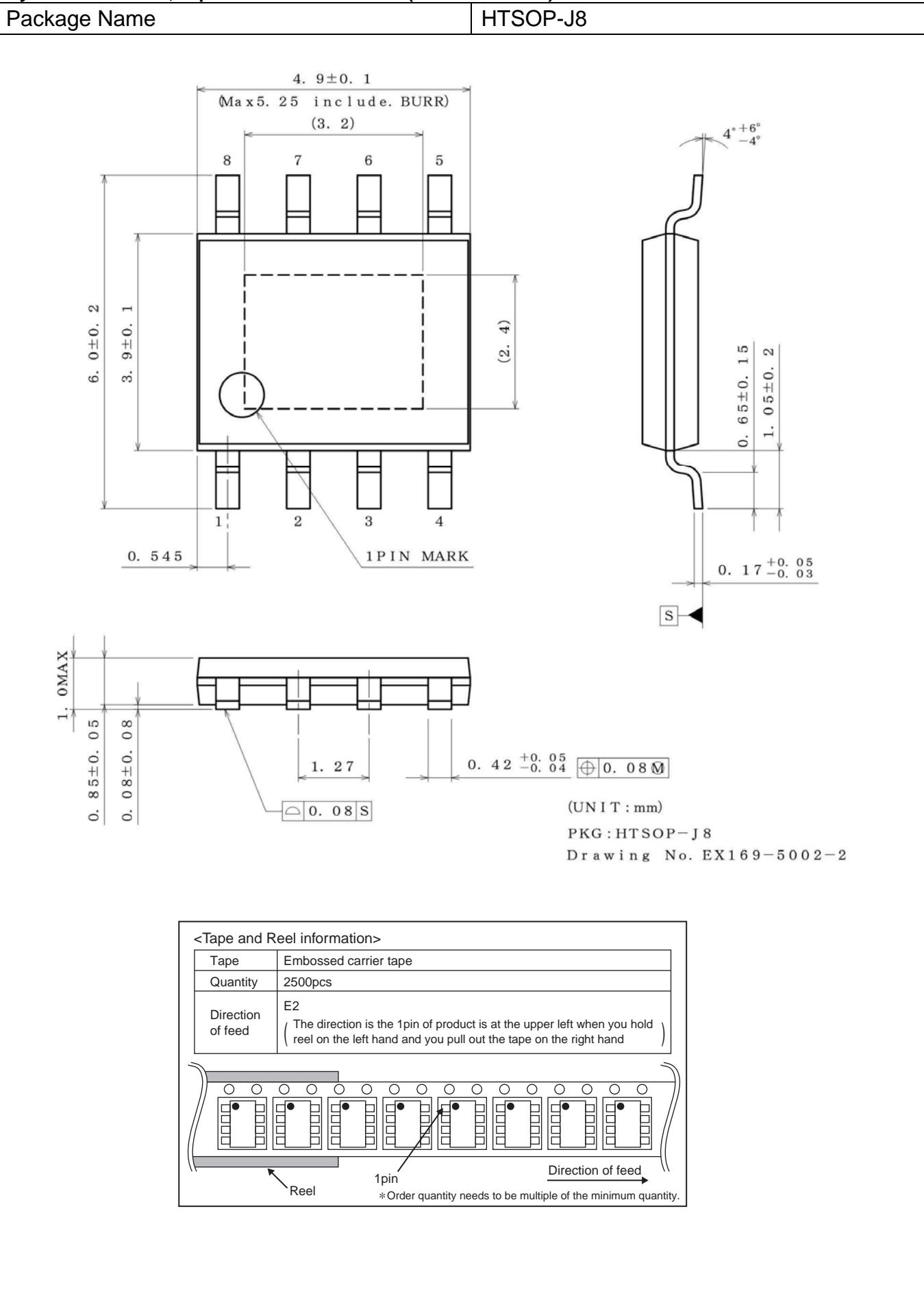
Marking Diagrams



Physical Dimension, Tape and Reel Information(BD8374HFP-M)



Physical Dimension, Tape and Reel Information(BD8374VEFV-M)



Revision History

Date	Revision	Changes
6.Aug.2013	001	New Release
14.May.2013	002	<p>General Added the capacitor to all Block Diagram</p> <p>Page.3 Absolute Maximum Ratings Revised</p> <p>Recommended Operating Conditions</p> <p>Minimum Pulse Width $100\mu\text{s} \rightarrow 20\mu\text{s}$</p> <p>Minimum capacitor connecting IOUT terminal C_{IOUT_MIN} added</p> <p>CRTIMER Frequency Range added</p> <p>Page.4 Electrical Characteristics</p> <p>IOUT Open detection Release Voltage added</p> <p>Page.5 Figure 7.(V_{IN} vs $V_{IN_F_REF}$) revised</p> <p>Page.7 Table of Operations revised</p> <p>Page.8 Figure 11. (PWM Dimming Operation) revised</p> <p>Page.11 the explanation of IOUT Current at GND Short added</p> <p>Page.12 the explanation about Active zone of LED Open Detective & LED Short Detective Function and IOUT Terminal Hi-Z zone added</p> <p>Page.15 Caution of driving IC used multi-power supply added</p> <p>Page.17 Guaranteed Range of Current Accuracy and LED Open Detection Range Tenor Revised</p> <p>Page.18 How to Connect LED LED Tenor Revised</p> <p>Page.23 I/O equivalence circuits Number1,2 Revised</p>

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	
CLASS IV		CLASS III	CLASS III

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