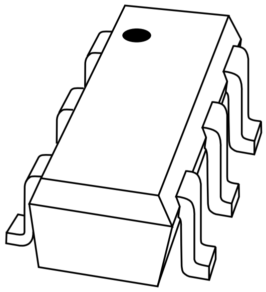
DATA SHEET



BF1204
Dual N-channel dual gate MOS-FET

Product specification
Supersedes data of 2001 Apr 25

2010 Sep 16

Dual N-channel dual gate MOS-FET | BF1204

FEATURES

- Two low noise gain controlled amplifiers in a single package
- Superior cross-modulation performance during AGC
- High forward transfer admittance
- High forward transfer admittance to input capacitance ratio.

APPLICATIONS

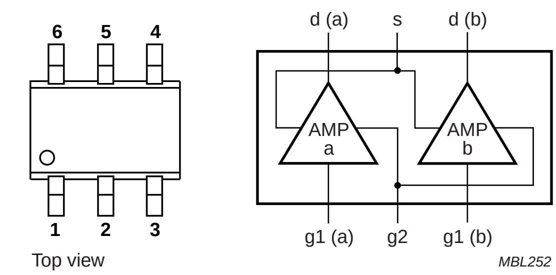
- Gain controlled low noise amplifiers for VHF and UHF applications with 3 to 9 V supply voltage, such as digital and analog television tuners and professional communications equipment.

DESCRIPTION

The BF1204 is a combination of two equal dual gate MOS-FET amplifiers with shared source and gate 2 leads. The source and substrate are interconnected. Internal bias circuits enable DC stabilization and a very good cross-modulation performance during AGC. Integrated diodes between the gates and source protect against excessive input voltage surges. The transistor has a SOT363 micro-miniature plastic package.

PINNING - SOT363

PIN	DESCRIPTION
1	gate 1 (a)
2	gate 2
3	gate 1 (b)
4	drain (b)
5	source
6	drain (a)



Marking code: L3*

* = - : made in Hong Kong
* = p : made in Hong Kong
* = t : made in Malaysia

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per MOS-FET; unless otherwise specified						
V_{DS}	drain-source voltage		–	–	10	V
I_D	drain current (DC)		–	–	30	mA
P_{tot}	total power dissipation	$T_s \leq 102$ °C; note 1	–	–	200	mW
$\|y_{fs}\|$	forward transfer admittance	I_D = 12 mA; f = 1 MHz	25	30	40	mS
C_{ig1-s}	input capacitance at gate 1	I_D = 12 mA; f = 1 MHz	–	1.7	2.2	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	15	–	fF
NF	noise figure	f = 800 MHz	–	1.1	1.8	dB
X_{mod}	cross-modulation	input level for k = 1% at 40 dB AGC	100	105	–	dBμV
T_j	operating junction temperature		–	–	150	°C

Note

1. T_s is the temperature at the soldering point of the source lead.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per MOS-FET; unless otherwise specified					
V_{DS}	drain-source voltage		–	10	V
I_D	drain current (DC)		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	$T_s \leq 102$ °C	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	240	K/W

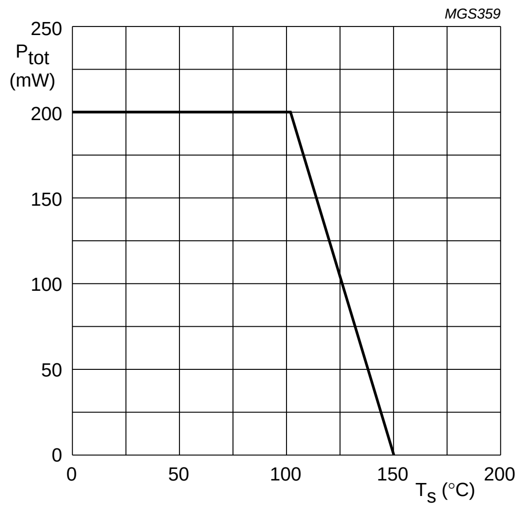


Fig.2 Power derating curve.

STATIC CHARACTERISTICS

T_j = 25 °C; per MOS-FET; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$; $I_D = 10\ \mu A$	10	–	V
$V_{(BR)G1-SS}$	gate-source breakdown voltage	$V_{GS} = V_{DS} = 0$; $I_{G1-S} = 10$ mA	6	10	V
$V_{(BR)G2-SS}$	gate-source breakdown voltage	$V_{GS} = V_{DS} = 0$; $I_{G2-S} = 10$ mA	6	10	V
$V_{(F)S-G1}$	forward source-gate voltage	$V_{G2-S} = V_{DS} = 0$; $I_{S-G1} = 10$ mA	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate voltage	$V_{G1-S} = V_{DS} = 0$; $I_{S-G2} = 10$ mA	0.5	1.5	V
$V_{G1-S(th)}$	gate-source threshold voltage	$V_{DS} = 5$ V; $V_{G2-S} = 4$ V; $I_D = 100\ \mu A$	0.3	1	V
$V_{G2-S(th)}$	gate-source threshold voltage	$V_{DS} = 5$ V; $V_{G1-S} = 4$ V; $I_D = 100\ \mu A$	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2-S} = 4$ V; $V_{DS} = 5$ V; $R_G = 120\ k\Omega$; note 1	8	16	mA
I_{G1-S}	gate cut-off current	$V_{G1-S} = 5$ V; $V_{G2-S} = V_{DS} = 0$	–	50	nA
I_{G2-S}	gate cut-off current	$V_{G2-S} = 4$ V; $V_{G1-S} = V_{DS} = 0$	–	20	nA

Note

1. R_{G1} connects gate 1 to $V_{GG} = 5$ V.

DYNAMIC CHARACTERISTICS

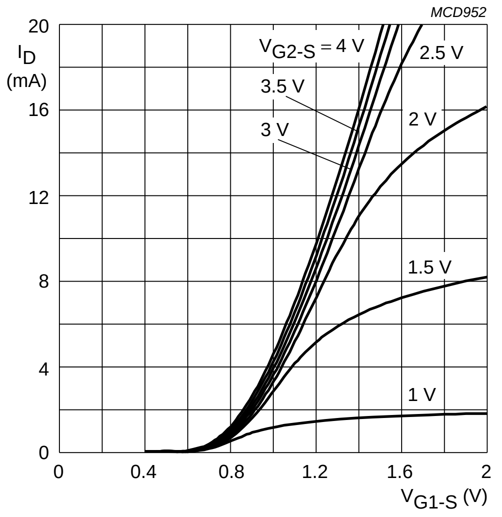
Common source; T_{amb} = 25 °C; $V_{G2-S} = 4$ V; $V_{DS} = 5$ V; $I_D = 12$ mA; per MOS-FET (1); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|y_{fs}\|$	forward transfer admittance	T_j = 25 °C	25	30	40	mS
C_{ig1-ss}	input capacitance at gate 1	f = 1 MHz	–	1.7	2.2	pF
C_{ig2-ss}	input capacitance at gate 2	f = 1 MHz	–	3.3	–	pF
C_{oss}	output capacitance	f = 1 MHz	–	0.85	–	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	15	–	fF
G_{tr}	power gain	f = 200 MHz; $G_S = 2$ mS; $B_S = B_{S(opt)}$; $G_L = 0.5$ mS; $B_L = B_{L(opt)}$; note 1	30	34	38	dB
		f = 400 MHz; $G_S = 2$ mS; $B_S = B_{S(opt)}$; $G_L = 1$ mS; $B_L = B_{L(opt)}$; note 1	26	30	34	dB
		f = 800 MHz; $G_S = 3.3$ mS; $B_S = B_{S(opt)}$; $G_L = 1$ mS; $B_L = B_{L(opt)}$; note 1	21	25	29	dB
NF	noise figure	f = 10.7 MHz; $G_S = 20$ mS; $B_S = 0$	–	9	11	dB
		f = 400 MHz; $Y_S = Y_{S(opt)}$	–	0.9	1.5	dB
		f = 800 MHz; $Y_S = Y_{S(opt)}$	–	1.1	1.8	dB
X_{mod}	cross-modulation	input level for k = 1% at 0 dB AGC; $f_w = 50$ MHz; $f_{unw} = 60$ MHz; note 2	90	–	–	dBμV
		input level for k = 1% at 10 dB AGC; $f_w = 50$ MHz; $f_{unw} = 60$ MHz; note 2	–	92	–	dBμV
		input level for k = 1% at 40 dB AGC; $f_w = 50$ MHz; $f_{unw} = 60$ MHz; note 2	100	105	–	dBμV

Notes

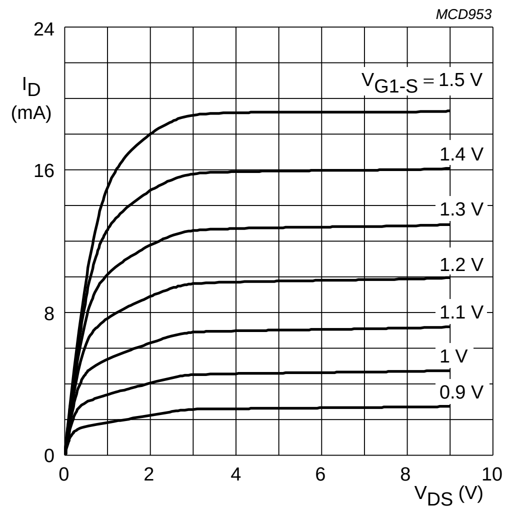
1. For the MOS-FET not in use: $V_{G1-S} = 0$; $V_{DS} = 0$.
2. Measured in Fig.19 test circuit.

ALL GRAPHS FOR ONE MOS-FET



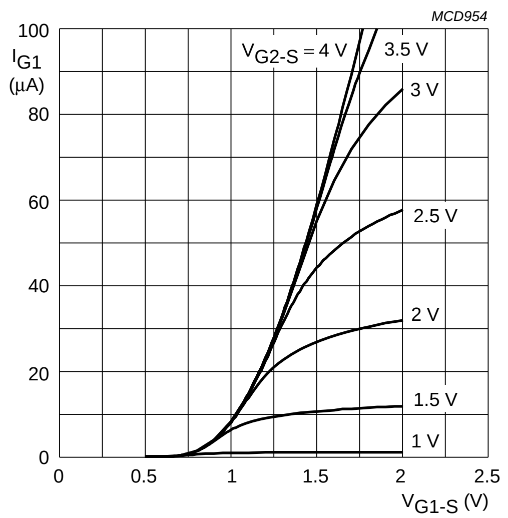
V_{DS} = 5 V.
T_j = 25 °C.

Fig.3 Transfer characteristics; typical values.



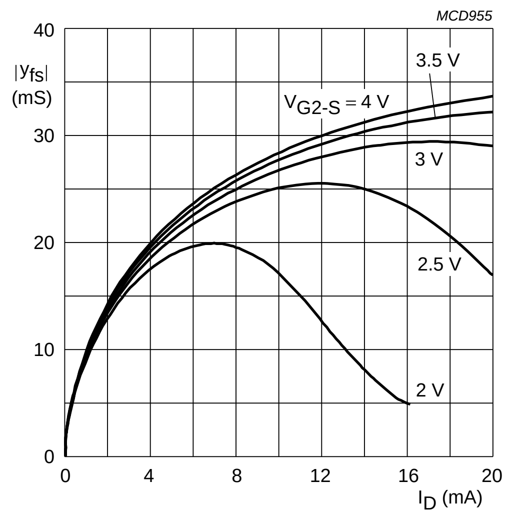
$V_{G2\text{-}S}$ = 4 V.
T_j = 25 °C.

Fig.4 Output characteristics; typical values.



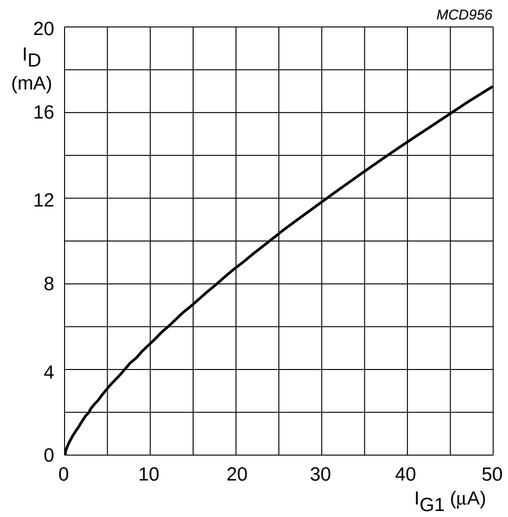
V_{DS} = 5 V.
T_j = 25 °C.

Fig.5 Gate 1 current as a function of gate 1 voltage; typical values.



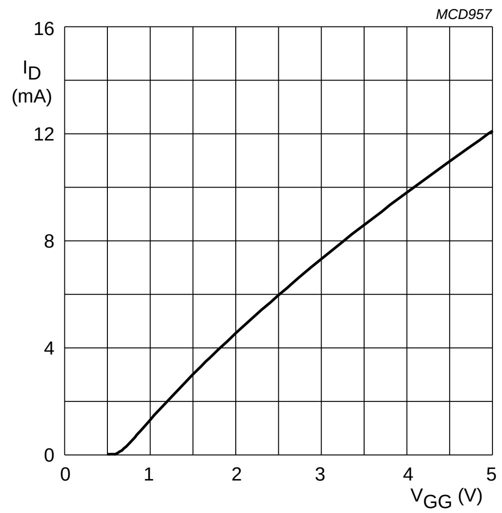
V_{DS} = 5 V.
T_j = 25 °C.

Fig.6 Forward transfer admittance as a function of drain current; typical values.



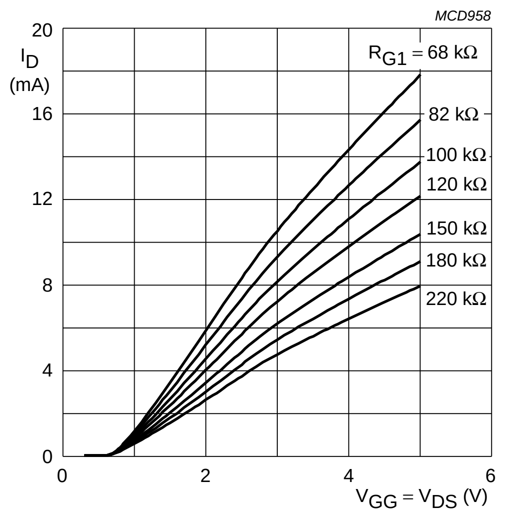
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V.
T_j = 25 °C.

Fig.7 Drain current as a function of gate 1 current; typical values.



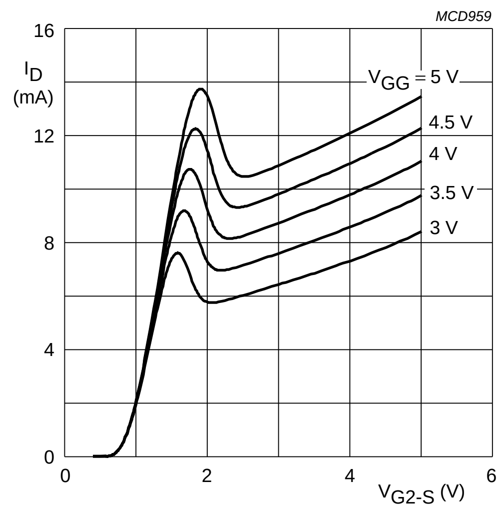
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}); see Fig.19.

Fig.8 Drain current as a function of gate 1 supply voltage (= V_{GG}); typical values.



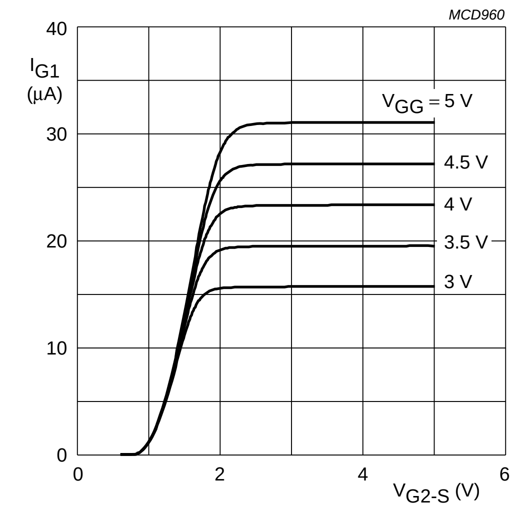
$V_{G2\text{-}S}$ = 4 V; T_j = 25 °C.
R_{G1} connected to V_{GG}; see Fig.19.

Fig.9 Drain current as a function of gate 1 (= V_{GG}) and drain supply voltage; typical values.



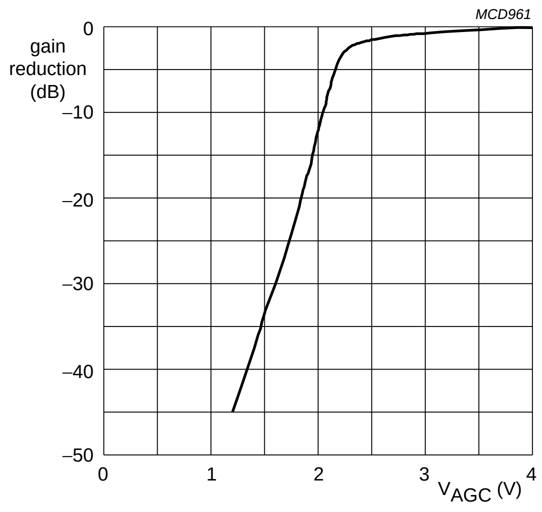
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}); see Fig.19.

Fig.10 Drain current as a function of gate 2 voltage; typical values.



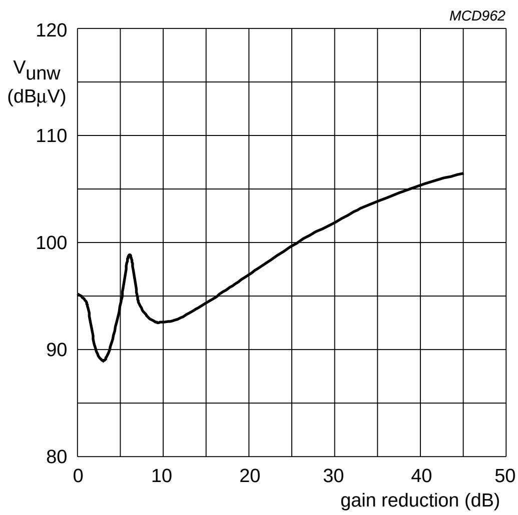
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}); see Fig.19.

Fig.11 Gate 1 current as a function of gate 2 voltage; typical values.



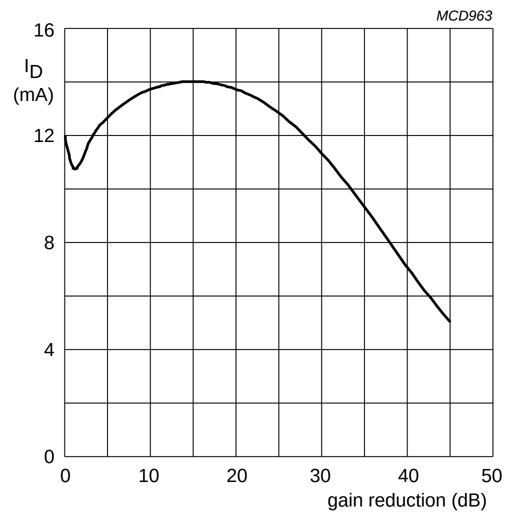
V_{DS} = 5 V; V_{GG} = 5 V; R_{G1} = 120 kΩ;
f = 50 MHz; T_{amb} = 25 °C.

Fig.12 Typical gain reduction as a function of AGC voltage; see Fig.19.



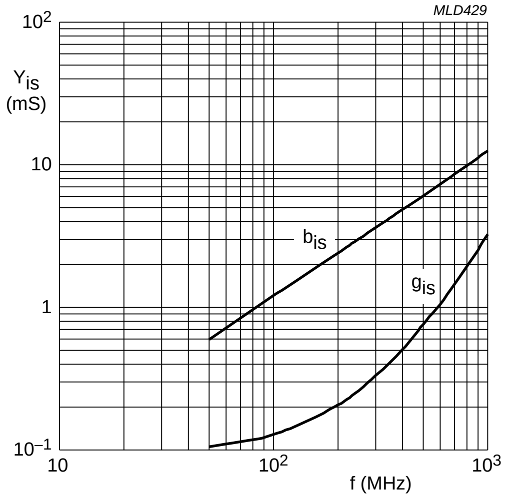
V_{DS} = 5 V; V_{GG} = 5 V; R_{G1} = 120 kΩ;
f= 50 MHz; f_{unw} = 60 MHz; T_{amb} = 25 °C.

Fig.13 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.19.



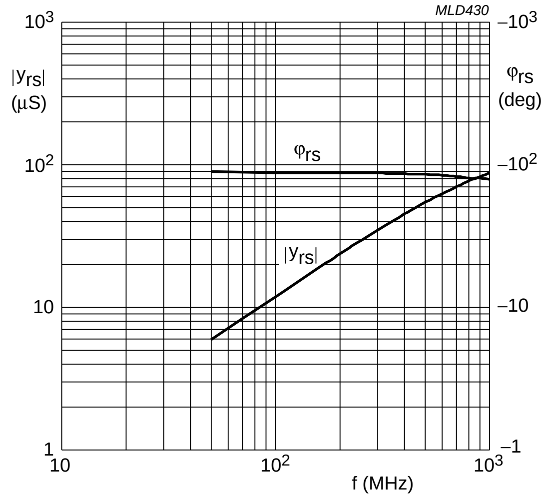
V_{DS} = 5 V; V_{GG} = 5 V; R_{G1} = 120 kΩ;
f = 50 MHz; T_{amb} = 25 °C.

Fig.14 Drain current as a function of gain reduction; typical values; see Fig.19.



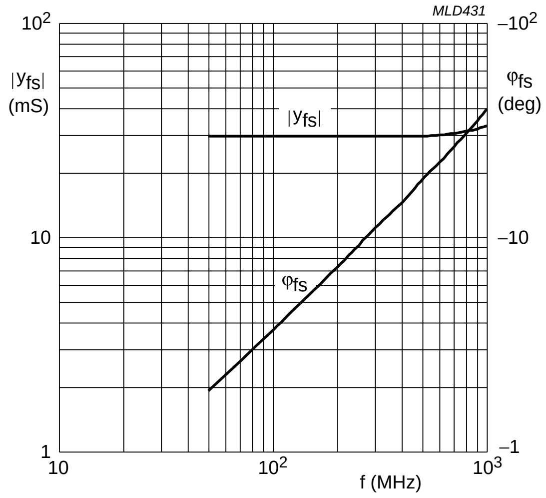
V_{DS} = 5 V; V_{G2} = 4 V.

Fig.15 Input admittance as a function of frequency; typical values.



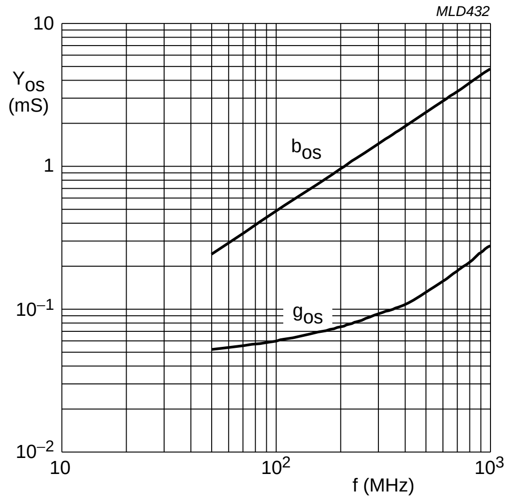
V_{DS} = 5 V; V_{G2} = 4 V.

Fig.16 Reverse transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.

Fig.17 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.

Fig.18 Output admittance as a function of frequency; typical values.

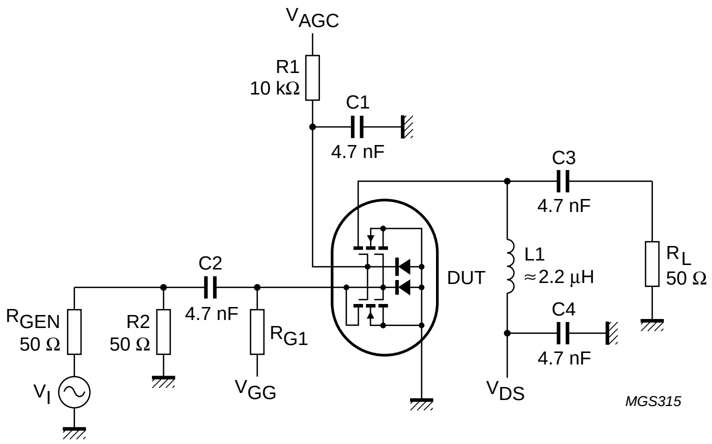


Fig.19 Cross-modulation test set-up (for one MOS-FET).

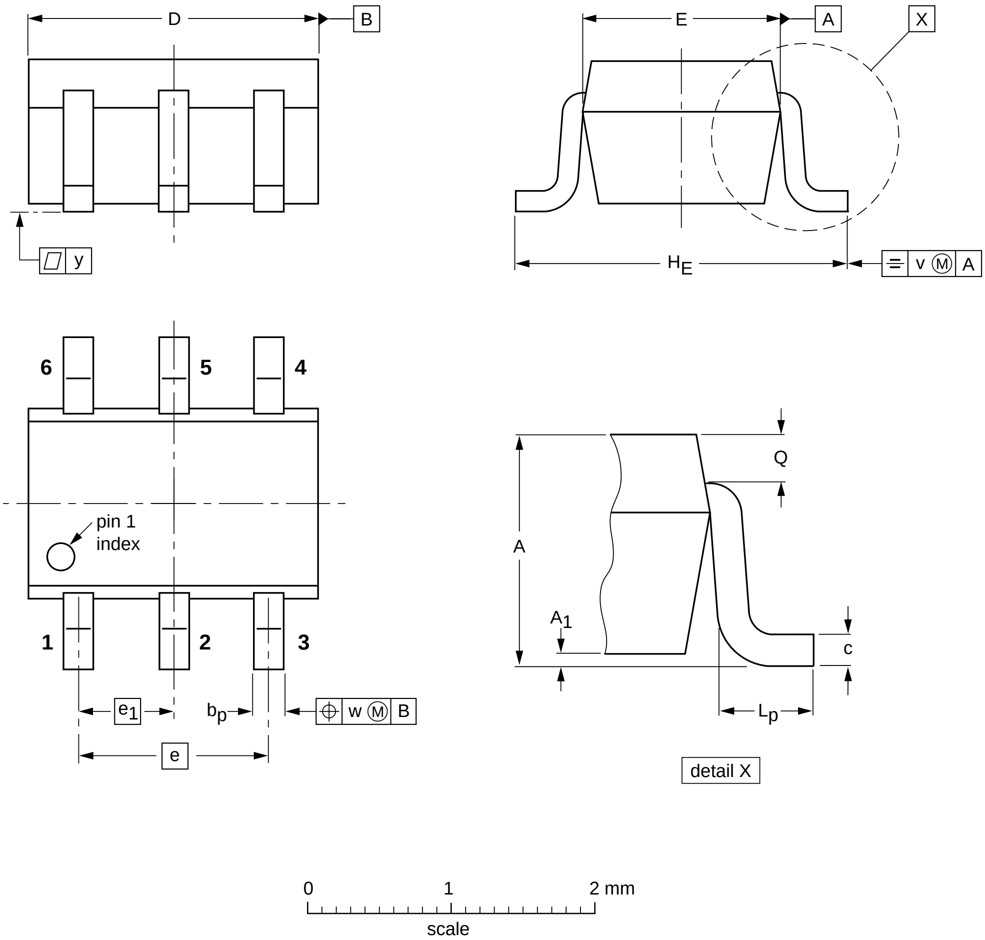
Scattering parameters

V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 12 mA; T_{amb} = 25 °C.

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.991	–3.29	2.95	175.78	0.00060	85.25	0.995	–1.44
100	0.987	–7.12	2.90	171.61	0.00119	84.74	0.994	–2.90
200	0.981	–14.21	2.86	163.45	0.00234	80.85	0.992	–5.70
300	0.969	–21.22	2.83	155.11	0.00339	75.77	0.989	–8.50
400	0.958	–28.14	2.79	147.37	0.00429	72.23	0.987	–11.25
500	0.939	–35.01	2.74	139.04	0.00508	68.24	0.983	–13.96
600	0.921	–41.75	2.68	131.35	0.00565	64.97	0.981	–16.67
700	0.898	–48.51	2.62	123.38	0.00611	61.90	0.976	–19.36
800	0.874	–54.96	2.55	115.74	0.00646	57.77	0.973	–22.04
900	0.847	–61.62	2.49	107.84	0.00662	55.04	0.969	–24.80
1000	0.817	–67.84	2.41	100.24	0.00670	52.16	0.966	–27.45

PACKAGE OUTLINE

Plastic surface-mounted package; 6 leads **SOT363**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT363			SC-88			~~04-11-08~~ 06-03-16

DATA SHEET STATUS

DOCUMENT STATUS(1)	PRODUCT STATUS(2)	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

DISCLAIMERS

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

NXP Semiconductors

provides High Performance Mixed Signal and Standard Product solutions that leverage its leading RF, Analog, Power Management, Interface, Security and Digital Processing expertise

Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for the marking codes and the package outline drawings which were updated to the latest version.

Contact information

For additional information please visit: **http://www.nxp.com**
For sales offices addresses send e-mail to: **salesaddresses@nxp.com**

Printed in The Netherlands R77/03/pp13 Date of release: 2010 Sep 16