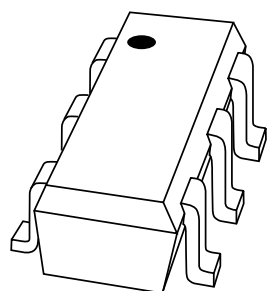


# DATA SHEET



## **BGA2031/1** MMIC variable gain amplifier

Product specification  
Supersedes data of 2000 Mar 02

2001 Feb 05



## MMIC variable gain amplifier

BGA2031/1

## FEATURES

- High gain
- Excellent adjacent channel power rejection
- Small SMD package
- Low dissipation.

## APPLICATIONS

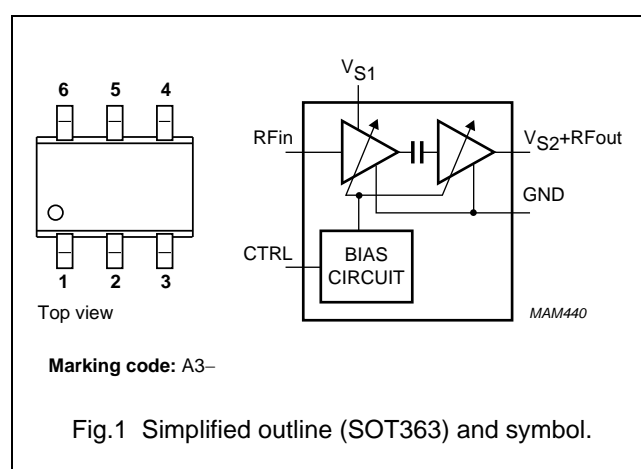
- General purpose variable gain amplifier for low voltage and medium power
- Driver for power amplifiers in systems that require good linearity, such as CDMA, both cellular band (850 MHz) and PCS (1.9 GHz). This is because of the high output power and good linearity.

## DESCRIPTION

Silicon Monolithic Microwave Integrated Circuit (MMIC)  
2 stage variable gain amplifier in double polysilicon technology in a 6-pin SOT363 SMD plastic package for low voltage medium power applications.

## PINNING

PIN	DESCRIPTION
1	RFin
2	CTRL
3	V <sub>S1</sub>
4	V <sub>S2</sub> + RFout
5	GND
6	GND



## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V <sub>S1</sub>	supply voltage		3	3.3	V
V <sub>S2</sub>	supply voltage		3	3.3	V
I <sub>S</sub>	supply current; pins 3 and 4	V <sub>CTRL</sub> = 0	0	10	μA
		V <sub>CTRL</sub> = 2.7 V; V <sub>S</sub> = 3 V	51	63	mA
		V <sub>CTRL</sub> = 2.4 V; V <sub>S</sub> = 3 V	30	37	mA
P <sub>L</sub>	load power	at 1 dB gain compression point; f = 1.9 GHz	13	—	dBm
ACPR	adjacent channel power rejection	f = 1.9 GHz; P <sub>L</sub> = 10 dBm	49	—	dBc
		f = 836 MHz; P <sub>L</sub> = 8 dBm	48	—	dBc
G <sub>p</sub>	power gain	f = 1.9 GHz; P <sub>L</sub> = 12 dBm	23	—	dB
		f = 836 MHz; P <sub>L</sub> = 8 dBm	24	—	dB
ΔG	gain control range	f = 836 MHz; P <sub>L</sub> = 8 dBm	62	—	dB

## CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling.

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_S$	DC supply voltage		–	3.3	V
$V_{CTRL}$	control voltage		–	$< V_S$	V
$I_{CTRL}$	control current		–	1.2	mA
$I_{S1}$	supply current; pin 3		–	27	mA
$I_{S2}$	supply current; pin 4		–	50	mA
$P_D$	drive power		–	+10	dBm
$P_{tot}$	total power dissipation	$T_s \leq 80\text{ }^{\circ}\text{C}$	–	200	mW
$T_{stg}$	storage temperature		–65	+150	$^{\circ}\text{C}$
$T_j$	operating junction temperature		–	150	$^{\circ}\text{C}$

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to solder point	350	K/W

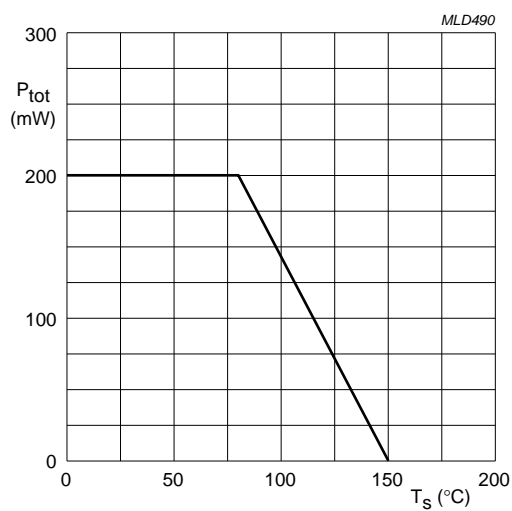


Fig.2 Power derating.

## MMIC variable gain amplifier

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## CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ ;  $Z_S = Z_L = 50\text{ }\Omega$ ;  $V_S = 3\text{ V}$ ; unless otherwise specified.

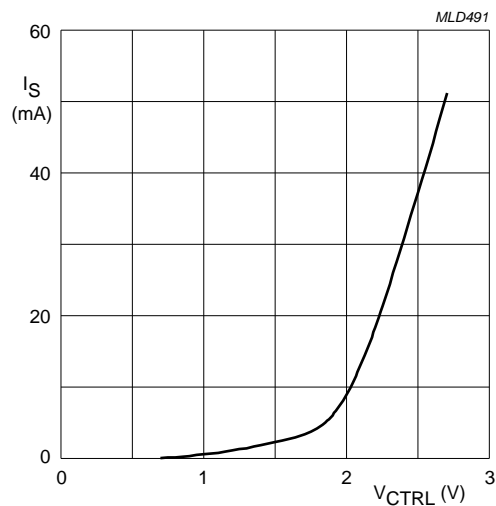
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f	frequency range		800	–	2500	MHz
$V_{S1}$	supply voltage		2.7	3	3.3	V
$V_{S2}$	supply voltage		2.7	3	3.3	V
$I_S$	supply current; pins 3 and 4	$V_{CTRL} = 0$ ; $P_D = 0\text{ mW}$	–	0	10	$\mu\text{A}$
		$V_{CTRL} = 2.7\text{ V}$ ; $V_S = 3\text{ V}$ ; $P_D = 0\text{ mW}$	37	51	63	mA
		$V_{CTRL} = 2.4\text{ V}$ ; $V_S = 3\text{ V}$ ; $P_D = 0\text{ mW}$	23	30	37	mA
$I_{CTRL}$	control current	$V_{CTRL} = 2.7\text{ V}$	0.7	0.92	1.1	mA
<b>f = 1900 MHz</b>						
f	frequency range		1850	–	1950	MHz
$G_p$	power gain	$V_{CTRL} = 2.7\text{ V}$ ; $P_L = 12\text{ dBm}$	–	23	–	dB
$\Delta G$	gain control range	$0 < V_{CTRL} < 2.7\text{ V}$	–	56	–	dB
$G_{CS}$	gain control slope	note 1	–	21	–	dB/V
ACPR	adjacent channel power rejection	$\pm 1.23\text{ MHz}$ offset; $BW_{ACP} = 30\text{ kHz}$ ; $BW_{carrier} = 1.23\text{ MHz}$ ; $P_L = 10\text{ dBm}$	–	49	–	dBc
		$\pm 1.98\text{ MHz}$ offset; $BW_{ACP} = 30\text{ kHz}$ ; $BW_{carrier} = 1.23\text{ MHz}$ ; $P_L = 10\text{ dBm}$	–	74	–	dBc
$P_L$	load power	at 1 dB gain compression point	–	13	–	dBm
$V_{SWR_{IN}}$	input VSWR	$V_{CTRL} = 2.7\text{ V}$	–	1:3.5	–	
$V_{SWR_{OUT}}$	output VSWR	$V_{CTRL} = 2.7\text{ V}$	–	1:1.3	–	
<b>f = 836 MHz</b>						
f	frequency range		824	–	849	MHz
$G_p$	power gain	$V_{CTRL} = 2.7\text{ V}$ ; $P_L = 8\text{ dBm}$	–	24	–	dB
$\Delta G$	gain control range	$0 < V_{CTRL} < 2.7\text{ V}$	–	62	–	dB
$G_{CS}$	gain control slope	note 1	–	22	–	dB/V
ACPR	adjacent channel power rejection	$\pm 885\text{ kHz}$ offset; $BW_{ACP} = 30\text{ kHz}$ ; $BW_{carrier} = 1.23\text{ MHz}$ ; $P_L = 8\text{ dBm}$	–	49	–	dBc
		$\pm 1.98\text{ MHz}$ offset; $BW_{ACP} = 30\text{ kHz}$ ; $BW_{carrier} = 1.23\text{ MHz}$ ; $P_L = 8\text{ dBm}$	–	74	–	dBc
$P_L$	load power	at 1 dB gain compression point	–	11	–	dBm
$V_{SWR_{IN}}$	input VSWR	$V_{CTRL} = 2.7\text{ V}$	–	1:2	–	
$V_{SWR_{OUT}}$	output VSWR	$V_{CTRL} = 2.7\text{ V}$	–	1:1.4	–	

## Note

1.  $G_{CS} = (G \text{ at } V_{CTRL} = 2.5\text{ V} - G \text{ at } V_{CTRL} = 1.5\text{ V}) / (V_{CTRL} = 2.5\text{ V} - V_{CTRL} = 1.5\text{ V})$

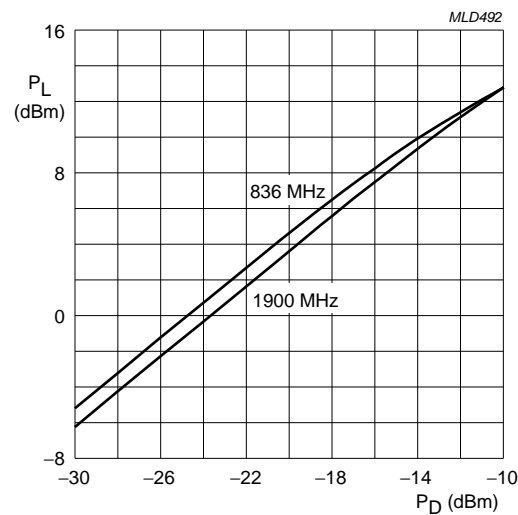
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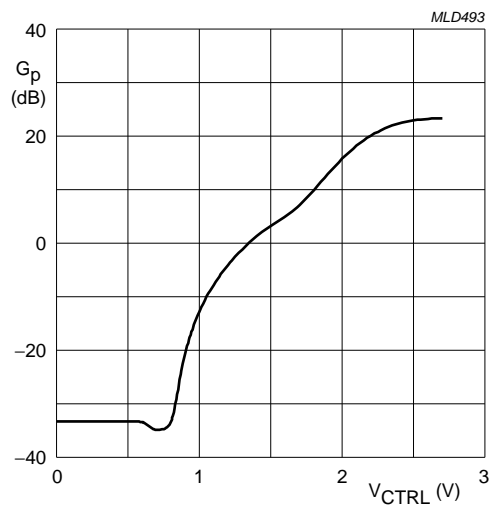
$V_S = 3\text{ V}$ .

Fig.3 Total supply current as a function of control voltage; typical values.



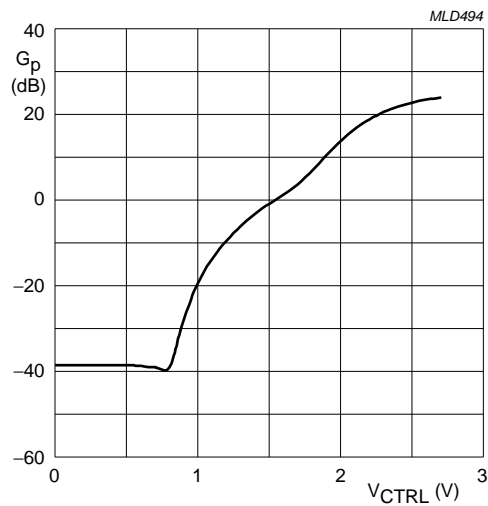
$V_S = 3\text{ V}$ ;  $V_{CTRL} = 2.7\text{ V}$ .

Fig.4 Load power as a function of drive power; typical values.



$V_S = 3\text{ V}$ ;  $P_D = -14\text{ dBm}$ ;  $f = 1.9\text{ GHz}$ .

Fig.5 Power gain as a function of control voltage; typical values.

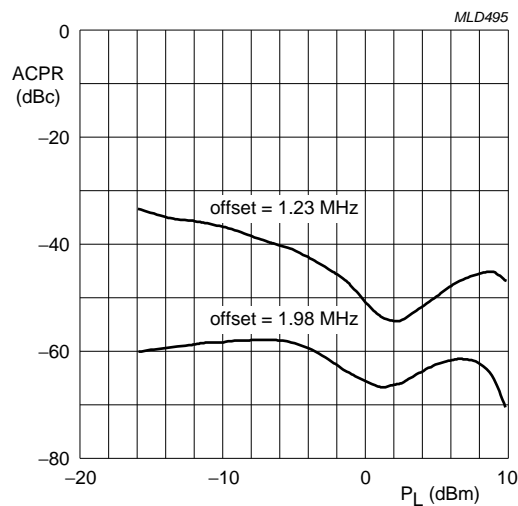


$V_S = 3\text{ V}$ ;  $P_D = -14\text{ dBm}$ ;  $f = 836\text{ MHz}$ .

Fig.6 Power gain as a function of control voltage; typical values.

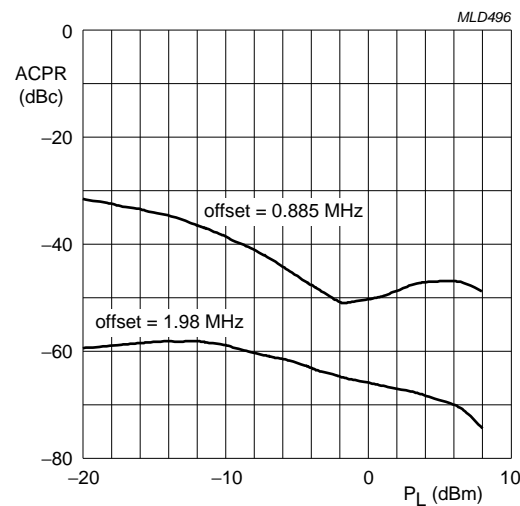
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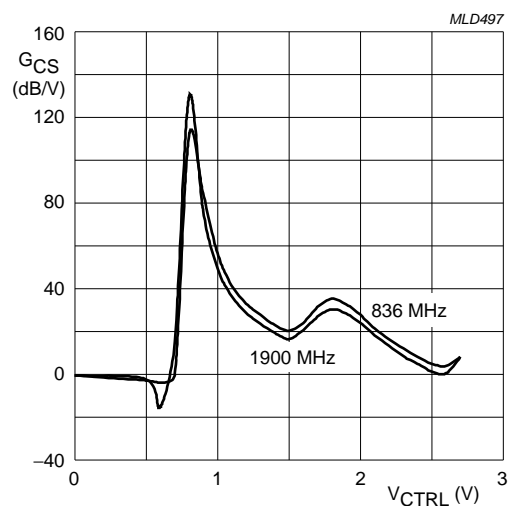
$V_S = 3\text{ V}$ ;  $f = 1.9\text{ GHz}$ ;  $P_D = -12.8\text{ dBm}$ .

Fig.7 Adjacent channel power rejection as a function of load power; typical values.



$V_S = 3.6\text{ V}$ ;  $f = 836\text{ MHz}$ ;  $P_D = -16\text{ dBm}$ .

Fig.8 Adjacent channel power rejection as a function of load power; typical values.



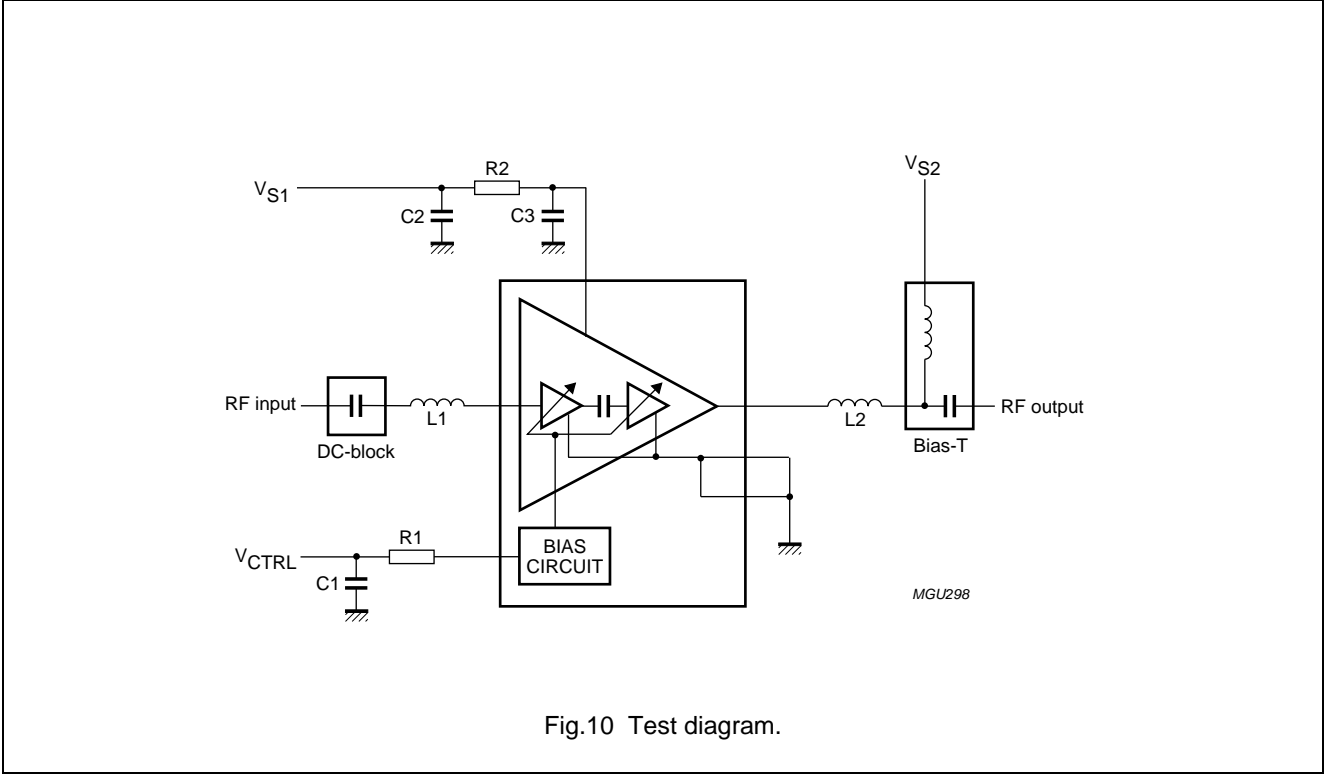
$V_S = 3\text{ V}$ ;  $P_D = -14\text{ dBm}$ .

Fig.9 Gain control slope as a function of control voltage; typical values.

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ELECTRICAL BLOCK DIAGRAM



List of components (see Fig.10)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1	multilayer ceramic chip capacitor	10 nF	0603
C2	multilayer ceramic chip capacitor	22 nF	0603
C3	multilayer ceramic chip capacitor	1.5 nF	0603
L1, L2	stripline; note 1	50 $\Omega$	
R1	SMD resistor	22 $\Omega$ ; 0.16 W	0603
R2	SMD resistor	2.4 $\Omega$ ; 0.16 W	0603

Note

1. The striplines are on a gold plated double copper-clad printed-circuit board ( $\epsilon_r = 6.15$ ), board thickness = 0.64 mm, copper thickness = 35  $\mu\text{m}$ , gold thickness = 5  $\mu\text{m}$ .

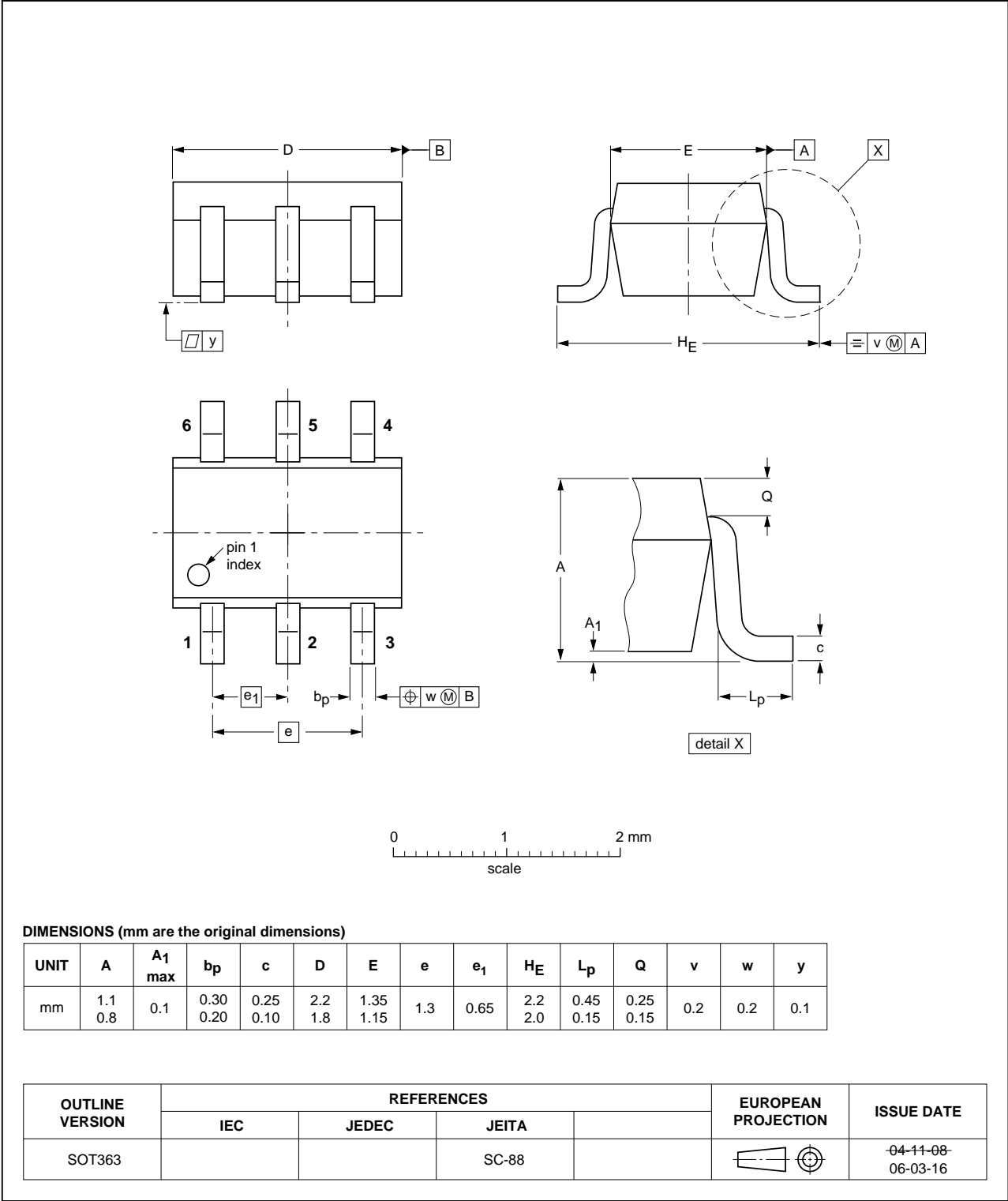
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PACKAGE OUTLINE

Plastic surface-mounted package; 6 leads

SOT363





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## DATA SHEET STATUS

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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