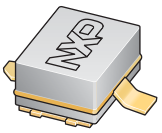


BLF1043

UHF power LDMOS transistor

Rev. 8 — 6 May 2013 Product data sheet

1. Product profile

1.1 General description

10 W LDMOS power transistor for base station applications at frequencies from HF to 1000 MHz.

Table 1. Typical performance

RF performance at T_h = 25 °C in a common source test circuit.

Mode of operation	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, 2-tone, class-AB	f_1 = 960; f_2 = 960.1	26	85	10 (PEP)	18.5	40	≤-31
CW, 1-tone, class-AB	f = 960	26	85	10	18.5	52	-

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

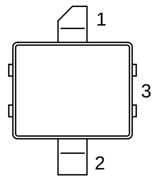
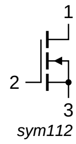
- Typical 2-tone performance at a supply voltage of 26 V and I_{DQ} of 85 mA
  - Output power = 10 W (PEP)
  - Gain = 18.5 dB
  - Efficiency = 40%
  - d_{im} = -31 dBc
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (HF to 1000 MHz)
- No internal matching for broadband operation
- SMD package.

1.3 Applications

- RF power amplifiers for GSM, EDGE and CDMA base stations and multicarrier applications in the 800 to 1000 MHz frequency range
- Broadcast drivers.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source, connected to flange		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF1043	-	ceramic surface mounted package; 2 leads	SOT538A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-	±15	V
I_D	drain current (DC)		-	2.2	A
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th\ j-h}$	thermal resistance from junction to heatsink	T_{mb} = 25 °C	[1]	9	K/W

[1] Thermal resistance is determined under RF operating conditions. Typical value with device soldered on PC board with 32 via holes (diameter 0.3 mm) and thermal compound between PCB and heatsink.

6. Characteristics

Table 6. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 0.2 mA	65	-	-	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 20 mA	4	-	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	-	-	1.5	µA
I_{DSX}	drain cut-off current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	2.8	-	-	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	-	-	40	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 0.75 A	-	0.5	-	S
R_{DSon}	drain-source on-state resistance	V_{DS} = 10 V; I_D = 0.75 A	-	1.05	-	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	-	11	-	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	-	9	-	pF
C_{rss}	feedback capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	-	0.5	-	pF

7. Application information

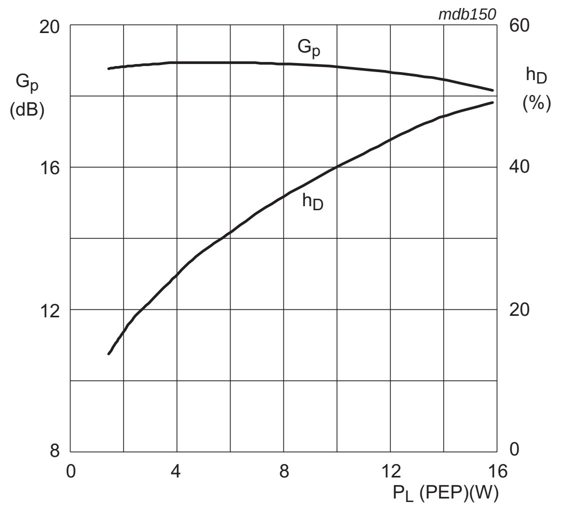
Table 7. RF performance in a common source class-AB circuit

T_h = 25 °C; $R_{th\ j\text{-}h}$ = 9 K/W, unless otherwise specified.

Mode of operation	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, 2-tone, class-AB	f_1 = 960; f_2 = 960.1	26	85	10 (PEP)	>16.5	>38	≤-25

7.1 Ruggedness in class-AB operation

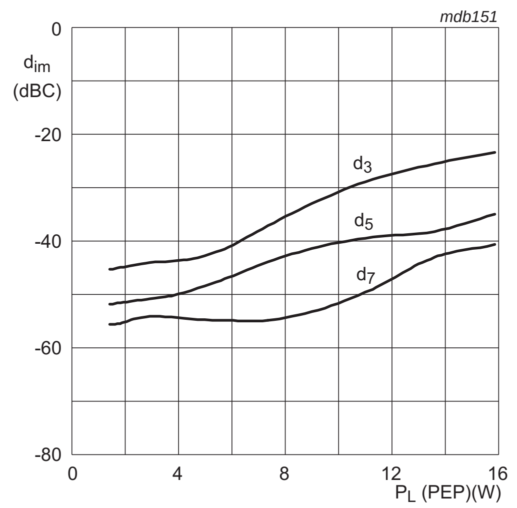
The BLF1043 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; f = 960 MHz at rated load power.



Two-tone performance.

V_{DS} = 26 V; I_{DQ} = 85 mA; $T_h \leq 25$ °C;
f_1 = 960 MHz; f_2 = 960.1 MHz.

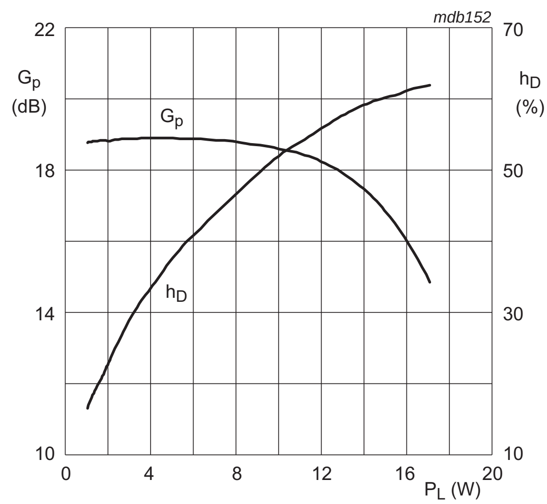
Fig 1. Power gain and efficiency as functions of peak envelope load power; typical values.



Two-tone performance.

V_{DS} = 26 V; I_{DQ} = 85 mA; $T_h \leq 25$ °C;
f_1 = 960 MHz; f = 960.1 MHz.

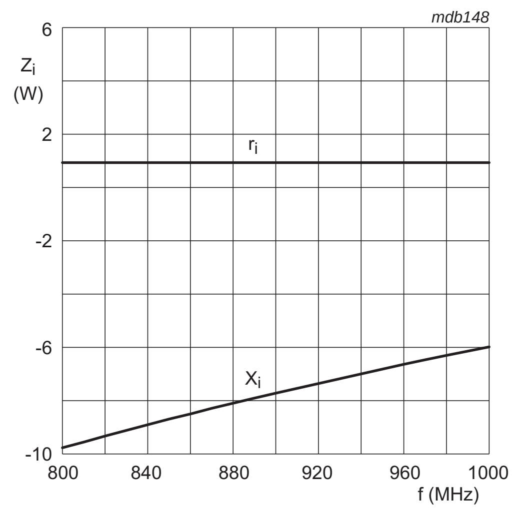
Fig 2. Intermodulation distortion as a function of peak envelope load power; typical values.



Single-tone performance.

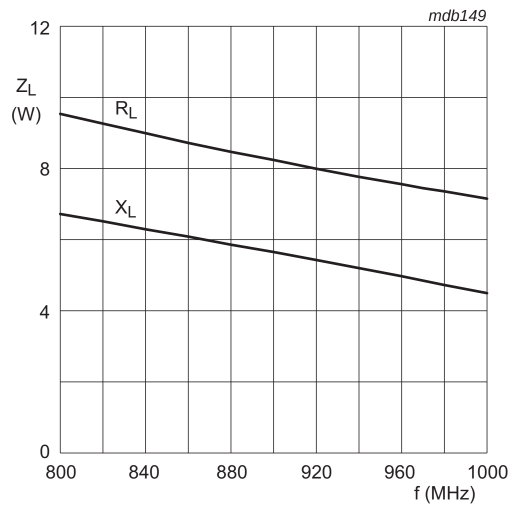
V_{DS} = 26 V; I_{DQ} = 85 mA; $T_h \leq 25$ °C;
f = 960 MHz.

Fig 3. Power gain and efficiency as functions of load power; typical values.



V_{DS} = 26 V; I_{DQ} = 85 mA; P_L = 10 W; $T_h \leq 25$ °C.
Impedance measured at reference planes; see Figure 6.

Fig 4. Input impedance as a function of frequency (series components); typical values.



V_{DS} = 26 V; I_{DQ} = 85 mA; T_h ≤ 25 °C.

Impedance measured at reference planes; see Figure 6.

Fig 5. Input impedance as a function of frequency (series components); typical values.

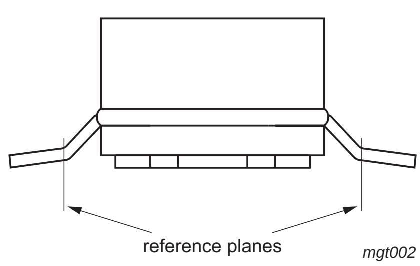


Fig 6. Measuring reference planes: SOT538A.

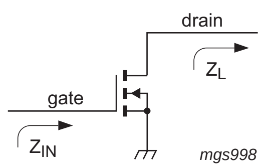


Fig 7. Definition of transistor impedance.

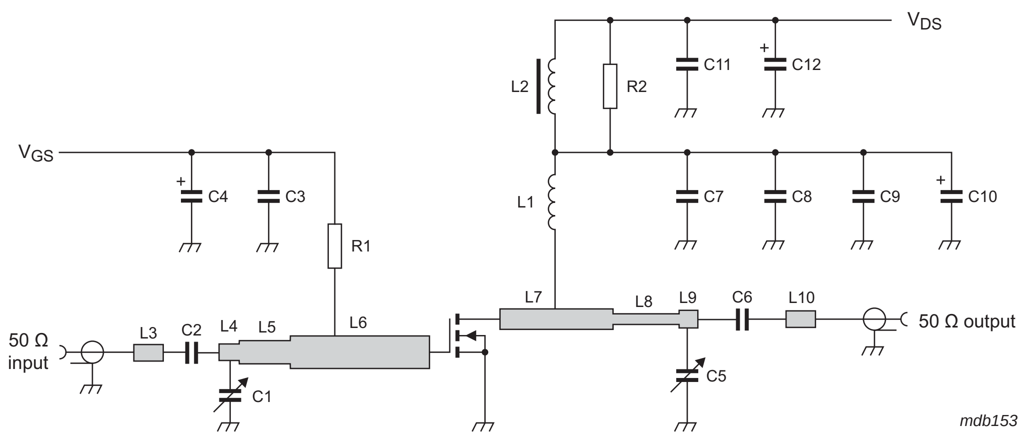


Fig 8. Class-AB test circuit for 960 MHz.

8. Test information

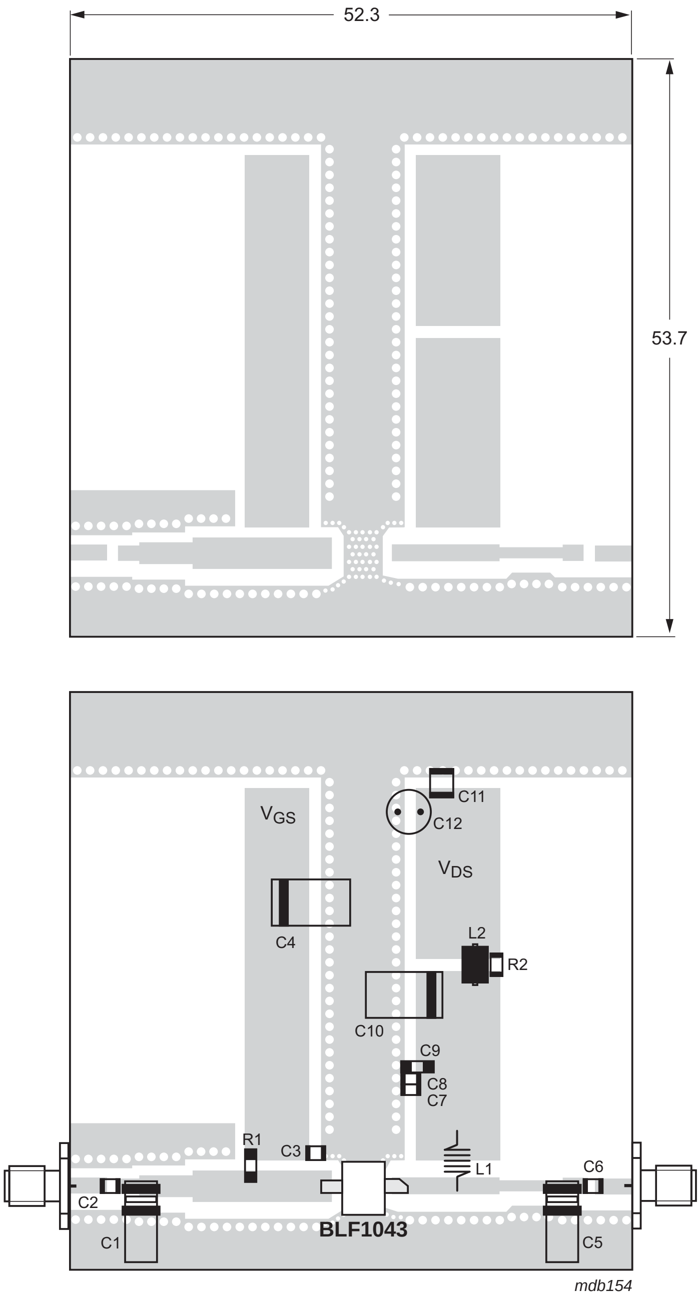
Table 8. List of components
(see Figure 8 and Figure 9)

Component	Description		Value	Dimension	Catalogue no.
C1, C5	Tekelec variable capacitor		0.8 to 8 pF		
C2, C3, C6, C7	multilayer ceramic chip capacitor	[1]	56 pF		
C4, C10	tantalum SMD capacitor		10 μF; 35 V		
C8	multilayer ceramic chip capacitor	[1]	1 nF		
C9	multilayer ceramic chip capacitor		100 nF		2222 581 16641
C11	multilayer ceramic chip capacitor	[2]	1 nF		
C12	electrolytic capacitor		100 μF; 63 V		2222 037 58101
L1	3 turns enamelled 0.5 mm copper wire			3 loops; d = 3.5 mm	
L2	ferrite bead; ferroxcube CBD4.6/3/3-4S2				
L3	stripline	[3]	50 Ω	3.5 x 1.5 mm	
L4	stripline	[3]	50 Ω	2 x 1.5 mm	
L5	stripline	[3]	42 Ω	5 x 2 mm	
L6	stripline	[3]	31 Ω	13 x 3 mm	
L7	stripline	[3]	50 Ω	10 x 1.5 mm	
L8	stripline	[3]	65 Ω	5.9 x 1 mm	
L9	stripline	[3]	50 Ω	2 x 1.5 mm	
L10	stripline	[3]	50 Ω	3.5 x 1.5 mm	
R1	metal film resistor		39 Ω, 0.6 W		
R2	metal film resistor		10 Ω, 0.6 W		2322 256 11009

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

[3] The striplines are on a double copper-clad printed-circuit board with Rogers 5880 dielectric (ε_r = 2.2); thickness 0.51 mm.



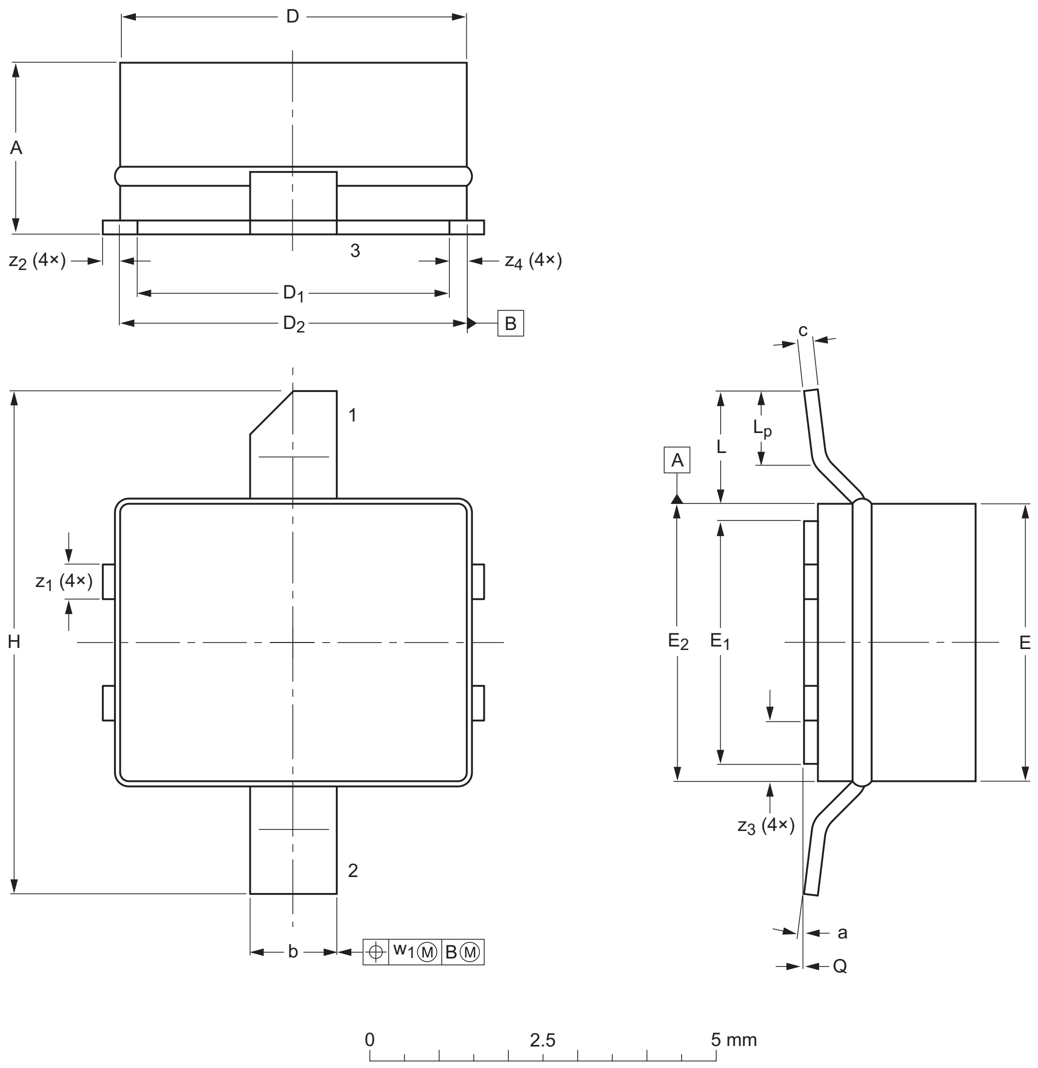
Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric (ε_r = 2.2), thickness 0.51 mm.
The other side is unetched and serves as a ground plane.

Fig 9. Component layout for 960 MHz class-AB test circuit.

9. Package outline

Ceramic surface-mounted package; 2 leads **SOT538A**



Dimensions (mm are the original dimensions)

Unit		A	b	c	D	D_1	D_2	E	E_1	E_2	H	L	L_p	Q	w_1	z_1	z_2	z_3	z_4	θ
mm	max	2.34	1.35	0.23	5.16	4.65	5.16	4.14	3.63	4.14	7.49	2.03	1.02	0.1		0.58	0.25	0.97	0.51	7°
	nom														0.25					
	min	2.13	1.19	0.18	5.00	4.50	5.00	3.99	3.48	3.99	7.24	1.27	0.51	0.0		0.43	0.18	0.81	0.00	0°

sot538a_po

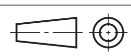
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT538A						~~06-03-16~~ 13-02-07

Fig 10. Package outline SOT538A

10. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF1043 v.8	20130506	Product data sheet	-	BLF1043 v.7
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Package outline drawings have been updated to the latest version.			
BLF1043 v.7	20030313	Product specification	-	BLF1043 v.6

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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13. Contents

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