

# BLF8G09LS-400PW; BLF8G09LS-400PGW

Power LDMOS transistor

Rev. 5 — 1 September 2015

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

400 W LDMOS power transistor for base station applications at frequencies from 716 MHz to 960 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in a common source class-AB production test circuit, tested on straight lead device.

Test signal	f (MHz)	$I_{Dq}$ (mA)	$V_{DS}$ (V)	$P_{L(AV)}$ (W)	$G_p$ (dB)	$\eta_D$ (%)	ACPR <sub>5M</sub> (dBc)
2-carrier W-CDMA	716 to 728	3400	28	95	20.6	30	-35 <a href="#">[1]</a>

[1] 3GPP test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; 10 MHz carrier spacing.

### 1.2 Features and benefits

- Excellent ruggedness
- Device can operate with the supply current delivered through the video leads
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Designed for broadband operation
- Lower output capacitance for improved performance in Doherty applications
- Decoupling leads to enable improved video bandwidth (45 MHz typical)
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Design optimized for gull-wing
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 716 MHz to 960 MHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLF8G09LS-400PW (SOT1242B)</b>			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source <a href="#">[1]</a>		
6	decoupling1 <a href="#">[2]</a>		
7	decoupling2 <a href="#">[2]</a>		
8	n.c.		
9	n.c.		
<b>BLF8G09LS-400PGW (SOT1242C)</b>			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source <a href="#">[1]</a>		
6	decoupling1 <a href="#">[2]</a>		
7	decoupling2 <a href="#">[2]</a>		
8	n.c.		
9	n.c.		

[1] Connected to flange.

[2] Device can operate with the supply current delivered through the combined decoupling leads.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF8G09LS-400PW	-	earless flanged ceramic package; 8 leads	SOT1242B
BLF8G09LS-400PGW	-	earless flanged ceramic package; 8 leads	SOT1242C

## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 95\text{ W}$	0.26	K/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$ ; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 3\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 300\text{ mA}$	1.5	1.8	2.3	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 28\text{ V}; I_D = 1700\text{ mA}$	1.7	2	2.5	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	2.8	μA
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	55	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 15\text{ A}$	-	26	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 12.25\text{ A}$	-	0.06	-	Ω

**Table 7. RF characteristics**

Test signal: 2-carrier W-CDMA; PAR = 8.4 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1-64 DPCH;  $f_1 = 718.5\text{ MHz}; f_2 = 723.5\text{ MHz}; f_3 = 720.5\text{ MHz}; f_4 = 725.5\text{ MHz}$ ; RF performance at  $V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}; T_{case} = 25\text{ °C}$ ; unless otherwise specified; in a class-AB production test circuit, tested on straight lead device.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 95\text{ W}$	18.8	20.6	-	dB
$RL_{in}$	input return loss	$P_{L(AV)} = 95\text{ W}$	-	-19	-11	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 95\text{ W}$	26	30	-	%
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)} = 95\text{ W}$	-	-35	-32	dBc

## 7. Test information

### 7.1 Ruggedness in class-AB operation

The BLF8G09LS-400PW and BLF8G09LS-400PGW are capable of withstanding a load mismatch corresponding to VSWR = 7 : 1 through all phases under the following conditions:  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 3400\text{ mA}$ ; 2-carrier W-CDMA signal;  $P_L = 200\text{ W}$ ;  $f = 716\text{ MHz}$ ; 5 MHz carrier spacing; 46 % clipping.

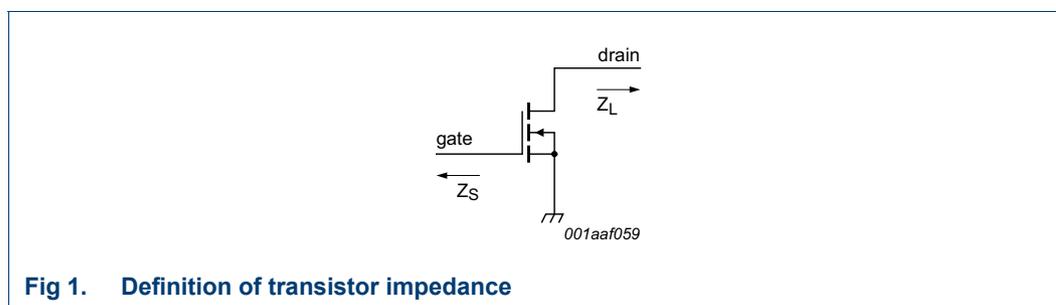
### 7.2 Impedance information

**Table 8. Typical impedance**

Measured load-pull data for the top-half of the push-pull package;  $I_{Dq} = 1800\text{ mA}$ ;  $V_{DS} = 28\text{ V}$ ;  $T_{case} = 25\text{ °C}$ , water cooled.

f (MHz)	$Z_S$ <sup>[1]</sup> ( $\Omega$ )	$Z_L$ <sup>[1]</sup> ( $\Omega$ )
<b>BLF8G09LS-400PW (straight lead)</b>		
720	1.26 – j2.89	1.8 – j1.94
757	1.44 – j3.82	2 – j1.6
769	1.55 – j3.64	1.9 – j1.75
805	1.7 – j4.5	1.5 – j1.3
<b>BLF8G09LS-400PGW (gull-wing)</b>		
720	1.37 – j3	1.7 – j2.1
757	1.4 – j3.6	1.6 – j2.3
769	1.3 – j3.9	1.7 – j2.2
805	1.6 – j4.3	1.48 – j1.97

[1]  $Z_S$  and  $Z_L$  defined in [Figure 1](#).

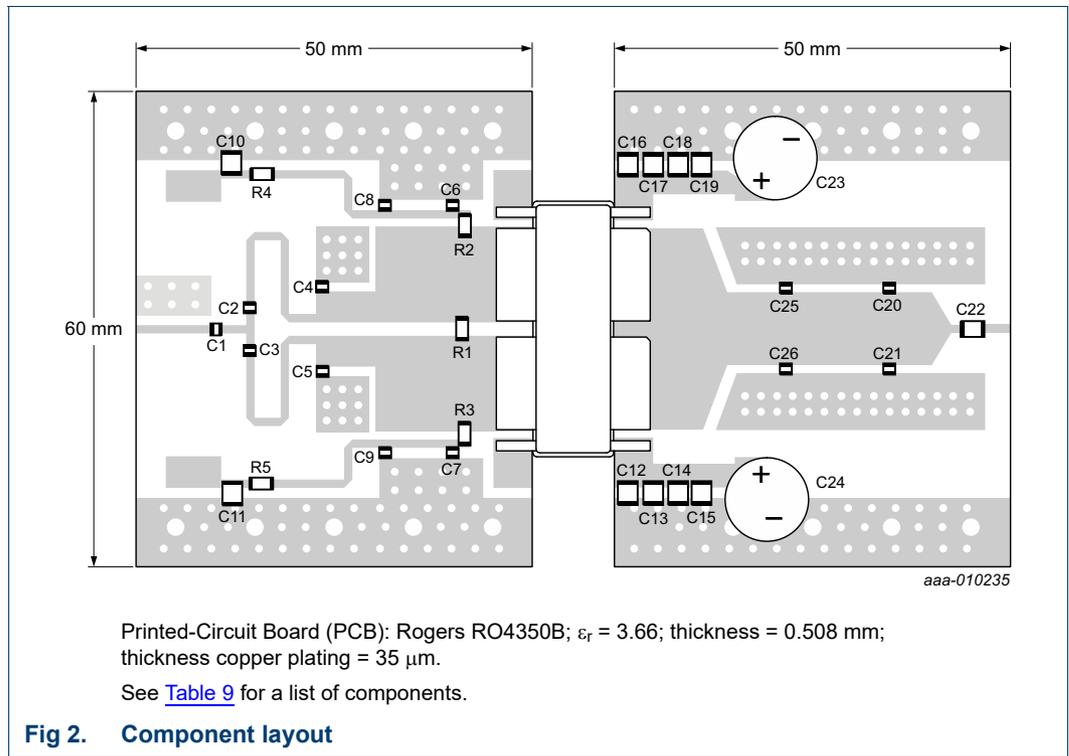


**Fig 1. Definition of transistor impedance**

### 7.3 VBW in class-AB operation

The BLF8G09LS-400PW and BLF8G09LS-400PGW show 45 MHz (typical) video bandwidth in class-AB test circuit in 722 MHz band at  $V_{DS} = 28\text{ V}$  and  $I_{Dq} = 3400\text{ mA}$ .

7.4 Test circuit



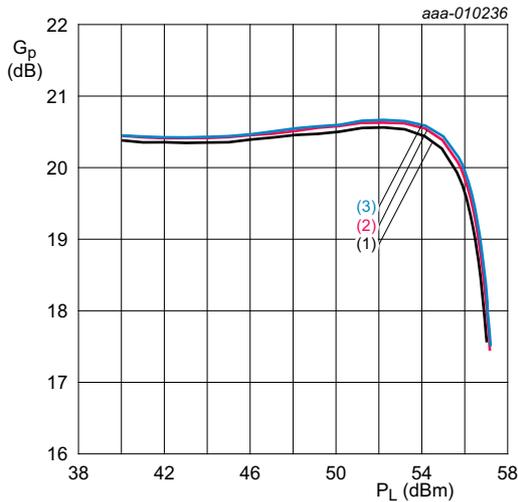
**Table 9. List of components**

For test circuit see [Figure 2](#).

Component	Description	Value	Remarks
C1, C2, C3, C8, C9	multilayer ceramic chip capacitor	100 pF	ATC 100A
C4, C5	multilayer ceramic chip capacitor	9.1 pF	ATC 100A
C6, C7	multilayer ceramic chip capacitor	10 pF	ATC 100A
C10, C11, C13, C17	multilayer ceramic chip capacitor	1 $\mu\text{F}$ , 50 V	Murata
C12, C16	multilayer ceramic chip capacitor	100 nF, 50 V	Murata
C14, C15, C18, C19	multilayer ceramic chip capacitor	10 $\mu\text{F}$ , 50 V	Murata
C20, C21	multilayer ceramic chip capacitor	5.1 pF	ATC 100A
C22	multilayer ceramic chip capacitor	82 pF	ATC 100B
C23, C24	electrolytic capacitor	470 $\mu\text{F}$ , 63 V	
C25, C26	multilayer ceramic chip capacitor	3 pF	ATC 100A
R1	resistor	10 $\Omega$	
R2, R3, R4, R5	resistor	5.1 $\Omega$	

7.5 Graphical data

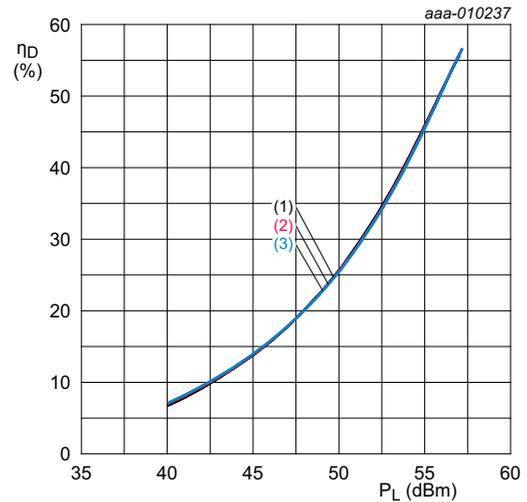
7.5.1 Pulsed CW



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}; t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .

- (1)  $f = 716\text{ MHz}$
- (2)  $f = 722\text{ MHz}$
- (3)  $f = 728\text{ MHz}$

**Fig 3. Power gain as a function of output power; typical values**

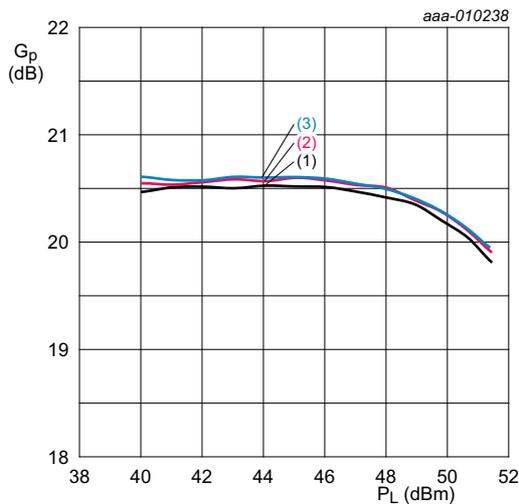


$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}; t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .

- (1)  $f = 716\text{ MHz}$
- (2)  $f = 722\text{ MHz}$
- (3)  $f = 728\text{ MHz}$

**Fig 4. Drain efficiency as a function of output power; typical values**

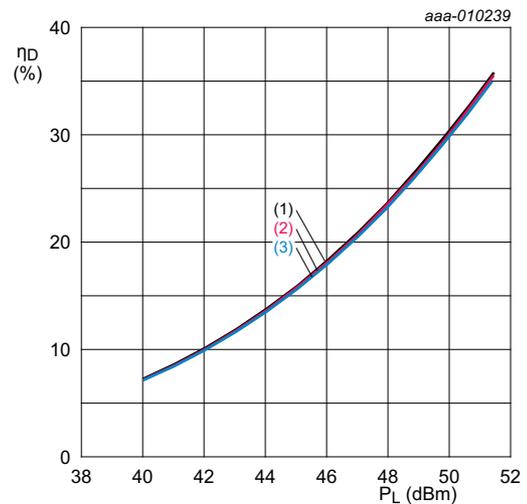
7.5.2 IS-95



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA.}$

- (1)  $f = 716\text{ MHz}$
- (2)  $f = 722\text{ MHz}$
- (3)  $f = 728\text{ MHz}$

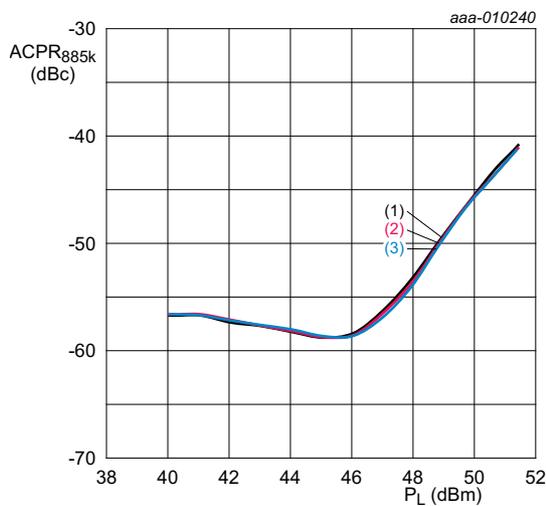
**Fig 5. Power gain as a function of output power; typical values**



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA.}$

- (1)  $f = 716\text{ MHz}$
- (2)  $f = 722\text{ MHz}$
- (3)  $f = 728\text{ MHz}$

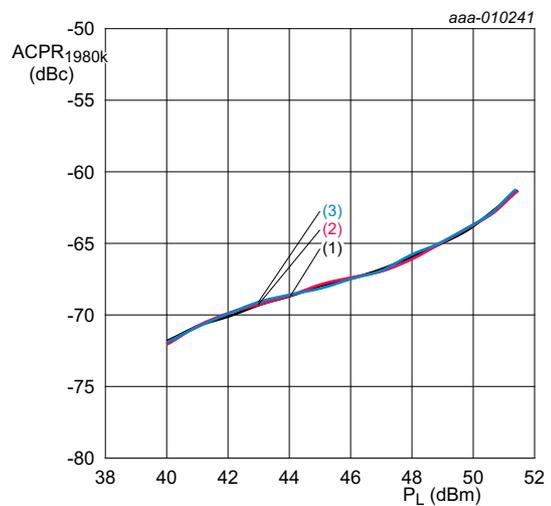
**Fig 6. Drain efficiency as a function of output power; typical values**



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA.}$

- (1)  $f = 716\text{ MHz}$
- (2)  $f = 722\text{ MHz}$
- (3)  $f = 728\text{ MHz}$

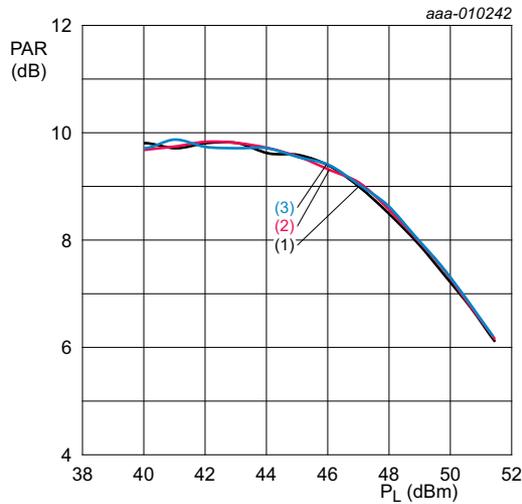
**Fig 7. Adjacent channel power ratio (885 kHz) as a function of output power; typical values**



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA.}$

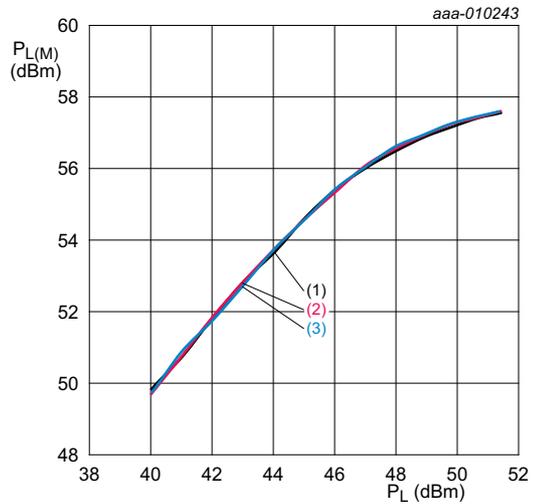
- (1)  $f = 716\text{ MHz}$
- (2)  $f = 722\text{ MHz}$
- (3)  $f = 728\text{ MHz}$

**Fig 8. Adjacent channel power ratio (1980 kHz) as a function of output power; typical values**



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}.$   
 (1)  $f = 716\text{ MHz}$   
 (2)  $f = 722\text{ MHz}$   
 (3)  $f = 728\text{ MHz}$

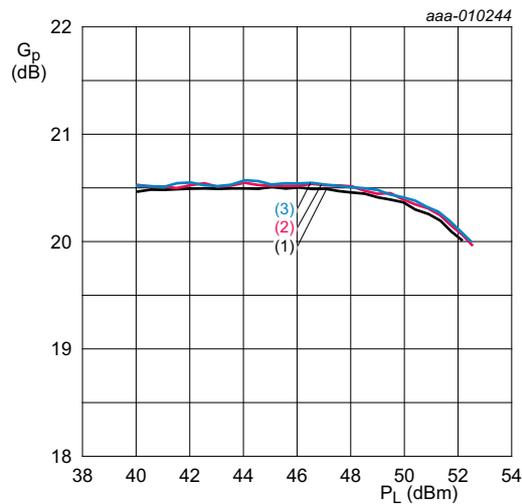
**Fig 9. Peak-to-average ratio as a function of output power; typical values**



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}.$   
 (1)  $f = 716\text{ MHz}$   
 (2)  $f = 722\text{ MHz}$   
 (3)  $f = 728\text{ MHz}$

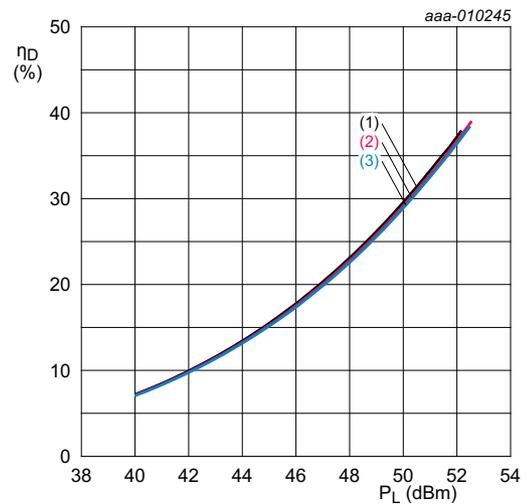
**Fig 10. Peak output power as a function of output; typical values**

7.5.3 1-Carrier W-CDMA



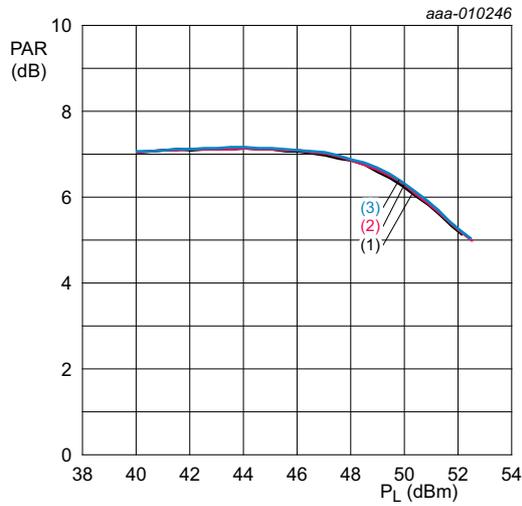
$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}.$   
 (1)  $f = 716\text{ MHz}$   
 (2)  $f = 722\text{ MHz}$   
 (3)  $f = 728\text{ MHz}$

**Fig 11. Power gain as a function of output power; typical values**



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}.$   
 (1)  $f = 716\text{ MHz}$   
 (2)  $f = 722\text{ MHz}$   
 (3)  $f = 728\text{ MHz}$

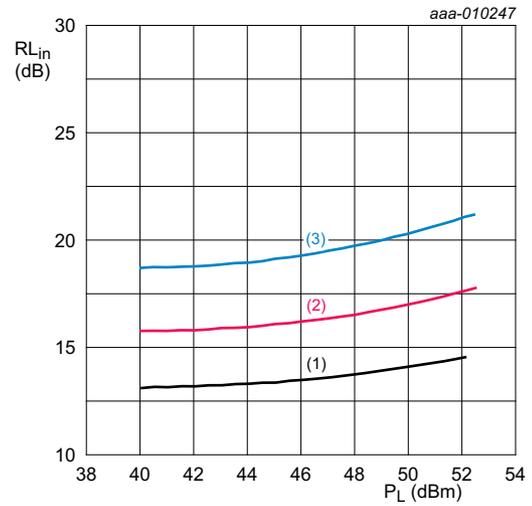
**Fig 12. Drain efficiency as a function of output power; typical values**



V<sub>DS</sub> = 28 V; I<sub>Dq</sub> = 3400 mA.

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

Fig 13. Peak-to-average ratio as a function of output power; typical values

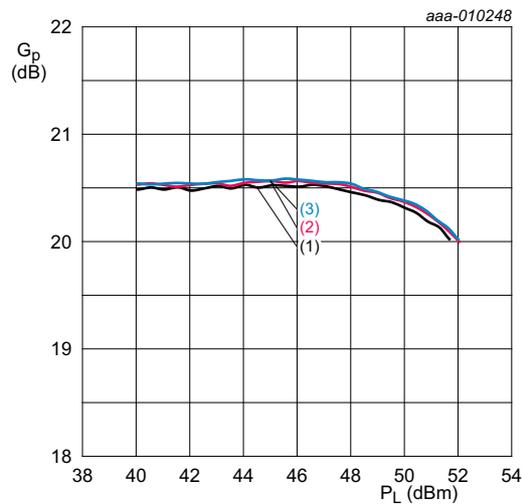


V<sub>DS</sub> = 28 V; I<sub>Dq</sub> = 3400 mA.

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

Fig 14. Input return loss as a function of output power; typical values

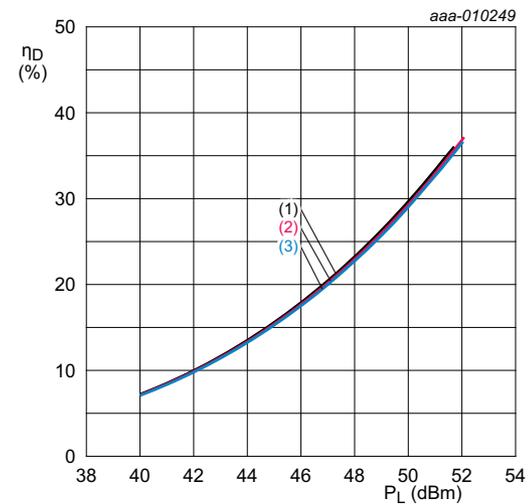
7.5.4 2-Carrier W-CDMA



V<sub>DS</sub> = 28 V; I<sub>Dq</sub> = 3400 mA.

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

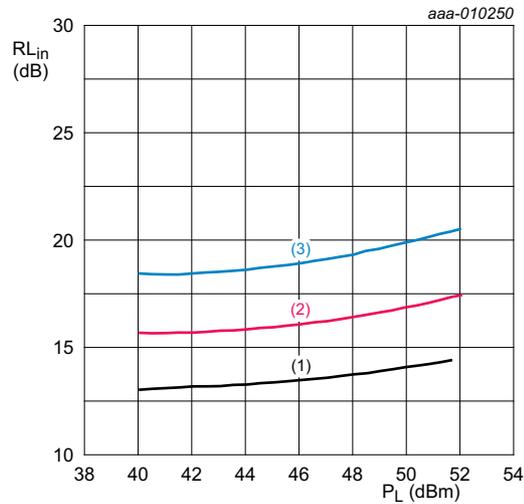
Fig 15. Power gain as a function of output power; typical values



V<sub>DS</sub> = 28 V; I<sub>Dq</sub> = 3400 mA.

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

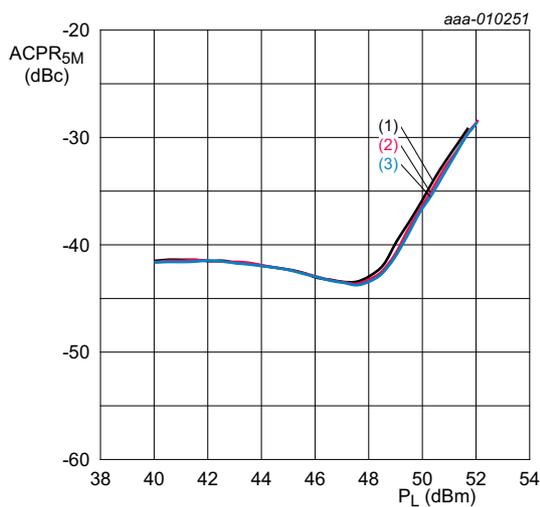
Fig 16. Drain efficiency as a function of output power; typical values



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}$ .

- (1)  $f = 716\text{ MHz}$
- (2)  $f = 722\text{ MHz}$
- (3)  $f = 728\text{ MHz}$

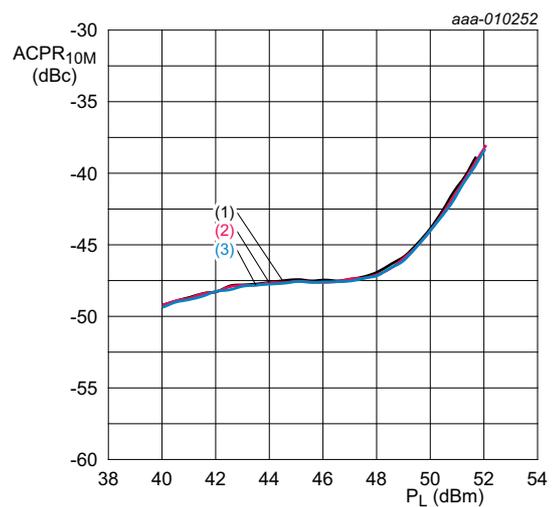
**Fig 17. Input return loss as a function of output power; typical values**



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}$ .

- (1)  $f = 716\text{ MHz}$
- (2)  $f = 722\text{ MHz}$
- (3)  $f = 728\text{ MHz}$

**Fig 18. Adjacent channel power ratio (5 MHz) as a function of output power; typical values**

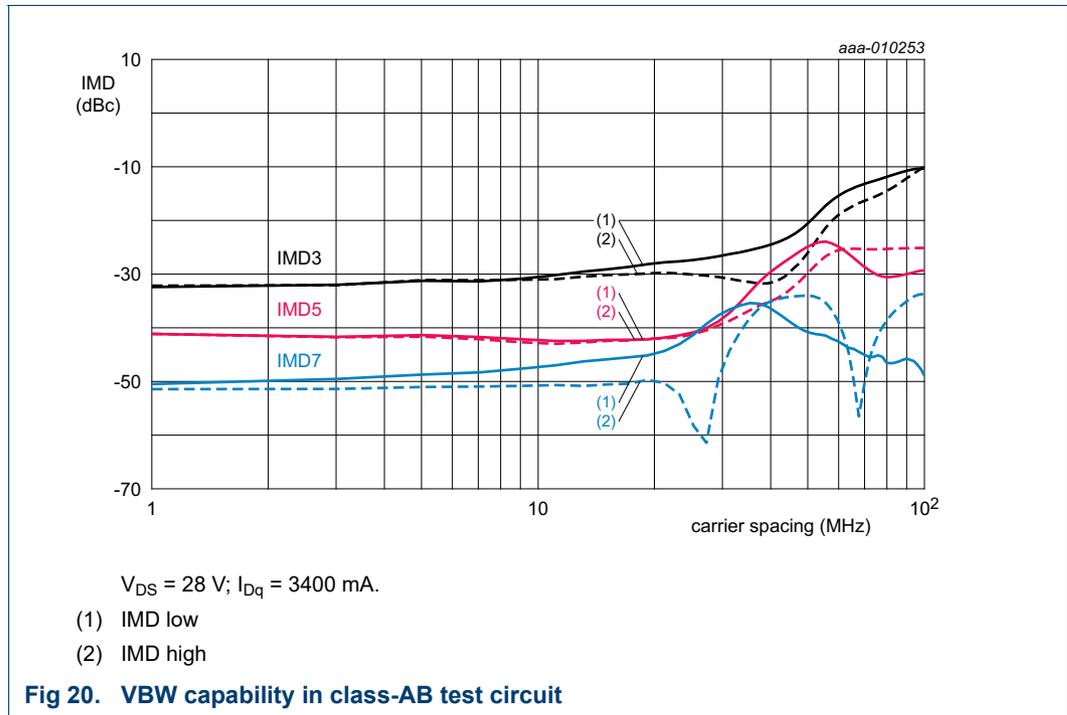


$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}$ .

- (1)  $f = 716\text{ MHz}$
- (2)  $f = 722\text{ MHz}$
- (3)  $f = 728\text{ MHz}$

**Fig 19. Adjacent channel power ratio (10 MHz) as a function of output power; typical values**

7.5.5 2-Tone VBW



8. Package outline

Earless flanged ceramic package; 8 leads

SOT1242B

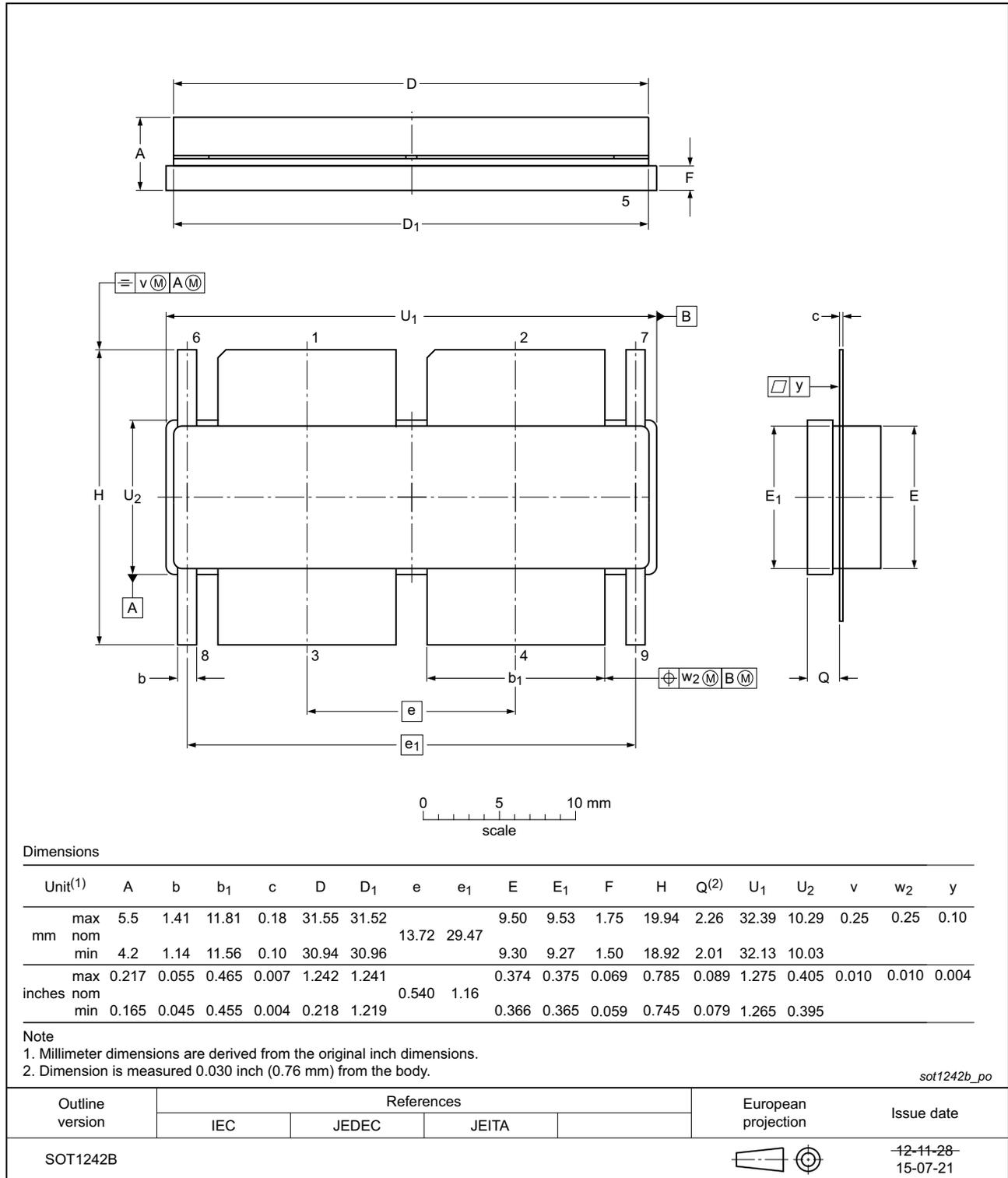


Fig 21. Package outline SOT1242B

Earless flanged ceramic package; 8 leads

SOT1242C

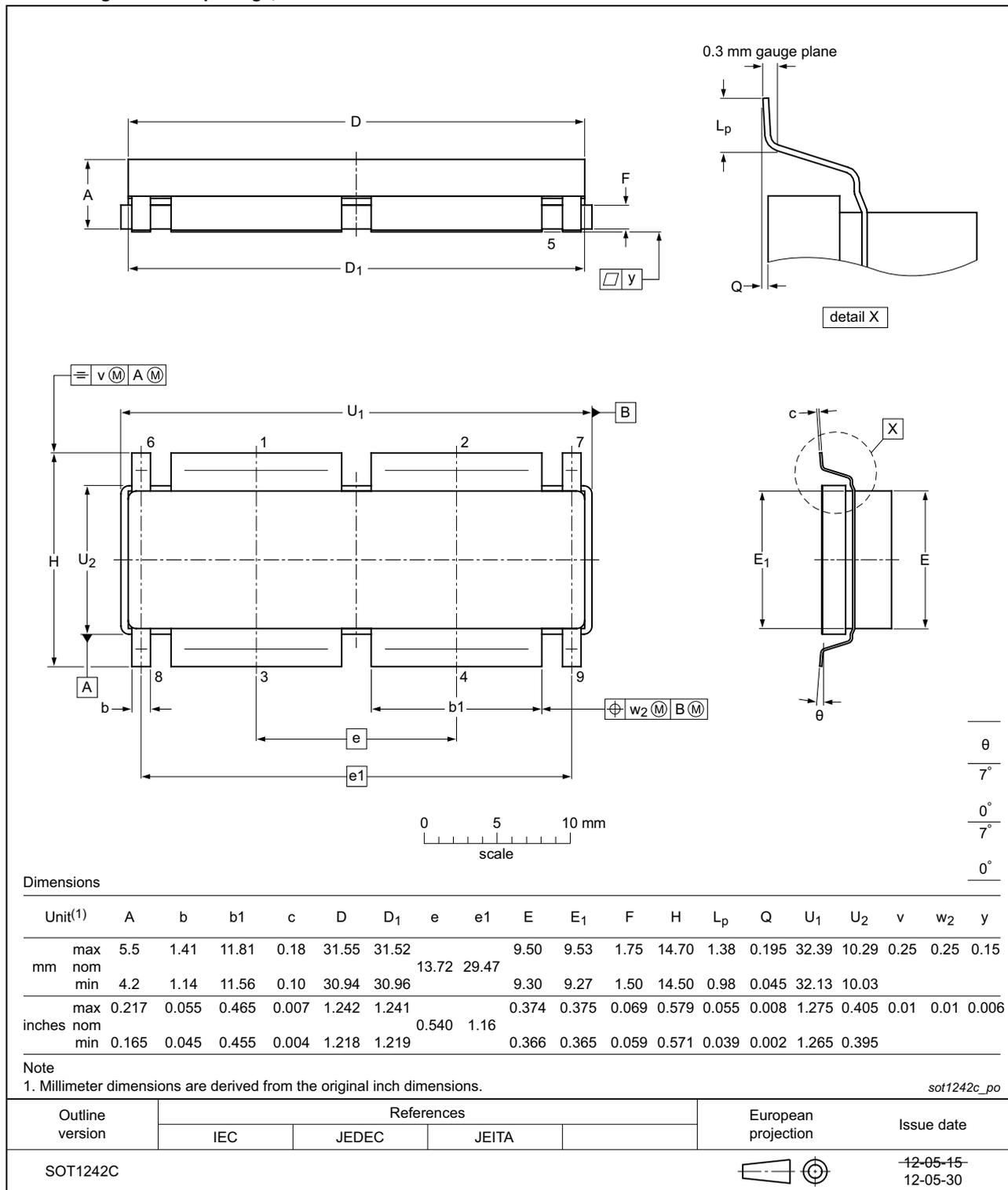


Fig 22. Package outline SOT1242C

## 9. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
IS-95	Interim Standard 95
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
VBW	Video Bandwidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G09LS-400PW_8G09LS-400PGW#5	20150901	Product data sheet	-	BLF8G09LS-400PW_8G09LS-400PGW v.4
Modifications:	<ul style="list-style-type: none"> <li>The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
BLF8G09LS-400PW_8G09LS-400PGW v.4	20150728	Product data sheet	-	BLF8G09LS-400PW_8G09LS-400PGW v.3
BLF8G09LS-400PW_8G09LS-400PGW v.3	20140324	Product data sheet	-	BLF8G09LS-400PW_8G09LS-400PGW v.2
BLF8G09LS-400PW_8G09LS-400PGW v.2	20131220	Preliminary data sheet	-	BLF8G09LS-400PW_8G09LS-400PGW v.1
BLF8G09LS-400PW_8G09LS-400PGW v.1	20130927	Objective data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.ampleon.com>.

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