

# BLL8H1214L-250; BLL8H1214LS-250

LDMOS L-band radar power transistor

Rev. 3 — 1 September 2015

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

250 W LDMOS power transistor intended for L-band radar applications in the 1.2 GHz to 1.4 GHz range.

**Table 1. Test information**

Typical RF performance at  $T_{case} = 25\text{ °C}$ ;  $t_p = 300\text{ }\mu\text{s}$ ;  $\delta = 10\%$ ;  $I_{Dq} = 100\text{ mA}$ ; in a class-AB production test circuit.

Test signal	f	V <sub>DS</sub>	P <sub>L</sub>	G <sub>p</sub>	$\eta_D$	t <sub>r</sub>	t <sub>f</sub>
	(GHz)	(V)	(W)	(dB)	(%)	(ns)	(ns)
pulsed RF	1.2 to 1.4	50	250	17	55	15	5

### 1.2 Features and benefits

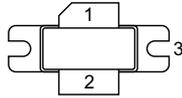
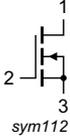
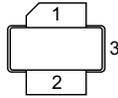
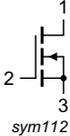
- Easy power control
- Integrated dual side ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1.2 GHz to 1.4 GHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

### 1.3 Applications

- L-band power amplifiers for radar applications in the 1.2 GHz to 1.4 GHz frequency range

## 2. Pinning information

**Table 2. Pinning**

Pin	Description	Simplified outline	Graphic symbol
<b>BLL8H1214L-250 (SOT502A)</b>			
1	drain		 sym112
2	gate		
3	source <a href="#">[1]</a>		
<b>BLL8H1214LS-250 (SOT502B)</b>			
1	drain		 sym112
2	gate		
3	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BLL8H1214L-250	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLL8H1214LS-250	-	earless flanged ceramic package; 2 leads	SOT502B

## 4. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	100	V
$V_{GS}$	gate-source voltage		-6	+13	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	<a href="#">[1]</a>	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_{case} = 85\text{ °C}; P_L = 250\text{ W}$		
		$t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.10	K/W
		$t_p = 200\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.13	K/W
		$t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.15	K/W
		$t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ }\%$	0.14	K/W
		$t_p = 500\text{ }\mu\text{s}; \delta = 20\text{ }\%$	0.20	K/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.7\text{ mA}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 270\text{ mA}$	1.3	1.8	2.25	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	1.4	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	32	42	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 270\text{ mA}$	1.6	2.3	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 9.5\text{ A}$	-	100	169	m $\Omega$

**Table 7. RF characteristics**

Test signal: pulsed RF;  $t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$ ; RF performance at  $V_{DS} = 50\text{ V}; I_{Dq} = 100\text{ mA}$ ;  $T_{case} = 25\text{ °C}$ ; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$P_L = 250\text{ W}$	-	-	50	V
$G_p$	power gain	$P_L = 250\text{ W}$	15	17	-	dB
$RL_{in}$	input return loss	$P_L = 250\text{ W}$	-	-10	-	dB
$P_{L(1dB)}$	output power at 1 dB gain compression		-	300	-	W
$\eta_D$	drain efficiency	$P_L = 250\text{ W}$	49	55	-	%
$P_{droop(pulse)}$	pulse droop power	$P_L = 250\text{ W}$	-	0	0.3	dB
$t_r$	rise time	$P_L = 250\text{ W}$	-	15	-	ns
$t_f$	fall time	$P_L = 250\text{ W}$	-	5	-	ns

## 7. Application information

### 7.1 Ruggedness in class-AB operation

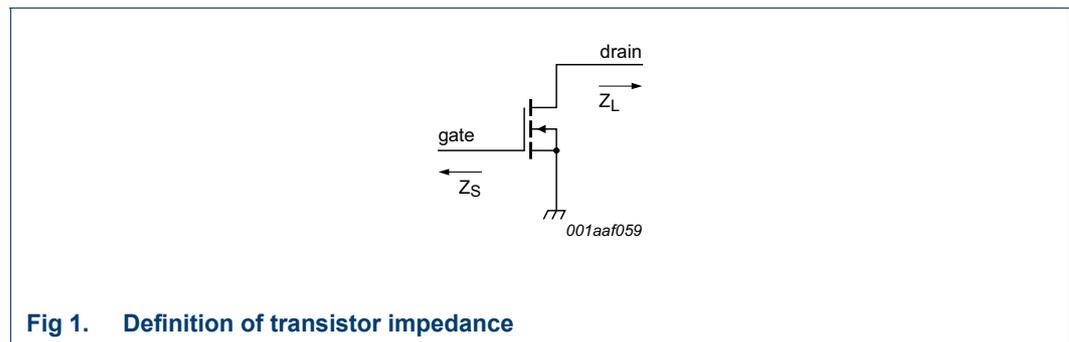
The BLL8H1214L-250 and BLL8H1214LS-250 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 50\text{ V}$ ;  $I_{DQ} = 100\text{ mA}$ ;  $P_L = 250\text{ W}$ ;  $t_p = 300\text{ }\mu\text{s}$ ;  $\delta = 10\text{ }\%$ .

### 7.2 Impedance information

**Table 8. Typical impedance**

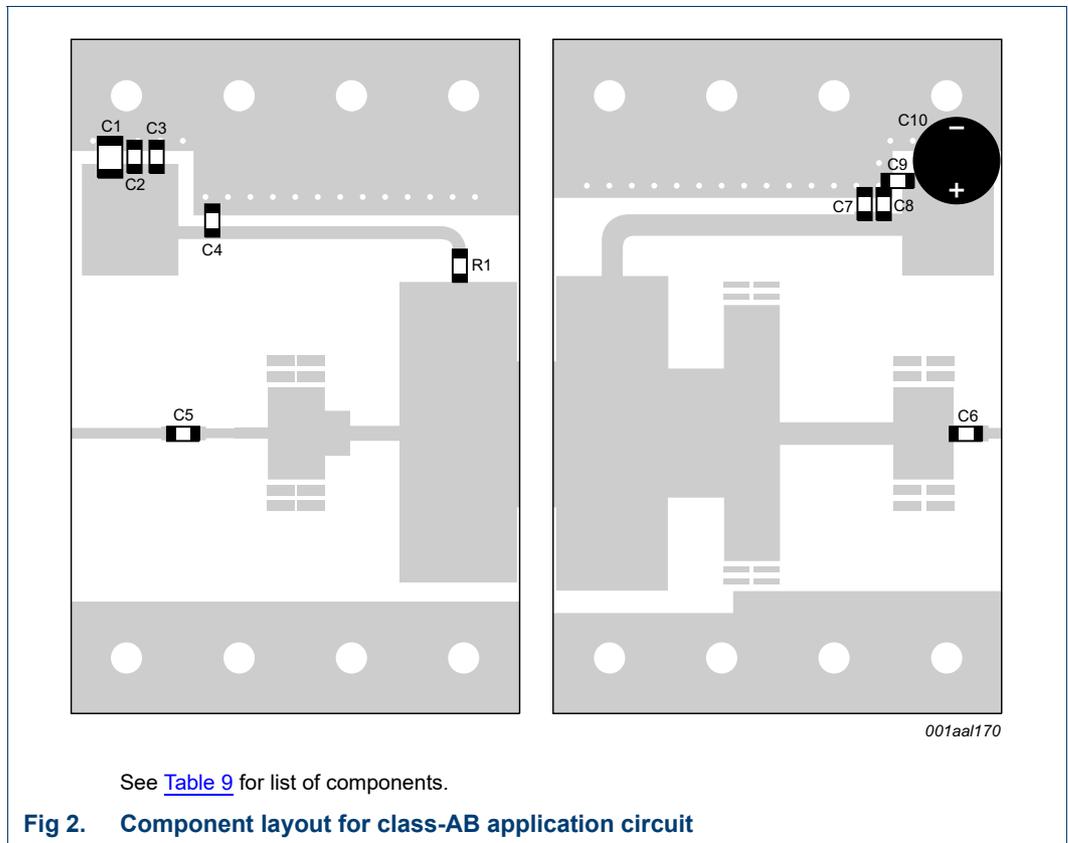
*Typical values unless otherwise specified.*

<b>f</b> <b>(GHz)</b>	<b>Z<sub>S</sub></b> <b>(<math>\Omega</math>)</b>	<b>Z<sub>L</sub></b> <b>(<math>\Omega</math>)</b>
1.2	1.268 – j2.623	2.987 – j1.664
1.3	2.193 – j2.457	2.162 – j1.326
1.4	2.359 – j2.052	1.604 – j1.887



**Fig 1. Definition of transistor impedance**

7.3 Application circuit



**Table 9. List of components**

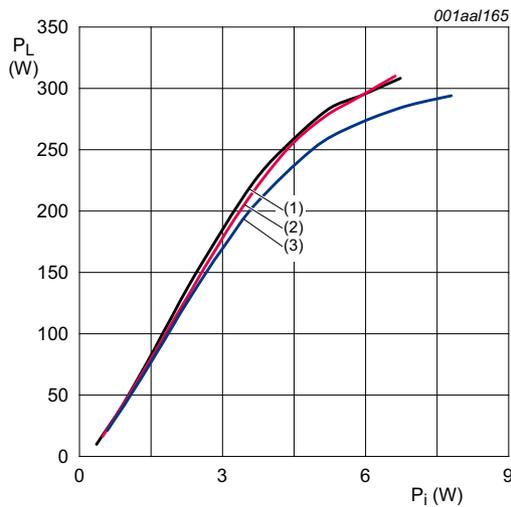
See [Figure 2](#).

Striplines are on a Rogers Duroid 6006 Printed-Circuit Board (PCB);  $\epsilon_r = 6.15$  F/m; thickness = 0.64 mm

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	10 $\mu$ F, 35 V <a href="#">[1]</a>	
C2, C4	multilayer ceramic chip capacitor	51 pF <a href="#">[2]</a>	
C3, C8	multilayer ceramic chip capacitor	1 nF <a href="#">[2]</a>	
C5	multilayer ceramic chip capacitor	82 pF <a href="#">[3]</a>	
C6, C7	multilayer ceramic chip capacitor	56 pF <a href="#">[3]</a>	
C9	multilayer ceramic chip capacitor	100 pF <a href="#">[3]</a>	
C10	electrolytic capacitor	47 $\mu$ F, 63 V	
R1	SMD resistor	10 $\Omega$	SMD 0603

- [1] American Technical Ceramics type 100A or capacitor of same quality.
- [2] American Technical Ceramics type 100B or capacitor of same quality.
- [3] American Technical Ceramics type 800B or capacitor of same quality.

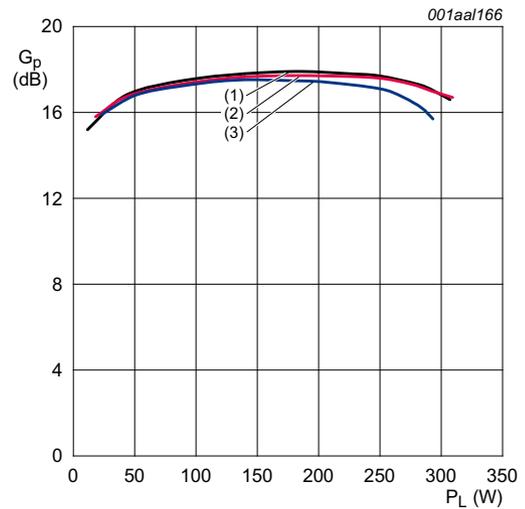
7.4 RF performance graphs



$V_{DS} = 50 \text{ V}$ ;  $t_p = 300 \text{ } \mu\text{s}$ ;  $\delta = 10 \%$ ;  $I_{Dq} = 100 \text{ mA}$ .

- (1)  $f = 1200 \text{ MHz}$
- (2)  $f = 1300 \text{ MHz}$
- (3)  $f = 1400 \text{ MHz}$

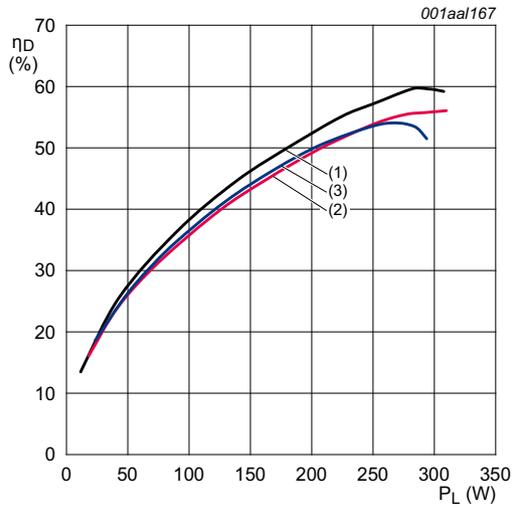
**Fig 3. Output power as a function of input power; typical values**



$V_{DS} = 50 \text{ V}$ ;  $t_p = 300 \text{ } \mu\text{s}$ ;  $\delta = 10 \%$ ;  $I_{Dq} = 100 \text{ mA}$ .

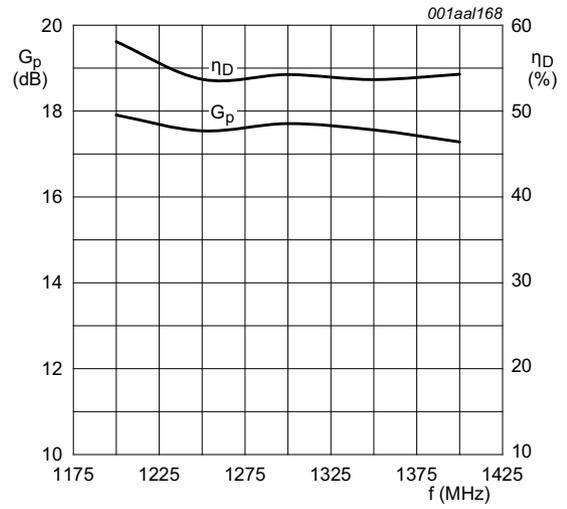
- (1)  $f = 1200 \text{ MHz}$
- (2)  $f = 1300 \text{ MHz}$
- (3)  $f = 1400 \text{ MHz}$

**Fig 4. Power gain as a function of output power; typical values**



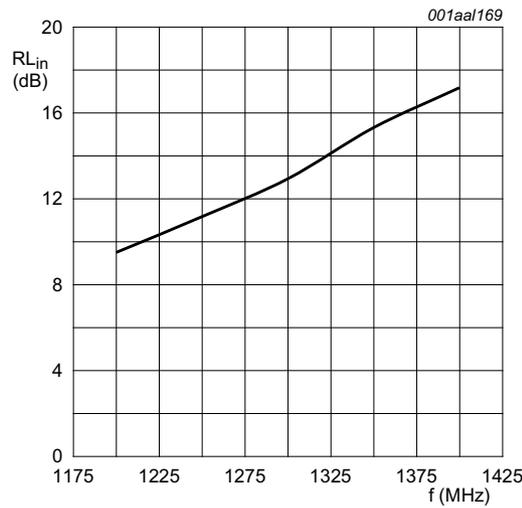
$V_{DS} = 50\text{ V}; t_p = 300\ \mu\text{s}; \delta = 10\%; I_{Dq} = 100\text{ mA}.$   
 (1)  $f = 1200\text{ MHz}$   
 (2)  $f = 1300\text{ MHz}$   
 (3)  $f = 1400\text{ MHz}$

**Fig 5. Drain efficiency as a function of output power; typical values**



$P_L = 250\text{ W}; V_{DS} = 50\text{ V}; t_p = 300\ \mu\text{s}; \delta = 10\%; I_{Dq} = 100\text{ mA}.$

**Fig 6. Power gain and drain efficiency as function of frequency; typical values**



$P_L = 250\text{ W}; V_{DS} = 50\text{ V}; t_p = 300\ \mu\text{s}; \delta = 10\%; I_{Dq} = 100\text{ mA}.$

**Fig 7. Input return loss as a function of frequency; typical value**

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

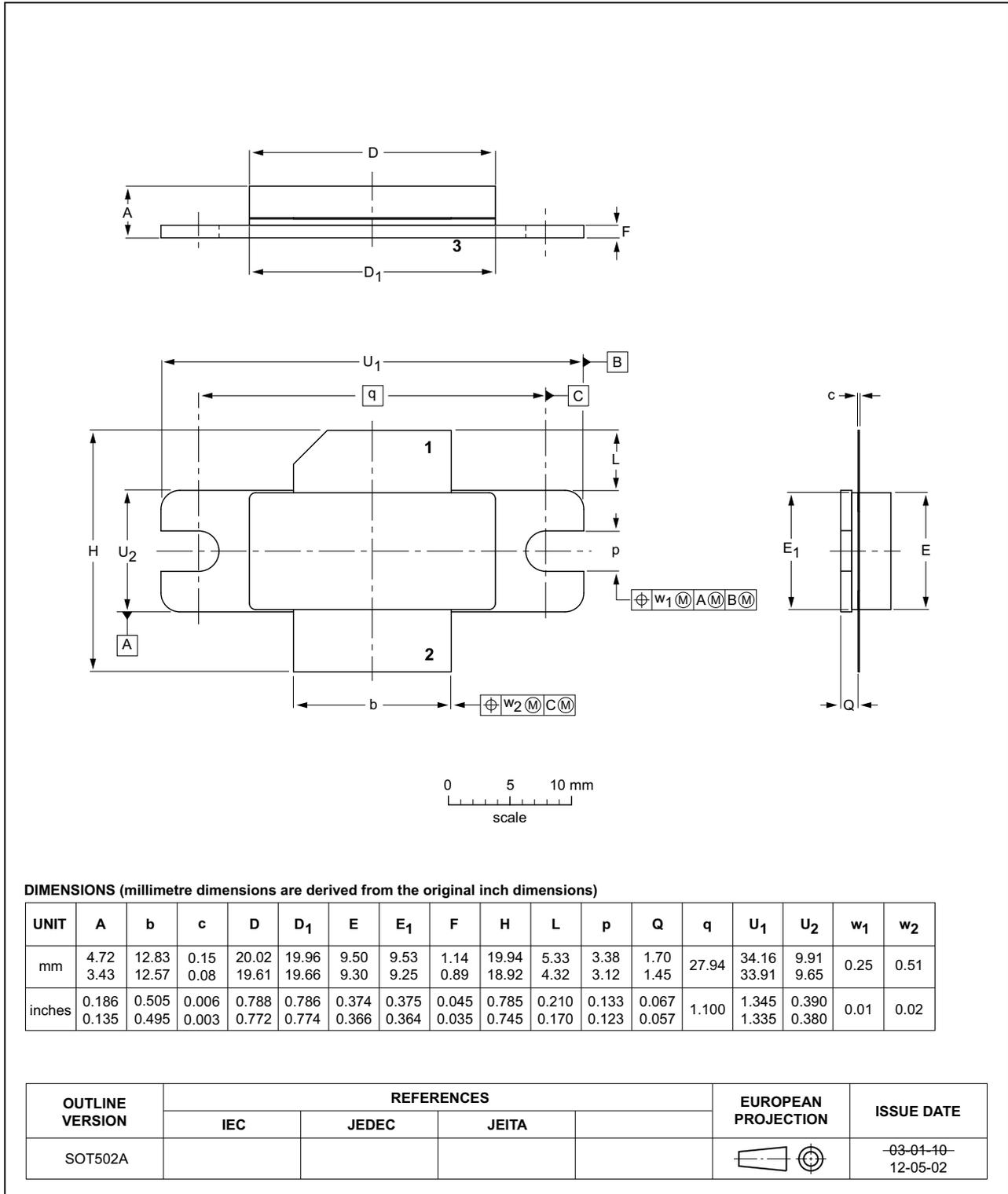


Fig 8. Package outline SOT502A

Earless flanged ceramic package; 2 leads

SOT502B

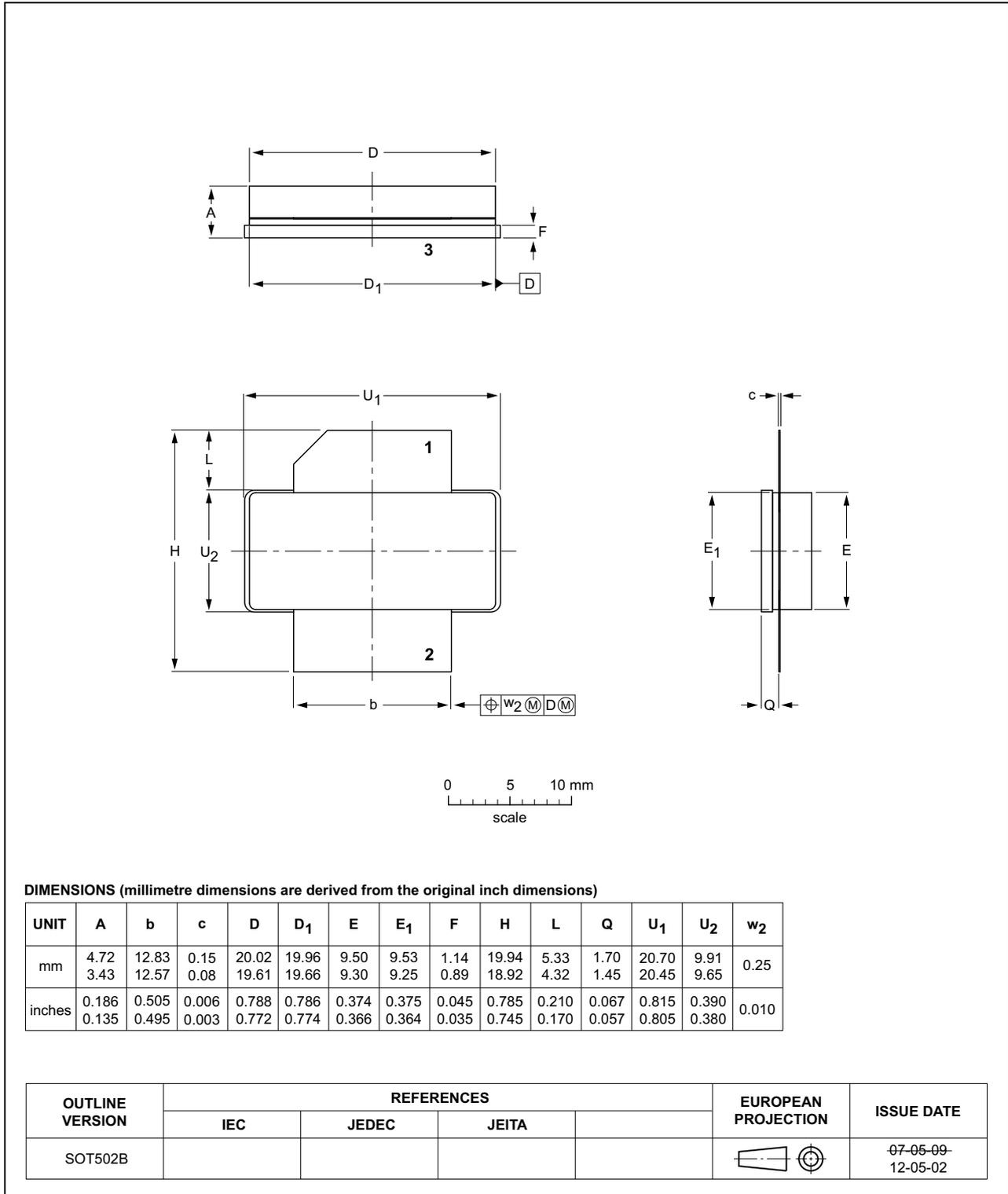


Fig 9. Package outline SOT502B

## 9. Handling information

CAUTION	
	<p>This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.</p> <p>Such precautions are described in the <i>ANSI/ESD S20.20</i>, <i>IEC/ST 61340-5</i>, <i>JESD625-A</i> or equivalent standards.</p>

## 10. Abbreviations

Table 10. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
L-band	Long wave Band
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLL8H1214L-250_1214LS-250#3	20150901	Product data sheet	-	BLL8H1214L-250_1214LS-250 #2
Modifications:	<ul style="list-style-type: none"> <li>The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
BLL8H1214L-250_1214LS-250 #2	20150113	Product data sheet	-	BLL8H1214L-250_1214LS-250 #1
BLL8H1214L-250_1214LS-250 #1	20140930	Objective data sheet	-	-

## 12. Legal information

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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