

BLP10H605

Broadband LDMOS driver transistor

Rev. 3 — 2 October 2014

Product data sheet

1. Product profile

1.1 General description

A 5 W plastic LDMOS power transistor for broadcast transmitter and ISM applications at frequencies from HF to 1400 MHz.

Table 1. Application performance

Test signal	f	V _{DS}	P _L	G _p	η _D
	(MHz)	(V)	(W)	(dB)	(%)
CW	860	50	5	22.4	59.6

1.2 Features and benefits

- Easy power control
- Integrated dual side ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 1400 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

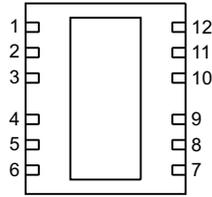
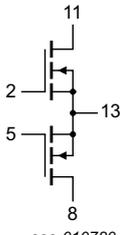
1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications



2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1, 3, 4, 6, 7, 9, 10, 12	n.c.	 <p>Transparent top view</p>	 <p>aaa-010780</p>
2	gate1		
5	gate2		
8	drain2		
11	drain1		
13	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLP10H605	HVSON12	plastic thermal enhanced very thin small outline package; no leads; 12 terminals; body 5 × 6 × 0.85 mm	SOT1352-1

4. Limiting values

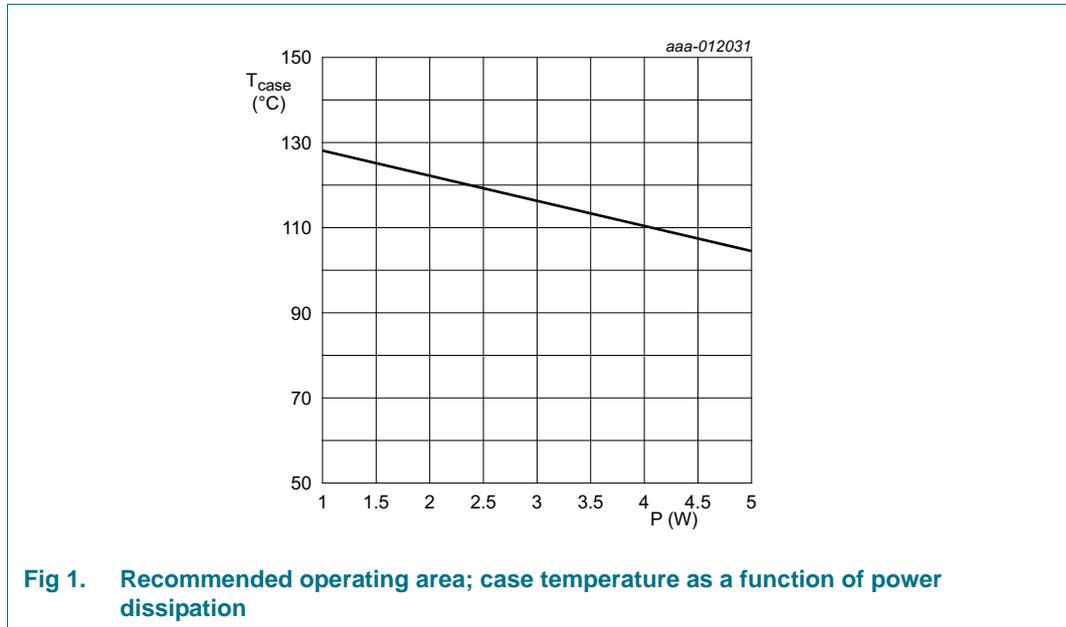
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	104	V
V_{GS}	gate-source voltage		-6	+11	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	150	°C

5. Recommended operating conditions

See application note AN11520 for more details.



6. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
R _{th(j-c)}	thermal resistance from junction to case	T _{case} = 80 °C; P _L = 5 W [1]	5.5	K/W

[1] R_{th(j-c)} is measured under RF conditions

7. Characteristics

Table 6. DC characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.06 mA	104	-	-	V
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 6 mA	1.25	1.7	2.25	V
V _{GSq}	gate-source quiescent voltage	V _{DS} = 50 V; I _D = 30 mA	1.35	1.78	2.25	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 50 V	-	-	1.4	μA
I _{DSX}	drain cut-off current	V _{GS} = V _{GS(th)} + 3.75 V; V _{DS} = 10 V	-	0.95	-	A
I _{GSS}	gate leakage current	V _{GS} = 11 V; V _{DS} = 0 V	-	-	140	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = V _{GS(th)} + 3.75 V; I _D = 210 mA	-	4580	-	mΩ

Table 7. AC characteristics
T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C _{rs}	feedback capacitance	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz	-	0.07	-	pF
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 0 V; f = 1 MHz	-	6.8	-	pF
C _{oss}	output capacitance	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz	-	2.24	-	pF

Table 8. RF characteristics
Test signal: CW pulsed; t_p = 50 μs; δ = 10 %; f = 860 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 30 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production test circuit [1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G _p	power gain	P _L = 5 W	20.2	22.4	27.4	dB
η _D	drain efficiency	P _L = 5 W	57	59.6	-	%

[1] The industrial test method is performed on special hardware to accommodate the requirements of production. The test results in this table are correlated to correspond with a performance in the application.

8. Test information

8.1 Ruggedness in class-AB operation

The BLP10H605 is capable of withstanding a load mismatch corresponding to VSWR = 35 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 30 mA; P_L = 5 W; f = 860 MHz.

8.2 Test circuit

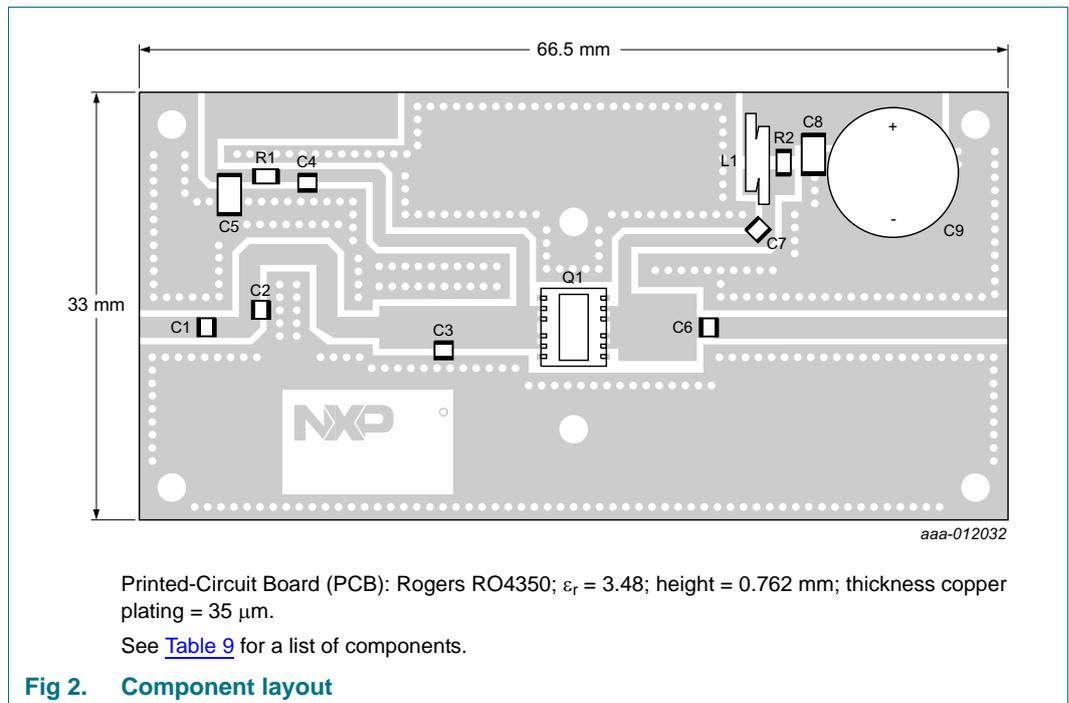
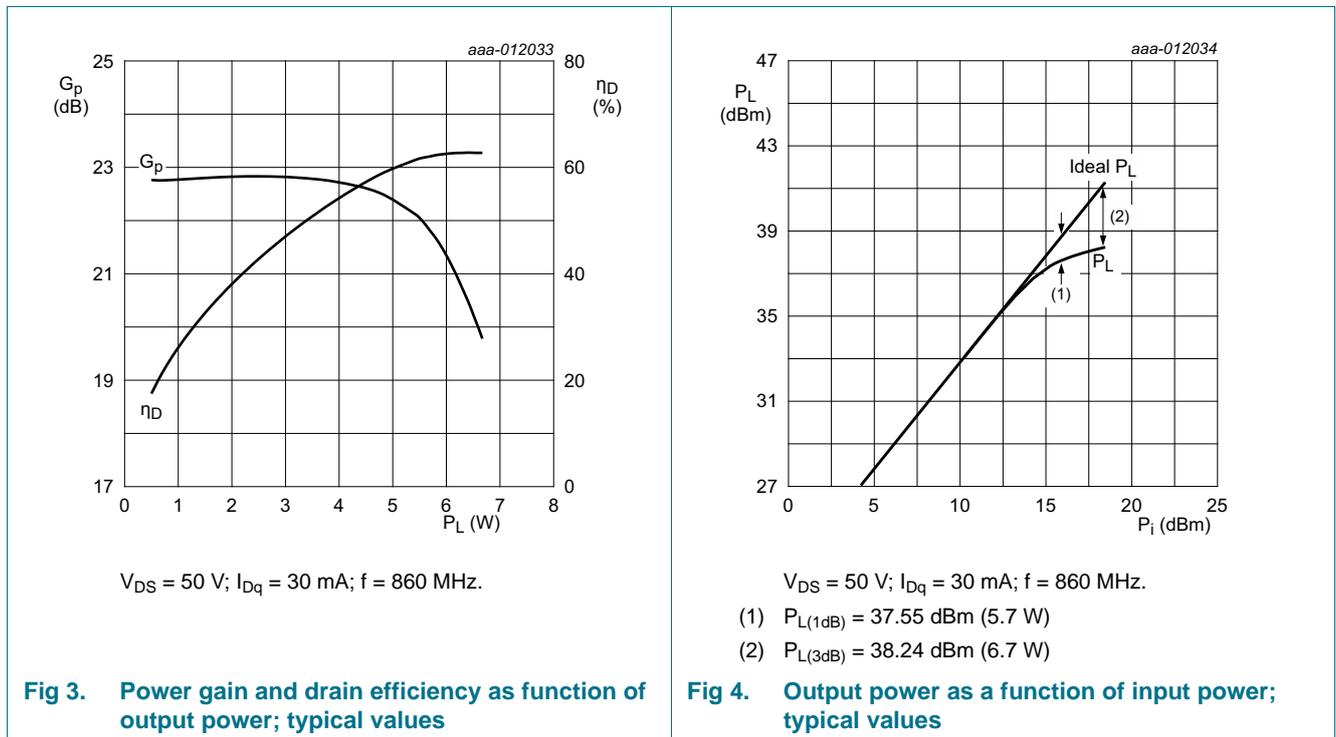


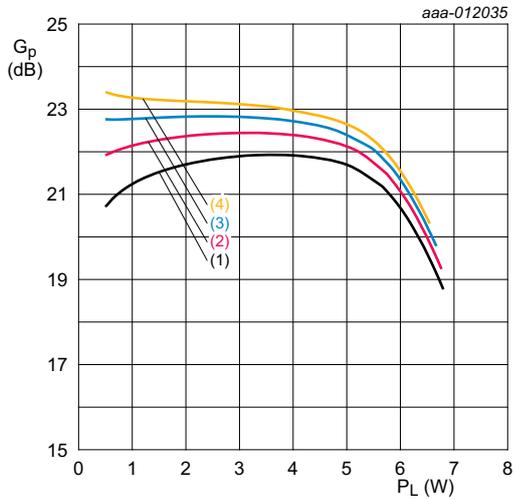
Table 9. List of components
See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1, C4, C7	multilayer ceramic chip capacitor	100 pF	[1]
C2	multilayer ceramic chip capacitor	8.2 pF	[1]
C3	multilayer ceramic chip capacitor	5.1 pF	[1]
C5	multilayer ceramic chip capacitor	1 μ F, 25 V	Murata GRM31MR71E105KA01L
C6	multilayer ceramic chip capacitor	2.2 pF	[1]
C8	multilayer ceramic chip capacitor	1 μ F, 50 V	Murata GRM32RR71H105KA01L
C9	electrolytic capacitor	220 μ F, 63 V	
L1	wire inductor, 0.8 mm copper wire	2 turn, D = 3 mm	
R1	resistor	0 Ω	SMD 0805
R2	resistor	10 Ω	SMD 0805
Q1	transistor	-	BLP10H605

[1] American Technical Ceramics type 100A or capacitor of same quality.

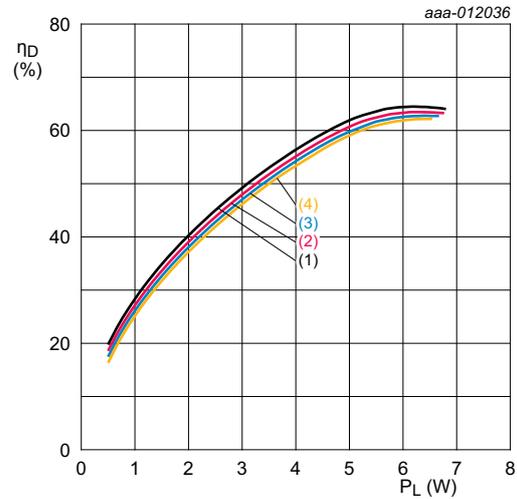
8.3 Graphical data





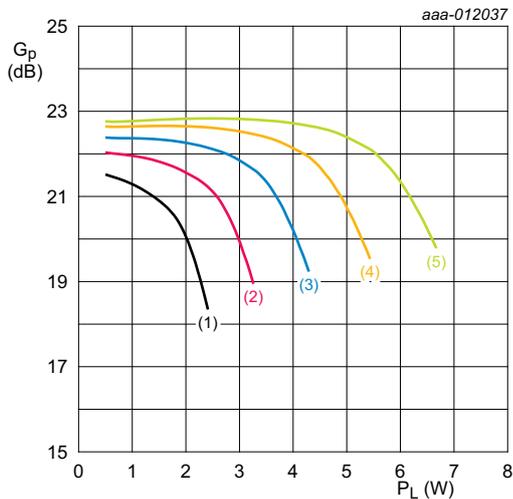
- $V_{DS} = 50\text{ V}; f = 860\text{ MHz}.$
- (1) $I_{Dq} = 10\text{ mA}$
 - (2) $I_{Dq} = 20\text{ mA}$
 - (3) $I_{Dq} = 30\text{ mA}$
 - (4) $I_{Dq} = 40\text{ mA}$

Fig 5. Power gain as a function of output power; typical values



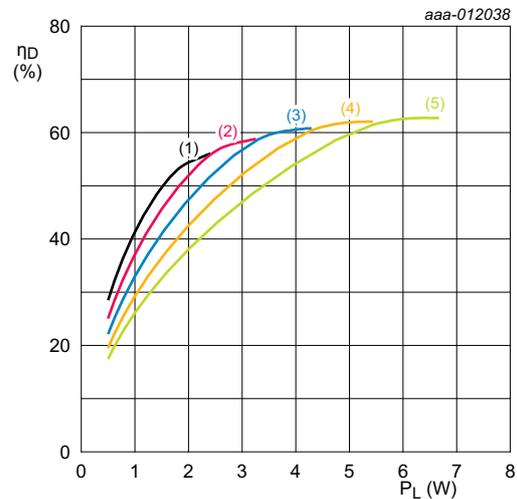
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 - (3) $I_{Dq} = 30\text{ mA}$
 - (4) $I_{Dq} = 40\text{ mA}$

Fig 6. Drain efficiency as a function of output power; typical values



- $I_{Dq} = 30\text{ mA}; f = 860\text{ MHz}.$
- (1) $V_{DS} = 30\text{ V}$
 - (2) $V_{DS} = 35\text{ V}$
 - (3) $V_{DS} = 40\text{ V}$
 - (4) $V_{DS} = 45\text{ V}$
 - (5) $V_{DS} = 50\text{ V}$

Fig 7. Power gain as a function of output power; typical values



- $I_{Dq} = 30\text{ mA}; f = 860\text{ MHz}.$
- (1) $V_{DS} = 30\text{ V}$
 - (2) $V_{DS} = 35\text{ V}$
 - (3) $V_{DS} = 40\text{ V}$
 - (4) $V_{DS} = 45\text{ V}$
 - (5) $V_{DS} = 50\text{ V}$

Fig 8. Drain efficiency as a function of output power; typical values

9. Package outline

HVSON12: plastic thermal enhanced very thin small outline package; no leads; 12 terminals; body 5 x 6 x 0.85 mm

SOT1352-1

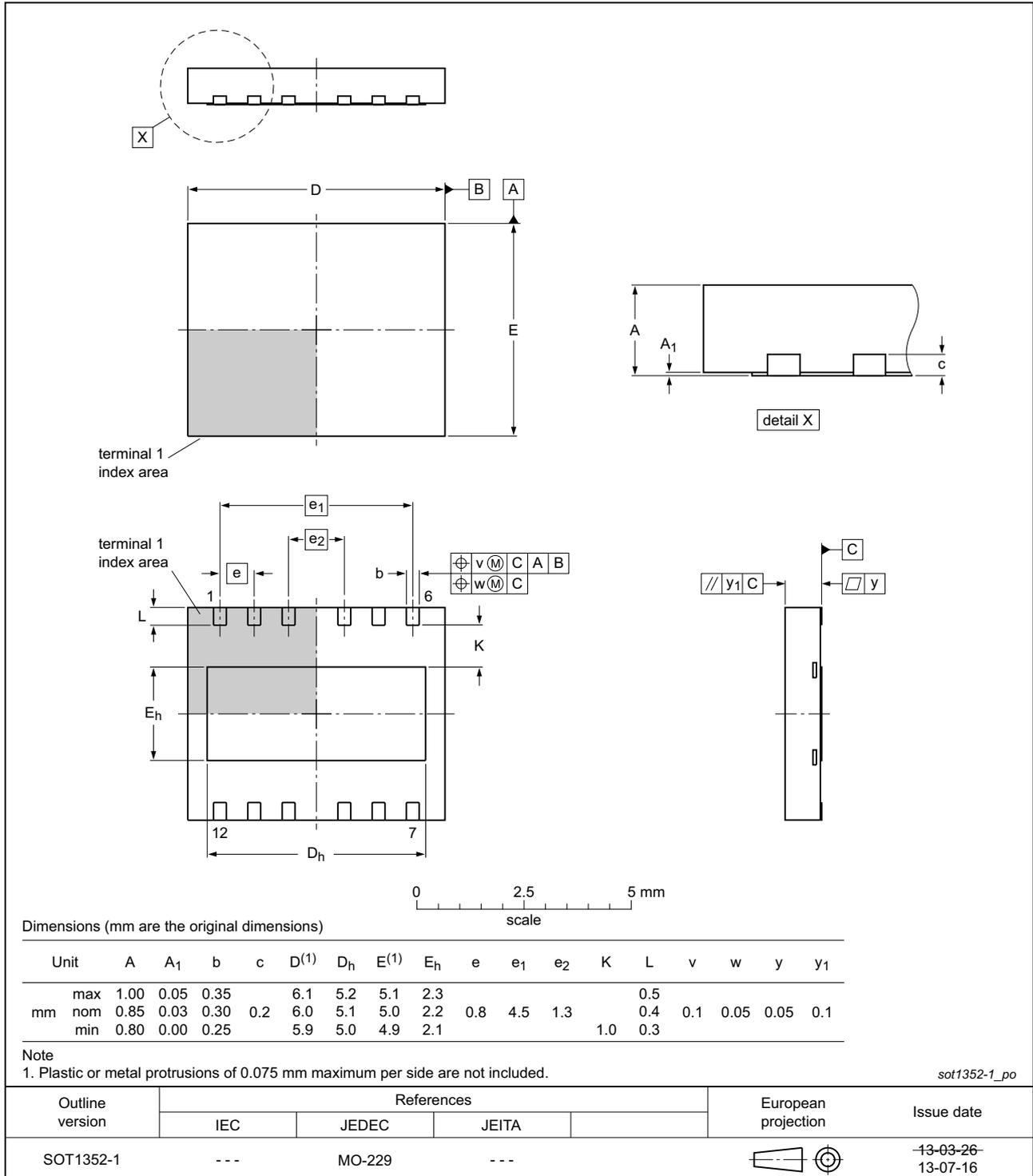


Fig 9. Package outline SOT1352-1 (HVSON12)

10. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

11. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
HF	High Frequency
ISM	Industrial, Scientific and Medical
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP10H605 v.3	20141002	Product data sheet	-	BLP10H605 v.2
Modifications	<ul style="list-style-type: none"> Table 6 on page 3: table updated Table 8 on page 4: table updated 			
BLP10H605 v.2	20140418	Objective data sheet	-	BLP10H605 v.1
BLP10H605 v.1	20140221	Objective data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 2 October 2014
 Document identifier: BLP10H605

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