

BLS7G2730L-200P; BLS7G2730LS-200P

LDMOS S-band radar power transistor

Rev. 4 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

200 W LDMOS power transistor for S-band radar applications in the frequency range from 2700 MHz to 3000 MHz.

Table 1. Typical performance
Typical RF performance at $T_{case} = 25\text{ °C}$.

| Test signal | f (GHz) | V _{DS} (V) | P _L (W) | G _p (dB) | η _D (%) | t _r (ns) | t _f (ns) |
|---|------------|------------------------|-----------------------|------------------------|-----------------------|------------------------|------------------------|
| Class-AB production test circuit | | | | | | | |
| pulsed RF [1] | 2.7 to 3.0 | 32 | 200 | 12 | 48 | 8 | 5 |
| Application circuit | | | | | | | |
| pulsed RF [2] | 2.7 to 3.0 | 32 | 220 | 12.5 | 50 | 20 | 6 |
| pulsed RF [3] | 2.9 to 3.1 | 32 | 220 | 12.5 | 50 | 20 | 6 |

[1] $t_p = 300\text{ }\mu\text{s}$; $\delta = 10\%$; $I_{Dq} = 100\text{ mA}$

[2] $t_p = 3000\text{ }\mu\text{s}$; $\delta = 20\%$; $I_{Dq} = 50\text{ mA}$

[3] $t_p = 500\text{ }\mu\text{s}$; $\delta = 20\%$; $I_{Dq} = 50\text{ mA}$

1.2 Features and benefits

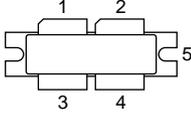
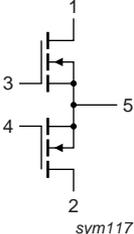
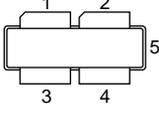
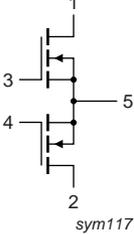
- High efficiency
- Excellent ruggedness
- Designed for broadband operation
- Excellent thermal stability
- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- S-band radar applications in the frequency range 2700 MHz to 3000 MHz

2. Pinning information

Table 2. Pinning

| Pin | Description | Simplified outline | Graphic symbol |
|-----------------------------------|-------------|---|--|
| BLS7G2730L-200P (SOT539A) | | | |
| 1 | drain1 |  |  sym117 |
| 2 | drain2 | | |
| 3 | gate1 | | |
| 4 | gate2 | | |
| 5 | source | | |
| BLS7G2730LS-200P (SOT539B) | | | |
| 1 | drain1 |  |  sym117 |
| 2 | drain2 | | |
| 3 | gate1 | | |
| 4 | gate2 | | |
| 5 | source | | |

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|------------------|---------|---|---------|
| | Name | Description | Version |
| BLS7G2730L-200P | - | flanged balanced ceramic package; 2 mounting holes; 4 leads | SOT539A |
| BLS7G2730LS-200P | - | earless flanged balanced ceramic package; 4 leads | SOT539B |

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Min | Max | Unit |
|-----------|----------------------|-------|------|------|
| V_{DS} | drain-source voltage | - | 65 | V |
| V_{GS} | gate-source voltage | -0.5 | +13 | V |
| T_{stg} | storage temperature | -65 | +150 | °C |
| T_j | junction temperature | [1] - | 225 | °C |

[1] Continuous use at maximum temperature will affect the reliability.

5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|---------------|---|--|------|------|
| $Z_{th(j-c)}$ | transient thermal impedance from junction to case | $T_{case} = 85\text{ °C}; P_L = 200\text{ W}$ | | |
| | | $t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$ | 0.13 | K/W |
| | | $t_p = 3000\text{ }\mu\text{s}; \delta = 20\text{ }\%$ | 0.19 | K/W |

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|----------------------------------|---|-----|------|-----|---------------|
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $V_{GS} = 0\text{ V}; I_D = 1.2\text{ mA}$ | 65 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $V_{DS} = 10\text{ V}; I_D = 120\text{ mA}$ | 1.5 | 1.9 | 2.3 | V |
| I_{DSS} | drain leakage current | $V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$ | - | - | 2.8 | μA |
| I_{DSX} | drain cut-off current | $V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$ | - | 22.5 | - | A |
| I_{GSS} | gate leakage current | $V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$ | - | - | 280 | nA |
| g_{fs} | forward transconductance | $V_{DS} = 10\text{ V}; I_D = 0.12\text{ A}$ | - | 1 | - | S |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 4.2\text{ A}$ | - | 0.13 | - | Ω |

Table 7. RF characteristics

Test signal: pulsed RF; $t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$; RF performance at $V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; T_{case} = 25\text{ °C};$ unless otherwise specified, in a class-AB production test circuit.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|-------------------|----------------------|-----|-----|------|------|
| G_p | power gain | $P_L = 200\text{ W}$ | 9.8 | 12 | - | dB |
| RL_{in} | input return loss | $P_L = 200\text{ W}$ | - | -10 | -6 | dB |
| η_D | drain efficiency | $P_L = 200\text{ W}$ | 43 | 48 | - | % |
| $P_{droop(pulse)}$ | pulse droop power | $P_L = 200\text{ W}$ | - | 0 | 0.25 | dB |
| t_r | rise time | $P_L = 200\text{ W}$ | - | 8 | 50 | ns |
| t_f | fall time | $P_L = 200\text{ W}$ | - | 5 | 50 | ns |

7. Test information

7.1 Ruggedness in class-AB operation

The BLS7G2730L-200P and BLS7G2730LS-200P are capable of withstanding a load mismatch corresponding to $VSWR = 10 : 1$ through all phases under following conditions: $V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; P_L = 200\text{ W}; f = 2700\text{ MHz}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$

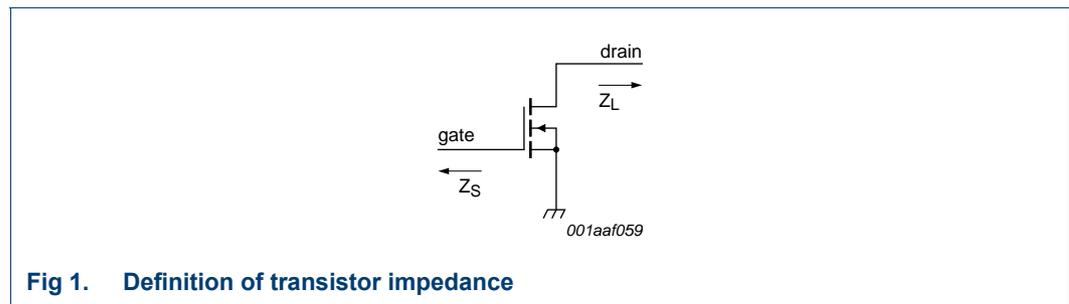
7.2 Impedance information

Table 8. Typical impedance

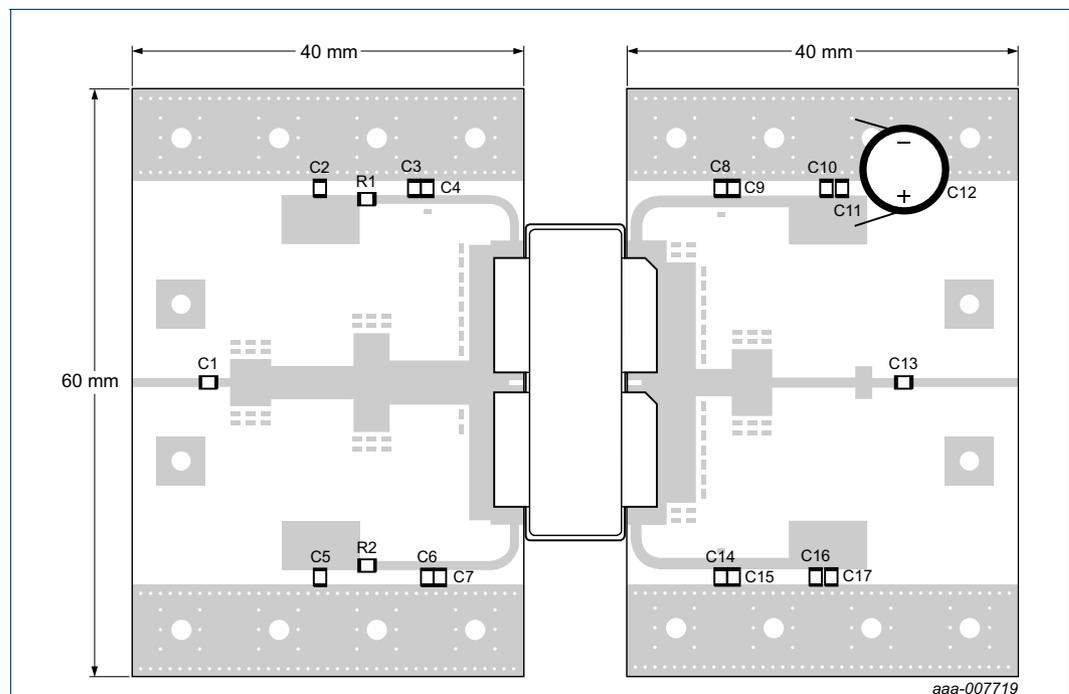
Measured load-pull data half device; $V_{DS} = 32\text{ V}$; $I_{Dq} = 100\text{ mA}$.

| f (MHz) | Z_S [1] (Ω) | Z_L [1] (Ω) |
|---------|------------------------|------------------------|
| 2700 | 2.0 – j5.8 | 3.7 – j6.4 |
| 2800 | 1.6 – j5.9 | 3.8 – j6.9 |
| 2900 | 2.6 – j6.2 | 3.8 – j6.9 |
| 3000 | 3.4 – j6.0 | 3.7 – j6.4 |

[1] Z_S and Z_L defined in Figure 1.



7.3 Production test circuit



Printed-Circuit Board (PCB): Arlon TC600 with a thickness of 0.64 mm.

See Table 9 for a list of components.

Fig 2. Component layout for a class-AB production test circuit

Table 9. List of components test circuit

See [Figure 2](#).

| Component | Description | Value | Remarks |
|--------------------------|-----------------------------------|---------------|-------------|
| C1, C3, C6, C9, C13, C15 | multilayer ceramic chip capacitor | 18 pF | [1] ATC600F |
| C2, C5, C10, C16 | multilayer ceramic chip capacitor | 1 μF | [2] |
| C4, C7, C8, C14 | multilayer ceramic chip capacitor | 12 pF | [1] ATC600F |
| C11, C17 | multilayer ceramic chip capacitor | 10 μF | [2] |
| C12 | electrolytic capacitor | 2200 μF, 63 V | |
| R1, R2 | chip resistor | 9.1 Ω | [3] |

[1] American Technical Ceramics type 600F or capacitor of same quality.

[2] Murata or capacitor of same quality.

[3] Vishay Dale or capacitor of same quality.

7.4 Application circuit

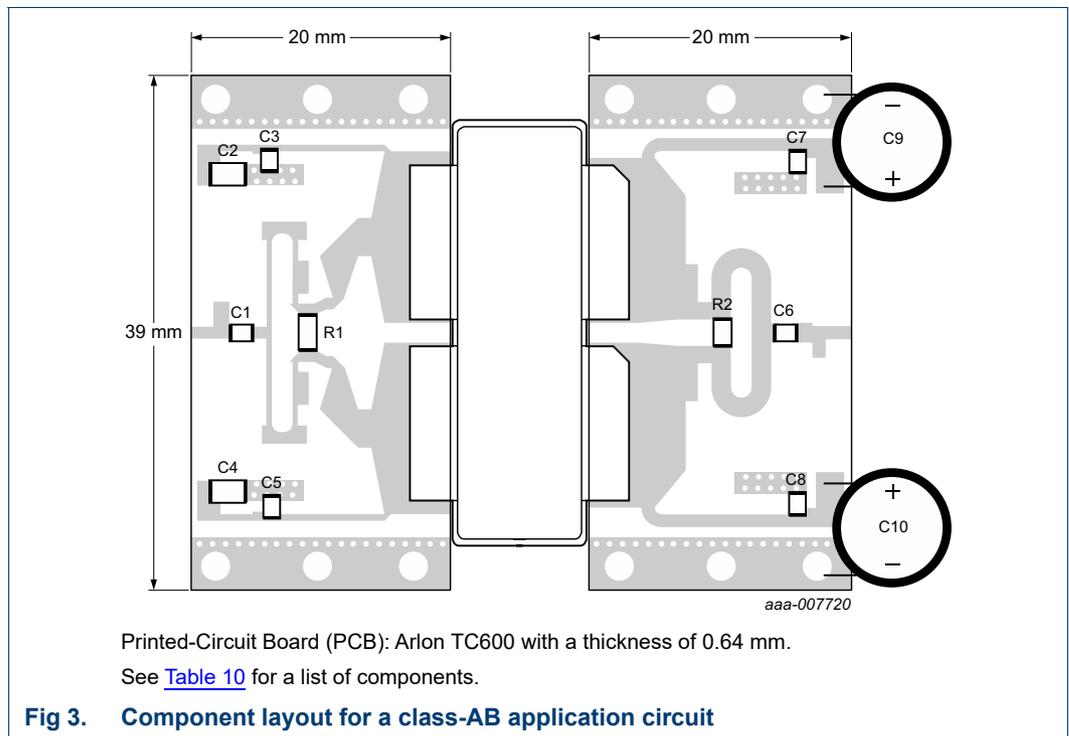


Table 10. List of components application circuit

See [Figure 2](#).

| Component | Description | Value | Remarks |
|------------------------|-----------------------------------|---------------|-------------|
| C1, C3, C5, C6, C7, C8 | multilayer ceramic chip capacitor | 12 pF | [1] ATC600F |
| C2, C4 | multilayer ceramic chip capacitor | 1 μF | [2] |
| C9, C10 | electrolytic capacitor | 2200 μF, 50 V | |
| R1, R2 | chip resistor | 50 Ω | [3] |

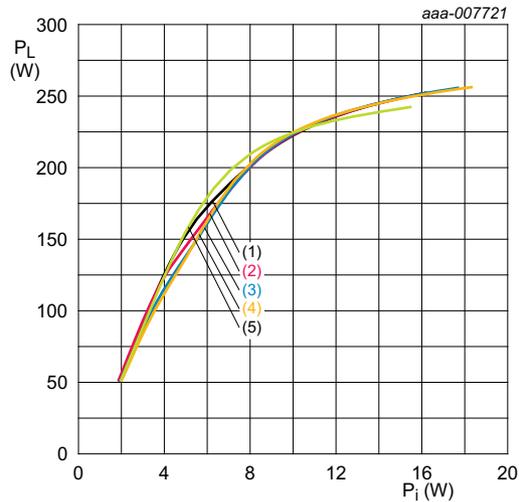
[1] American Technical Ceramics type 600F or capacitor of same quality.

[2] Murata or capacitor of same quality.

[3] Vishay Dale or capacitor of same quality.

7.5 Graphical data

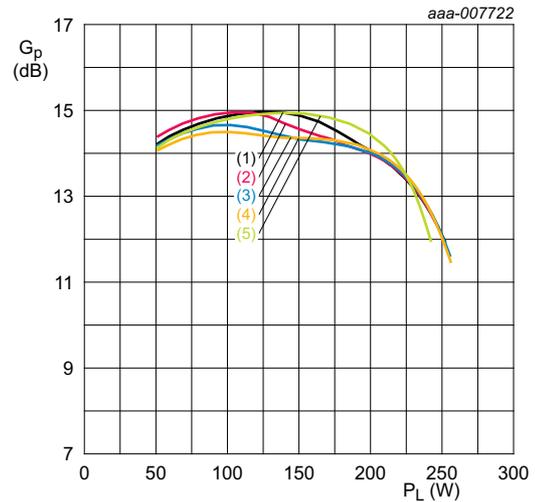
7.5.1 Test circuit



$V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$.

- (1) $f = 2700\text{ MHz}$
- (2) $f = 2800\text{ MHz}$
- (3) $f = 2850\text{ MHz}$
- (4) $f = 2900\text{ MHz}$
- (5) $f = 3000\text{ MHz}$

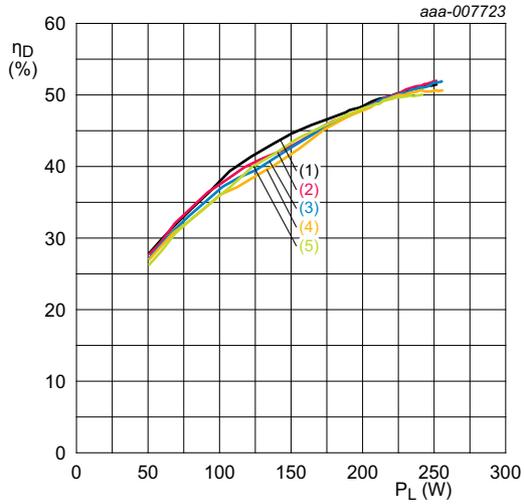
Fig 4. Output power as a function of input power; typical values



$V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$.

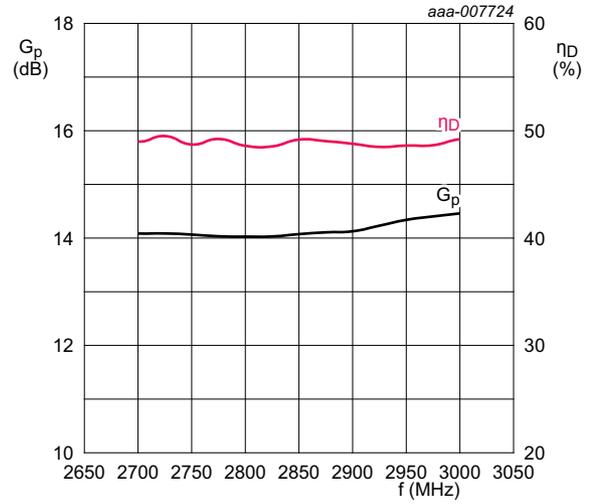
- (1) $f = 2700\text{ MHz}$
- (2) $f = 2800\text{ MHz}$
- (3) $f = 2850\text{ MHz}$
- (4) $f = 2900\text{ MHz}$
- (5) $f = 3000\text{ MHz}$

Fig 5. Power gain as a function of output power; typical values



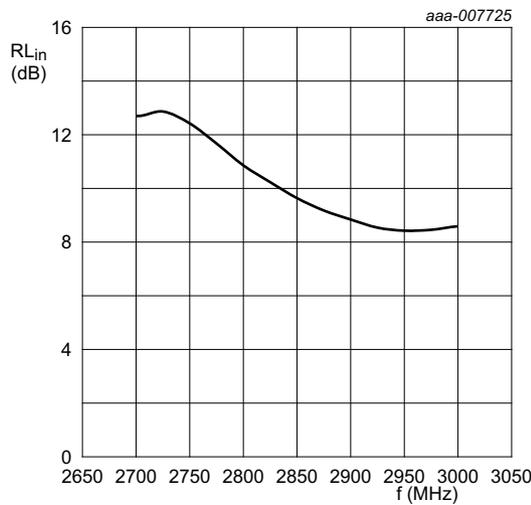
$V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$.
 (1) $f = 2700\text{ MHz}$
 (2) $f = 2800\text{ MHz}$
 (3) $f = 2850\text{ MHz}$
 (4) $f = 2900\text{ MHz}$
 (5) $f = 3000\text{ MHz}$

Fig 6. Drain efficiency as a function of output power; typical values



$V_{DS} = 32\text{ V}; P_L = 200\text{ W}; I_{Dq} = 100\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$.

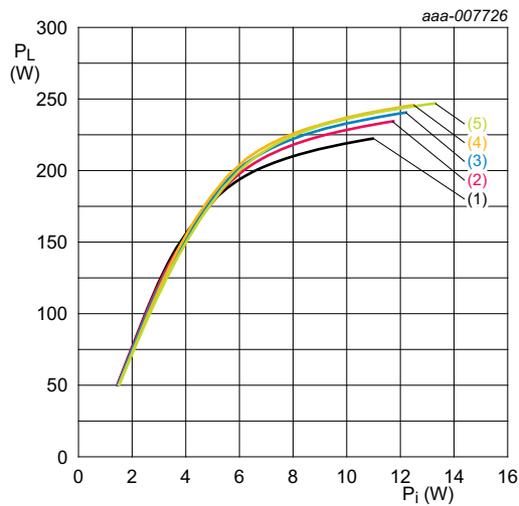
Fig 7. Power gain and drain efficiency as function of frequency; typical values



$V_{DS} = 32\text{ V}; P_L = 200\text{ W}; I_{Dq} = 100\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$.

Fig 8. Input return loss as a function of frequency; typical values

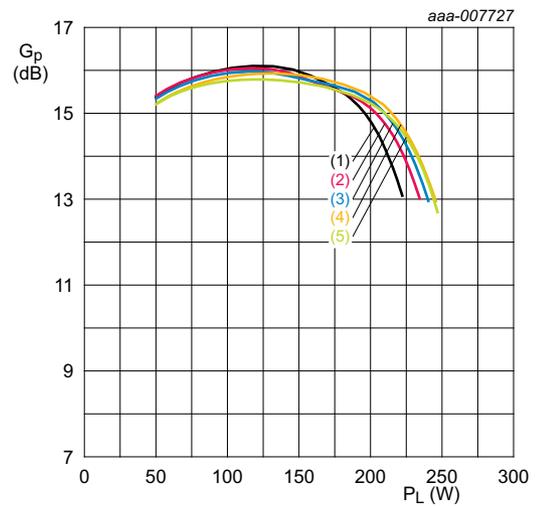
7.5.2 Application circuit



$V_{DS} = 32\text{ V}; I_{Dq} = 50\text{ mA}; t_p = 3000\ \mu\text{s}; \delta = 20\ \%$.

- (1) $f = 2700\text{ MHz}$
- (2) $f = 2800\text{ MHz}$
- (3) $f = 2850\text{ MHz}$
- (4) $f = 2900\text{ MHz}$
- (5) $f = 3000\text{ MHz}$

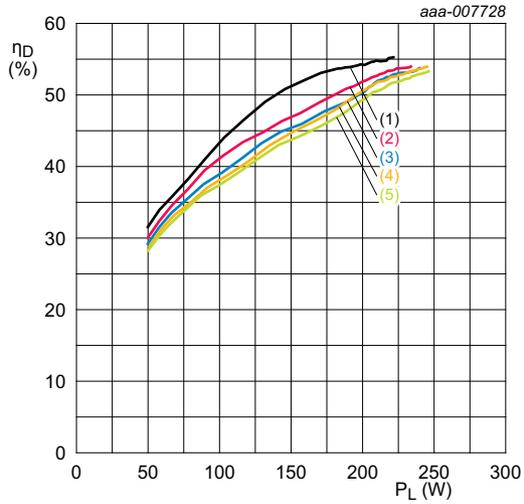
Fig 9. Output power as a function of input power; typical values



$V_{DS} = 32\text{ V}; I_{Dq} = 50\text{ mA}; t_p = 3000\ \mu\text{s}; \delta = 20\ \%$.

- (1) $f = 2700\text{ MHz}$
- (2) $f = 2800\text{ MHz}$
- (3) $f = 2850\text{ MHz}$
- (4) $f = 2900\text{ MHz}$
- (5) $f = 3000\text{ MHz}$

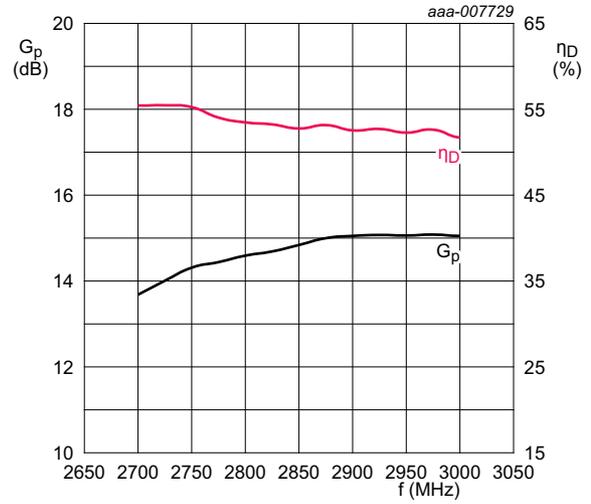
Fig 10. Power gain as a function of output power; typical values



$V_{DS} = 32\text{ V}$; $I_{Dq} = 50\text{ mA}$; $t_p = 3000\text{ }\mu\text{s}$; $\delta = 20\text{ }\%$.

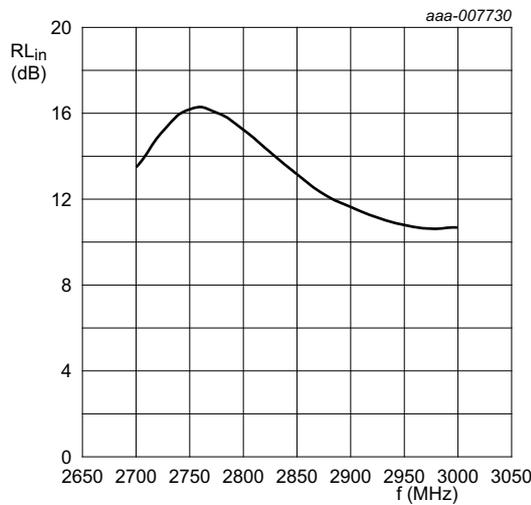
- (1) $f = 2700\text{ MHz}$
- (2) $f = 2800\text{ MHz}$
- (3) $f = 2850\text{ MHz}$
- (4) $f = 2900\text{ MHz}$
- (5) $f = 3000\text{ MHz}$

Fig 11. Drain efficiency as a function of output power; typical values



$V_{DS} = 32\text{ V}$; $P_L = 220\text{ W}$; $I_{Dq} = 50\text{ mA}$; $t_p = 3000\text{ }\mu\text{s}$; $\delta = 20\text{ }\%$.

Fig 12. Power gain and drain efficiency as function of frequency; typical values



$V_{DS} = 32\text{ V}$; $P_L = 220\text{ W}$; $I_{Dq} = 50\text{ mA}$; $t_p = 3000\text{ }\mu\text{s}$; $\delta = 20\text{ }\%$.

Fig 13. Input return loss as a function of frequency; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A

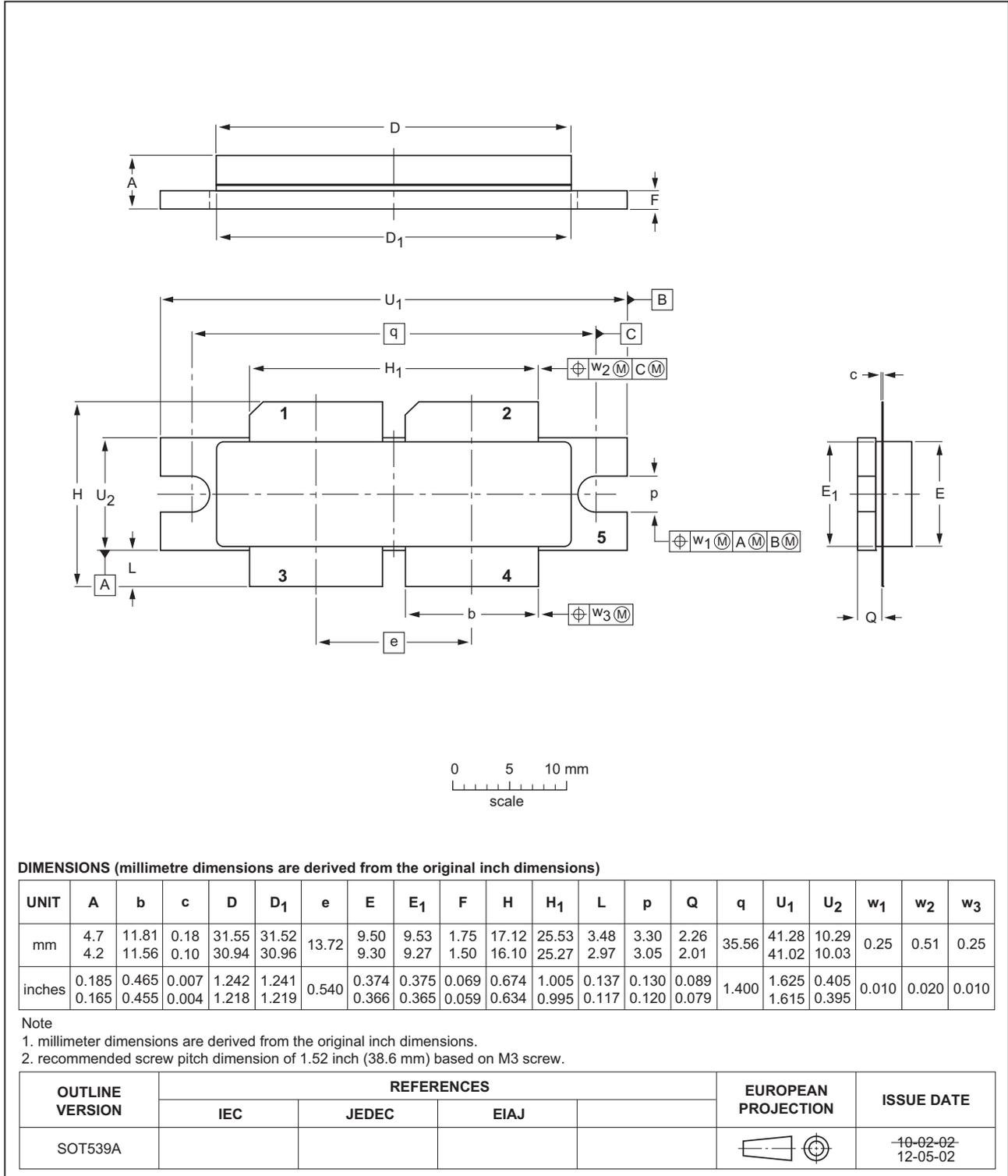


Fig 14. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads

SOT539B

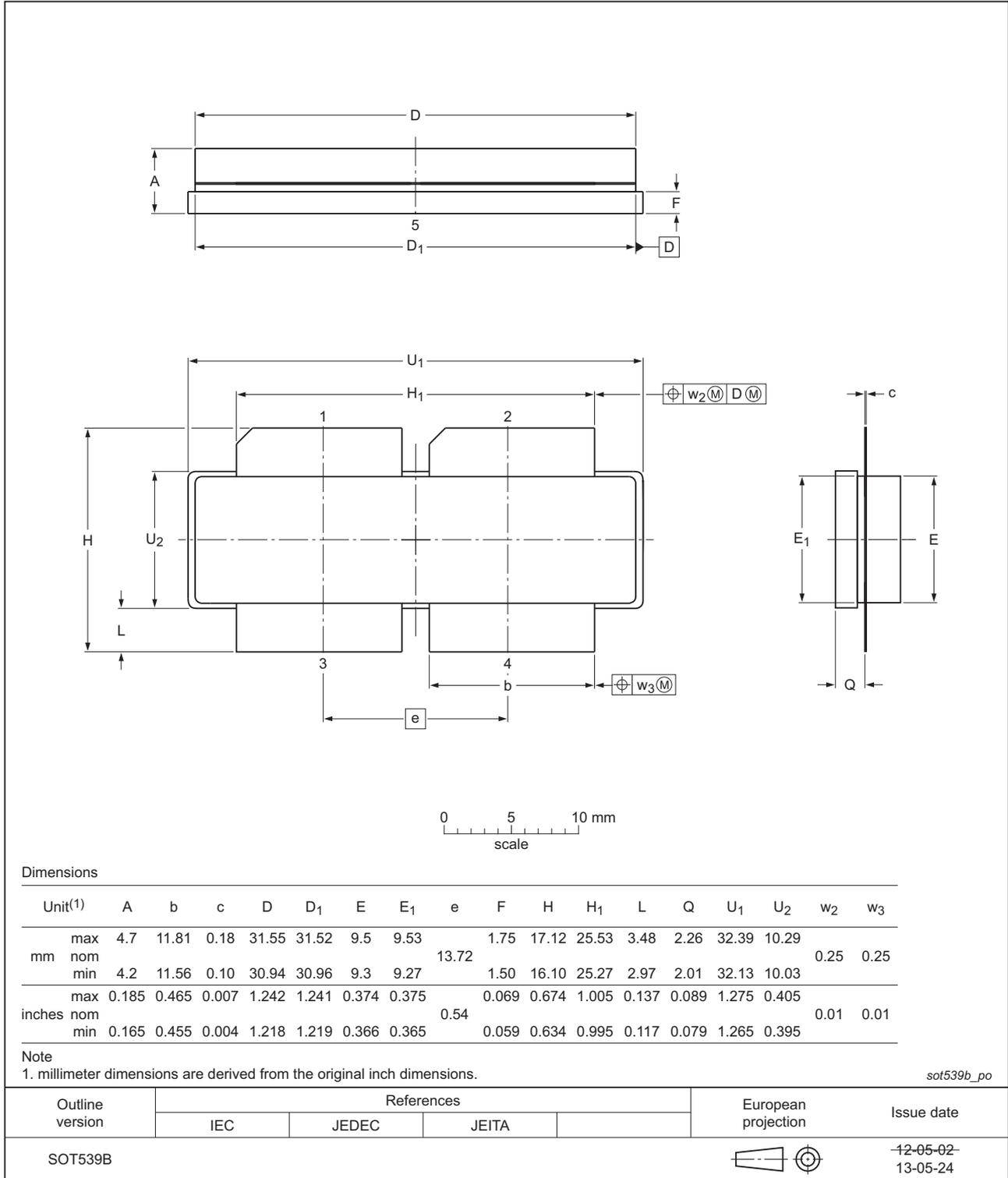


Fig 15. Package outline SOT539B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|--|
| ESD | ElectroStatic Discharge |
| LDMOS | Laterally Diffused Metal-Oxide Semiconductor |
| S-band | Short wave band |
| VSWR | Voltage Standing-Wave Ratio |

11. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------------------|--|----------------------|---------------|-----------------------------|
| BLS7G2730S-200P_LS-200P#4 | 20150901 | Product data sheet | | BLS7G2730S-200P_LS-200P v.3 |
| Modifications: | <ul style="list-style-type: none"> The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. Legal texts have been adapted to the new company name where appropriate. | | | |
| BLS7G2730S-200P_LS-200P v.3 | 20130712 | Product data sheet | - | BLS7G2730S-200P_LS-200P v.2 |
| BLS7G2730S-200P_LS-200P v.2 | 20130603 | Product data sheet | - | BLS7G2730S-200P_LS-200P v.1 |
| BLS7G2730S-200P_LS-200P v.1 | 20130129 | Objective data sheet | - | - |

12. Legal information

12.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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<http://www.ampleon.com/sales>

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Date of release: 1 September 2015

Document identifier: BLS7G2730L-200P_LS-200P#4

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