

## MOSFET

Metal Oxide Semiconductor Field Effect Transistor

## OptiMOS™ Power-Transistor, 100V

OptiMOS™ 3 Power Transistor  
BSZ160N10NS3

## Data Sheet

Rev. 2.1  
Final

**OptiMOS™3 Power-Transistor**
**Features**

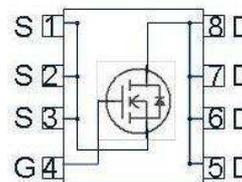
- Ideal for high frequency switching
- Optimized technology for DC/DC converters
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Halogen-free according to IEC61249-2-21



Type	Package	Marking
BSZ160N10NS3 G	PG-TSDSON-8	160N10N

**Product Summary**

$V_{DS}$	100	V
$R_{DS(on),max}$	16	m $\Omega$
$I_D$	40	A

**PG-TSDSON-8**

**Maximum ratings, at  $T_A=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$	40	A
		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$	28	
		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=60\text{ K/W}^{2)}$	8	
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	160	
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	$I_D=20\text{ A}, R_{GS}=25\text{ }\Omega$	80	mJ
Gate source voltage	$V_{GS}$		$\pm 20$	V

<sup>1)</sup> J-STD20 and JESD22

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

**Maximum ratings**, at  $T_A=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	$P_{\text{tot}}$	$T_C=25\text{ °C}$	63	W
		$T_A=25\text{ °C}$ , $R_{\text{thJA}}=60\text{ K/W}^2)$	2.1	
Operating and storage temperature	$T_j, T_{\text{stg}}$		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - case	$R_{\text{thJC}}$		-	-	2.1	K/W
Device on PCB	$R_{\text{thJA}}$	minimal footprint	-	-	62	
		6 cm <sup>2</sup> cooling area <sup>2)</sup>	-	-	60	

**Electrical characteristics**, at  $T_j=25\text{ °C}$ , unless otherwise specified

**Static characteristics**

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}$ , $I_{\text{D}}=1\text{ mA}$	100	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}$ , $I_{\text{D}}=33\text{ }\mu\text{A}$	2	2.8	3.5	
Zero gate voltage drain current	$I_{\text{DSS}}$	$V_{\text{DS}}=100\text{ V}$ , $V_{\text{GS}}=0\text{ V}$ , $T_j=25\text{ °C}$	-	0.1	1	$\mu\text{A}$
		$V_{\text{DS}}=100\text{ V}$ , $V_{\text{GS}}=0\text{ V}$ , $T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	$I_{\text{GSS}}$	$V_{\text{GS}}=20\text{ V}$ , $V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=10\text{ V}$ , $I_{\text{D}}=20\text{ A}$	-	14	16	m $\Omega$
		$V_{\text{GS}}=6\text{ V}$ , $I_{\text{D}}=10\text{ A}$	-	18	33	
Gate resistance	$R_{\text{G}}$		-	1.4	-	$\Omega$
Transconductance	$g_{\text{fs}}$	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}$ , $I_{\text{D}}=20\text{ A}$	16	33	-	S

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=50\text{ V}, f=1\text{ MHz}$	-	1300	1700	pF
Output capacitance	$C_{oss}$		-	240	320	
Reverse transfer capacitance	$C_{rss}$		-	11	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V}, I_D=10\text{ A}, R_{G,ext}=1.6\ \Omega$	-	13.0	-	ns
Rise time	$t_r$		-	10.0	-	
Turn-off delay time	$t_{d(off)}$		-	22.0	-	
Fall time	$t_f$		-	5.0	-	

**Gate Charge Characteristics<sup>5)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=50\text{ V}, I_D=10\text{ A}, V_{GS}=0\text{ to }10\text{ V}$	-	5.7	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	3.8	-	
Gate to drain charge	$Q_{gd}$		-	3.4	-	
Switching charge	$Q_{sw}$		-	5.3	-	
Gate charge total	$Q_g$		-	19	25	
Gate plateau voltage	$V_{plateau}$		-	4.2	-	V
Output charge	$Q_{oss}$	$V_{DD}=40\text{ V}, V_{GS}=0\text{ V}$	-	25	33	nC

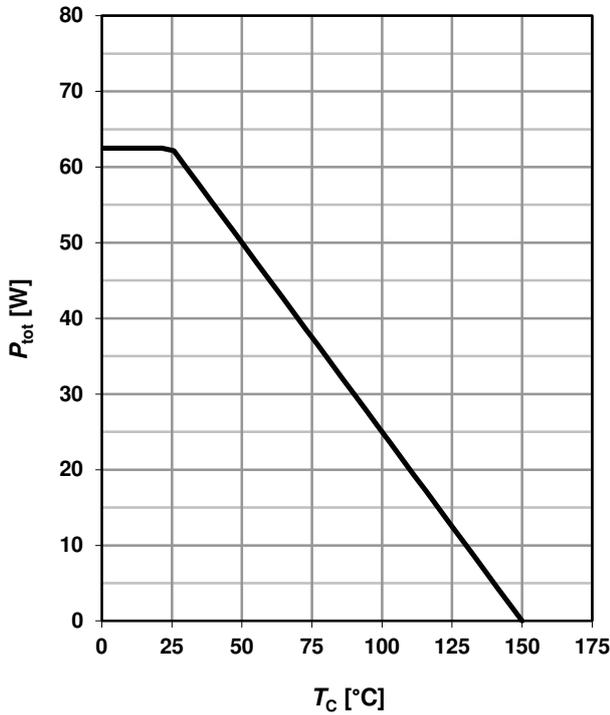
**Reverse Diode**

Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	40	A
Diode pulse current	$I_{S,pulse}$		-	-	160	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=20\text{ A}, T_j=25\text{ }^\circ\text{C}$	-	0.9	1.2	V
Reverse recovery time	$t_{rr}$	$V_R=50\text{ V}, I_F=10\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$	-	73	-	ns
Reverse recovery charge	$Q_{rr}$		-	52	-	nC

<sup>5)</sup> See figure 16 for gate charge parameter definition

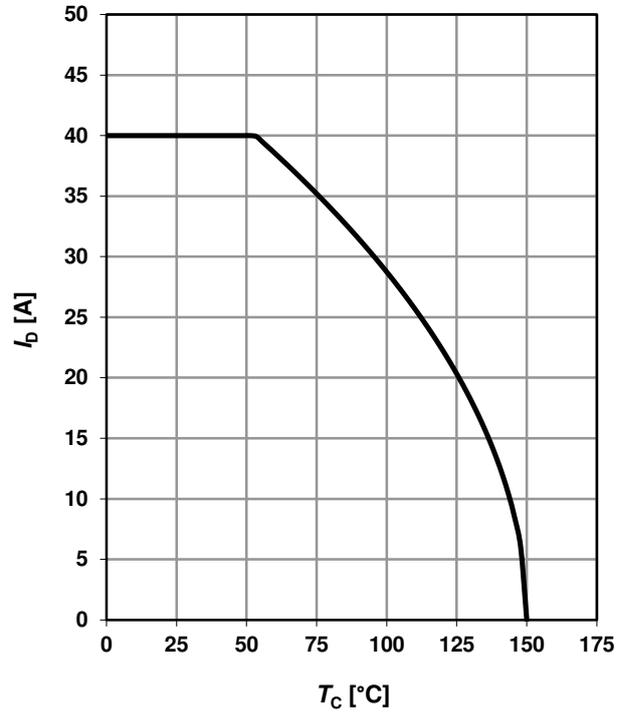
**1 Power dissipation**

$P_{tot}=f(T_C)$



**2 Drain current**

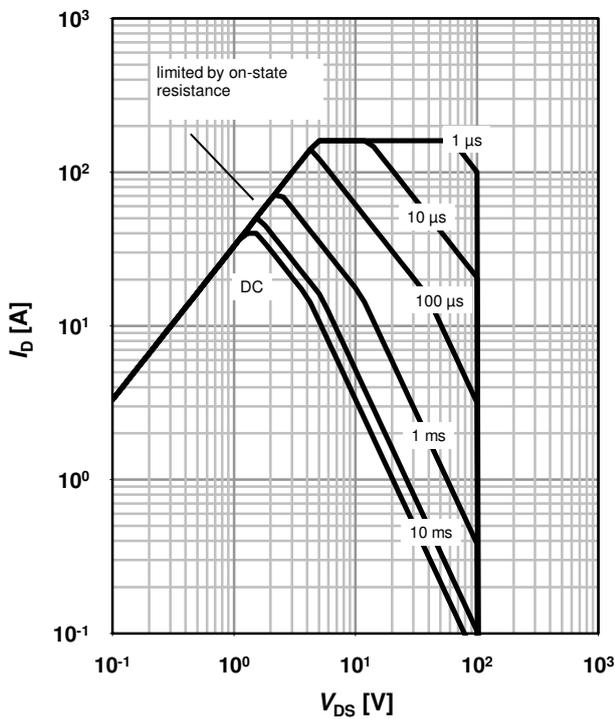
$I_D=f(T_C); V_{GS} \geq 10\text{ V}$



**3 Safe operating area**

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

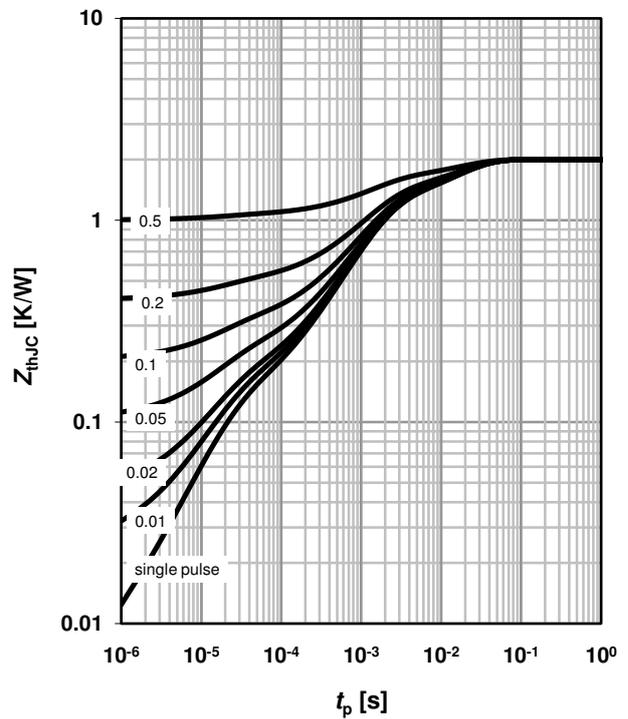
parameter:  $t_p$



**4 Max. transient thermal impedance**

$Z_{thJC}=f(t_p)$

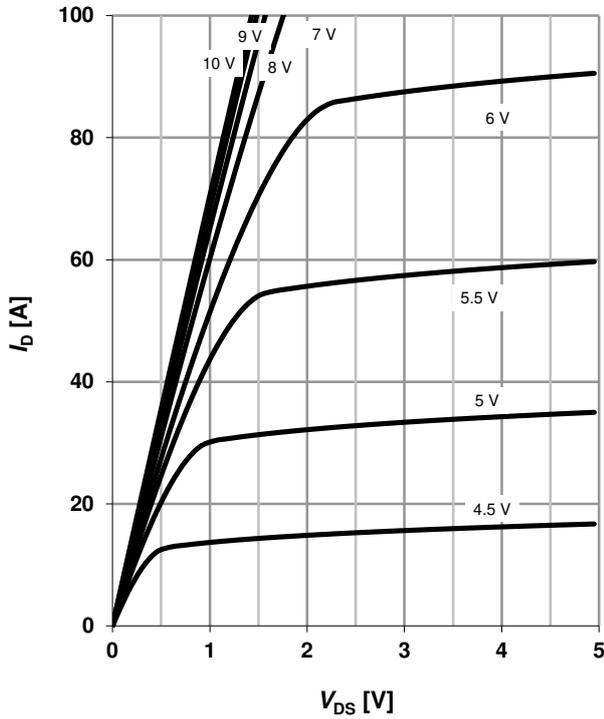
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

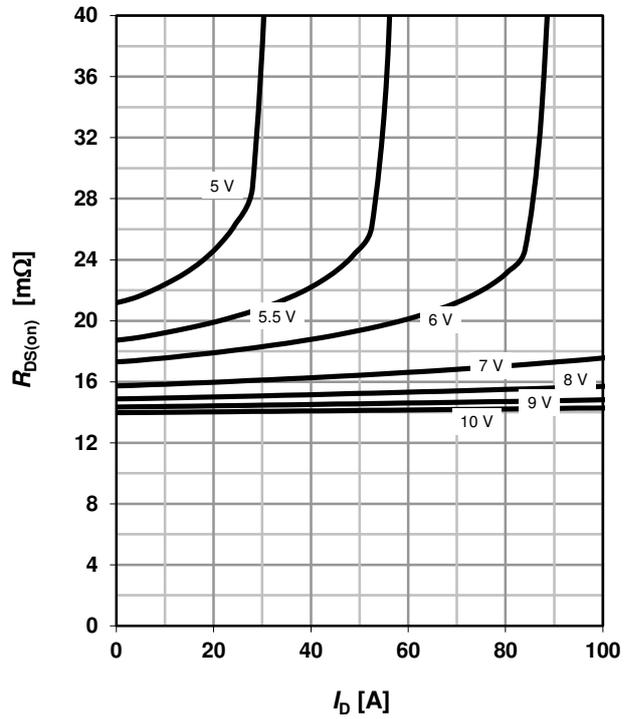
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

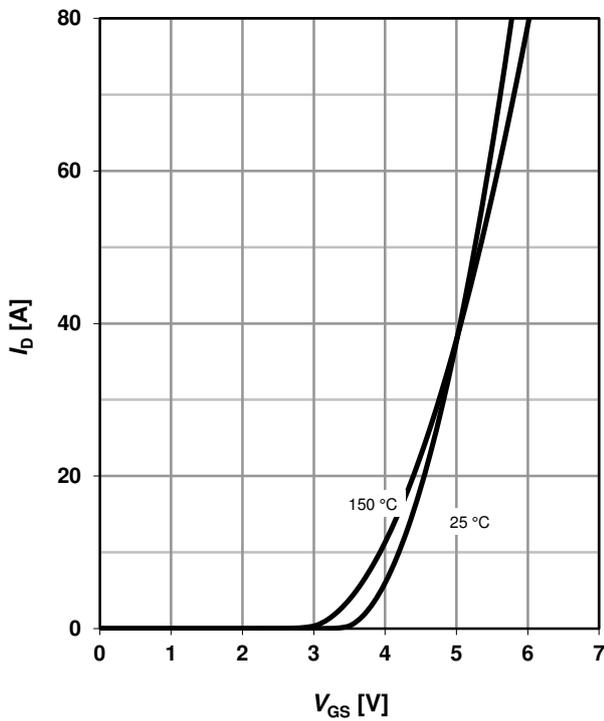
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

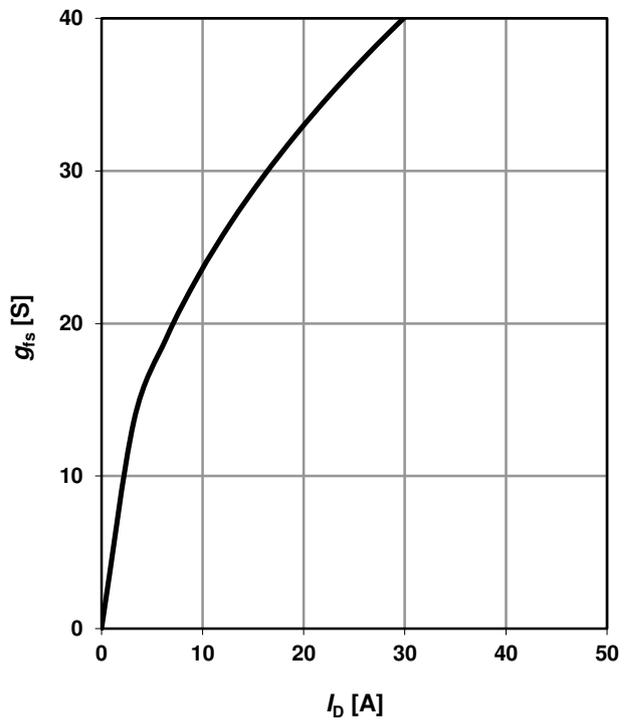
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter:  $T_j$



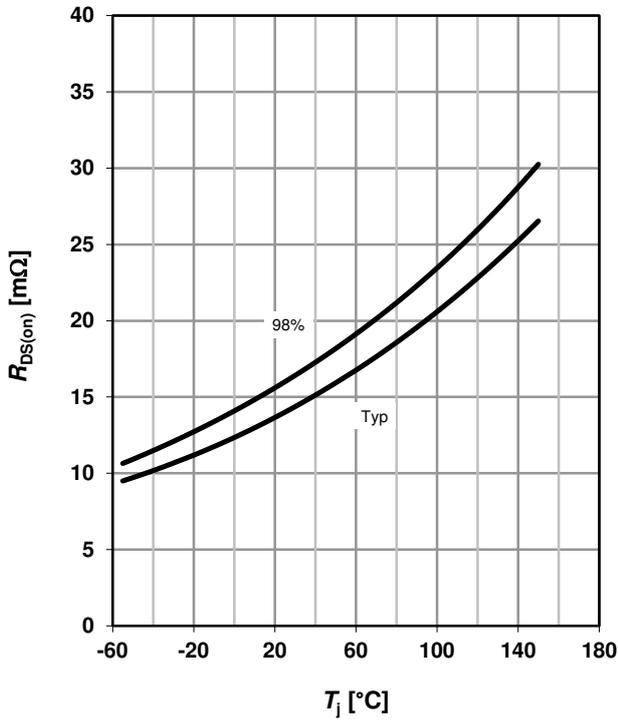
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ °C}$



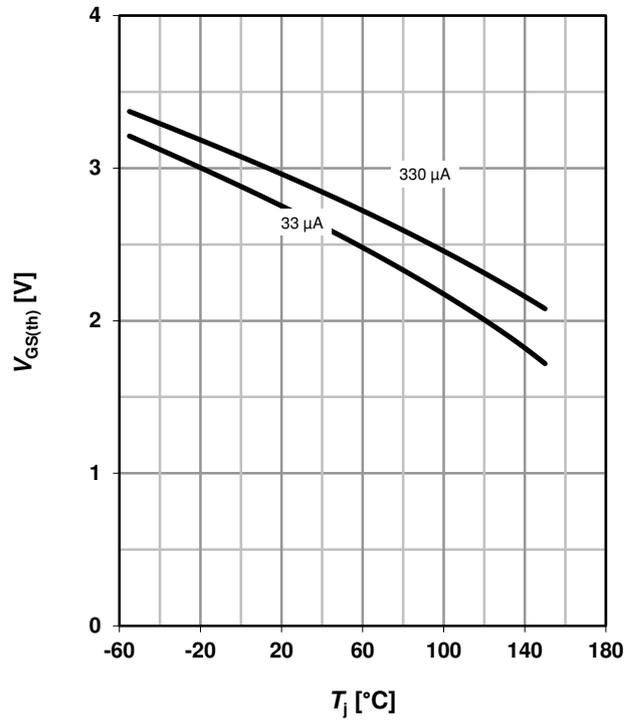
**9 Drain-source on-state resistance**

$R_{DS(on)}=f(T_j); I_D=20\text{ A}; V_{GS}=10\text{ V}$



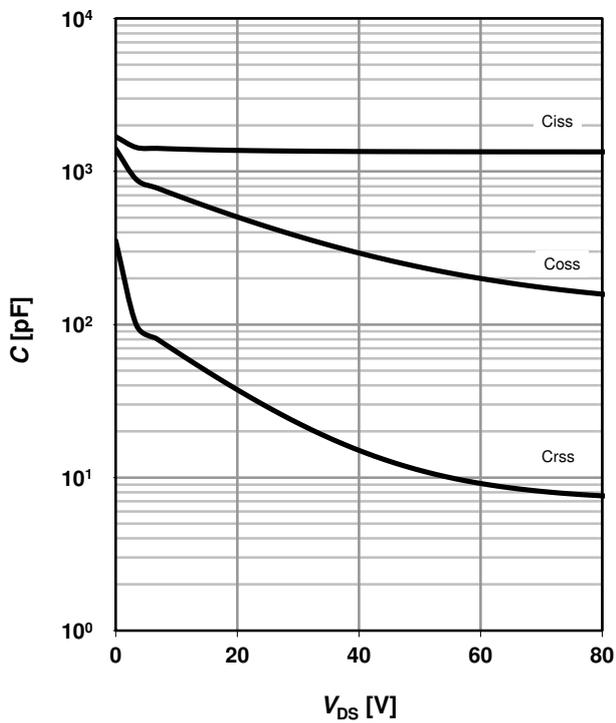
**10 Typ. gate threshold voltage**

$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}$



**11 Typ. capacitances**

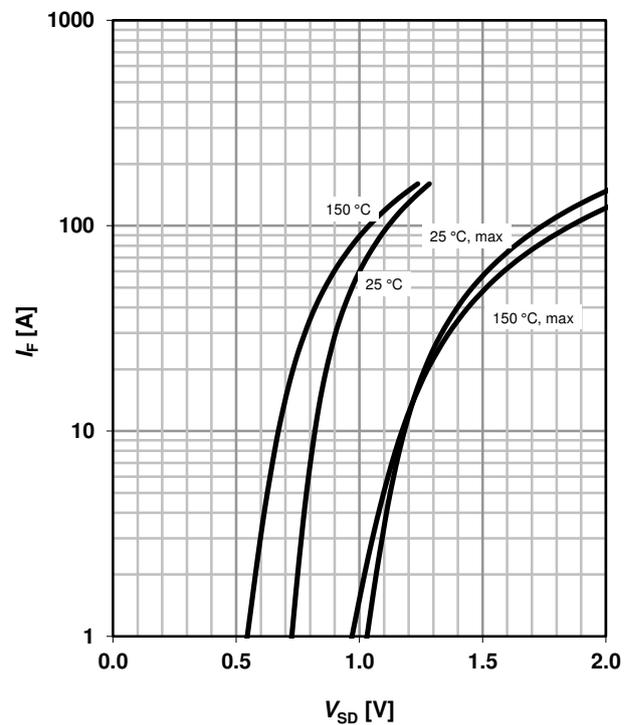
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$



**12 Forward characteristics of reverse diode**

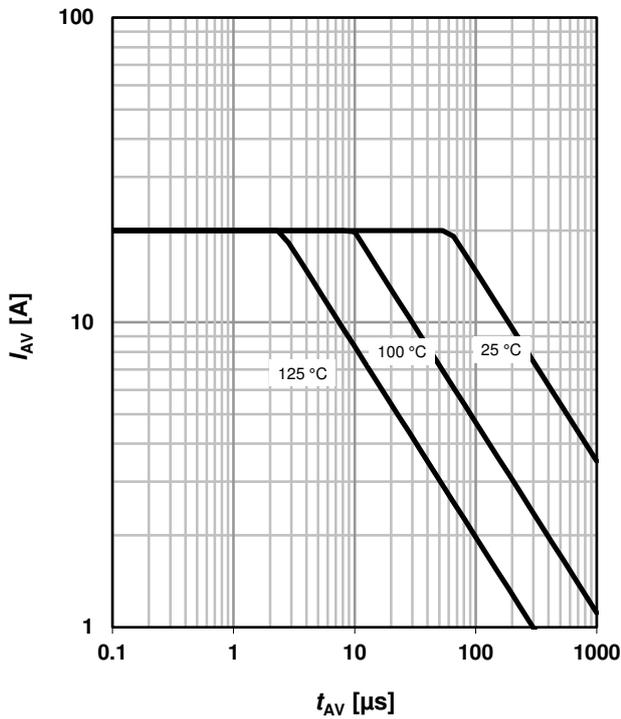
$I_F=f(V_{SD})$

parameter:  $T_j$

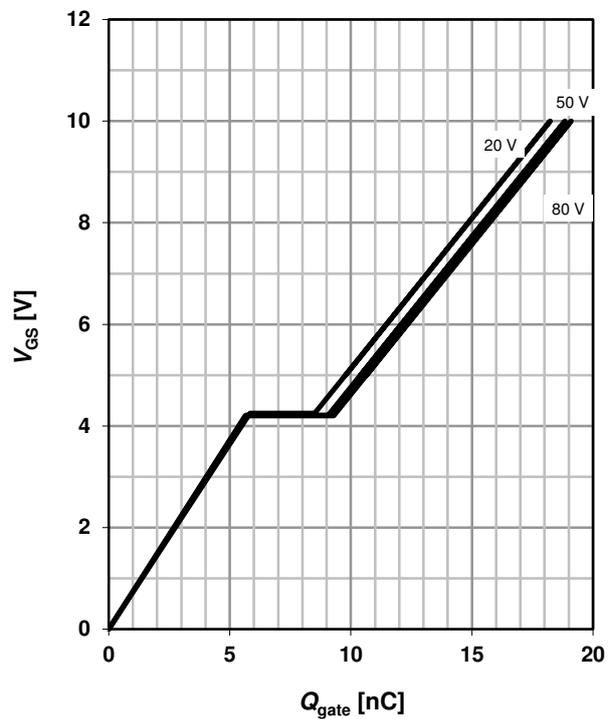


**13 Avalanche characteristics**

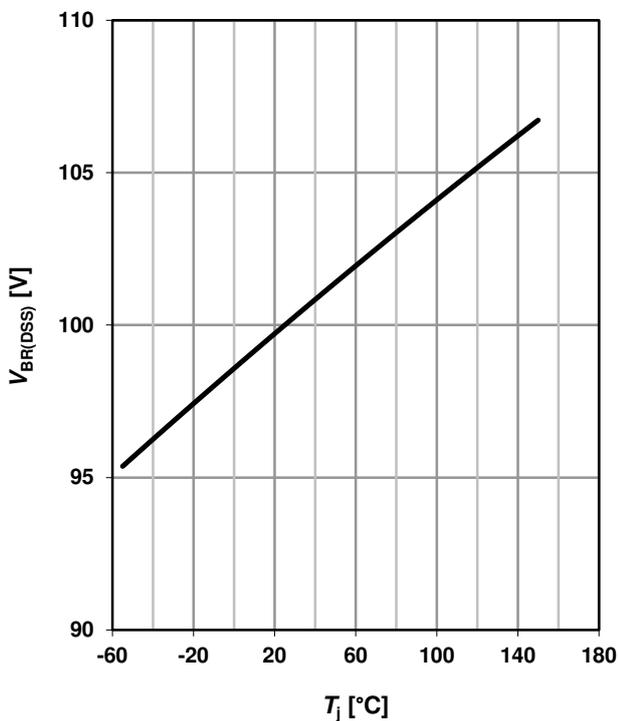
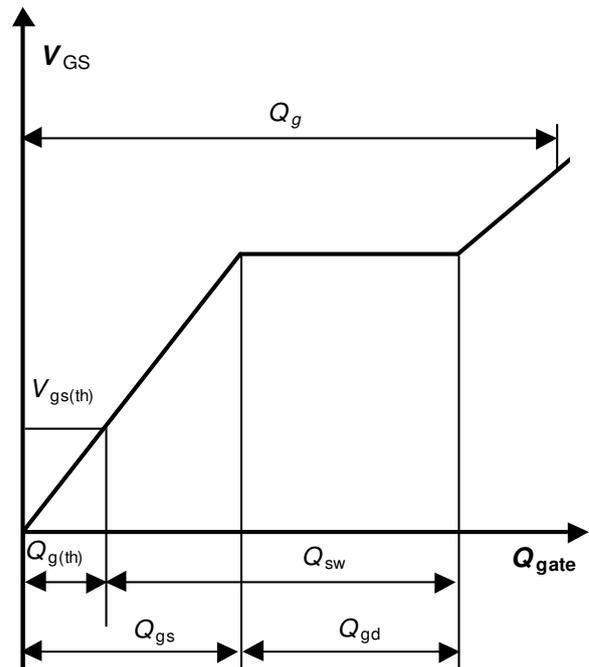
$$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$$

 parameter:  $T_{j(\text{start})}$ 

**14 Typ. gate charge**

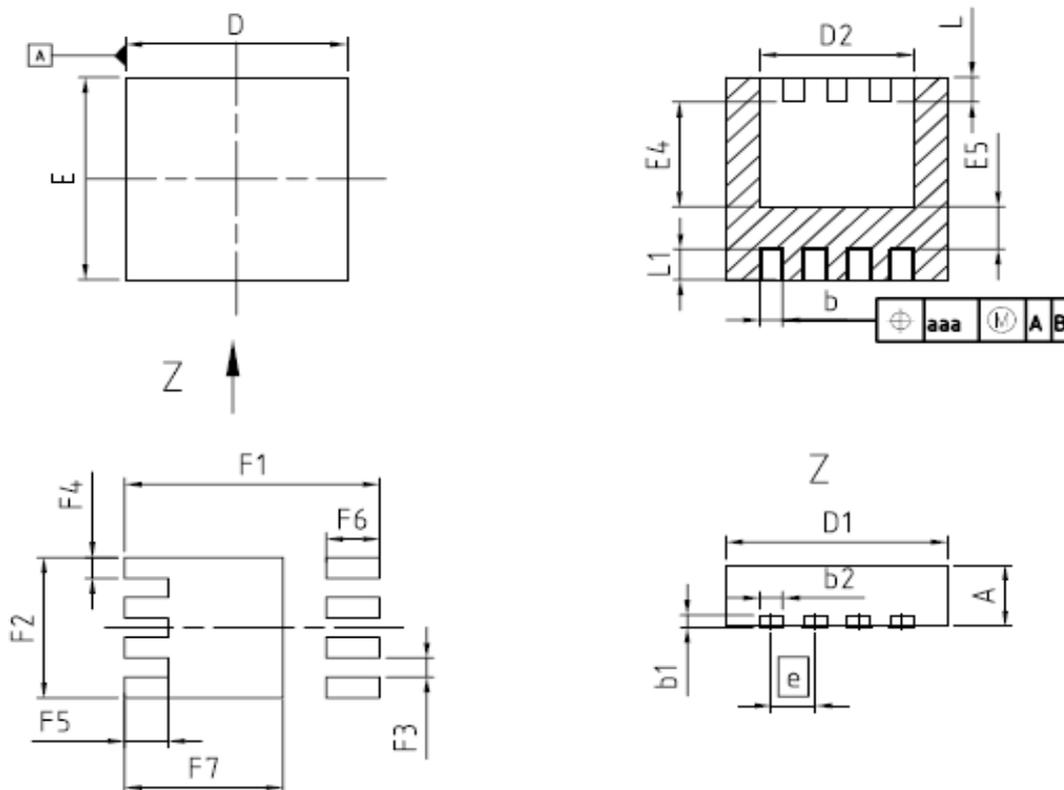
$$V_{GS}=f(Q_{\text{gate}}); I_D=10 \text{ A pulsed}$$

 parameter:  $V_{DD}$ 

**15 Drain-source breakdown voltage**

$$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$$


**16 Gate charge waveforms**


Package Outline: PG-TSDSON-8



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0,90	1,10	0,035	0,043
b	0,24	0,44	0,009	0,017
b1	0,10	0,30	0,004	0,012
b2	0,20	0,44	0,008	0,017
D=D1	3,20	3,40	0,126	0,134
D2	2,15	2,45	0,085	0,096
E	3,20	3,40	0,126	0,134
E4	1,60	1,81	0,063	0,071
E5	0,59	0,86	0,023	0,034
e	0,65		0,026	
N	8		8	
L	0,30	0,56	0,012	0,022
L1	0,33	0,60	0,013	0,024
aaa	0,25		0,010	
F1	3,80		0,150	
F2	2,29		0,090	
F3	0,31		0,012	
F4	0,34		0,013	
F5	0,65		0,026	
F6	0,80		0,031	
F7	2,36		0,093	

DOCUMENT NO.  
Z8B00131645

SCALE

EUROPEAN PROJECTION

ISSUE DATE  
17-09-2008

REVISION  
02

**Footprint**  
Dimensions in mm

## Revision History

BSZ160N10NS3

**Revision: 2015-10-05, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2015-10-05	Update Id condition for Vgs(th) and Tj to Ta condition for "Maximum ratings"

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### Published by

**Infineon Technologies AG**

**81726 München, Germany**

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