BT152-800R

SCR

Rev. 2 — 9 June 2011 Product data sheet

1. Product profile

1.1 General description

Planar passivated Silicon Controlled Rectifier in a SOT78 (TO-220AB) plastic package intended for use in applications requiring very high inrush current capability and high thermal cycling performance.

1.2 Features and benefits

- High thermal cycling performance
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Very high current surge capability

1.3 Applications

- Ignition circuits
- Motor control
- Protection circuits e.g. SMPS inrush current
- Voltage regulation

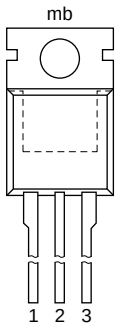
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
V_{RRM}	repetitive peak reverse voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; see Figure 4; see Figure 5	-	-	200	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms	-	-	220	A
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq$ 103 °C; see Figure 3	-	-	13	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; see Figure 1; see Figure 2	-	-	20	A
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; see Figure 7	-	3	32	mA

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode		
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

SOT78 (TO-220AB)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT152-800R	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
V_{RRM}	repetitive peak reverse voltage		-	800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 103$ °C; see Figure 3	-	13	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; see Figure 1; see Figure 2	-	20	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; see Figure 4; see Figure 5	-	200	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms	-	220	A
I^2t	I^2t for fusing	$t_p = 10$ ms; sine-wave pulse	-	200	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 50$ A; $I_G = 200$ mA; $dI_G/dt = 200$ mA/µs	-	200	A/µs
I_{GM}	peak gate current		-	5	A
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	20	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-	125	°C

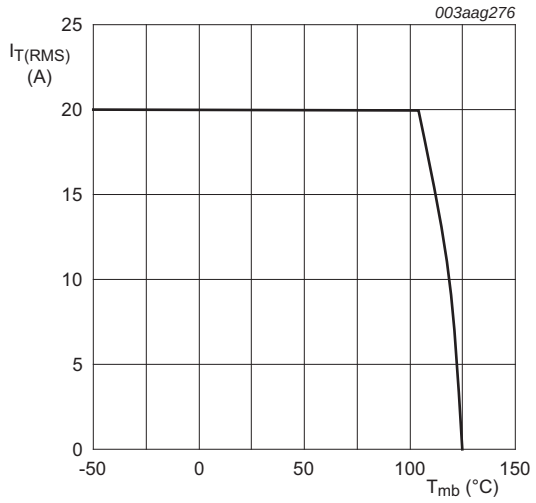
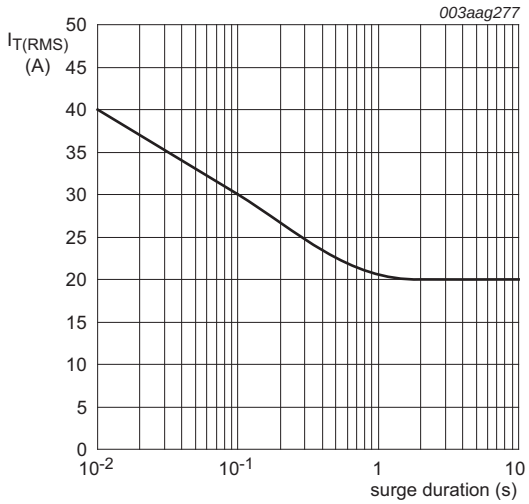
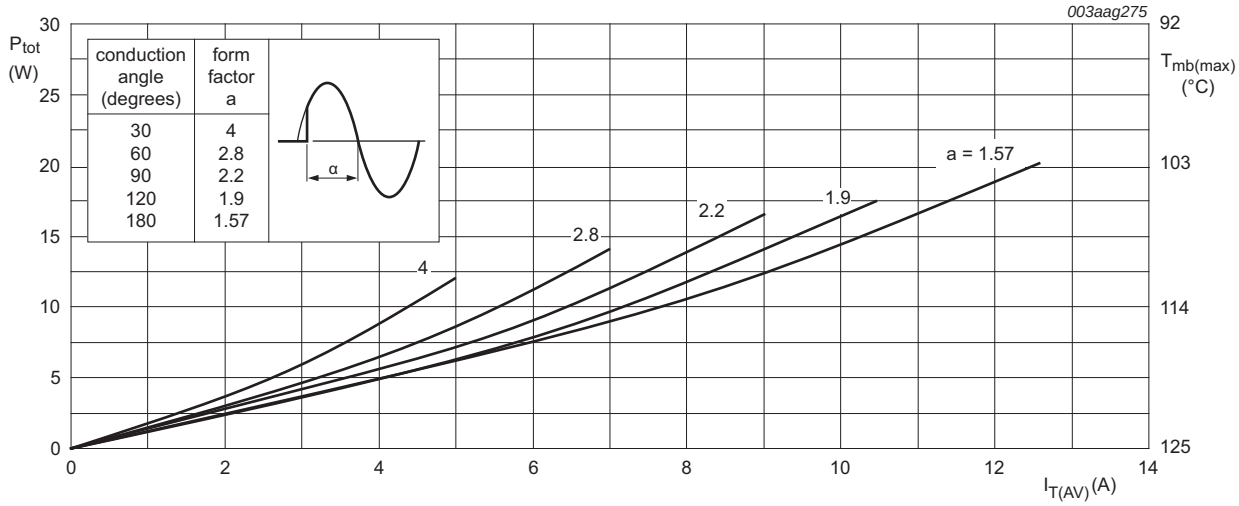


Fig 1. RMS on-state current as a function of mounting base temperature; maximum values



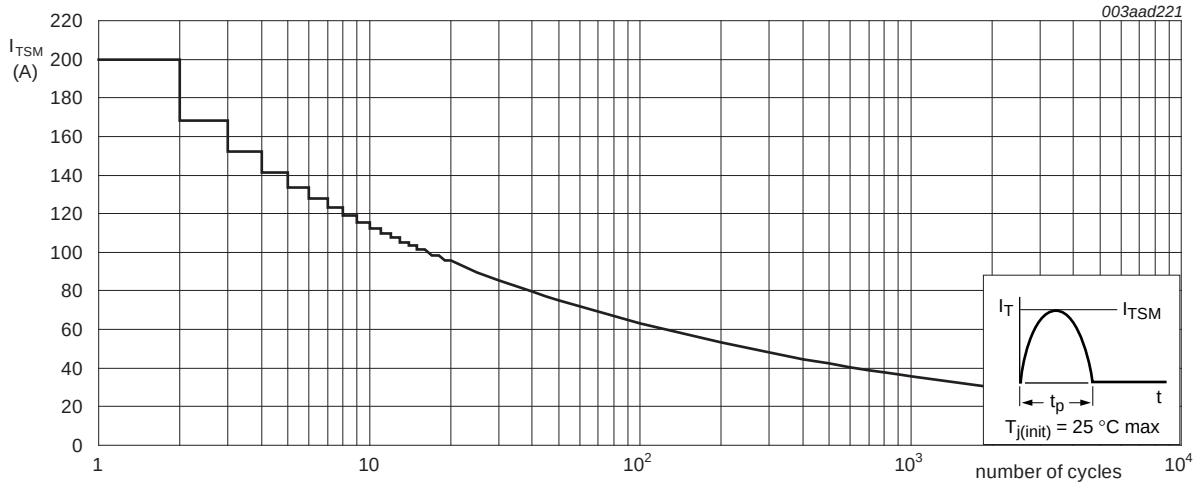
$f = 50\ Hz;\ T_{mb} = 103\ ^{\circ}C$

Fig 2. RMS on-state current as a function of surge duration; maximum values



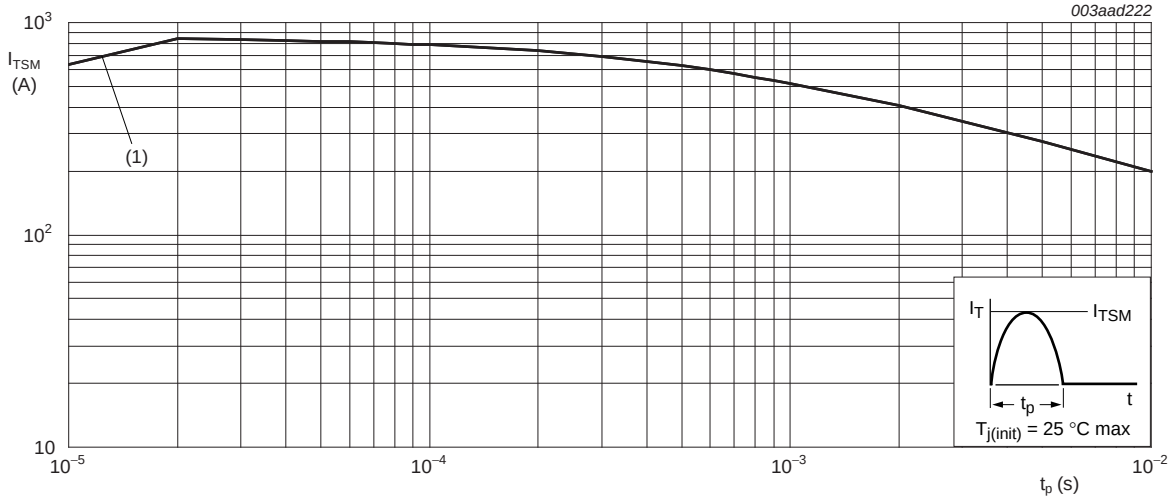
$a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$

Fig 3. Total power dissipation as a function of average on-state current; maximum values



f = 50 Hz

Fig 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 10$ ms; (1) dI_T/dt limit

Fig 5. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see Figure 6	-	-	1.1	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	in free air	-	60	-	K/W

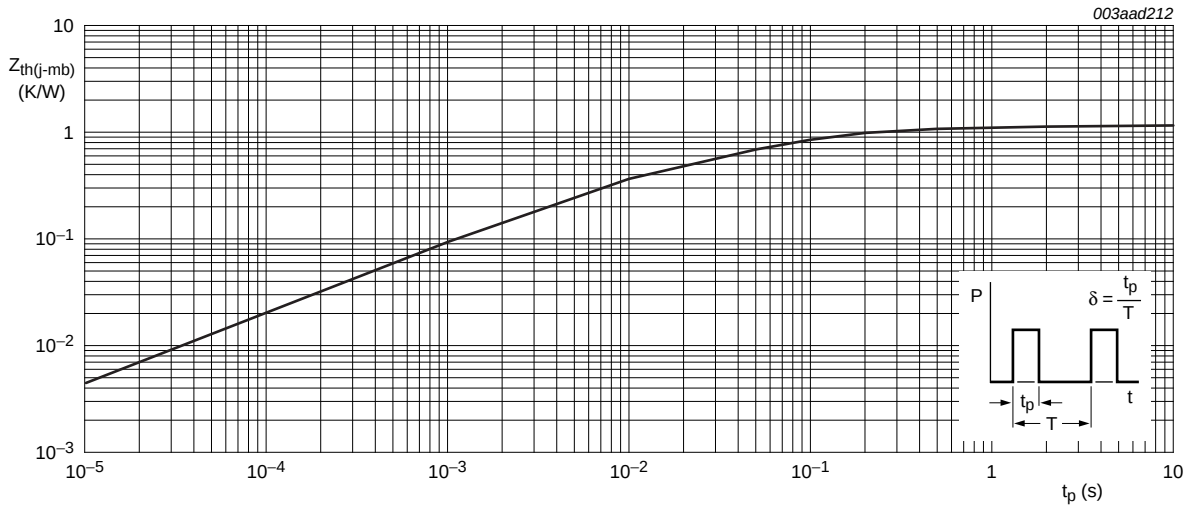


Fig 6. Transient thermal impedance from junction to mounting base as a function of pulse width

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; see Figure 7	-	3	32	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T_j = 25 °C; see Figure 8	-	25	80	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; see Figure 9	-	15	60	mA
V_T	on-state voltage	I_T = 40 A; T_j = 25 °C; see Figure 10	-	1.4	1.75	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; see Figure 11	-	0.6	1.5	V
		V_D = 800 V; I_T = 0.1 A; T_j = 125 °C	0.25	0.4	-	V
I_D	off-state current	V_D = 800 V; T_j = 125 °C	-	0.2	1	mA
I_R	reverse current	T_j = 125 °C; V_R = 800 V	-	0.2	1	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; exponential waveform; gate open circuit; see Figure 12	200	300	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 40 A; V_D = 800 V; I_G = 100 mA; dI_G/dt = 5 A/µs	-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 536 V; T_j = 125 °C; I_{TM} = 50 A; V_R = 25 V; $(dI_T/dt)_M$ = 30 A/µs; dV_D/dt = 50 V/µs; R_{GK} = 100 Ω	-	70	-	µs

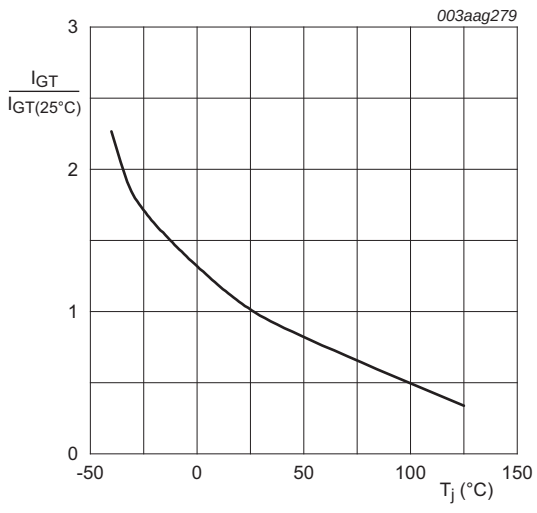


Fig 7. Normalized gate trigger current as a function of junction temperature

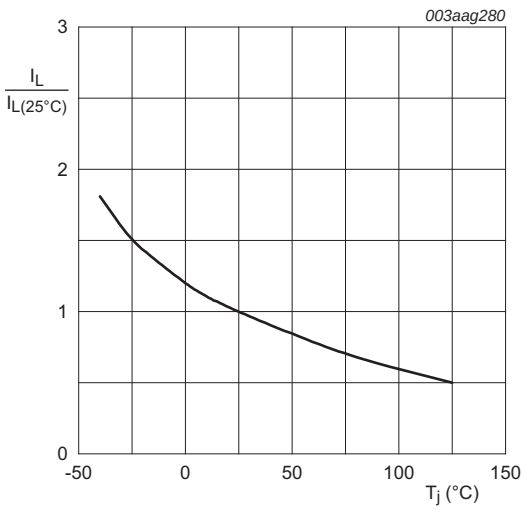


Fig 8. Normalized latching current as a function of junction temperature

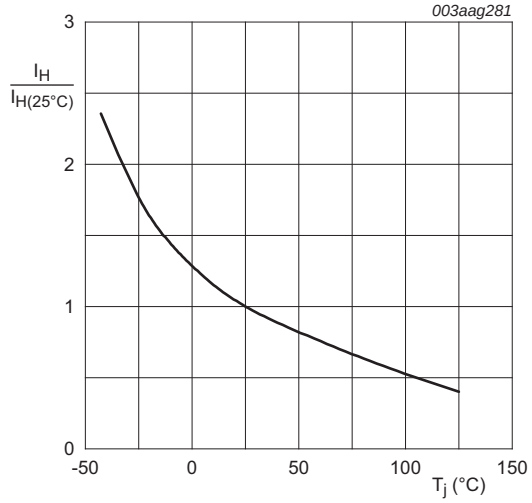
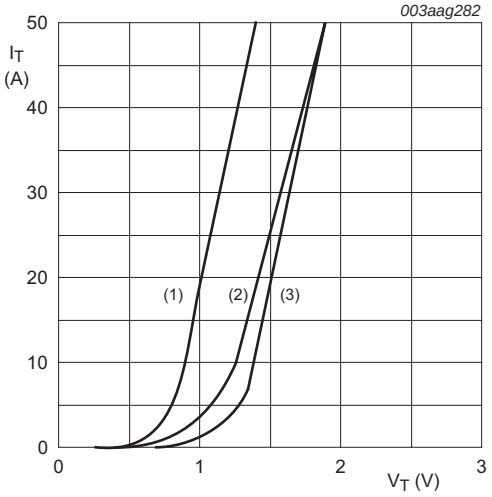


Fig 9. Normalized holding current as a function of junction temperature



Vo = 1.06 V; Rs = 0.03 Ω

(1) Tj = 125 °C; typical values

(2) Tj = 125 °C; maximum values

(3) Tj = 25 °C; maximum values

Fig 10. On-state current as a function of on-state voltage

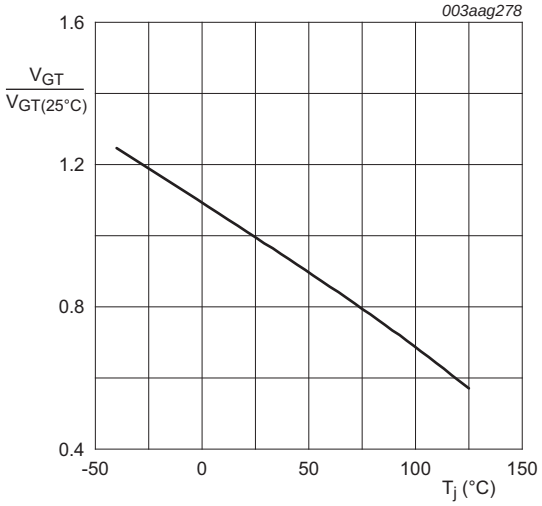
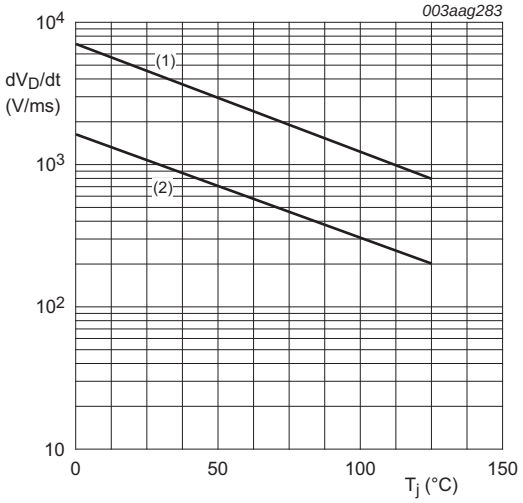


Fig 11. Normalized gate trigger voltage as a function of junction temperature



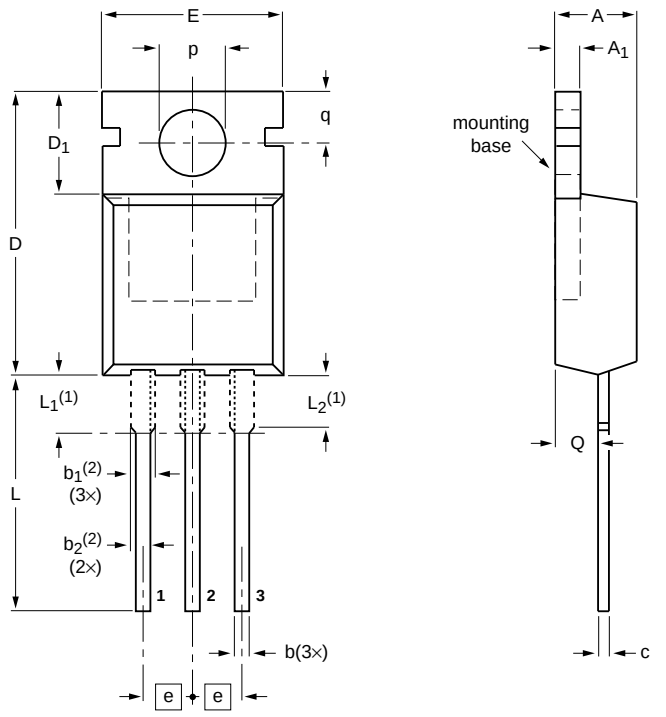
(1) $R_{GK} = 100\ \Omega$

(2) Gate open circuit

Fig 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1(2)	b_2(2)	c	D	D_1	E	e	L	L_1(1)	L_2(1) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

Notes
1. Lead shoulder designs may vary.
2. Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78		3-lead TO-220AB	SC-46			~~08-04-23~~ 08-06-13

Fig 13. Package outline SOT78 (TO-220AB)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BT152-800R v.2	20110609	Product data sheet	-	BT152_SERIES v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number BT152-800R separated from data sheet BT152_SERIES v.1.			
BT152_SERIES v.1	19970301	Product specification	-	-

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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11. Contents

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