Serial EEPROM Series Standard EEPROM

Plug & Play EEPROM

BU9883FV-W

●General Description

BU9883FV-W is for DDC 3 ports, 2K x 8 bit array 3 BANK EEPROM.

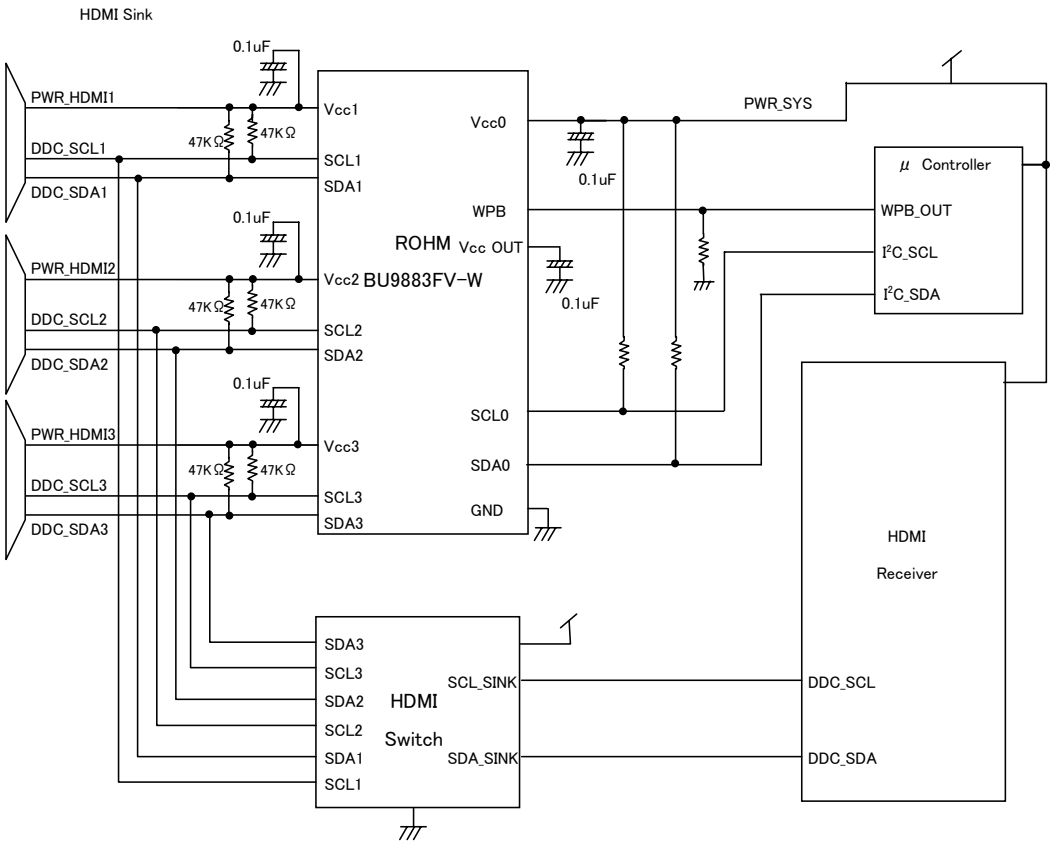
●Features

- There are 3 BANKs, 1 BANK compose of 256 word address x 8 bit EEPROM
- There are 3 DDC interface channels, and each channel can access each BANK independently from other ports.
- 2K bit X 3 BANK memory bits can be accessed from write port (Port0).
- Operate voltage (3.0V to 5.5V)
- Built in diode for power supply from HDMI ports and system.
- Automatic erase
- 8 byte page write mode
- Low power consumption
  - At write action (5.0V) : 1.2mA (Typ.)
  - At read action (5.0V) : 0.2mA(Typ.) 1port action
  - At Standby action (5.0V) : 50μA(Typ.)
- DATA security
- Write Protect pin can switch write port
- Inhibit to WRITE at low Vcc
- Endurance : 1,000,000 erase/write cycles
- Data retention 40 years
- Filtered inputs in all SCL・SDA for noise suppression
- Shipment data all address FFh

●Package W(Typ.) x D(Typ.) x H(Max.)

SSOP-B16
5.00mm x 6.40mm x 1.35mm

●Typical Application Circuit



○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

●**Absolute Maximum Ratings** (Ta=25℃)

Parameter	Symbol	Rating	Unit	Remarks
Supply Voltage	V_{CC}	-0.3 to 6.5	V	
Power Dissipation	Pd	400	mW	Degradation is done at 3.0mW/℃ for operation above 25℃
Storage Temperature	Tstg	-65 to 125	℃	
Operating Temperature	Topr	-40 to 85	℃	
Terminal Voltage	-	-0.3 to V_{CC}+0.3	V	The Max value of terminal voltage is not over 6.5V

●**Memory cell characteristics** (Ta=25℃, V_{CC}0 to 3 = 3.0V to 5.5V)

Parameter	Specification			Unit
	Min.	Typ.	Max.	
Write/Erase Cycle *1	1,000,000	-	-	Cycles
Data Retention *1	40	-	-	Years

*1:Not 100% TESTED

●**Recommended Operating Ratings**

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	3.0 to 5.5	V
Input Voltage	VIN	0 to V_{CC}0 to 3	

●**Input/output capacity** (Ta=25℃, Frequency=5MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SDA pins (SDA0,1,2,3) *1	C_{IN}	-	7	-	pF
SCL pins (SCL0,1,2,3) *1	C_{IN2}	-	7	-	pF

*1:Not 100% TESTED

●**Electrical characteristics -DC operating** (Unless otherwise specified, Ta=-40℃ to 85℃, V_{CC}0 to 3 = 3.0V to 5.5V)

Parameter	Symbol	Specification			Unit	Test condition
		Min.	Typ.	Max.		
"H" Input Voltage0	VIH0	0.7xV_{CC}0	-	V_{CC}0+0.5	V	3.0≦V_{CC} 0≦5.5V(SCL0, SDA0)
"L" Input Voltage0	VIL0	-0.3	-	0.3xV_{CC}0	V	3.0≦V_{CC} 0≦5.5V(SCL0, SDA0)
"H" Input Voltage1	VIH1	0.7xV_{CC}1	-	V_{CC}1+0.5	V	3.0≦V_{CC}1≦5.5V(SCL1, SDA1)
"L" Input Voltage1	VIL1	-0.3	-	0.3xV_{CC}1	V	3.0≦V_{CC}1≦5.5V(SCL1, SDA1)
"H" Input Voltage2	VIH2	0.7xV_{CC}2	-	V_{CC}2+0.5	V	3.0≦V_{CC}2≦5.5V(SCL2, SDA2)
"L" Input Voltage2	VIL2	-0.3	-	0.3xV_{CC}2	V	3.0≦V_{CC}2≦5.5V(SCL2, SDA2)
"H" Input Voltage3	VIH3	0.7xV_{CC}3	-	V_{CC}3+0.5	V	3.0≦V_{CC}3≦5.5V(SCL3, SDA3)
"H" Input Voltage3	VIL3	-0.3	-	0.3xV_{CC}3	V	3.0≦V_{CC}3≦5.5V(SCL3, SDA3)
"L" Output Voltage0	VOL0	-	-	0.4	V	IOL=3.0mA , 3.0V≦V_{CC}0≦5.5V(SDA0)
"L" Output Voltage1	VOL1	-	-	0.4	V	IOL=3.0mA , 3.0V≦V_{CC}1≦5.5V(SDA1)
"L" Output Voltage2	VOL2	-	-	0.4	V	IOL=3.0mA , 3.0V≦V_{CC}2≦5.5V(SDA2)
"L" Output Voltage3	VOL3	-	-	0.4	V	IOL=3.0mA , 3.0V≦V_{CC}3≦5.5V(SDA3)
WP "H" Input Voltage	VIH4	0.7xV_{CC}0	-	V_{CC}0+0.3	V	3.0≦V_{CC}0≦5.5V(WPB)
WP "L" Input Voltage	VIL4	-0.3	-	0.3xV_{CC}	V	3.0≦V_{CC}0≦5.5V(WPB)
Input Leakage Current0	ILI0	-1	-	1	μA	VIN=0 to 5.5V(SCL0 to 3)
Input Leakage Current1	ILI1	55	110	230	μA	WPB=5.5V , V_{CC}=5.5V
Output Leakage Current0	ILO0	-1	-	1	μA	VOUT=0 to 5.5(SDA0 to 3)
Operating Current	ICC1	-	-	2.0	mA	V_{CC}0=5.5V, fSCL=400kHz, tWR=5ms Byte Write, Page Write
	ICC2	-	-	1.0	mA	V_{CC}0 to 3=5.5V, fSCL=400kHz Random Read, Current Read,Sequential Read, (each port operation)
Standby Current	ISB0	-	-	100	μA	V_{CC}0=5.5V, SDA0 to 3=SCL0 to 3=5.5V, WPB=GND
Standby Current	ISB1	-	-	100	μA	V_{CC}1=5.5V, SDA0 to 3=SCL0 to 3=5.5V, WPB=GND
Standby Current	ISB2	-	-	100	μA	V_{CC}2=5.5V, SDA0 to 3=SCL0 to 3=5.5V, WPB=GND
Standby Current	ISB3	-	-	100	μA	V_{CC}3=5.5V, SDA0 to 3=SCL0 to 3=5.5V, WPB=GND

●**Electrical characteristics -AC Operating** (Ta=-40℃ to 85℃, V_{CC}0 to 3 = 3.0V to 5.5V)

Parameter	Symbol	3.0≦V_{CC}0 to 3≦5.5V			Unit
		Min.	Typ.	Max.	
Clock Frequency	fSCL	-	-	400	kHz
Data Clock High Period	tHIGH	0.6	-	-	μs
Data Clock Low Period	tLOW	1.2	-	-	μs
SDA0 to 3 and SCL0 to 3 Rise Time *1	tR	-	-	0.3	μs
SDA0 to 3 and SCL0 to 3 Fall Time*1	tF	-	-	0.3	μs
Start Condition Hold Time	tHD:STA	0.6	-	-	μs
Start Condition Setup Time	tSU:STA	0.6	-	-	μs
Input Data Hold Time	tHD:DAT	0	-	-	ns
Input Data Setup Time	tSU:DAT	100	-	-	ns
Output Data Delay Time	tPD	0.1	-	0.9	μs
Output Data Hold Time	tDH	0.1	-	-	μs
Stop Condition Setup Time	tSU:STO	0.6	-	-	μs
Bus Free Time	tBUF	1.2	-	-	μs
Write Cycle Time	tWR	-	-	5	ms
Noise Spike Width (SDA0 to 3 and SCL0 to 3)	tI	-	-	0.1	μs
WP Hold Time	tHD:WP	0	-	-	ns
WP Setup Time	tSU:WP	0.1	-	-	μs
WP valid time	tHIGH:WP	1.0	-	-	μs

*1 : Not 100% TESETED

●**Sync Data Input / Output Timing**

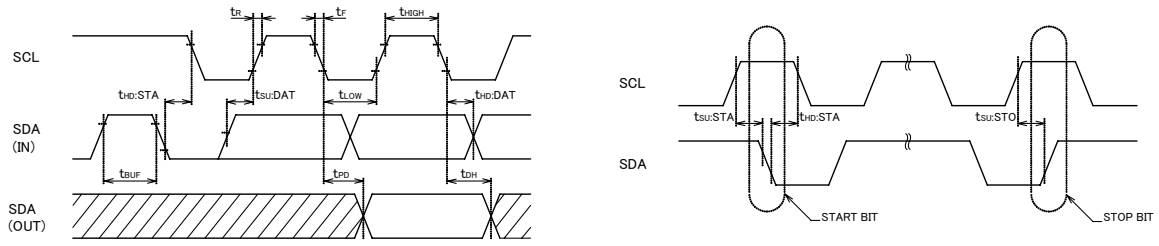
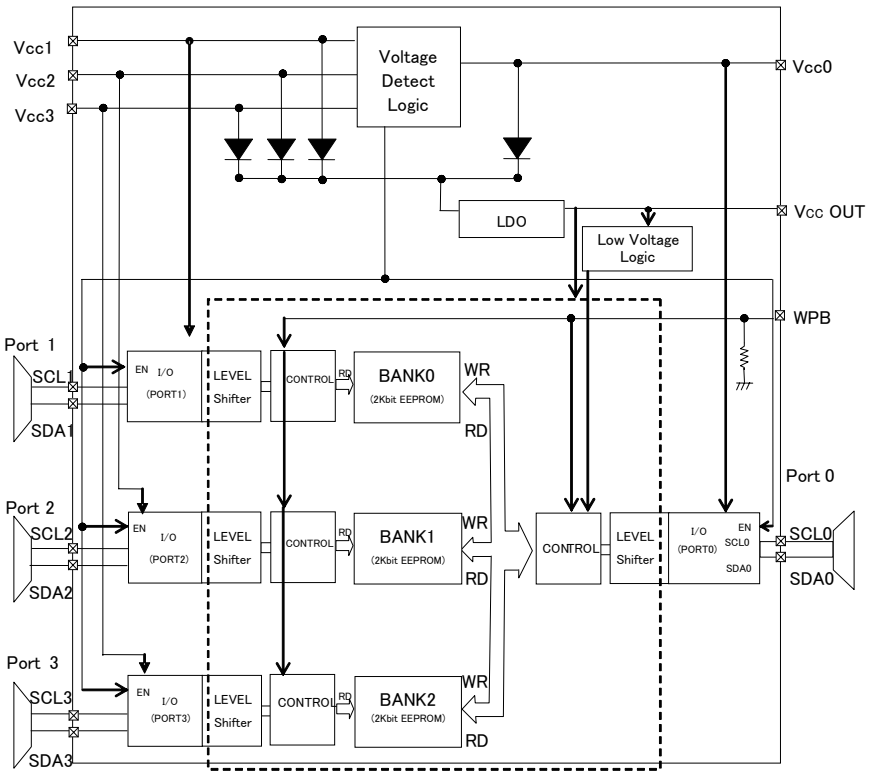


Figure 1. SYNCHRONOUS DATA TIMING

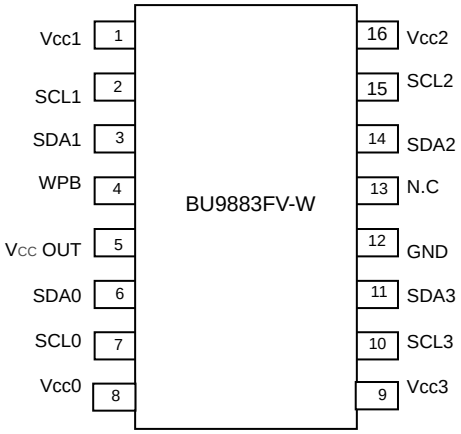
○SDA data is latched into the chip at the rising edge of the SCL clock. (This is commonness in all port.)
○Output date toggles at the falling edge of the SCL clock. (This is commonness in all port.)

●**Block Diagram**



●**Pin Configuration**

TOP VIEW



●**Pin Descriptions**

PIN No.	PIN NAME	I/O	FUNCTIONS
1	Vcc1	-	Power Supply
2	SCL1	Input	Serial clock input
3	SDA1	Input /output	Slave and word address, Serial data input serial data output
4	WPB	Input	Write protect terminal(1 : Write enable, 0 : Write disable)
5	Vcc OUT	-	Terminal of diode. Connect Bypass capacitor.
6	SDA0	Input /output	Slave and word address, Serial data input serial data output
7	SCL0	Input	Serial clock input
8	Vcc0	-	Power Supply
9	Vcc3	-	Power Supply
10	SCL3	Input	Serial clock input
11	SDA3	Input /output	Slave and word address, Serial data input serial data output
12	GND	-	Reference voltage of all input / output
13	N.C	-	None connect terminal. Don't connect each other.
14	SDA2	Input /output	Slave and word address, Serial data input serial data output
15	SCL2	Input	Serial clock input
16	Vcc2	-	Power Supply

●**Typical Performance Curves**
(The following values are Typ. ones.)

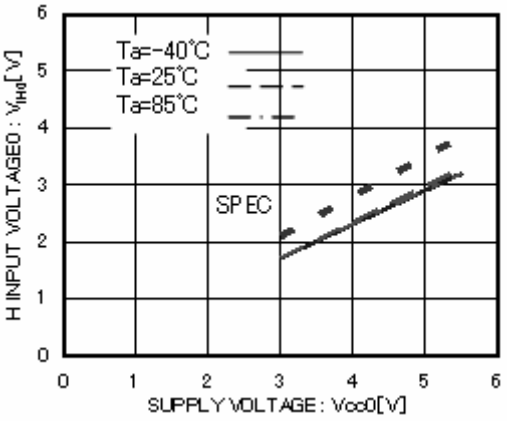


Figure 2. 'H' Input Voltage0 V_{IH0}
(SCL0,SDA0)

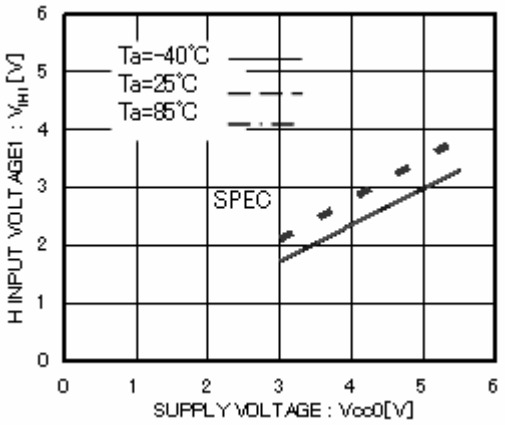


Figure 3. 'H' Input Voltage1 V_{IH1}
(SCL1,SDA1)

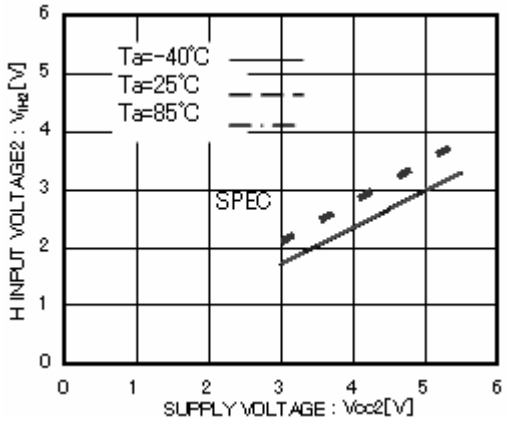


Figure 4. 'H' Input Voltage2 V_{IH2}
(SCL2,SDA2)

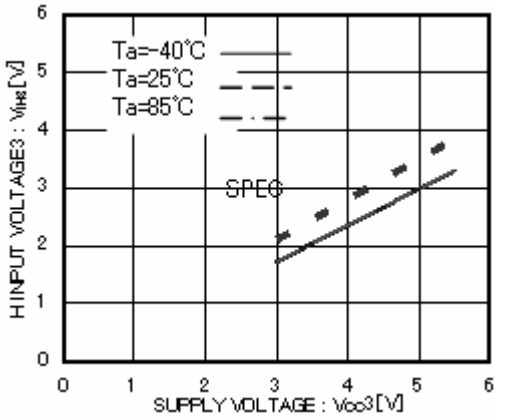


Figure 5. 'H' Input Voltage3 V_{IH3}
(SCL3,SDA3)

●**Typical Performance Curves – Continued**

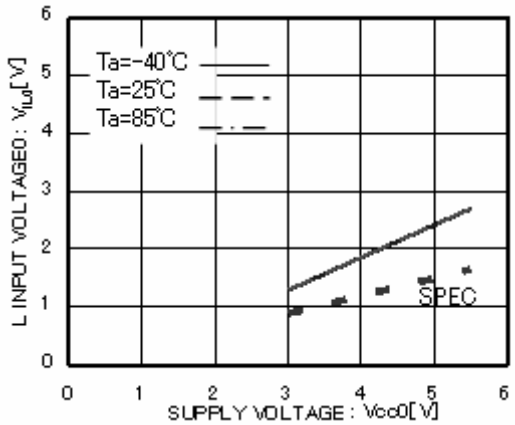


Figure 6. 'L' Input Voltage0 V_{IL0}
(SCL0,SDA0)

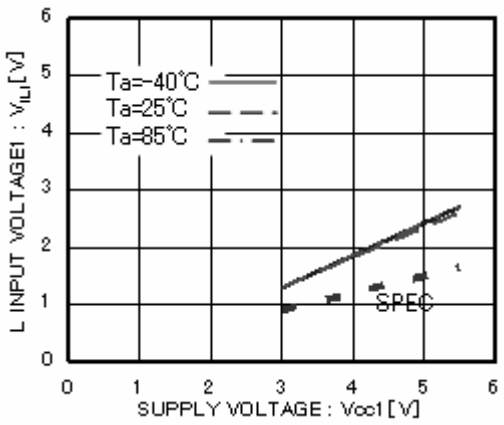


Figure 7. 'L' Input Voltage1 V_{IL1}
(SCL1,SDA1)

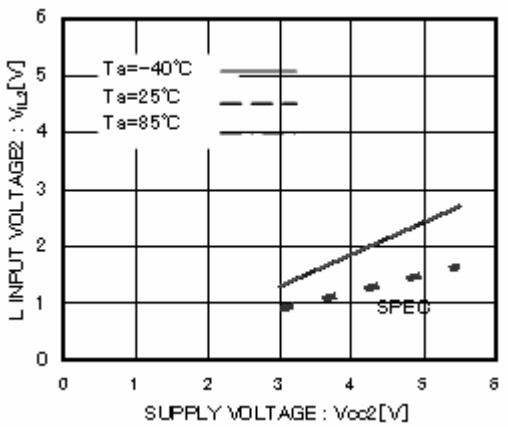


Figure 8. 'L' Input Voltage2 V_{IL2}
(SCL2,SDA2)

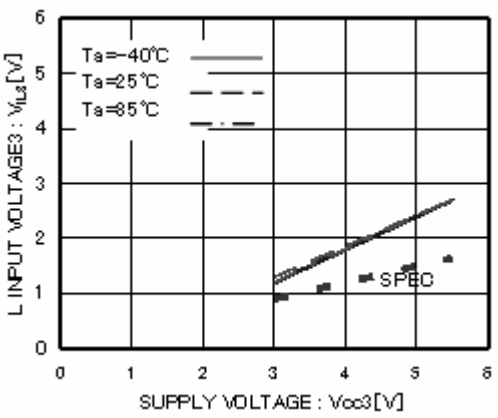


Figure 9. 'L' Input Voltage3 V_{IL3}
(SCL3,SDA3)

●**Typical Performance Curves – Continued**

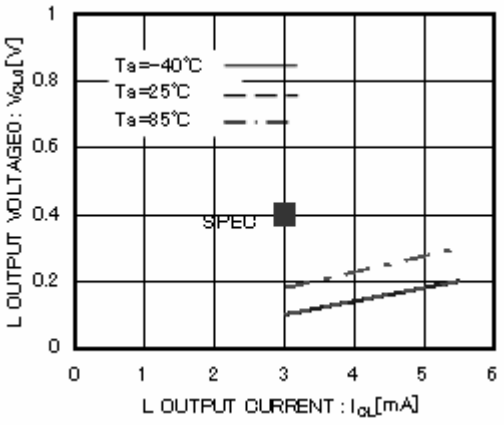


Figure 10. 'L' Output Voltage0
V_{0L0}-I_{0L}(Vcc0=3.0V)

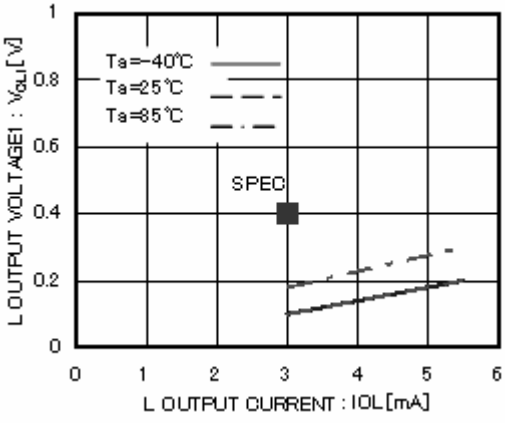


Figure 11. 'L' Output Voltage1
V_{0L1}-I_{0L}(Vcc1=3.0V) (SDA1)

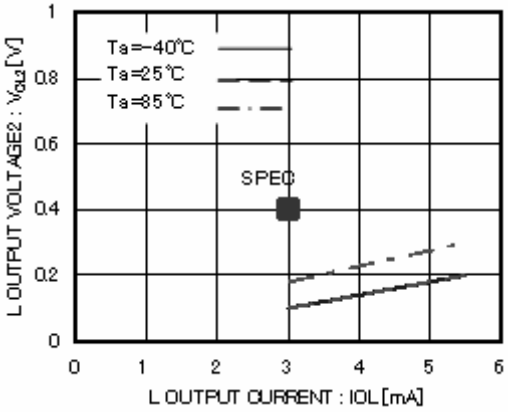


Figure 12. 'L' Output Voltage2
V_{0L2}-I_{0L}(Vcc2=3.0V) (SDA2)

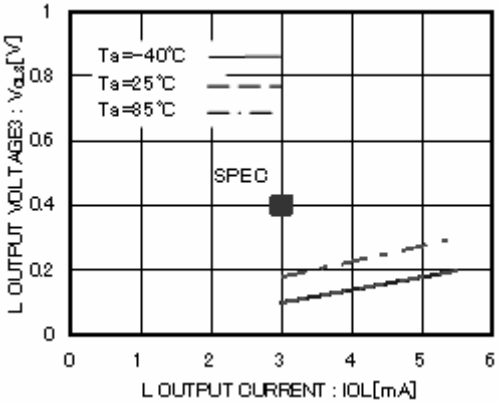


Figure 13. 'L' Output Voltage3
V_{0L3}-I_{0L}(Vcc3=3.0V) (SDA3)

●**Typical Performance Curves – Continued**

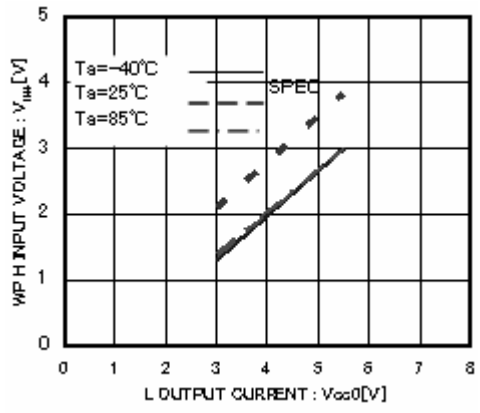


Figure 14. WP 'H' Input Voltage V_{IH4}

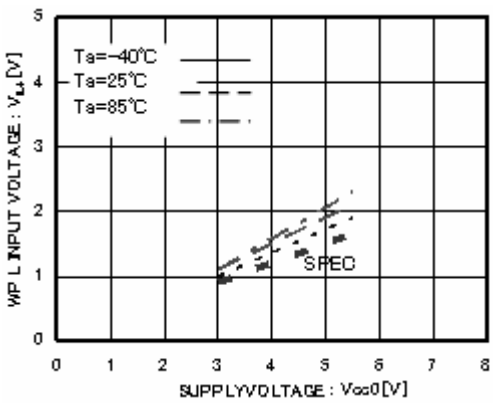


Figure 15. WP 'L' Input Voltage V_{IL4}

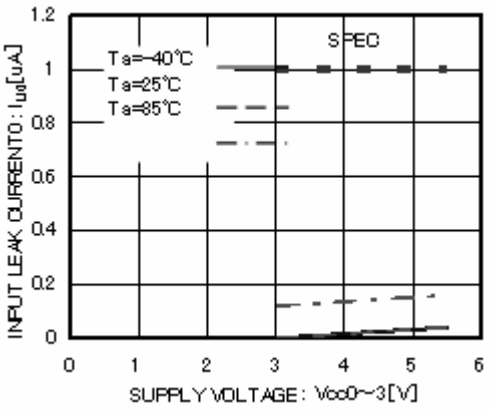


Figure 16. Input Leak Current0 I_{U0}(SCL0 to 3)

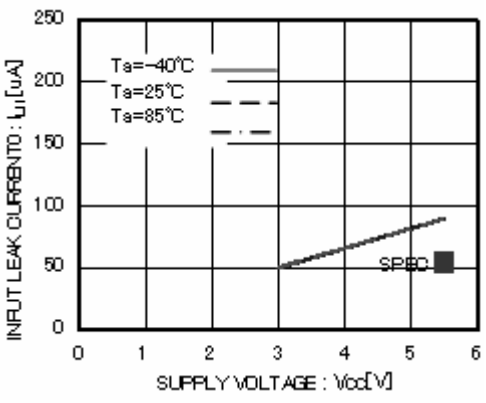


Figure 17. Input Leak Current1 I_{LI1}(WPB)

●**Typical Performance Curves – Continued**

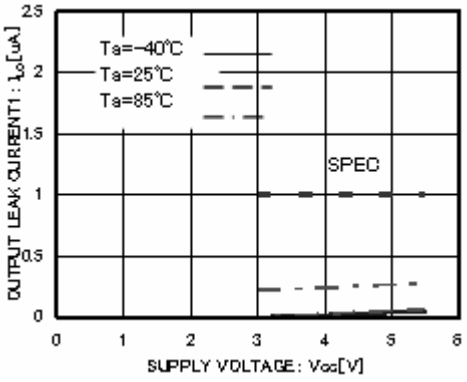


Figure 18. OUTPUT LEAK CURRENT0 I_{LO0} (SDA0 to 3)

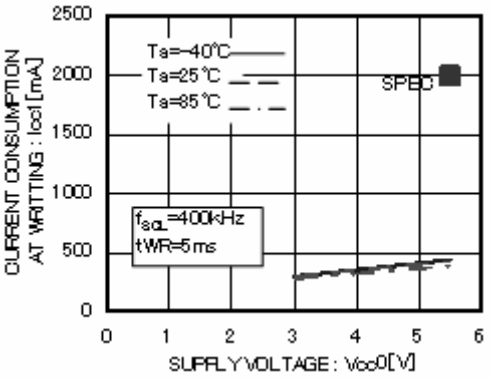


Figure 19. Current Consumption at Reading I_{CC1}

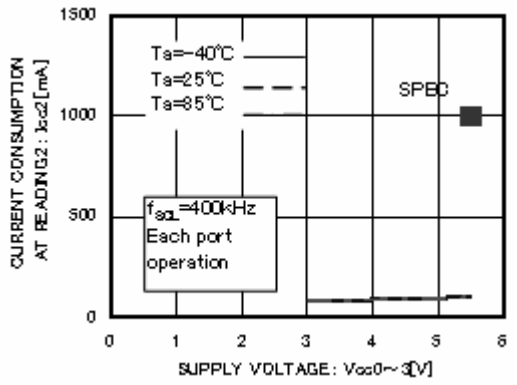


Figure 20. Current Consumption at Reading I_{CC2}

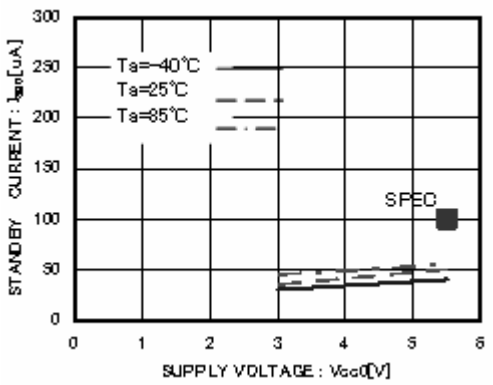


Figure 21. Standby Current0 I_{SB0}

●**Typical Performance Curves – Continued**

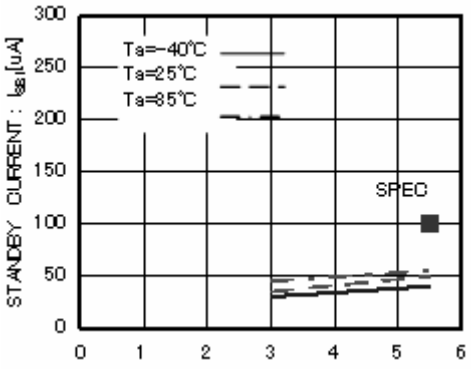


Figure 22. Standby Current1 I_{SB1}

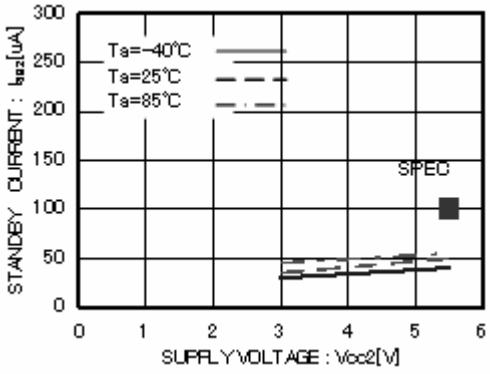


Figure 23. Standby Current2 I_{SB2}

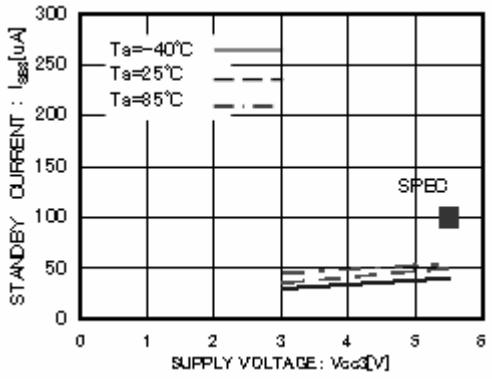


Figure 24. Standby Current3 I_{SB3}

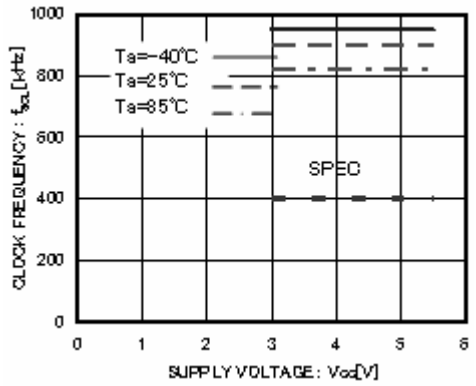


Figure 25. Clock Frequency f_{SCL}

●**Typical Performance Curves – Continued**

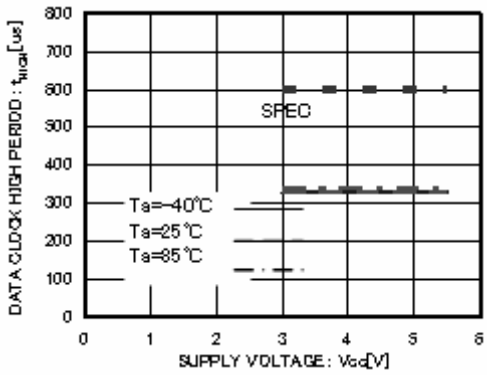


Figure 26. Data Clock High Period t_{HIGH}

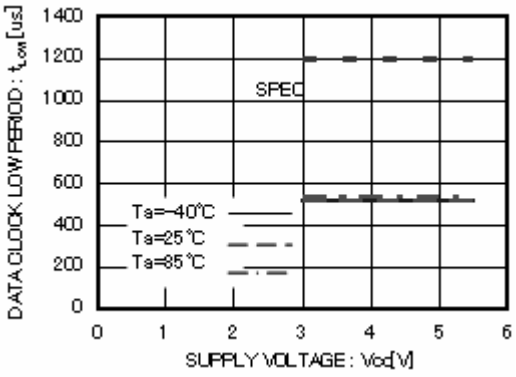


Figure 27. Data Clock Low Period t_{LOW}

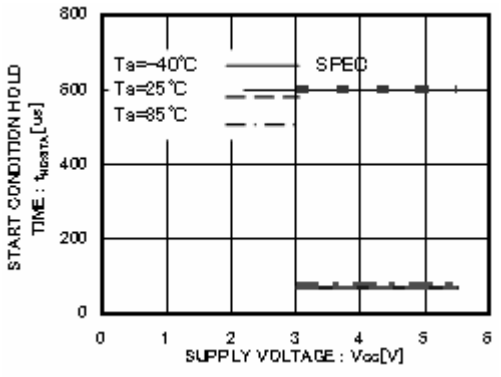


Figure 28. Start Condition Hold Time $t_{HD:STA}$

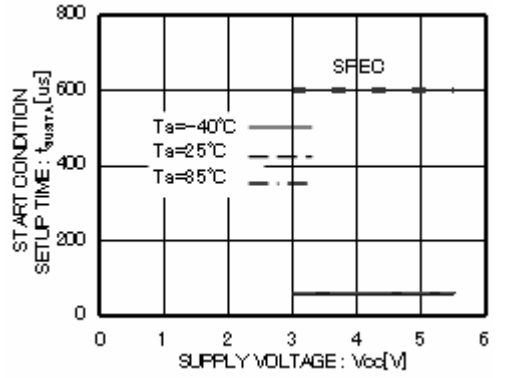


Figure 29. Start Condition Setup Time $t_{SU:STA}$

●**Typical Performance Curves – Continued**

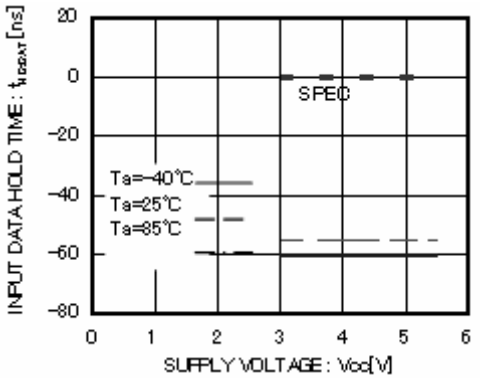


Figure 30. Input Data Hold Time $t_{HD:DAT}$

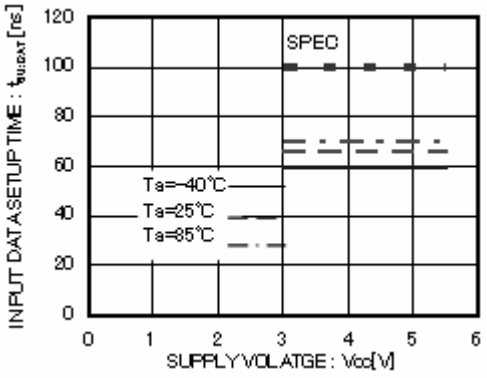


Figure 31. Input Data Setup Time $t_{SU:DAT}$

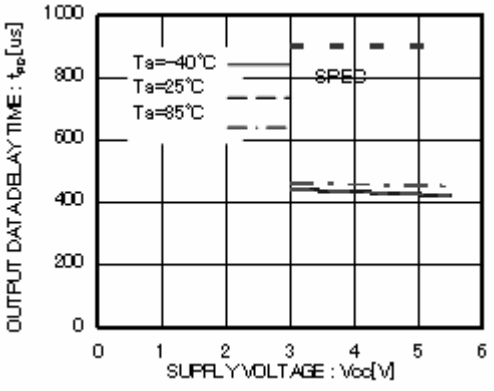


Figure 32. Output Data Delay Time t_{PD}

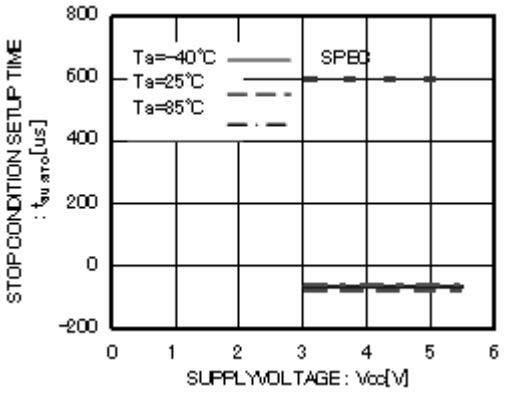


Figure 33. Stop Condition Setup Time $t_{SU:STO}$

●**Typical Performance Curves – Continued**

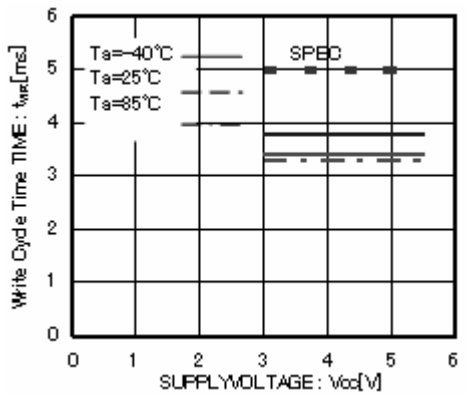


Figure 34. Write Cycle Time t_{WR}

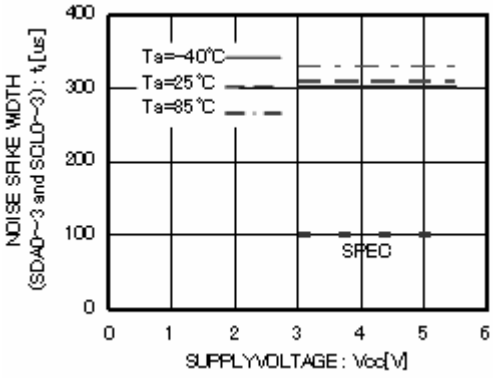


Figure 35. Noise Spike Width t_I (SDA0 to 3 and SCL0 to 3)

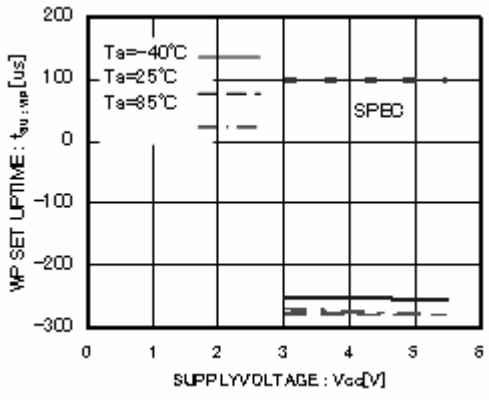


Figure 36. WP Setup Time $t_{SU:WP}$

●**WRITE CYCLE TIMING**

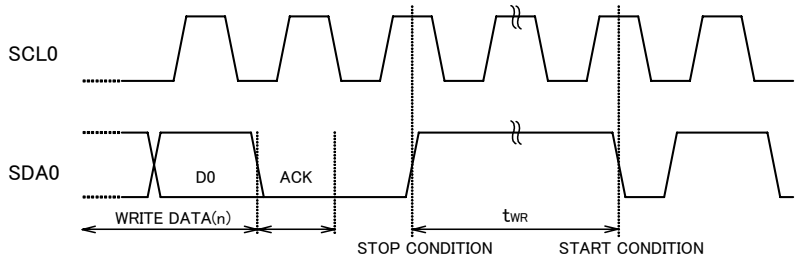


Figure 37. WRITE CYCLE TIMING

●**WRITE OPERATION**

BU9883FV-W has 2K bit EEPROM in each port, there are three BANKs, 6K bit EEPROM in this device.
Each BANK EEPROM can be written through PORT0.
There is no write operation through PORT1,2,3.
When this device is accessed throgh PORT0, WPB terminal must be set to “HIGH”.
(See to Table 1)

●**READ OPERATION**

Each BANK EEPROM can be read through each port.
The relation ship of access port and access BANK is describe Table2.

Table 1

Port0	BANK1 to 3
Port1	No write operation
Port2	No write operation
Port3	No write operation

Table 2

Port0	BANK1 to 3
Port1	BANK1
Port2	BANK2
Port3	BANK3

◯When EEPROM access through PORT0, P1, P0 bits in slave address appoint access BANK.(Refer to Table 3)

Table 3

P1	P0	P1,P0 bit and access BANK
0	0	No bank selected
0	1	BANK1
1	0	BANK2
1	1	BANK3

Note) When P1=0, P0=0 : this device doesn’t return Acknowlege.

◯During PORT0 access, WPB terminal must be set to “HIGH”, then PORT1 to 3 accesses will be cancelled.
◯In accessing from PORT1 to 3, set WPB termianl to “LOW”

●**DEVICE OPERATION**

◯START CONDITION

・All commands are proceeded by the start condition, which is a HIGH to LOW transition of SDA0 to 3 when SCL0 to 3 is HIGH.
・This device continuously monitors the SDA0 to 3 and SCL0 to 3 lines for the start condition and will not respond to any command until this condition has been met. (Refer to Figure 1)

◯STOP CONDITION

・All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA0 to 3 when SCL0 to 3 is HIGH. (Refer to Figure 1) The stop condition initiates internal write cycle to write the data into memory array after write sequence. The stop condition is also used to place the device into the standby power mode after read sequence. A stop condition can only be issued after the transmitting device has released the bus.

◯NOTICE ON WRITE COMMAND

・In Write command, after transmit write data, if there are no stop condition, EEPROM data don’t change.

○DEVICE ADDRESSING

・Following a START condition, the master output the device address of the slave to be accessed.

・The most significant four bits of the slave address are the “device type indentifier,” for this device, this is fixed as “1010.”

・The next three bit specify a particular device. For PORT0 access, that are set “0”, “P1”, “P0”, for PORT 1 to 3 access, that must be set “000”.

・The last bit of the stream determines the operation to be performed. When set to “1” a read operation is selected ; when set to “0,” a write operation is selected.

R/$\overline{W}$ set to “0” ・・・・・・・・・ WRITE
R/$\overline{W}$ set to “1” ・・・・・・・・・ READ

○ACKNOWLEDGE

・Acknowledge is a software convention used to indicate successful data transfers.The master or the slave will release the bus after transmitting eight bits.During the ninth clock cycle, the receiver will pull the SDA line LOW to Acknowledgethat the eight bits of data has been received.

・This device will respond with an Acknowledge after recognition of a START condition and its slave address.If both the device and a write operation have been selected, this device will respond with an Acknowledge, after the receipt of each subsequent 8-bit word.

・In the READ mode, this device will transmit eight bit of data, release the SDA line, and monitor the line for an Acknowledge.

・If an Acknowledge is detected, and no STOP condition is generated by the master, this device will continue to transmit the data.

・If an Acknowledge is not detected, this device will terminate further data transmissions and await a STOP condition before returning to the standby mode.

・This device dosen't return Acknouwedge in internal write cycle.

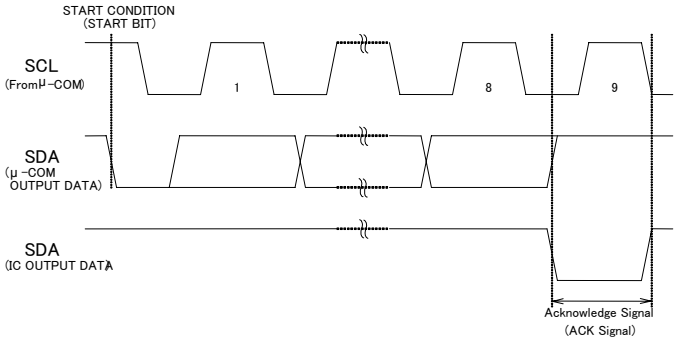


Figure 38. ACKNOWLEDGE RESPONSE FROM RECEIVER

●PORT0 access commands

○For PORT0 access, WPB terminal must be set to “HIGH”.

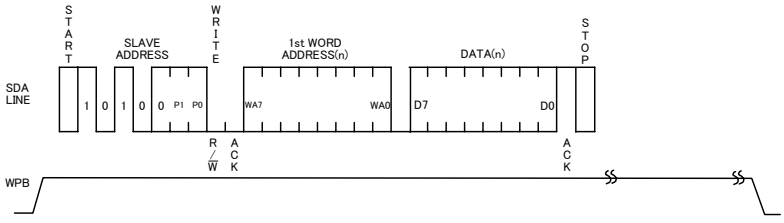


Figure 39. BYTE WRITE CYCLE TIMING (PORT0)

○This write commands operate EEPROM write sequence at address which is appointed by P1, P0.

○When the master generates a STOP condition, this device begins the internal write cycle to the nonvolatile array.

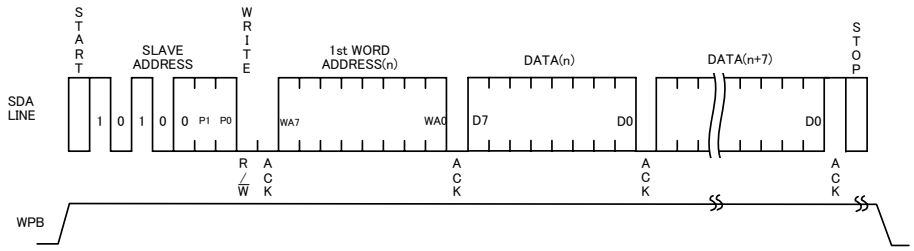


Figure 40. PAGE WRITE CYCLE TIMING (PORT0)

○This device is capable of eight byte page write operation.
○After the receipt of each word, the three low order address bits are internally incremented by one. The most significant address bits (WA7 to WA3) remain constant, if the master transmits more than 8 words.
○The relationship of P1, P0 inputs and access BANK is described as follows.

P1	P0	BANK
0	0	No opearation
0	1	BANK1
1	0	BANK2
1	1	BANK3

○Don't set P1, P0=0, 0. If P1, P0 are set to 0, there is no target bank, so this device doesn't return acknowledge.
○WPB terminal must be set to “HIGH” during Byte Write cycle, and Page Write cycle, and internal Write cycles. If WPB is set to “LOW” in above condition, programing doesn't work, and during internal Write cycle, WPB terminal set to “LOW”, this device terminate programing, and the data in programing address is not stored correctly.

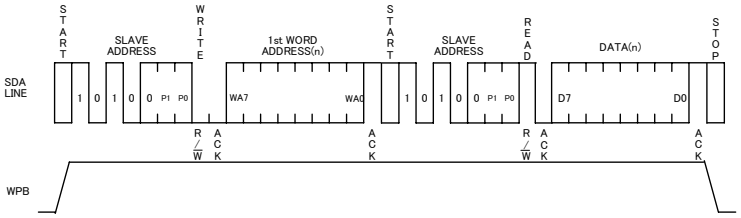


Figure 41. RANDOM READ CYCLE TIMING（PORT0）

○Random read operation allows the master to access any memory location which is appointed by P1, P0 bit. This operation
involves a two-step process. First, the master issue a write command which includes the start condition and the slave address field (with R/$\overline{W}$ set to “0”) followed by the address of the word be read.
○This procedure sets the internal address counter of this device to the desired address. After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by the slave address field with R/$\overline{W}$ the set to “1.” This device will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location.
○If the master does not acknowledge the transmission but does generate the stop condition, at this point this device discontinues transmission.

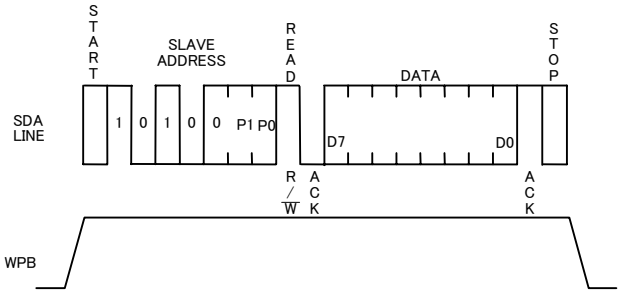


Figure 42. CURRENT READ CYCLE TIMING (PORT0)

○When the command just before Current Read cycle is Random Read cycle or Current Read cycle (each including Sequential Read cycle), data of incremented last read address (n)-th address, i.e.n, data of the (n+1)-th address is output. When the command just before Current Read cycle is Byte Write or Page write, data of latest write address is output.

○Current Read operation allows the master to access data word stored in internal address counter which is appointed by P1, P0 bit. This operation involves a two-step process. This device will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location.
If the master does not acknowledge the transmission but does generate the stop condition, at this point this device discontinues transmission.

note)If the master send Acknowredge at after D0 output, Sequential Read is selected, and this device output next address data, and master can't send stop condition, so master can't discontinues transmission.
To stop read command, the master must send no Acknowledge at after D0 output, and issue stop condition.

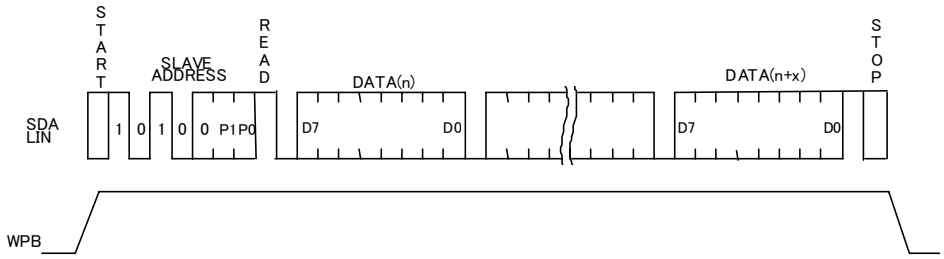


Figure 43. SEQUENTIAL READ CYCLE TIMING （PORT0）

○During the sequential read operation, the internal address counter of this device automatically increments with each acknowledge received ensuring the data from address will be followed with the data from n+1. For read operations, all bits of the address counter are incremented allowing the entire array to be read during a single operation. When the counter reaches the top of the array, it will “roll over” to the bottom of the array of BANK and continue to transmit the data.

○The sequential read operation can be performed with both current read and random read.

●PORT1,2,3 access commands

○If the master access send commands by port1,2,3, WPB pin must be “L”.

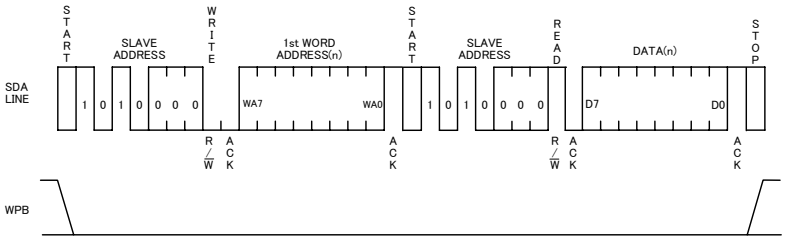


Figure 44. RANDOM READ CYCLE TIMING（PORT1 to 3）

○Random read operation allows the master to access any memory location of the BANK which is appointed by P1, P0. This operation involves a two-step process.
First, the master issues a write command which includes the start condition and the slave address field (with R/W set to “0”) followed by the address of the word be read.
This procedure sets the internal address counter of this device to the desired address.
After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by the slave address field with R/W the set to “1.”
This device will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. If the master does not acknowledge the transmission but does generate the stop condition, at this point this device discontinues transmission.

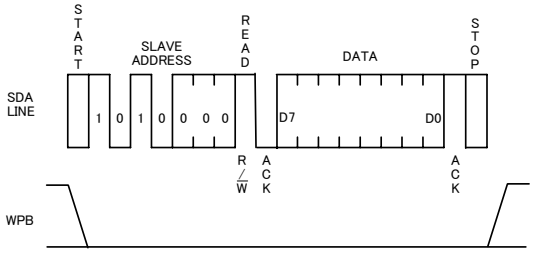


Figure 45. CURRENT READ CYCLE TIMING（PORT1 to 3）

○When the command just before Current Read cycle is Random Read cycle or Current Read cycle (each including Sequential Read cycle), data of incremented last read address (n)-th address, i.e.n, data of the (n+1)-th address is output. When the command just before Current Read cycle is Byte Write or Page write, data of latest write address is output.

○Random read operation allows the master to access any memory location. The BANK which is appointed by P1, P0. This operation involves a two-step process.

First, the master issues a write command which includes the start condition and the slave address field (with R/$\overline{W}$ set to "0") followed by the address of the word be read. This procedure sets the internal address counter of this device to the desired address. After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by the slave address field with R/W the set to "1." This device will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location.

If the master does not acknowledge the transmission but does generate the stop condition, at this point this device discontinues transmission.

note)If the master send Acknowredge at after D0 output, Sequential Read is selected, and this device output next address data, and master can't send stop condition, so master can't discontinues transmission. To stop read command, the master must send no Acknowledge at after D0 output, and issue stop condition.

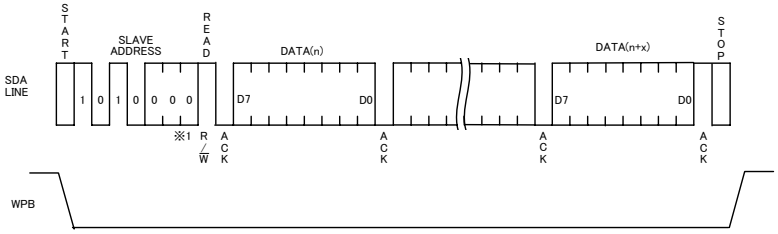


Figure 46. SEQUENTIAL READ CYCLE TIMING （PORT1 to 3）

○During the sequential read operation, the internal address counter of this device automatically increments with each acknowledge received ensuring the data from address n will be followed with the data from n+1. For read operations, all bits of the address counter are incremented allowing the entire array to be read during a single operation. When the counter reaches the top of the array, it will "roll over to the bottom of the array and continue to transmit the data.

○The sequential read operation can be performed with both current read and random read.

●Access Control of PORT0,1,2,3

WPB terminal controls access enable of each PORT, as follows.

PORT	WPB terminal inputs	
	0	1
PORT0	not accessible	Read/Write
PORT1	Read	not accessible
PORT2	Read	not accessible
PORT3	Read	not accessible

Table4 WPB terminal and port accesibility

○ When WPB terminal is "HIGH", PORT0 only can access this device.
In this case, when commands from PORT1, 2, 3 are inputted, these ports don't return acknowledge.

O When WPB terminal is "LOW", PORT0 access is not valid, but PORT1, 2, 3 can access this device this device.
Commands from PORT1, 2, 3 is performs independently other port.

●Software reset

Software reset is executed when to avoid malfunction after power on, and to reset during command input. Software reset has several kinds, and 3 kinds of them are shown in the figure below. (Refer to Figure 47-(a), Figure 47-(b), and Figure 47-(c).) In dummy clock input area, release the SDA0 to 3 buses ('H' by pull up). In dummy clock area, ACK output and read data '0' (both 'L' level) may be output from EEPROM, therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

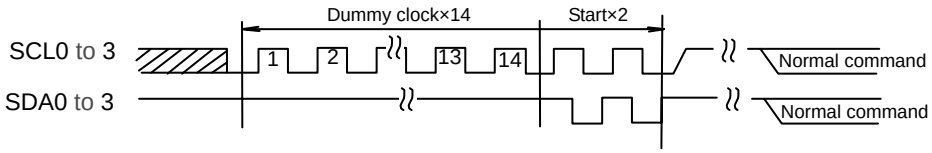


Figure 47-(a) The case of dummy clock +START+START+ command input

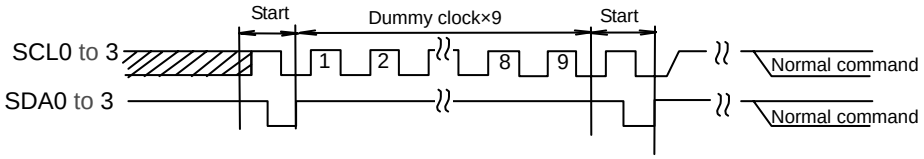


Figure 47-(b) The case of START +9 dummy clocks +START+ command input

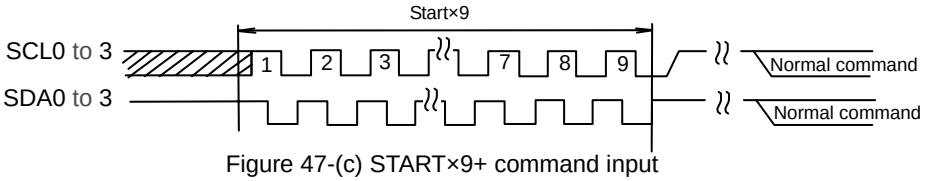


Figure 47-(c) START×9+ command input

*Start command from START input.

●Acknowledge polling

During internal write execution, all input commands are ignored, therefore ACK is not sent back. During internal automatic write execution after write cycle input, next command (slave address) is sent, and if the first ACK signal sends back 'L', then it means end of write action, while if it sends back 'H', it means now in writing. By use of acknowledge polling, next command can be executed without waiting for tWR = 5ms.

When to write continuously, R/$\overline{W}$ = 0, when to carry out current read cycle after write, slave address R/$\overline{W}$ = 1 is sent, and if ACK signal sends back 'L', then execute word address input and data output and so forth.

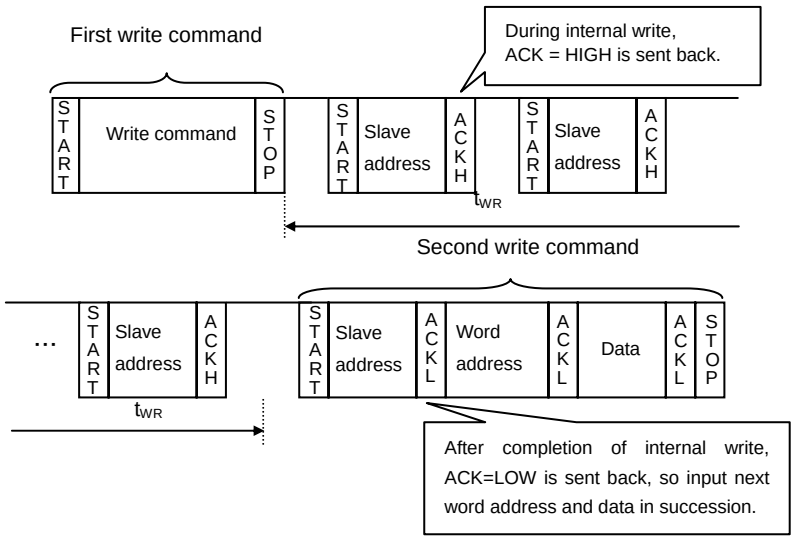


Figure 48. Case to continuously write by acknowledge polling

●Command cancel by start condition and stop condition

During command input, by continuously inputting start condition and stop condition, command can be cancelled.
(Refer to Figure 49.)
However, in ACK output area and during data read, SDA0 to 3 buses may output 'L', and in this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. And when command is cancelled by start, stop condition, during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined, therefore, it is not possible to carry out current read cycle in succession. When to carry out read cycle in accession, carry out random read cycle.

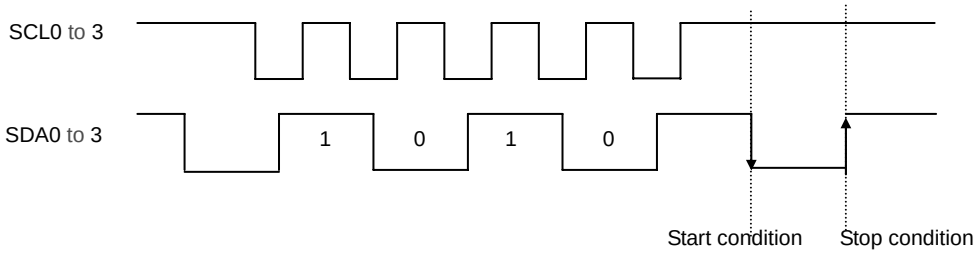


Figure 49. Case of cancel by start, stop condition during slave address input

●I/O peripheral circuit

○Pull up resistance of SDA0 to 3 terminal

SDA0 to 3 is NMOS open drain, so requires pull up resistance. As for this resistance value (R_{PU}), select an appropriate value to this resistance value from microcontroller V_{IL}, I_L, and $V_{OL}0$ to 3-I_{OL} characteristics of this IC. If R_{PU} is large, action frequency is limited. The smaller the R_{PU}, the larger the consumption current at action.

○Maximum value of R_{PU}

The maximum value of R_{PU} is determined by the following factors. The following V_{CC}, SDA, R_{PU} and I_L correspond to them of each port.

(1)SDA0 to 3 rise time to be determined by the capacitance (CBUS) of bus line of R_{PU} and SDA0 to 3 should be tR or below.

And AC timing should be satisfied even when SDA0 to 3 rise time is late.

(2)The bus electric potential Ⓐ to be determined by input leak total (I_L) of device connected to bus at output of 'H' to SDA0 to 3 bus and R_{PU} should sufficiently secure the input 'H' level (V_{IH}) of microcontroller and EEPROM including recommended noise margin 0.2V_{CC}.

$$Vcc - I_L R_{PU} - 0.2Vcc \geqq V_{IH}$$

$$\therefore \quad R_{PU} \leqq \frac{0.8Vcc - V_{IH}}{I_L}$$

Ex.) When V_{CC} =3V, I_L=10μA, V_{IH}=0.7 V_{CC},

from (2)

$$R_{PU} \leqq \frac{0.8 \times 3 - 0.7 \times 3}{10 \times 10^{-6}}$$

$$\leqq 300\ [k\Omega]$$

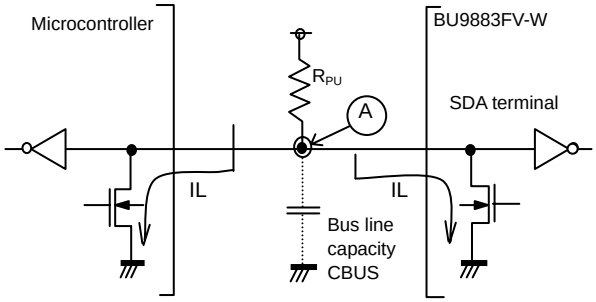


Figure 50. I/O circuit diagram

○Minimum value of R_{PU}

The minimum value of R_{PU} is determined by the following factors. The following V_{CC}, V_{OL}, I_{OL}, and R_{PU} correspond to them of each port.

(1)When IC outputs LOW, it should be satisfied that V_{OLMAX}=0.4V and I_{OLMAX}=3mA.

$$\frac{V_{CC} - V_{OL}}{R_{PU}} \leqq I_{OL} \qquad \therefore \quad R_{PU} \leqq \frac{Vcc - V_{OL}}{I_{OL}}$$

(2)V_{OLMAX}=0.4V should secure the input 'L' level (V_{IL}) of microcontroller and EEPROM including recommended noise margin 0.1V_{CC}.

$V_{OLMAX} \leqq V_{IL} - 0.1\ V_{CC}$

Ex.) When V_{CC} =3V, V_{OL}=0.4V, I_{OL}=3mA, microcontroller, EEPROM V_{IL}=0.3V_{CC}

from (1)

$$R_{PU} \geqq \frac{3 - 0.4}{3 \times 10^{-3}}$$

$$\geqq 867\ [\Omega]$$

And

$$V_{OL} = 0.4\ [V]$$

$$V_{IL} = 0.3 \times 3$$

$$= 0.9\ [V]$$

Therefore, the condition (2) is satisfied.

○Pull up resistance of SCL0 to 3 terminal

When SCL0 to 3 control is made at CMOS output port, there is no need, but in the case there is timing where SCL0 to 3 becomes 'Hi-Z', add a pull up resistance. As for the pull up resistance, one of several kΩ to several ten kΩ is recommended in consideration of drive performance of output port of microcontroller.

●Cautions on microcontroller connection

○Rs

In I2C BUS, it is recommended that SDA port is of open drain input/output. However, when to use CMOS input / output of tri state to SDA port, insert a series resistance Rs between the pull up resistance Rpu and the SDA terminal of EEPROM. This is controls over current that occurs when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. Rs also plays the role of protection of SDA terminal against surge. Therefore, even when SDA port is open drain input/output, Rs can be used. The following SCL SDA R_{PU} and R_S correspond to them of each port.

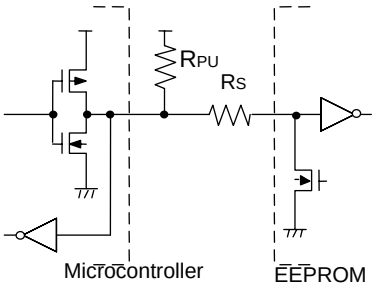


Figure 51. I/O circuit diagram

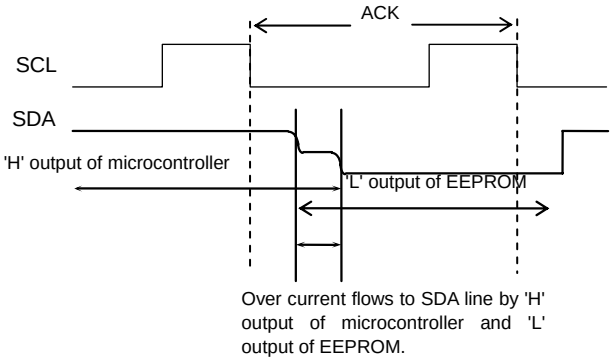


Figure 52. Input / output collision timing

○Maximum value of Rs

The maximum value of Rs is determined by the following relations. The following V_{CC}, V_{OL}, R_S, R_{PU}, I_{OL}, and SDA correspond to them of each port.

(1)SDA rise time to be determined by the capacity (CBUS) of bus line of Rpu and SDA should be tR or below.
And AC timing should be satisfied even when SDA rise time is late.

(2)The bus electric potential Ⓐ to be determined by Rpu and Rs the moment when EEPROM outputs 'L' to SDA bus should sufficiently secure the input 'L' level (V_{IL}) of microcontroller including recommended noise margin 0.1V_{CC}.

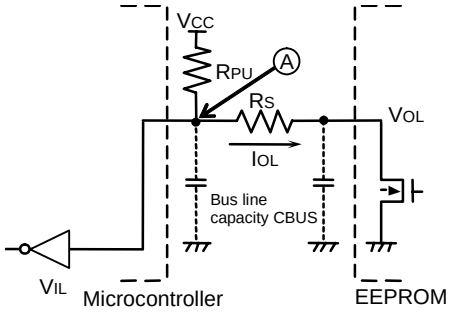


Figure 53. I/O circuit diagram

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S} + V_{OL}+0.1V_{CC} \leqq V_{IL}$$

$$\therefore \quad R_S \leqq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

Example) When V_{CC}=3V, V_{IL}=0.3V_{CC}, V_{OL}=0.4V, R_{PU}=20kΩ,

$$\text{from (2)}, \quad R_S \leqq \frac{0.3\times3-0.4-0.1\times3}{1.1\times3-0.3\times3} \times 20\times10^3$$

$$\leqq 1.67\,[k\Omega]$$

○Minimum value of Rs

The minimum value of Rs is determined by over current at bus collision. When over current flows, noises in power source line, and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of impedance of power source line in set and so forth. Set the over current to EEPROM 10mA or below. The following V_{CC}, R_{PU}, R_S, and I correspond to them of each port.

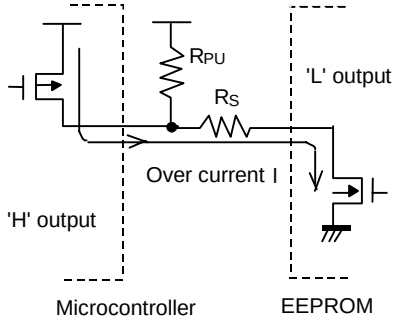


Figure 54. I/O circuit diagram

$$\frac{V_{CC}}{R_S} \leqq I$$

$$\therefore \quad R_S \geqq \frac{V_{CC}}{I}$$

Example) When V_{CC}=3V, I=10mA

$$R_S \geqq \frac{3}{10\times10^{-3}}$$

$$\geqq 300\,[\Omega]$$

●**I²C BUS input / output circuit**

○Input (SCL0 to 3)

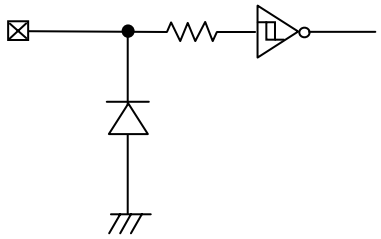


Figure 55. Input pin circuit diagram

○Input / output (SDA0 to 3)

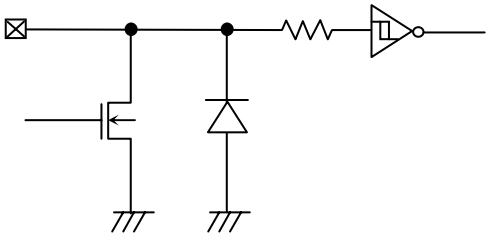


Figure 56.Input / output pin circuit diagram

○Input (WPB)

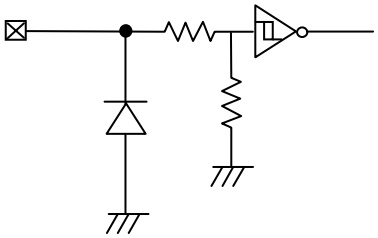


Figure 57. Input pin circuit diagram

●**Notes on power ON**

At power on, in IC internal circuit and set, Vcc rises through unstable low voltage area, and IC inside is not completely reset, and malfunction may occur. To prevent this, functions of POR circuit and LVCC circuit are equipped. To assure the action, observe the following conditions at power on.

1. Set SDA0 to 3 = 'H' and SCL0 to 3 ='L' or 'H'
2. Start power source so as to satisfy the recommended conditions of t_R, t_{OFF}, and Vbot for operating POR circuit.

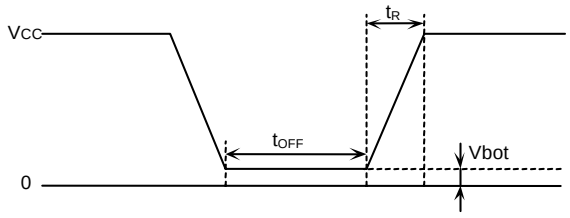


Figure 58. Rise waveform diagram

Recommended conditions of t_R, t_{OFF},Vbot

t_R	t_{OFF}	Vbot
10ms or below	10ms or longer	0.3V or below
100ms or below	10ms or longer	0.2V or below

3. Set SDA0 to 3 and SCL0 to 3 so as not to become 'Hi-Z'.
When the above conditions 1 and 2 cannot be observed, take the following countermeasures.
a) In the case when the above condition 1 cannot be observed. When SDA0 to 3 becomes 'L' at power on.
→Control SCL0 to 3 and SDA0 to 3 as shown below, to make SCL0 to 3 and SDA0 to 3, 'H' and 'H'.

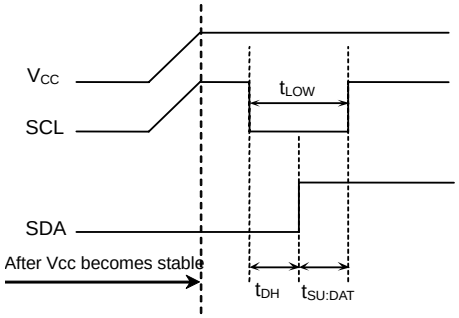


Figure 59. When SCL0 to 3= 'H' and SDA0 to 3= 'L'

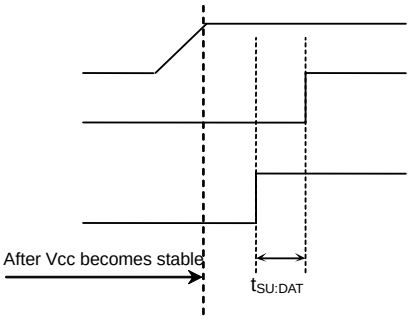


Figure 60. When SCL0 to 3='L' and SDA0 to 3='L'

b) In the case when the above condition 2 cannot be observed.
→After power source becomes stable, execute software reset(Page 19).
c) In the case when the above conditions 1 and 2 cannot be observed.
→Carry out a), and then carry out b).

●Low voltage malfunction prevention function

LVCC circuit prevents data rewrite action at low power, and prevents wrong write. At LVCC voltage (Typ. =1.2V) or below, it prevent data rewrite.

●Vcc noise countermeasures

○Bypass capacitor

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1μF) between IC VCCOUT and GND. At that moment, attach it as close to IC as possible. And, it is also recommended to attach a bypass capacitor between board VCCOUT and GND.

●Cautions on use

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute maximum ratings

If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential

Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

(5) Terminal design

In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal shortcircuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

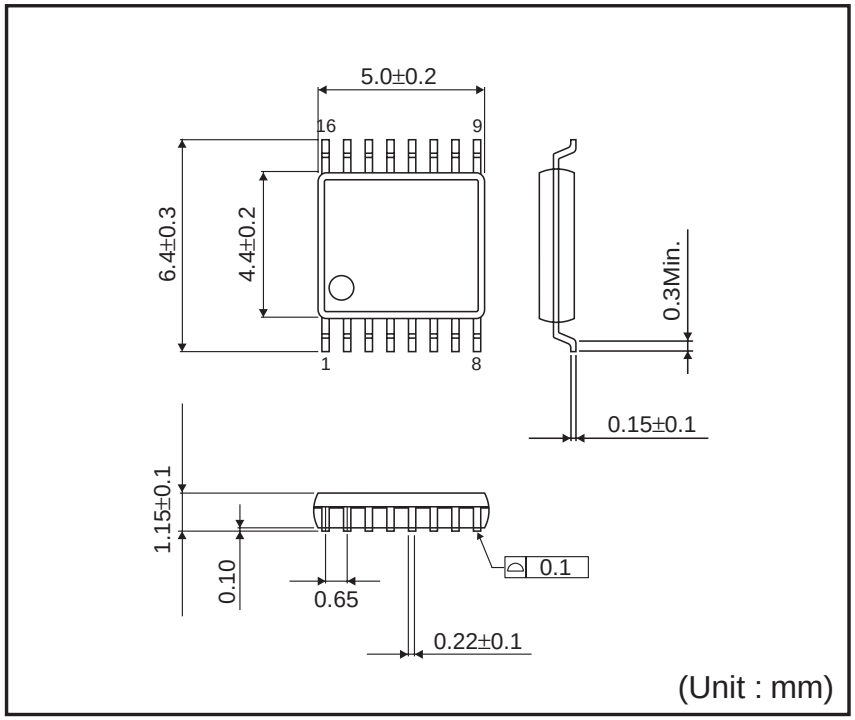
Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority.

●**Ordering Information**

B U 9 8 8 3 F V - W	E 2
Part Number	Package FV: SSOP-B16
	Packaging and forming specification E2: Embossed tape and reel

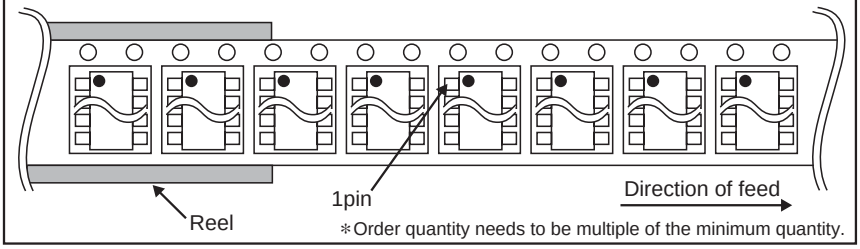
●**Physical Dimension Tape and Reel Information**

SSOP-B16 (BU9883FV-W)



<Tape and Reel information>

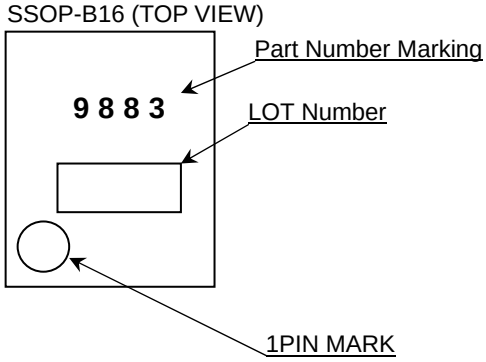
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●**Marking Diagram**

SSOP-B16 (TOP VIEW)



●**Revision History**

Date	Revision	Changes
30.Aug.2012	001	New Release

Notice

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1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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