

# CAT34TS02

## Digital Output Temperature Sensor with On-board SPD EEPROM

### Description

The CAT34TS02 combines a JC42.4 compliant Temperature Sensor (TS) with 2-Kb of Serial Presence Detect (SPD) EEPROM.

The TS measures temperature at least 10 times every second. Temperature readings can be retrieved by the host via the serial interface, and are compared to high, low and critical trigger limits stored into internal registers. Over or under limit conditions can be signaled on the open-drain **EVENT** pin.

The integrated 2-Kb SPD EEPROM is internally organized as 16 pages of 16 bytes each, for a total of 256 bytes. It features a page write buffer and supports both the Standard (100 kHz) as well as Fast (400 kHz) I<sup>2</sup>C protocol.

Write operations to the lower half memory can be inhibited via software commands. The CAT34TS02 features Permanent, as well as Reversible Software Write Protection, as defined for DDR3 DIMMs.

### Features

- JEDEC JC42.4 Compliant Temperature Sensor
- Temperature Range: -20°C to +125°C
- DDR3 DIMM Compliant SPD EEPROM
- Supply Range: 3.3 V ± 10%
- I<sup>2</sup>C / SMBus Interface
- Schmitt Triggers and Noise Suppression Filters on SCL and SDA Inputs
- Low Power CMOS Technology
- 2 x 3 x 0.75 mm TDFN Package and 2 x 3 x 0.5 mm UDFN Package
- These Devices are Pb-Free and are RoHS Compliant

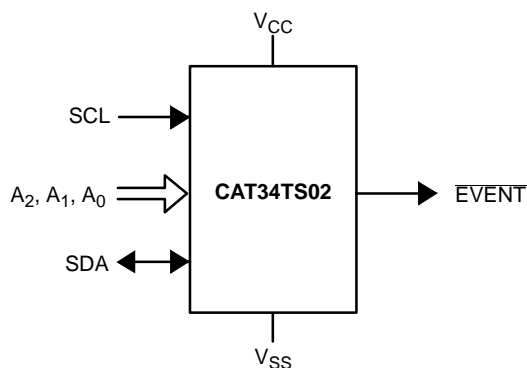


Figure 1. Functional Symbol



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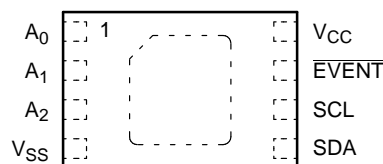


**TDFN-8**  
**VP2 SUFFIX**  
**CASE 511AK**



**UDFN-8**  
**HU4 SUFFIX**  
**CASE 517AZ**

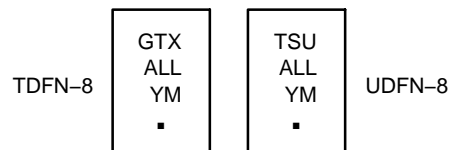
### PIN CONFIGURATION



(Top View)

For the location of Pin 1, please consult the corresponding package drawing.

### MARKING DIAGRAM



GTX, TSU = Specific Device Code  
A = Assembly Location Code  
LL = Assembly Lot Number (Last Two Digits)  
Y = Production Year (Last Digit)  
M = Production Month (1 – 9, O, N, D)  
■ = Pb-Free Package

### PIN FUNCTIONS

| Pin Name                                         | Function                                |
|--------------------------------------------------|-----------------------------------------|
| A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> | Device Address Input                    |
| SDA                                              | Serial Data Input/Output                |
| SCL                                              | Serial Clock Input                      |
| EVENT                                            | Open-drain Event Output                 |
| V <sub>CC</sub>                                  | Power Supply                            |
| V <sub>SS</sub>                                  | Ground                                  |
| DAP                                              | Backside Exposed DAP at V <sub>SS</sub> |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 21 of this data sheet.

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**Table 1. ABSOLUTE MAXIMUM RATINGS**

| Parameter                                                                   | Rating        | Units |
|-----------------------------------------------------------------------------|---------------|-------|
| Operating Temperature                                                       | –45 to +130   | °C    |
| Storage Temperature                                                         | –65 to +150   | °C    |
| Voltage on any pin (except A <sub>0</sub> ) with respect to Ground (Note 1) | –0.5 to +6.5  | V     |
| Voltage on pin A <sub>0</sub> with respect to Ground                        | –0.5 to +10.5 | V     |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The DC input voltage on any pin should not be lower than –0.5 V or higher than  $V_{CC} + 0.5$  V. The A<sub>0</sub> pin can be raised to a HV level for RSWP command execution. SCL and SDA inputs can be raised to the maximum limit, irrespective of  $V_{CC}$ .

**Table 2. RELIABILITY CHARACTERISTICS**

| Symbol                    | Parameter               | Min       | Units        |
|---------------------------|-------------------------|-----------|--------------|
| N <sub>END</sub> (Note 2) | Endurance (EEPROM)      | 1,000,000 | Write Cycles |
| T <sub>DR</sub>           | Data Retention (EEPROM) | 100       | Years        |

2. Page Mode,  $V_{CC} = 3.3$  V, 25°C

**Table 3. TEMPERATURE CHARACTERISTICS** ( $V_{CC} = 3.3$  V  $\pm$  10%,  $T_A = -20^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise specified)

| Parameter                                              | Test Conditions/Comments                                             | Max       | Unit |
|--------------------------------------------------------|----------------------------------------------------------------------|-----------|------|
| Temperature Reading Error<br>Class B, JC42.4 compliant | $+75^\circ\text{C} \leq T_A \leq +95^\circ\text{C}$ , active range   | $\pm 1.0$ | °C   |
|                                                        | $+40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , monitor range | $\pm 2.0$ | °C   |
|                                                        | $-20^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , sensing range | $\pm 3.0$ | °C   |
| ADC Resolution                                         |                                                                      | 12        | Bits |
| Temperature Resolution                                 |                                                                      | 0.0625    | °C   |
| Conversion Time                                        |                                                                      | 100       | ms   |
| Thermal Resistance (Note 3) $\theta_{JA}$              | Junction-to-Ambient (Still Air)                                      | 92        | °C/W |

3. Power Dissipation is defined as  $P_J = (T_J - T_A)/\theta_{JA}$ , where  $T_J$  is the junction temperature and  $T_A$  is the ambient temperature. The thermal resistance value refers to the case of a package being used on a standard 2-layer PCB.

**Table 4. D.C. OPERATING CHARACTERISTICS** ( $V_{CC} = 3.3$  V  $\pm$  10%,  $T_A = -20^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise specified)

| Symbol            | Parameter               | Test Conditions/Comments                 | Min                 | Max                 | Unit |
|-------------------|-------------------------|------------------------------------------|---------------------|---------------------|------|
| I <sub>CC</sub>   | Supply Current          | TS active, SPD and Bus idle              |                     | 500                 | μA   |
|                   |                         | SPD Write, TS shut-down                  |                     | 500                 | μA   |
| I <sub>SHDN</sub> | Standby Current         | TS shut-down; SPD and Bus idle           |                     | 10                  | μA   |
| I <sub>LKG</sub>  | I/O Pin Leakage Current | Pin at GND or $V_{CC}$                   |                     | 2                   | μA   |
| V <sub>IL</sub>   | Input Low Voltage       |                                          | –0.5                | $0.3 \times V_{CC}$ | V    |
| V <sub>IH</sub>   | Input High Voltage      |                                          | $0.7 \times V_{CC}$ | $V_{CC} + 0.5$      | V    |
| V <sub>OL1</sub>  | Output Low Voltage      | I <sub>OL</sub> = 3 mA, $V_{CC} > 2.7$ V |                     | 0.4                 | V    |
| V <sub>OL2</sub>  | Output Low Voltage      | I <sub>OL</sub> = 1 mA, $V_{CC} < 2.7$ V |                     | 0.2                 | V    |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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**Table 5. PIN IMPEDANCE CHARACTERISTICS** ( $V_{CC} = 3.3 \text{ V} \pm 10\%$ ,  $T_A = -20^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise specified)

| Symbol               | Parameter                                                  | Conditions                                   | Max | Units         |
|----------------------|------------------------------------------------------------|----------------------------------------------|-----|---------------|
| $C_{IN}$<br>(Note 4) | SDA, EVENT Pin Capacitance                                 | $V_{IN} = 0 \text{ V}$ , $f = 1 \text{ MHz}$ | 8   | pF            |
|                      | Input Capacitance (other pins)                             |                                              | 6   |               |
| $I_A$<br>(Note 5)    | Address Input Current (A0, A1, A2)<br><b>Product Rev C</b> | $V_{IN} < V_{IH}$                            | 35  | $\mu\text{A}$ |
|                      |                                                            | $V_{IN} > V_{IH}$                            | 2   |               |

- These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
- When not driven, the A0, A1 and A2 pins are pulled down to GND internally. For improved noise immunity, the internal pull-down is relatively strong; therefore the external driver must be able to supply the pull-down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer ( $\sim 0.5 \times V_{CC}$ ), the strong pull-down reverts to a weak current source.

**Table 6. A.C. CHARACTERISTICS** ( $V_{CC} = 3.3 \text{ V} \pm 10\%$ ,  $T_A = -20^\circ\text{C}$  to  $+125^\circ\text{C}$ ) (Note 6)

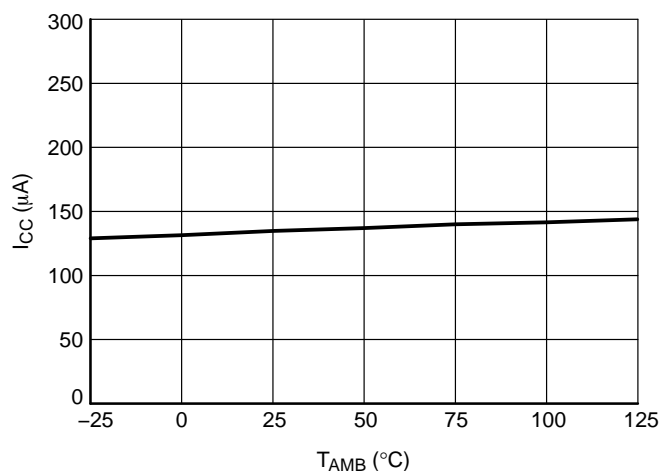
| Symbol                 | Parameter                                     | Min  | Max | Units |
|------------------------|-----------------------------------------------|------|-----|-------|
| $F_{SCL}$ (Note 7)     | Clock Frequency                               | 10   | 400 | kHz   |
| $t_{HIGH}$             | High Period of SCL Clock                      | 600  |     | ns    |
| $t_{LOW}$              | Low Period of SCL Clock                       | 1300 |     | ns    |
| $t_{TIMEOUT}$ (Note 7) | SMBus SCL Clock Low Timeout                   | 25   | 35  | ms    |
| $t_R$ (Note 8)         | SDA and SCL Rise Time                         |      | 300 | ns    |
| $t_F$ (Note 8)         | SDA and SCL Fall Time                         |      | 300 | ns    |
| $t_{SU:DAT}$ (Note 9)  | Data Setup Time                               | 100  |     | ns    |
| $t_{SU:STA}$           | START Condition Setup Time                    | 600  |     | ns    |
| $t_{HD:STA}$           | START Condition Hold Time                     | 600  |     | ns    |
| $t_{SU:STO}$           | STOP Condition Setup Time                     | 600  |     | ns    |
| $t_{BUF}$              | Bus Free Time Between STOP and START          | 1300 |     | ns    |
| $t_{HD:DAT}$           | Input Data Hold Time                          | 0    |     | ns    |
| $t_{DH}$ (Note 8)      | Output Data Hold Time                         | 200  | 900 | ns    |
| $T_i$                  | Noise Pulse Filtered at SCL and SDA Inputs    |      | 100 | ns    |
| $t_{WR}$               | Write Cycle Time                              |      | 5   | ms    |
| $t_{PU}$ (Note 10)     | Power-up Delay to Valid Temperature Recording |      | 100 | ms    |

- Timing reference points are set at 30%, respectively 70% of  $V_{CC}$ , as illustrated in Figure 23. Bus loading must be such as to allow meeting the  $V_{IL}$ ,  $V_{OL}$  as well as the various timing limits.
- For the CAT34TS02 Rev. B, the TS interface will reset itself and will release the SDA line if the SCL line stays low beyond the  $t_{TIMEOUT}$  limit. The time-out count-down is activated in the interval between START and STOP when SCL is low and is reset while SCL is high. The minimum clock frequency of 10 kHz is an SMBus recommendation; the minimum operating clock frequency for the CAT34TS02's SPD component is DC, while the minimum operating frequency for the TS component is limited only by the SMBus time-out. For the CAT34TS02 Rev. C, both the TS and the SPD implement the time-out feature.
- In a "Wired-OR" system (such as I<sup>2</sup>C or SMBus), SDA rise time is determined by bus loading. Since each bus pull-down device must be able to sink the (external) bus pull-up current (in order to meet the  $V_{IL}$  and/or  $V_{OL}$  limits), it follows that SDA fall time is inherently faster than SDA rise time. SDA rise time can exceed the standard recommended  $t_R$  limit, as long as it does not exceed  $t_{LOW} - t_{DH} - t_{SU:DAT}$ , where  $t_{LOW}$  and  $t_{DH}$  are actual values (rather than spec limits). A shorter  $t_{DH}$  leaves more room for a longer SDA  $t_R$ , allowing for a more capacitive bus or a larger bus pull-up resistor. At the minimum  $t_{LOW}$  spec limit of 1300 ns, the maximum  $t_{DH}$  of 900 ns demands a maximum SDA  $t_R$  of 300 ns. The CAT34TS02's maximum  $t_{DH}$  is <700 ns, thus allowing for an SDA  $t_R$  of up to 500 ns at minimum  $t_{LOW}$ .
- The minimum  $t_{SU:DAT}$  of 100 ns is a limit recommended by standards. The CAT34TS02 will accept a  $t_{SU:DAT}$  of 0 ns.
- The first valid temperature recording can be expected after  $t_{PU}$  at nominal supply voltage.

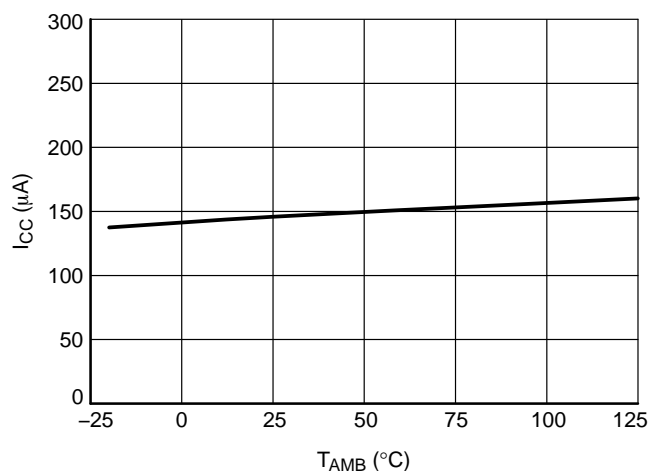
# CAT34TS02

## TYPICAL PERFORMANCE CHARACTERISTICS

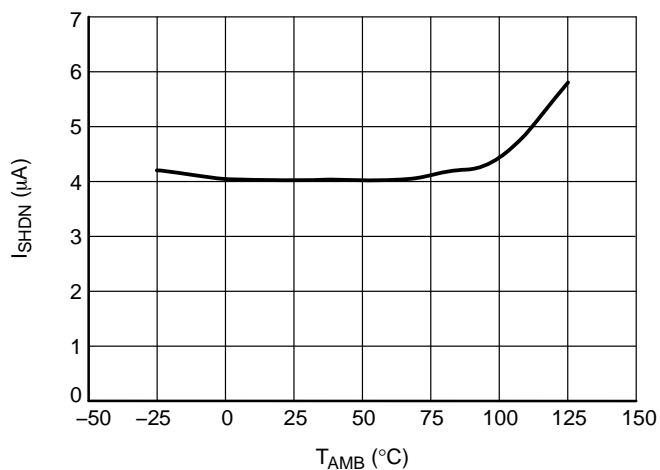
( $V_{CC} = 3.3\text{ V}$ ,  $T_A = -20^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise specified.)



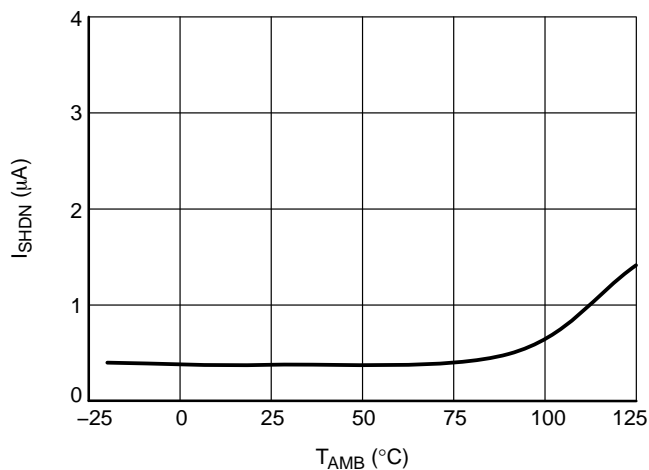
**Figure 2. TS Active Current (Rev. B)**  
(I<sup>2</sup>C-bus and SPD EEPROM Idle)



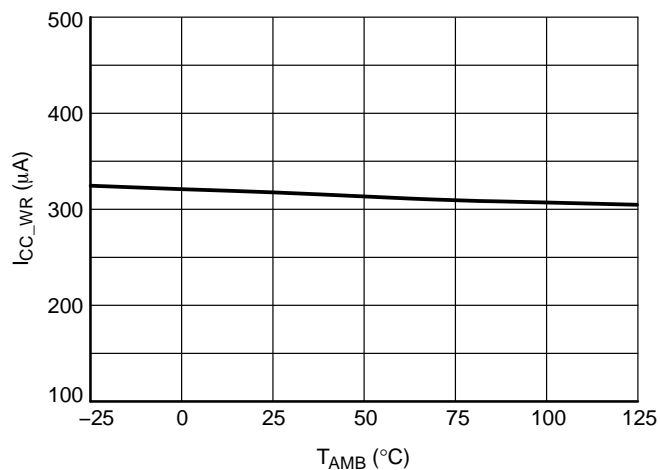
**Figure 3. TS Active Current (Rev. C)**  
(I<sup>2</sup>C-bus and SPD EEPROM Idle)



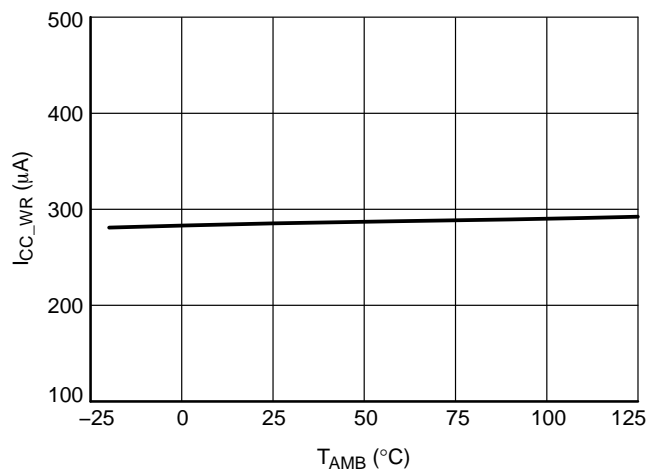
**Figure 4. Standby Current (Rev. B)** (I<sup>2</sup>C-bus and SPD EEPROM Idle, TS Shut-down)



**Figure 5. Standby Current (Rev. C)** (I<sup>2</sup>C-bus and SPD EEPROM Idle, TS Shut-down)



**Figure 6. SPD EEPROM Write Current (Rev. B)**  
(I<sup>2</sup>C-bus Idle, TS Shut-down)



**Figure 7. SPD EEPROM Write Current (Rev. C)**  
(I<sup>2</sup>C-bus Idle, TS Shut-down)

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## TYPICAL PERFORMANCE CHARACTERISTICS

( $V_{CC} = 3.3\text{ V}$ ,  $T_A = -20^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise specified.)

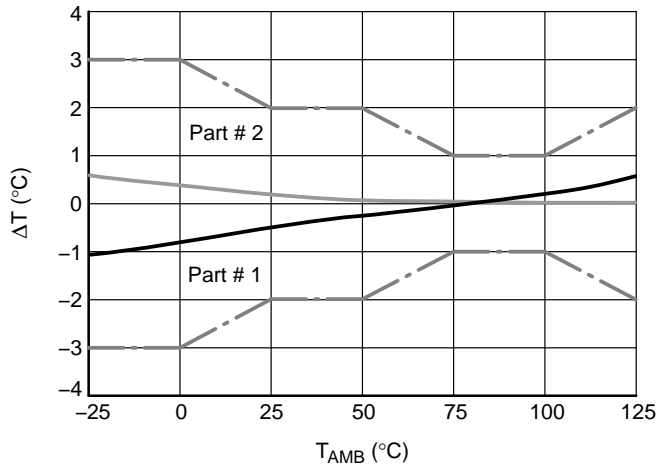


Figure 8. Temperature Read-Out Error (Rev. B)

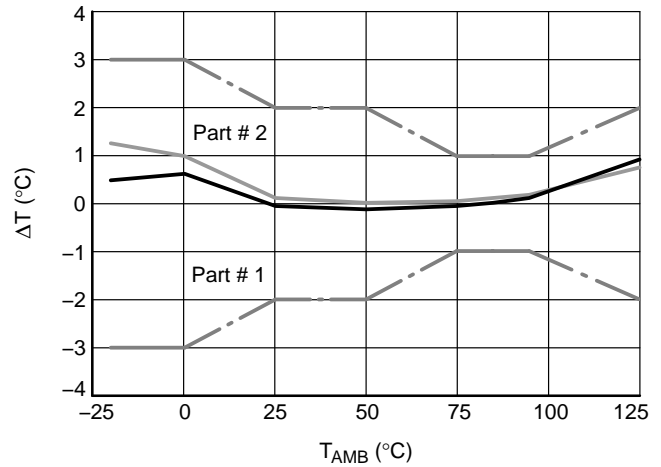


Figure 9. Temperature Read-Out Error (Rev. C)

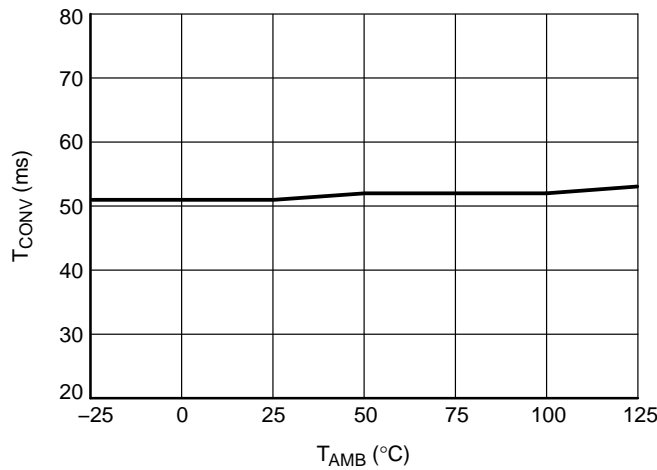


Figure 10. A/D Conversion Time (Rev. B)

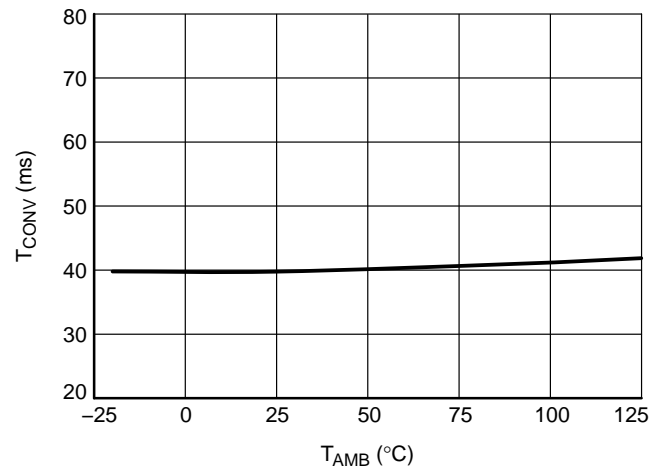


Figure 11. A/D Conversion Time (Rev. C)

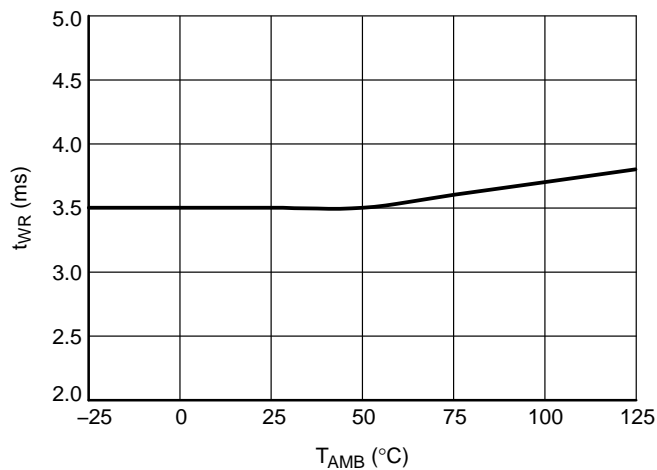


Figure 12. EEPROM Write Time (Rev. B)

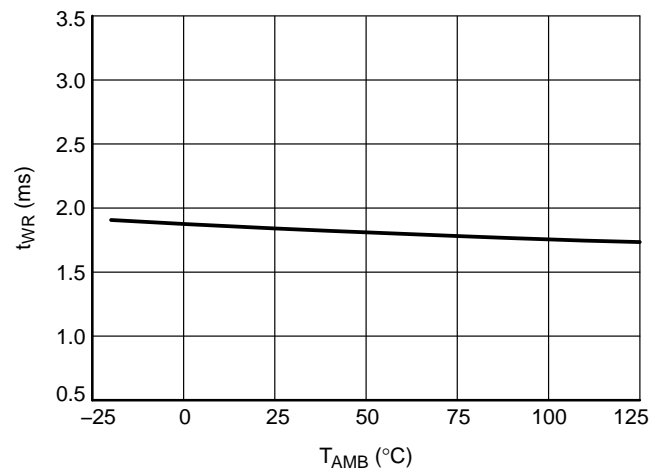


Figure 13. EEPROM Write Time (Rev. C)

# CAT34TS02

## TYPICAL PERFORMANCE CHARACTERISTICS

( $V_{CC} = 3.3\text{ V}$ ,  $T_A = -20^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise specified.)

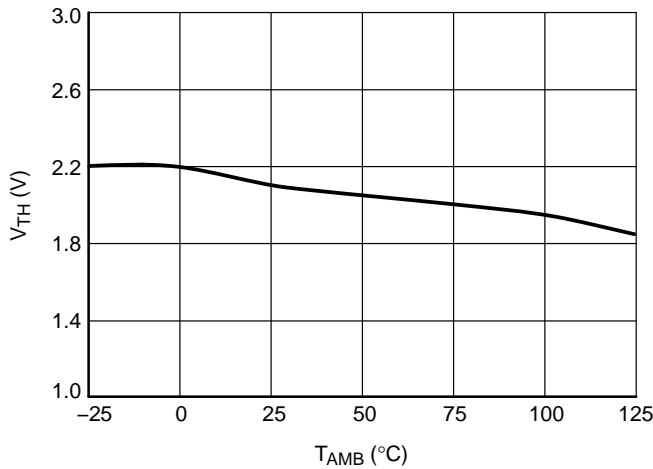


Figure 14. TS POR Threshold Voltage (Rev. B)

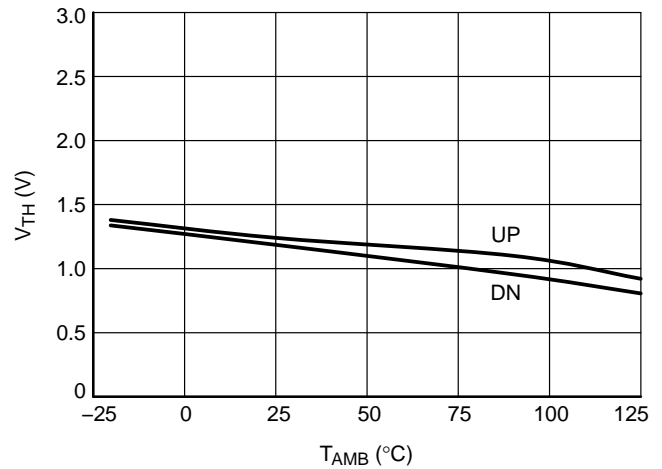


Figure 15. TS POR Threshold Voltage (Rev. C)

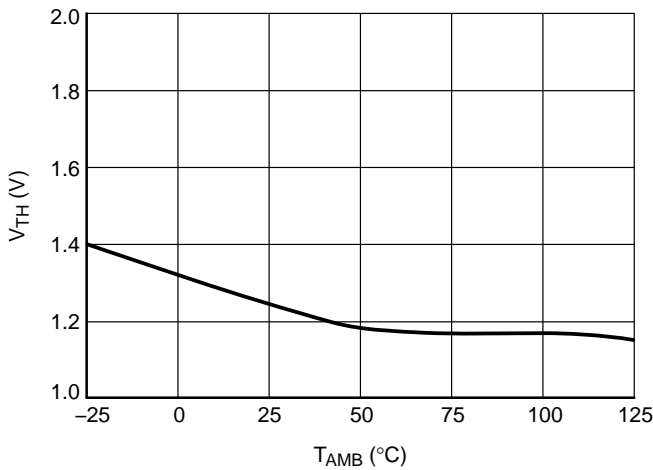


Figure 16. SPD POR Threshold Voltage (Rev. B)

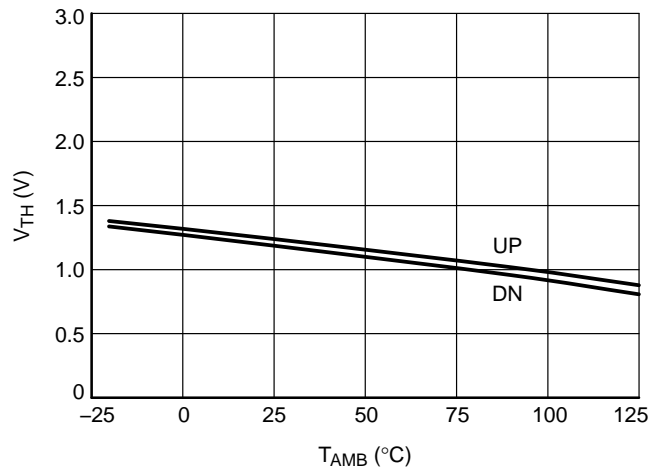


Figure 17. SPD POR Threshold Voltage (Rev. C)

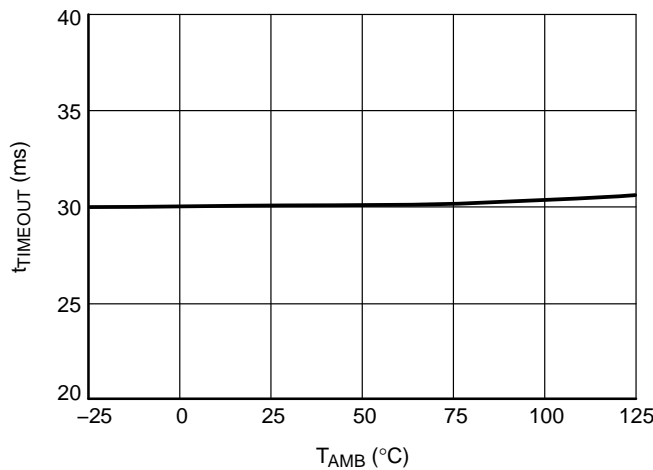


Figure 18. SMBus SCL Clock Low Timeout (Rev. B)

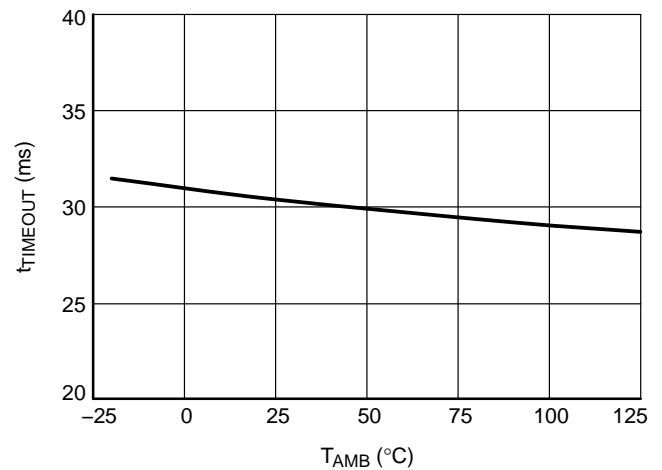


Figure 19. SMBus SCL Clock Low Timeout (Rev. C)

## Pin Description

**SCL:** The Serial Clock input pin accepts the Serial Clock generated by the Master (Host).

**SDA:** The Serial Data I/O pin receives input data and transmits data stored in the internal registers. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

**A0, A1 and A2:** The Address pins accept the device address. These pins have on-chip pull-down resistors.

**EVENT:** The open-drain  $\overline{\text{EVENT}}$  pin can be programmed to signal over/under temperature limit conditions.

## Power-On Reset (POR)

The CAT34TS02 incorporates Power-On Reset (POR) circuitry which protects the device against powering up to invalid state. The TS component will power up into conversion mode after  $V_{CC}$  exceeds the TS POR trigger level and the SPD component will power up into standby mode after  $V_{CC}$  exceeds the SPD POR trigger level. Both the TS and SPD components will power down into Reset mode when  $V_{CC}$  drops below their respective POR trigger levels. This bi-directional POR behavior protects the CAT34TS02 against brown-out failure following a temporary loss of power. The POR trigger levels are set below the minimum operating  $V_{CC}$  level.

## Device Interface

The CAT34TS02 supports the Inter-Integrated Circuit ( $I^2C$ ) and the System Management Bus (SMBus) data transmission protocols. These protocols describe serial communication between transmitters and receivers sharing a 2-wire data bus. Data flow is controlled by a Master device, which generates the serial clock and the START and STOP conditions. The CAT34TS02 acts as a Slave device. Master and Slave alternate as transmitter and receiver. Up to 8 CAT34TS02 devices may be present on the bus simultaneously, and can be individually addressed by matching the logic state of the address inputs A0, A1, and A2.

## $I^2C$ /SMBus Protocol

The  $I^2C$ /SMBus uses two 'wires', one for clock (SCL) and one for data (SDA). The two wires are connected to the  $V_{CC}$

supply via pull-up resistors. Master and Slave devices connect to the bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 20).

## START

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake-up' call to all Slaves. Absent a START, a Slave will not respond to commands.

## STOP

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP tells the Slave that no more data will be written to or read from the Slave.

## Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. The first 4 bits of the Slave address (the preamble) select either the Temperature Sensor (TS) registers (0011) or the EEPROM memory contents (1010), as shown in Figure 21. The next 3 bits, A2, A1 and A0, select one of 8 possible Slave devices. The last bit,  $R/\overline{W}$ , specifies whether a Read (1) or Write (0) operation is being performed.

## Acknowledge

A matching Slave address is acknowledged (ACK) by the Slave by pulling down the SDA line during the 9<sup>th</sup> clock cycle (Figure 22). After that, the Slave will acknowledge all data bytes sent to the bus by the Master. When the Slave is the transmitter, the Master will in turn acknowledge data bytes in the 9<sup>th</sup> clock cycle. The Slave will stop transmitting after the Master does not respond with acknowledge (NoACK) and then issues a STOP. Bus timing is illustrated in Figure 23.

# CAT34TS02

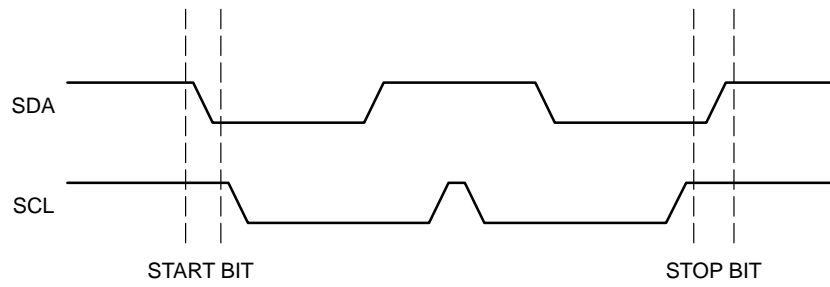


Figure 20. Start/Stop Timing

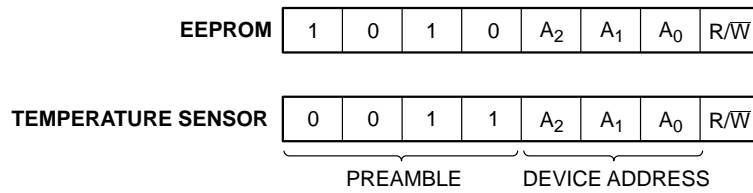


Figure 21. Slave Address Bits

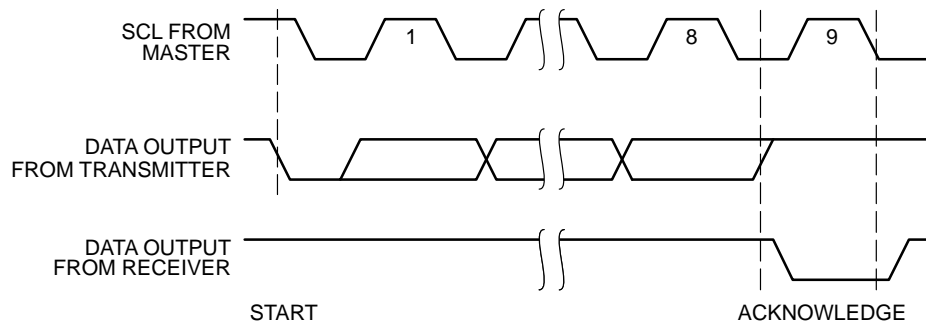


Figure 22. Acknowledge Timing

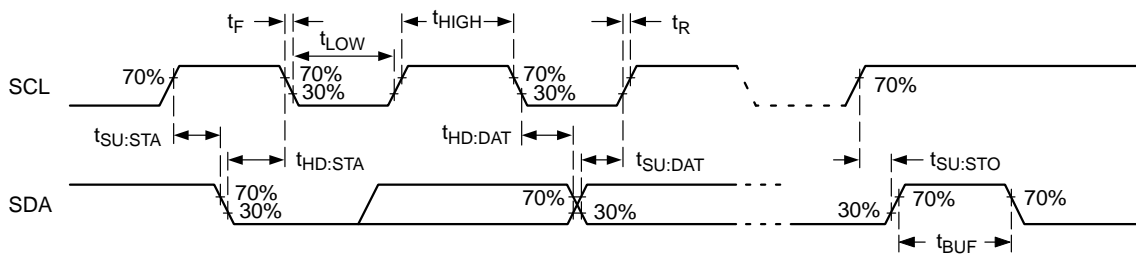


Figure 23. Bus Timing



## Write Operations

### EEPROM Byte and TS Register Write

To write data to a TS register, or to the on-board EEPROM, the Master creates a START condition on the bus, and then sends out the appropriate Slave address (with the  $R/\overline{W}$  bit set to '0'), followed by an address byte and data byte(s). The matching Slave will acknowledge the Slave address, EEPROM byte address or TS register address and the data byte(s), one for EEPROM data (Figure 24) and two for TS register data (Figure 25). The Master then ends the session by creating a STOP condition on the bus. The STOP completes the (volatile) TS register update or starts the internal Write cycle for the (non-volatile) EEPROM data (Figure 26).

### EEPROM Page Write

The on-board EEPROM contains 256 bytes of data, arranged in 16 pages of 16 bytes each. A page is selected by the 4 most significant bits of the address byte immediately following the Slave address, while the 4 least significant bits point to the byte within the page. Up to 16 bytes can be written in one Write cycle (Figure 27).

The internal EEPROM byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 16 data bytes, then earlier data will be overwritten by later data in a 'wrap-around' fashion within the selected page. The internal Write cycle, using the most recently loaded data, then starts immediately following the STOP.

### Acknowledge Polling

Acknowledge polling can be used to determine if the CAT34TS02 is busy writing to EEPROM, or is ready to accept commands. Polling is executed by interrogating the device with a 'Selective Read' command (see READ OPERATIONS). The CAT34TS02 will not acknowledge the Slave address as long as internal EEPROM Write is in progress.

### Delivery State

The CAT34TS02 is shipped 'unprotected', i.e. neither Software Write Protection (SWP) flag is set. The entire 2-Kb memory is erased, i.e. all bytes are 0xFF.

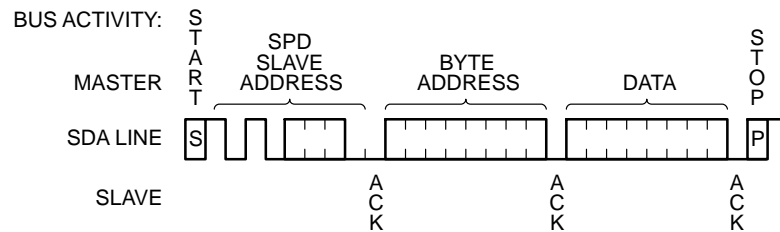


Figure 24. EEPROM Byte Write

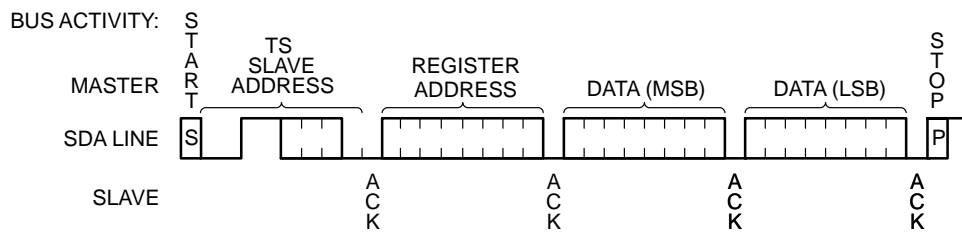


Figure 25. Temperature Sensor Register Write

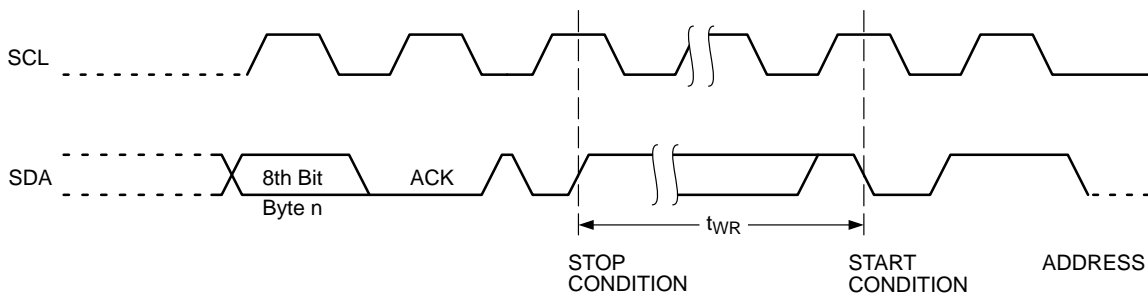
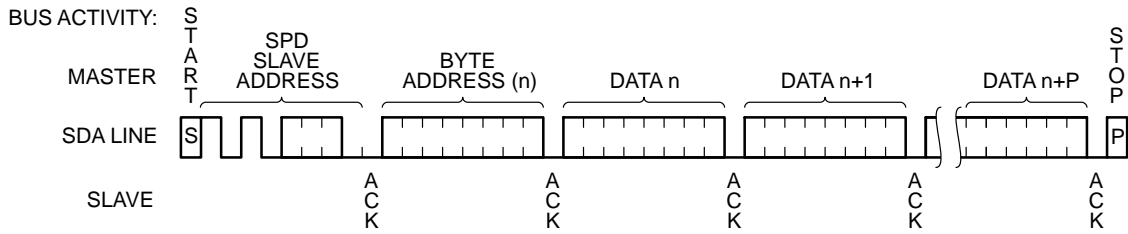


Figure 26. EEPROM Write Cycle Timing



NOTE: In this example  $n = \text{XXXX } 0000(\text{B})$ ;  $X = 1 \text{ or } 0$

Figure 27. EEPROM Page Write

## Read Operations

### Immediate Read

Upon power-up, the address counters for both the Temperature Sensor (TS) and on-board EEPROM are initialized to 00h. The TS address counter will thus point to the Capability Register and the EEPROM address counter will point to the first location in memory. The two address counters may be updated by subsequent operations.

A CAT34TS02 presented with a Slave address containing a '1' in the  $R/\overline{W}$  position will acknowledge the Slave address and will then start transmitting data being pointed at by the current EEPROM data or respectively TS register address counter. The Master stops this transmission by responding with NoACK, followed by a STOP (Figures 28a, 28b).

### Selective Read

The Read operation can be started at an address different from the one stored in the respective address counters, by preceding the Immediate Read sequence with a 'data less' Write operation. The Master sends out a START, Slave address and address byte, but rather than following up with data (as in a Write operation), the Master then issues another START and continuous with an Immediate Read sequence (Figures 29a, 29b).

### Sequential EEPROM Read

EEPROM data can be read out indefinitely, as long as the Master responds with ACK (Figure 30). The internal address count is automatically incremented after every data byte sent to the bus. If the end of memory is reached during continuous Read, then the address counter 'wraps-around' to beginning of memory, etc. Sequential Read works with either Immediate Read or Selective Read, the only difference being that in the latter case the starting address is intentionally updated.

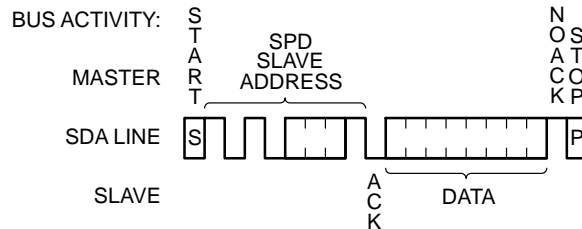


Figure 28a. EEPROM Immediate Read

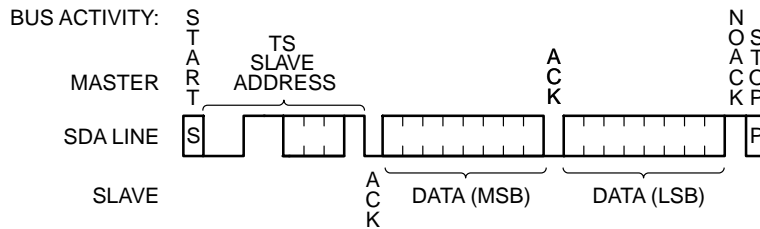
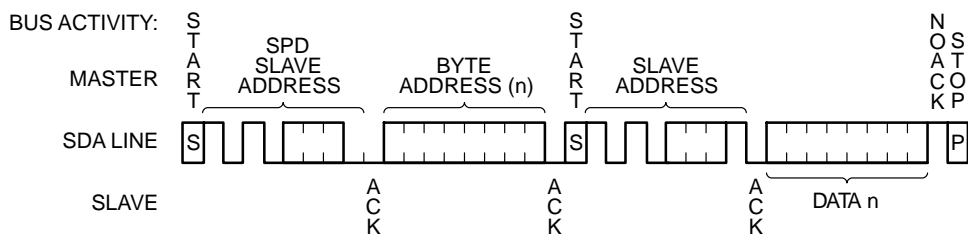
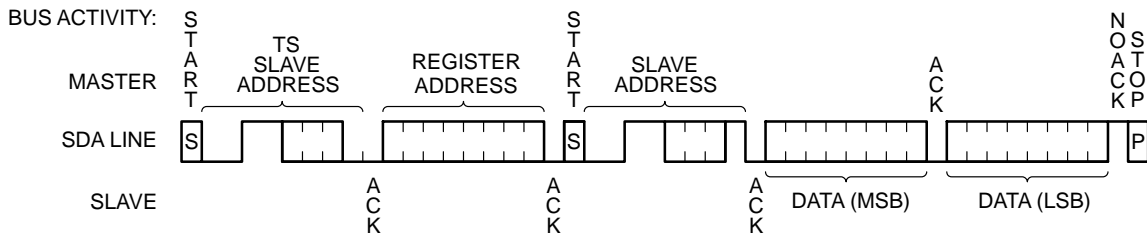


Figure 28b. Temperature Sensor Immediate Read

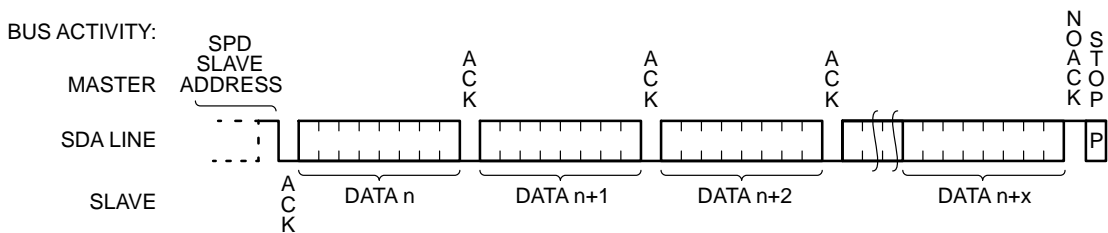
# CAT34TS02



### Figure 29a. EEPROM Selective Read



### Figure 29b. Temperature Sensor Selective Read



### Figure 30. EEPROM Sequential Read

## Software Write Protection

The lower half of memory (first 128 bytes) can be protected against Write requests by setting one of two Software Write Protection (SWP) flags.

The Permanent Software Write Protection (PSWP) flag can be set or read while all address pins are at regular CMOS levels (GND or  $V_{CC}$ ), whereas the very high voltage  $V_{HV}$  must be present on address pin A0 to set, clear or read the Reversible Software Write Protection (RSWP) flag. The D.C. OPERATING CONDITIONS for RSWP operations are shown in Table 7.

The SWP commands are listed in Table 8. All commands are preceded by a START and terminated with a STOP, following the ACK or NoACK from the CAT34TS02. All SWP related Slave addresses use the pre-*amble*: 0110 (6h), instead of the regular 1010 (Ah) used for memory access. For **PSWP** commands, the three address pins can be at any

logic level, whereas for **RSWP** commands the address pins must be at pre-assigned logic levels.

**V<sub>HV</sub> is interpreted as logic ‘1’. The V<sub>HV</sub> condition must be established on pin A0 before the START and maintained just beyond the STOP. Otherwise an RSWP request could be interpreted by the CAT34TS02 as a PSWP request.**

The SWP Slave addresses follow the standard I<sup>2</sup>C convention, i.e. to read the state of the SWP flag, the LSB of the Slave address must be ‘1’, and to set or clear a flag, it must be ‘0’. For Write commands a dummy byte address and dummy data byte must be provided (Figure 31). In contrast to a regular memory Read, a SWP Read does not return data. Instead the CAT34TS02 will respond with NoACK if the flag is set and with ACK if the flag is not set. Therefore, the Master can immediately follow up with a STOP, as there is no meaningful data following the ACK interval (Figure 32).

Table 7. RSWP D.C. OPERATION CONDITION

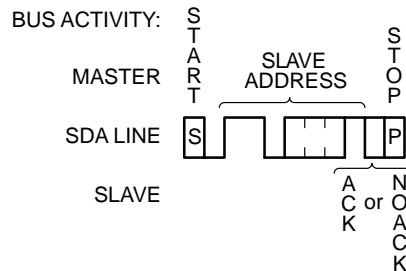
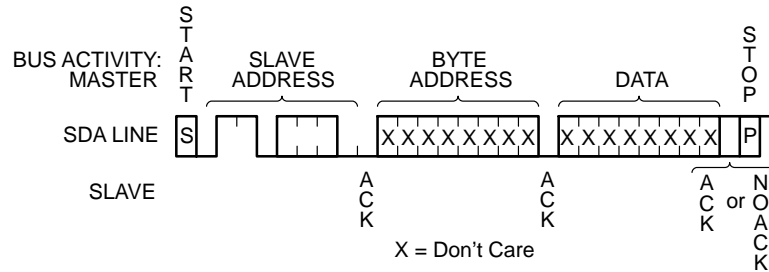
| Symbol          | Parameter                             | Test Conditions                        | Min | Max | Units |
|-----------------|---------------------------------------|----------------------------------------|-----|-----|-------|
| $\Delta V_{HV}$ | $A_0$ Overdrive ( $V_{HV} - V_{CC}$ ) | $1.7\text{ V} < V_{CC} < 3.6\text{ V}$ | 4.8 |     | V     |
| $I_{HVD}$       | $A_0$ High Voltage Detector Current   |                                        |     | 0.1 | mA    |
| $V_{HV}$        | $A_0$ Very High Voltage               |                                        | 7   | 10  | V     |

Table 8. SWP COMMANDS

|               | Control Pin Levels<br>(Note 11) |                 |                 | Flag State<br>(Note 12) |      | Slave Address |                |                |                |    | ACK<br>? | Address Byte | ACK<br>? | Data<br>Byte | ACK<br>? | Write<br>Cycle |
|---------------|---------------------------------|-----------------|-----------------|-------------------------|------|---------------|----------------|----------------|----------------|----|----------|--------------|----------|--------------|----------|----------------|
|               | A <sub>2</sub>                  | A <sub>1</sub>  | A <sub>0</sub>  | PSWP                    | RSWP | b7 to<br>b4   | b3             | b2             | b1             | b0 |          |              |          |              |          |                |
| Action        | A <sub>2</sub>                  | A <sub>1</sub>  | A <sub>0</sub>  | PSWP                    | RSWP | b7 to<br>b4   | b3             | b2             | b1             | b0 | ACK<br>? | Address Byte | ACK<br>? | Data<br>Byte | ACK<br>? | Write<br>Cycle |
| Set<br>PSWP   | A <sub>2</sub>                  | A <sub>1</sub>  | A <sub>0</sub>  | 1                       | X    | 0110          | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | X  | No       |              |          |              |          |                |
|               | A <sub>2</sub>                  | A <sub>1</sub>  | A <sub>0</sub>  | 0                       | X    |               | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | 0  | Yes      | X            | Yes      | X            | Yes      | Yes            |
|               | A <sub>2</sub>                  | A <sub>1</sub>  | A <sub>0</sub>  | 0                       | X    |               | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | 1  | Yes      |              |          |              |          |                |
| Set<br>RSWP   | GND                             | GND             | V <sub>HV</sub> | 1                       | X    |               | 0              | 0              | 1              | X  | No       |              |          |              |          |                |
|               | GND                             | GND             | V <sub>HV</sub> | 0                       | 1    |               | 0              | 0              | 1              | X  | No       |              |          |              |          |                |
|               | GND                             | GND             | V <sub>HV</sub> | 0                       | 0    |               | 0              | 0              | 1              | 0  | Yes      | X            | Yes      | X            | Yes      | Yes            |
|               | GND                             | GND             | V <sub>HV</sub> | 0                       | 0    |               | 0              | 0              | 1              | 1  | Yes      |              |          |              |          |                |
|               | GND                             | GND             | V <sub>HV</sub> | 0                       | 0    |               | 0              | 0              | 1              | 1  | Yes      |              |          |              |          |                |
| Clear<br>RSWP | GND                             | V <sub>CC</sub> | V <sub>HV</sub> | 1                       | X    |               | 0              | 1              | 1              | X  | No       |              |          |              |          |                |
|               | GND                             | V <sub>CC</sub> | V <sub>HV</sub> | 0                       | X    |               | 0              | 1              | 1              | 0  | Yes      | X            | Yes      | X            | Yes      | Yes            |
|               | GND                             | V <sub>CC</sub> | V <sub>HV</sub> | 0                       | X    |               | 0              | 1              | 1              | 1  | Yes      |              |          |              |          |                |

11. Here  $A_2$ ,  $A_1$  and  $A_0$  are either at  $V_{CC}$  or GND for PSWP operations.

12. 1 stands for 'Set', 0 stands for 'Not Set', X stands for 'don't care'.



## Temperature Sensor Operation

The TS component in the CAT34TS02 combines a Proportional to Absolute Temperature (PTAT) sensor with a  $\Sigma$ - $\Delta$  modulator, yielding a 12 bit plus sign digital temperature representation.

The TS runs on an internal clock, and starts a new conversion cycle at least every 100 ms. The result of the most recent conversion is stored in the **Temperature Data Register (TDR)**, and remains there following a TS Shut-Down. Reading from the **TDR** does not interfere with the conversion cycle.

The value stored in the **TDR** is compared against limits stored in the **High Limit Register (HLR)**, the **Low Limit Register (LLR)** and/or **Critical Temperature Register (CTR)**. If the measured value is outside the alarm limits or above the critical limit, then the **EVENT** pin may be asserted. The **EVENT** output function is programmable, via the **Configuration Register** for interrupt mode, comparator mode and polarity.

The temperature limit registers can be Read or Written by the host, via the serial interface. At power-on, all the (writable) internal registers default to 0x0000, and should therefore be initialized by the host to the desired values. The **EVENT** output starts out disabled (corresponding to polarity active low); thus preventing irrelevant event bus activity before the limit registers are initialized. While the TS is enabled (not shut-down), event conditions are normally generated by a change in measured temperature as recorded in the TDR, but limit changes can also trigger events as soon as the new limit creates an event condition, i.e. asynchronously with the temperature sampling activity.

In order to minimize the thermal resistance between sensor and PCB, it is recommended that the exposed backside die attach pad (DAP) be soldered to the PCB ground plane.

## Registers

The CAT34TS02 contains eight 16-bit wide registers allocated to TS functions, as shown in Table 9. Upon power-up, the internal address counter points to the capability register.

### Capability Register (User Read Only)

This register lists the capabilities of the TS, as detailed in the corresponding bit map.

### Configuration Register (Read/Write)

This register controls the various operating modes of the TS, as detailed in the corresponding bit map.

### Temperature Trip Point Registers (Read/Write)

The CAT34TS02 features 3 temperature limit registers, the **HLR**, **LLR** and **CLR** mentioned earlier. The temperature value recorded in the **TDR** is compared to the various limit values, and the result is used to activate the **EVENT** pin. To avoid undesirable **EVENT** pin activity, this pin is automatically disabled at power-up to allow the host to initialize the limit registers and the converter to complete the first conversion cycle under nominal supply conditions. Data format is two's complement with the LSB representing 0.25°C, as detailed in the corresponding bit maps.

### Temperature Data Register (User Read Only)

This register stores the measured temperature, as well as trip status information. B15, B14, and B13 are the trip status bits, representing the relationship between measured temperature and the 3 limit values; these bits are not affected by **EVENT** status or by Configuration register settings regarding **EVENT** pin. Measured temperature is represented by bits B12 to B0. Data format is two's complement, where B12 represents the sign, B11 represents 128°C, etc. and B0 represents 0.0625°C.

### Manufacturer ID Register (Read Only)

The manufacturer ID assigned by the PCI-SIG trade organization to the CAT34TS02 device is fixed at 0x1B09.

### Device ID and Revision Register (Read Only)

This register contains manufacturer specific device ID and device revision information.

**Table 9. THE TS REGISTERS**

| Register Address | Register Name               |        | Power-On Default | Read/Write |
|------------------|-----------------------------|--------|------------------|------------|
| 0x00             | Capability Register         |        | 0x007F           | Read       |
| 0x01             | Configuration Register      |        | 0x0000           | Read/Write |
| 0x02             | High Limit Register         |        | 0x0000           | Read/Write |
| 0x03             | Low Limit Register          |        | 0x0000           | Read/Write |
| 0x04             | Critical Limit Register     |        | 0x0000           | Read/Write |
| 0x05             | Temperature Data Register   |        | Undefined        | Read       |
| 0x06             | Manufacturer ID Register    |        | 0x1B09           | Read       |
| 0x07             | Device ID/Revision Register | Rev. B | 0x0813           | Read       |
|                  |                             | Rev. C | 0x0A00           |            |

## CAT34TS02

**Table 10. CAPABILITY REGISTER**

|            |            |            |            |            |            |           |           |
|------------|------------|------------|------------|------------|------------|-----------|-----------|
| <b>B15</b> | <b>B14</b> | <b>B13</b> | <b>B12</b> | <b>B11</b> | <b>B10</b> | <b>B9</b> | <b>B8</b> |
| RFU        | RFU        | RFU        | RFU        | RFU        | RFU        | RFU       | RFU       |
| <b>B7</b>  | <b>B6</b>  | <b>B5</b>  | <b>B4</b>  | <b>B3</b>  | <b>B2</b>  | <b>B1</b> | <b>B0</b> |
| EVSD       | TMOUT      | RFU        | TRES [1:0] |            | RANGE      | ACC       | EVENT     |

| Bit                 | Description                                                                                                                                                                                                                                                                      |
|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>B15:B8</b>       | Reserved for future use; can not be written; should be ignored; will read as 0                                                                                                                                                                                                   |
| <b>B7</b> (Note 13) | 0: Configuration Register bit 4 is frozen upon Configuration Register bit 8 being set (i.e. a TS shut-down freezes the EVENT output)<br>1: Configuration Register bit 4 is cleared upon Configuration Register bit 8 being set (i.e. a TS shut-down de-asserts the EVENT output) |
| <b>B6</b>           | 0: The TS implements SMBus time-out within the range 10 to 60 ms<br>1: The TS implements SMBus time-out within the range 25 to 35 ms                                                                                                                                             |
| <b>B5</b>           | 0: Pin A <sub>0</sub> V <sub>HV</sub> compliance required for RSWP Write/Clear operations not explicitly stated<br>1: Pin A <sub>0</sub> V <sub>HV</sub> compliance required for RSWP Write/Clear operations explicitly stated                                                   |
| <b>B4:B3</b>        | 00: LSB = 0.50°C (9 bit resolution)<br>01: LSB = 0.25°C (10 bit)<br>10: LSB = 0.125°C (11 bit)<br>11: LSB = 0.0625°C (12 bit)                                                                                                                                                    |
| <b>B2</b>           | 0: Positive Temperature Only<br>1: Positive and Negative Temperature                                                                                                                                                                                                             |
| <b>B1</b>           | 0: ±2°C over the active range and ±3°C over the operating range (Class C)<br>1: ±1°C over the active range and ±2°C over the monitor range (Class B)                                                                                                                             |
| <b>B0</b>           | 0: Critical Temperature only<br>1: Alarm and Critical Temperature                                                                                                                                                                                                                |

13. Configuration Register bit 4 can be cleared (but not set) after Configuration Register bit 8 is set, by writing a “1” to Configuration Register bit 5 (EVENT output can be de-asserted during TS shut-down periods)

Table 11. CONFIGURATION REGISTER

| B15        | B14        | B13   | B12       | B11        | B10        | B9        | B8         |
|------------|------------|-------|-----------|------------|------------|-----------|------------|
| RFU        | RFU        | RFU   | RFU       | RFU        | HYST [1:0] |           | SHDN       |
| B7         | B6         | B5    | B4        | B3         | B2         | B1        | B0         |
| TCRIT_LOCK | EVENT_LOCK | CLEAR | EVENT_STS | EVENT_CTRL | TCRIT_ONLY | EVENT_POL | EVENT_MODE |

| Bit                      | Description                                                                                                                                                                    |
|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>B15:B11</b>           | Reserved for future use; can not be written; should be ignored; will read as 0                                                                                                 |
| <b>B10:B9</b> (Note 14)  | 00: Disable hysteresis<br>01: Set hysteresis at 1.5°C<br>10: Set hysteresis at 3°C<br>11: Set hysteresis at 6°C                                                                |
| <b>B8</b> (Note 18)      | 0: Thermal Sensor is enabled; temperature readings are updated at sampling rate<br>1: Thermal Sensor is shut down; temperature reading is frozen to value recorded before SHDN |
| <b>B7</b> (Note 17)      | 0: Critical trip register can be updated<br>1: Critical trip register cannot be modified; this bit can be cleared only at POR                                                  |
| <b>B6</b> (Note 17)      | 0: Alarm trip registers can be updated<br>1: Alarm trip registers cannot be modified; this bit can be cleared only at POR                                                      |
| <b>B5</b> (Note 16)      | 0: Always reads as 0 (self-clearing)<br>1: Writing a 1 to this position clears an event recording in interrupt mode only                                                       |
| <b>B4</b> (Note 15)      | 0: EVENT output pin is not being asserted<br>1: EVENT output pin is being asserted                                                                                             |
| <b>B3</b> (Note 14)      | 0: EVENT output disabled; <i>polarity dependent</i> : open-drain for <b>B1</b> = 0; grounded for <b>B1</b> = 1<br>1: EVENT output enabled                                      |
| <b>B2</b> (Note 20)      | 0: event condition triggered by alarm or critical temperature limit crossing<br>1: event condition triggered by critical temperature limit crossing only                       |
| <b>B1</b> (Notes 14, 19) | 0: EVENT output active low<br>1: EVENT output active high                                                                                                                      |
| <b>B0</b> (Note 14)      | 0: Comparator mode<br>1: Interrupt mode                                                                                                                                        |

14. Can not be altered (set or cleared) as long as either one of the two lock bits, B6 or B7 is set.

15. This bit is a *polarity independent* 'software' copy of the EVENT pin, i.e. it is under the control of B3. This bit is read-only.

16. Writing a '1' to this bit clears an event condition in Interrupt mode, but has no effect in comparator mode. When read, this bit always returns 0. Once the measured temperature exceeds the critical limit, setting this bit has no effect (see Figure 33).

17. Cleared at power-on reset (POR). Once set, this bit can only be cleared by a POR condition.

18. The TS powers up into active mode, i.e. this bit is cleared at power-on reset (POR). When the TS is shut down the ADC is disabled and the temperature reading is frozen to the most recently recorded value. The TS can not be shut down (B8 can not be set) as long as either one of the two lock bits, B6 or B7 is set. However, the bit can be cleared at any time.

19. The EVENT output is "open-drain" and requires an external pull-up resistor for either polarity. The "natural" polarity is "active low", as it allows "wired-or" operation on the EVENT bus.

20. Can not be set as long as lock bit B6 is set.

## CAT34TS02

**Table 12. HIGH LIMIT REGISTER**

| B15 | B14 | B13 | B12  | B11   | B10    | B9   | B8   |
|-----|-----|-----|------|-------|--------|------|------|
| 0   | 0   | 0   | Sign | 128°C | 64°C   | 32°C | 16°C |
| B7  | B6  | B5  | B4   | B3    | B2     | B1   | B0   |
| 8°C | 4°C | 2°C | 1°C  | 0.5°C | 0.25°C | 0    | 0    |

**Table 13. LOW LIMIT REGISTER**

| B15 | B14 | B13 | B12  | B11   | B10    | B9   | B8   |
|-----|-----|-----|------|-------|--------|------|------|
| 0   | 0   | 0   | Sign | 128°C | 64°C   | 32°C | 16°C |
| B7  | B6  | B5  | B4   | B3    | B2     | B1   | B0   |
| 8°C | 4°C | 2°C | 1°C  | 0.5°C | 0.25°C | 0    | 0    |

**Table 14. TCRIT LIMIT REGISTER**

| B15 | B14 | B13 | B12  | B11   | B10    | B9   | B8   |
|-----|-----|-----|------|-------|--------|------|------|
| 0   | 0   | 0   | Sign | 128°C | 64°C   | 32°C | 16°C |
| B7  | B6  | B5  | B4   | B3    | B2     | B1   | B0   |
| 8°C | 4°C | 2°C | 1°C  | 0.5°C | 0.25°C | 0    | 0    |

**Table 15. TEMPERATURE DATA REGISTER**

| B15   | B14  | B13 | B12  | B11   | B10                 | B9                   | B8                    |
|-------|------|-----|------|-------|---------------------|----------------------|-----------------------|
| TCRIT | HIGH | LOW | Sign | 128°C | 64°C                | 32°C                 | 16°C                  |
| B7    | B6   | B5  | B4   | B3    | B2                  | B1                   | B0                    |
| 8°C   | 4°C  | 2°C | 1°C  | 0.5°C | 0.25°C<br>(Note 21) | 0.125°C<br>(Note 21) | 0.0625°C<br>(Note 21) |

21. When applicable (as defined by Capability bit TRES), unsupported bits will read as 0

| Bit        | Description                                                                                    |
|------------|------------------------------------------------------------------------------------------------|
| <b>B15</b> | 0: Temperature is below the TCRIT limit<br>1: Temperature is equal to or above the TCRIT limit |
| <b>B14</b> | 0: Temperature is equal to or below the High limit<br>1: Temperature is above the High limit   |
| <b>B13</b> | 0: Temperature is equal to or above the Low limit<br>1: Temperature is below the Low limit     |
| <b>B12</b> | 0: Positive temperature<br>1: Negative temperature                                             |



## Register Data Format

The values used in the temperature data register and the 3 temperature trip point registers are expressed in two's complement format. The measured temperature value is expressed with 12-bit resolution, while the 3 trip temperature limits are set with 10-bit resolution. The total temperature range is arbitrarily defined as 256°C, thus yielding an LSB of 0.0625°C for the measured temperature and 0.25°C for the 3 limit values. Bit B12 in all temperature registers represents the sign, with a '0' indicating a positive, and a '1' a negative value. In two's complement format, negative values are obtained by complementing their positive counterpart and adding a '1', so that the sum of opposite signed numbers, but of equal absolute value, adds up to zero.

Note that trailing '0' bits, are '0' irrespective of polarity. Therefore the don't care bits (B1 and B0) in the 10-bit resolution temperature limit registers, are always '0'.

**Table 16. 12-BIT TEMPERATURE DATA FORMAT**

| Binary (B12 to B0) | Hex  | Temperature |
|--------------------|------|-------------|
| 1 1100 1001 0000   | 1C90 | -55°C       |
| 1 1100 1110 0000   | 1CE0 | -50°C       |
| 1 1110 0111 0000   | 1E70 | -25°C       |
| 1 1111 1111 1111   | 1FFF | -0.0625°C   |
| 0 0000 0000 0000   | 000  | 0°C         |
| 0 0000 0000 0001   | 001  | +0.0625°C   |
| 0 0001 1001 0000   | 190  | +25°C       |
| 0 0011 0010 0000   | 320  | +50°C       |
| 0 0111 1101 0000   | 7D0  | +125°C      |

## Event Pin Functionality

The  $\overline{\text{EVENT}}$  output reacts to temperature changes as illustrated in Figure 33, and according to the operating mode defined by the Configuration register.

In **Interrupt Mode**, the enabled  $\overline{\text{EVENT}}$  output will be asserted every time the temperature crosses one of the alarm window limits, and can be de-asserted by writing a '1' to the clear event bit (B5) in the configuration register. Once the temperature exceeds the critical limit, the  $\overline{\text{EVENT}}$  remains asserted as long as the temperature stays above the critical limit and cannot be cleared. A clear request sent to the CAT34TS02 while the temperature is above the critical limit will be acknowledged, but will be executed only after the temperature drops below the critical limit.

In **Comparator Mode**, the  $\overline{\text{EVENT}}$  output is asserted outside the alarm window limits, while in **Critical Temperature Mode**,  $\overline{\text{EVENT}}$  is asserted only above the critical limit. Clear requests are ignored in this mode. The exact trip limits are determined by the 3 temperature limit settings and the hysteresis offsets, as illustrated in Figure 34.

Following a TS shut-down request, the converter is stopped and the most recently recorded temperature value present in the TDR is frozen; the  $\overline{\text{EVENT}}$  output will continue to reflect the state immediately preceding the shut-down command. Therefore, if the state of the  $\overline{\text{EVENT}}$  output creates an undesirable bus condition, appropriate action must be taken either before or after shutting down the TS. This may require clearing the event, disabling the  $\overline{\text{EVENT}}$  output or perhaps changing the  $\overline{\text{EVENT}}$  output polarity.

In normal use, events are triggered by a change in recorded temperature, but the CAT34TS02 will also respond to limit register changes. Whereas recorded temperature values are updated at sampling rate frequency, limits can be modified at any time. The enabled  $\overline{\text{EVENT}}$  output will react to limit changes as soon as the respective registers are updated. This feature may be useful during testing.

# CAT34TS02

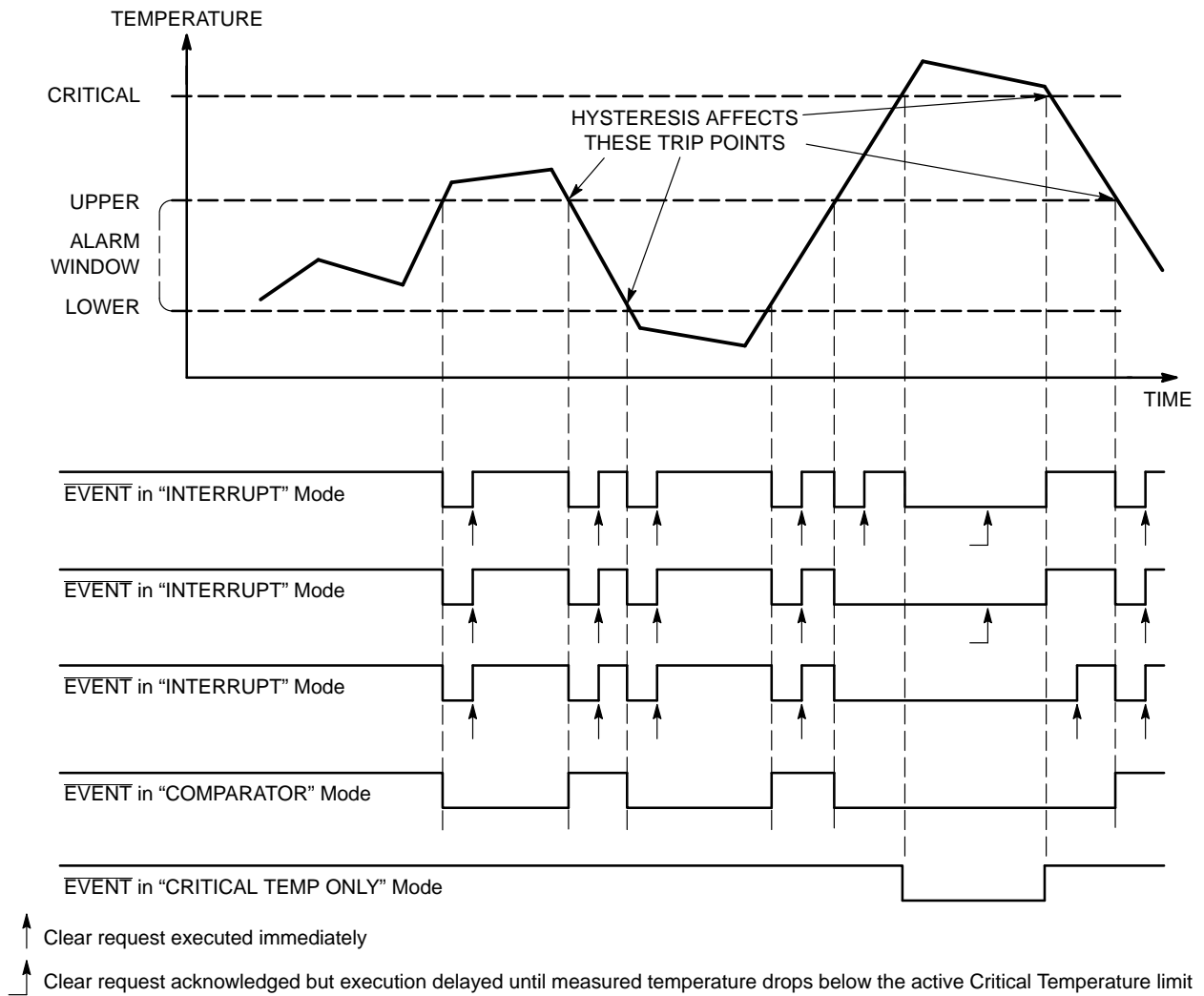


Figure 33. Event Detail

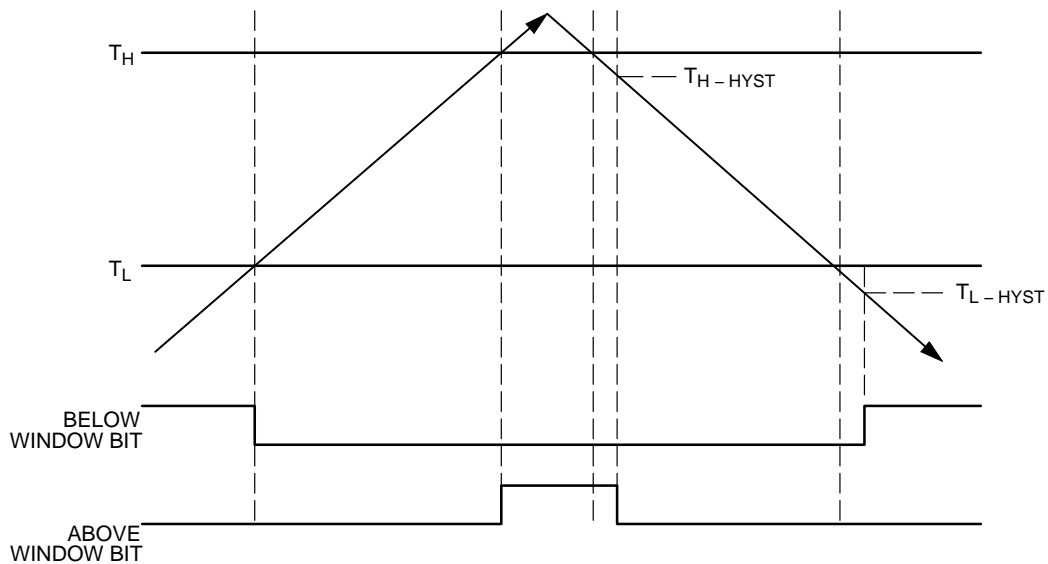
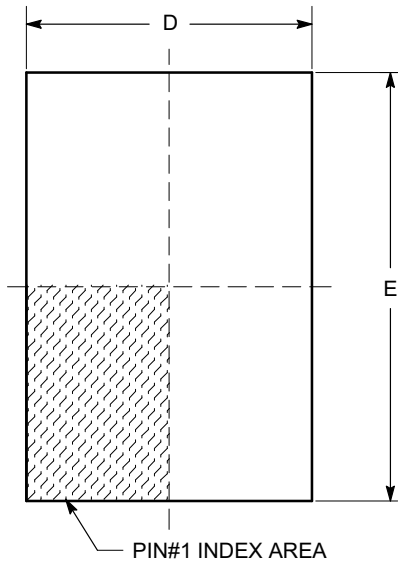


Figure 34. Hysteresis Detail

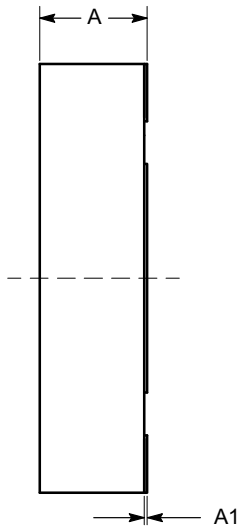
# CAT34TS02

## PACKAGE DIMENSIONS

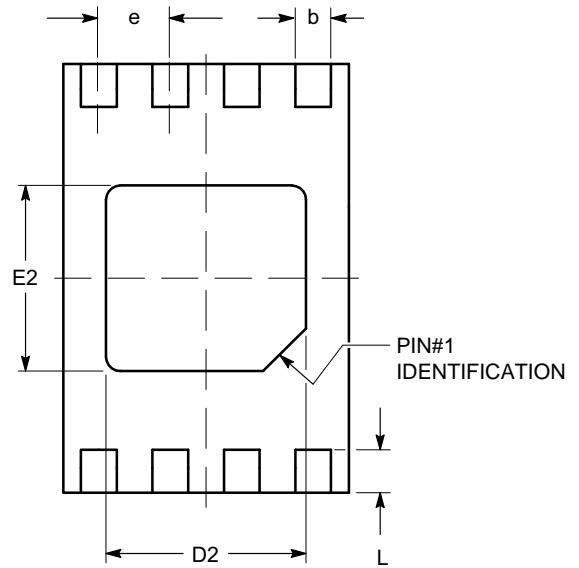
TDFN8, 2x3  
CASE 511AK  
ISSUE A



TOP VIEW

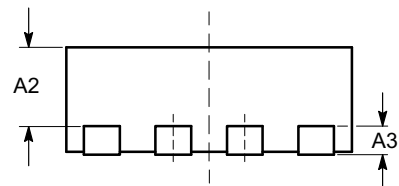


SIDE VIEW



BOTTOM VIEW

| SYMBOL | MIN      | NOM  | MAX  |
|--------|----------|------|------|
| A      | 0.70     | 0.75 | 0.80 |
| A1     | 0.00     | 0.02 | 0.05 |
| A2     | 0.45     | 0.55 | 0.65 |
| A3     | 0.20 REF |      |      |
| b      | 0.20     | 0.25 | 0.30 |
| D      | 1.90     | 2.00 | 2.10 |
| D2     | 1.30     | 1.40 | 1.50 |
| E      | 2.90     | 3.00 | 3.10 |
| E2     | 1.20     | 1.30 | 1.40 |
| e      | 0.50 TYP |      |      |
| L      | 0.20     | 0.30 | 0.40 |



FRONT VIEW

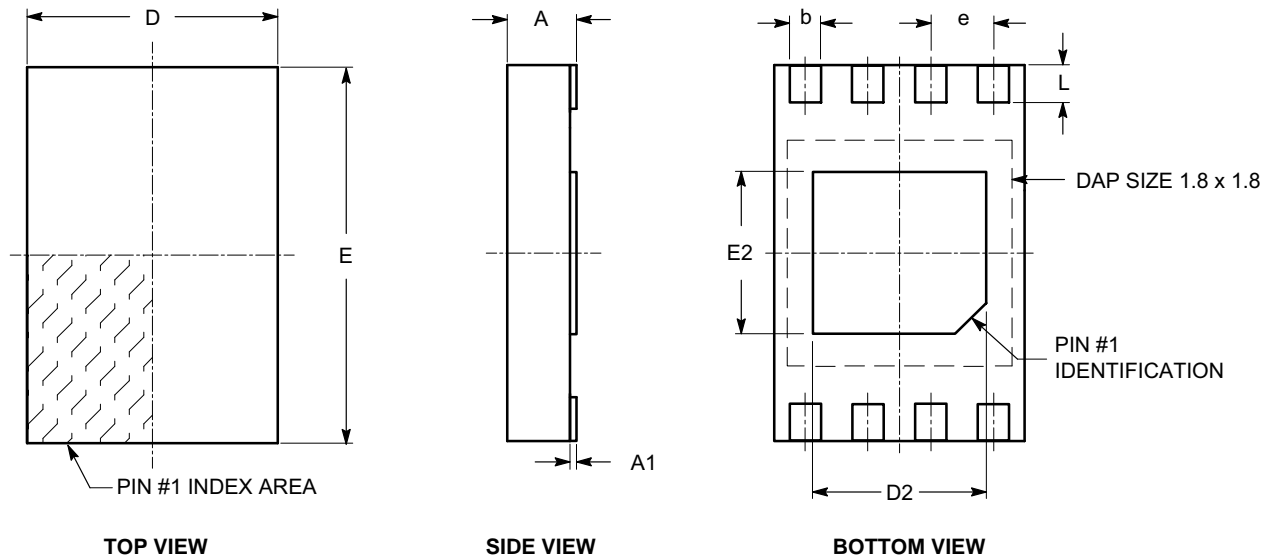
### Notes:

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MO-229.

# CAT34TS02

## PACKAGE DIMENSIONS

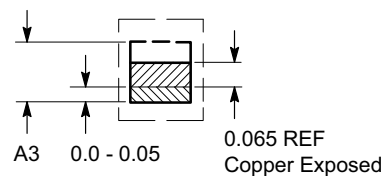
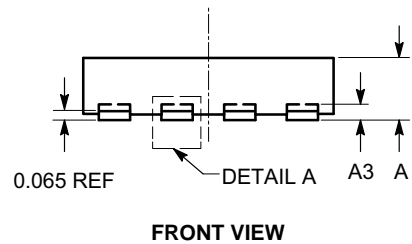
UDFN8, 2x3 EXTENDED PAD  
CASE 517AZ-01  
ISSUE O



| SYMBOL | MIN       | NOM  | MAX  |
|--------|-----------|------|------|
| A      | 0.45      | 0.50 | 0.55 |
| A1     | 0.00      | 0.02 | 0.05 |
| A3     | 0.127 REF |      |      |
| b      | 0.20      | 0.25 | 0.30 |
| D      | 1.95      | 2.00 | 2.05 |
| D2     | 1.35      | 1.40 | 1.45 |
| E      | 2.95      | 3.00 | 3.05 |
| E2     | 1.25      | 1.30 | 1.35 |
| e      | 0.50 REF  |      |      |
| L      | 0.25      | 0.30 | 0.35 |

### Notes:

- (1) All dimensions are in millimeters.
- (2) Refer JEDEC MO-236/MO-252.



**DETAIL A**

## CAT34TS02

### Example of Ordering Information


| Device Order Number                                    | Specific Device Marking | Package Type | Lead Finish | Shipping                           | Device Revision |
|--------------------------------------------------------|-------------------------|--------------|-------------|------------------------------------|-----------------|
| CAT34TS02VP2GT4B<br>(Not recommended for new designs.) | GTB                     | TDFN-8       | NiPdAu      | Tape & Reel,<br>4,000 Units / Reel | B               |
| CAT34TS02VP2GT4C                                       | GTC                     | TDFN-8       | NiPdAu      | Tape & Reel,<br>4,000 Units / Reel | C               |
| CAT34TS02HU4-GT4                                       | TSU                     | UDFN-8       | NiPdAu      | Tape & Reel,<br>4,000 Units / Reel | C               |

22. All packages are RoHS-compliant (Lead-free, Halogen-free)

23. The standard lead finish is NiPdAu.

24. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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