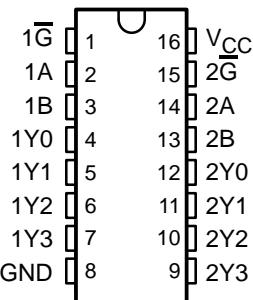


- AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage
- Buffered Inputs
- Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ± 24 -mA Output Drive Current – Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

CD54AC139 . . . F PACKAGE
CD74AC139 . . . E OR M PACKAGE
(TOP VIEW)



description/ordering information

The 'AC139 devices are dual 2-line to 4-line decoders/demultiplexers designed for 1.5-V to 5.5-V V_{CC} operation. These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The active-low enable (\bar{G}) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	PDIP – E	Tube	CD74AC139E	CD74AC139E
	SOIC – M	Tube	CD74AC139M	AC139M
		Tape and reel	CD74AC139M96	
	CDIP – F	Tube	CD54AC139F3A	CD54AC139F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

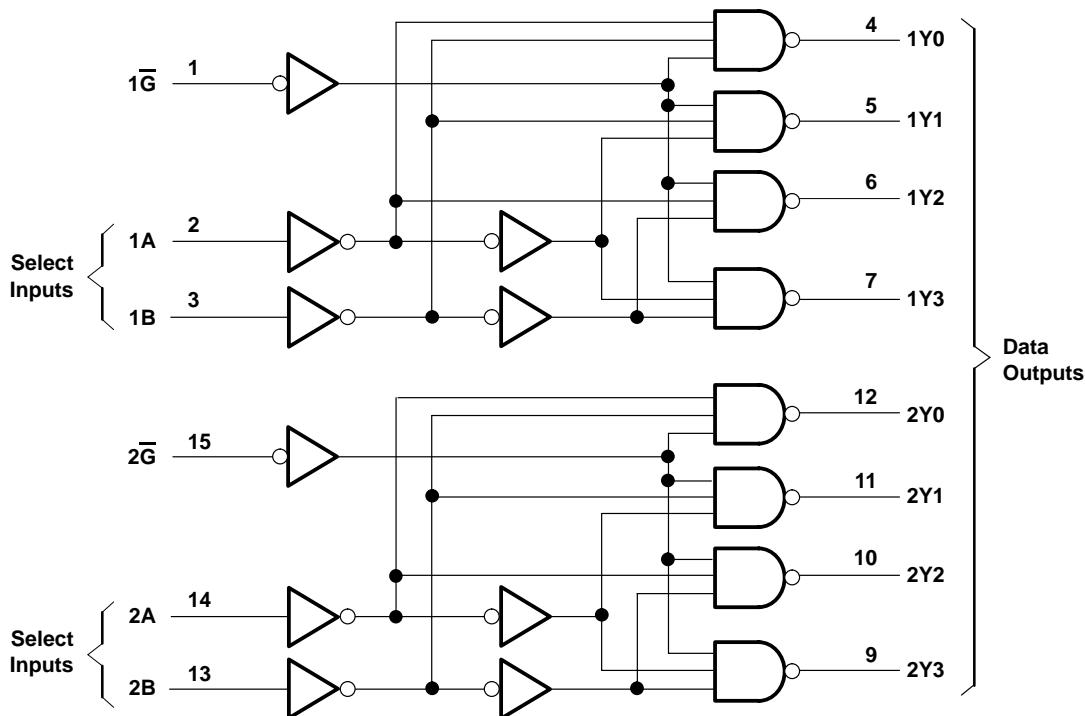
CD54AC139, CD74AC139 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

SCHS332 – MARCH 2003

FUNCTION TABLE (each decoder/demultiplexer)

INPUTS		OUTPUTS				
\bar{G}	SELECT		Y0	Y1	Y2	Y3
	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

CD54AC139, CD74AC139
DUAL 2-LINE TO 4-LINE DECODERS/DEMULITPLEXERS

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recommended operating conditions (see Note 3)

			$T_A = 25^\circ\text{C}$		$-55^\circ\text{C} \text{ to } 125^\circ\text{C}$		$-40^\circ\text{C} \text{ to } 85^\circ\text{C}$		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
V _{CC}	Supply voltage			1.5	5.5	1.5	5.5	1.5	5.5	V
V _{IH}	High-level input voltage		V _{CC} = 1.5 V		1.2		1.2		V	
			V _{CC} = 3 V		2.1		2.1			
			V _{CC} = 5.5 V		3.85		3.85			
V _{IL}	Low-level input voltage		V _{CC} = 1.5 V		0.3		0.3		V	
			V _{CC} = 3 V		0.9		0.9			
			V _{CC} = 5.5 V		1.65		1.65			
V _I	Input voltage			0	V _{CC}	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage			0	V _{CC}	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		V _{CC} = 4.5 V to 5.5 V		-24		-24		-24	mA
I _{OL}	Low-level output current		V _{CC} = 4.5 V to 5.5 V		24		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		V _{CC} = 1.5 V to 3 V		50		50		50	ns/V
			V _{CC} = 3.6 V to 5.5 V		20		20		20	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	$T_A = 25^\circ\text{C}$		$-55^\circ\text{C} \text{ to } 125^\circ\text{C}$		$-40^\circ\text{C} \text{ to } 85^\circ\text{C}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -50 μA	1.5 V	1.4	1.4		1.4		V
			3 V	2.9	2.9		2.9		
			4.5 V	4.4	4.4		4.4		
		I _{OH} = -4 mA	3 V	2.58	2.4		2.48		
		I _{OH} = -24 mA	4.5 V	3.94	3.7		3.8		
		I _{OH} = -50 mA [†]	5.5 V		3.85				
		I _{OH} = -75 mA [†]	5.5 V				3.85		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 50 μA	1.5 V	0.1	0.1		0.1		V
			3 V	0.1	0.1		0.1		
			4.5 V	0.1	0.1		0.1		
		I _{OL} = 12 mA	3 V	0.36	0.5		0.44		
		I _{OL} = 24 mA	4.5 V	0.36	0.5		0.44		
		I _{OL} = 50 mA [†]	5.5 V		1.65		–		
		I _{OL} = 75 mA [†]	5.5 V				1.65		
I _I	V _I = V _{CC} or GND		5.5 V	± 0.1	± 1		± 1	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0		5.5 V	8	160		80	μA	
C _i				10	10		10	pF	

[†] Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50- Ω transmission-line drive capability at 85°C and 75- Ω transmission-line drive capability at 125°C.

CD54AC139, CD74AC139 DUAL 2-LINE TO 4-LINE DECODERS/DEMULITPLEXERS

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**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 1.5$ V, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	–55°C to 125°C		–40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	$C_L = 50$ pF	131		119		ns
t_{PHL}				131		119		
t_{PLH}	\overline{G}	Any Y	$C_L = 50$ pF	131		119		ns
t_{PHL}				131		119		

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3$ V ± 0.3 V, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	–55°C to 125°C		–40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	$C_L = 50$ pF	3.7	14.7	3.9	13.4	ns
t_{PHL}				3.7	14.7	3.9	13.4	
t_{PLH}	\overline{G}	Any Y	$C_L = 50$ pF	3.7	14.7	3.9	13.4	ns
t_{PHL}				3.7	14.7	3.9	13.4	

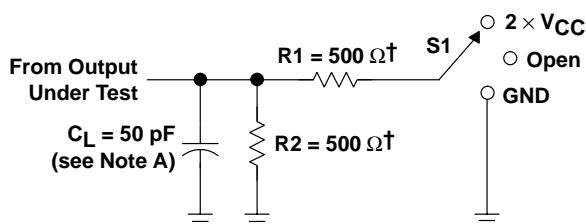
**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5$ V ± 0.5 V, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	–55°C to 125°C		–40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	$C_L = 50$ pF	2.6	10.5	2.8	9.5	ns
t_{PHL}				2.6	10.5	2.8	9.5	
t_{PLH}	\overline{G}	Any Y	$C_L = 50$ pF	2.6	10.5	2.8	9.5	ns
t_{PHL}				2.6	10.5	2.8	9.5	

operating characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

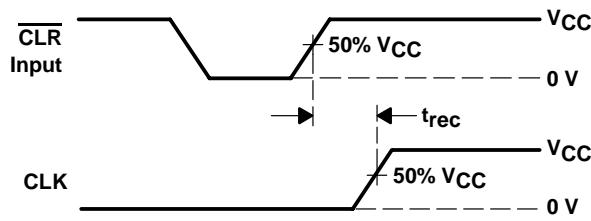
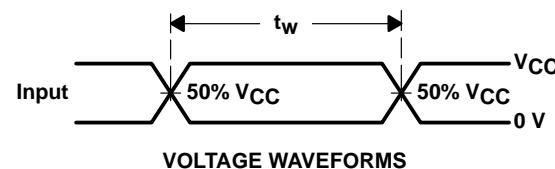
PARAMETER				TYP	UNIT
C_{pd} Power dissipation capacitance				83	pF

PARAMETER MEASUREMENT INFORMATION

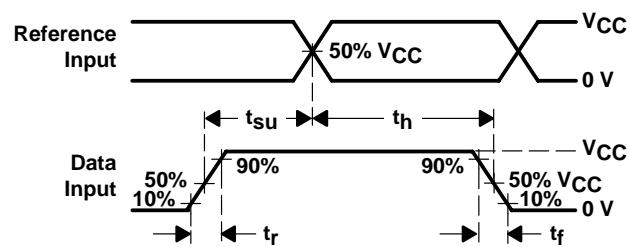


† When $V_{CC} = 1.5$ V, $R1 = R2 = 1$ k Ω

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

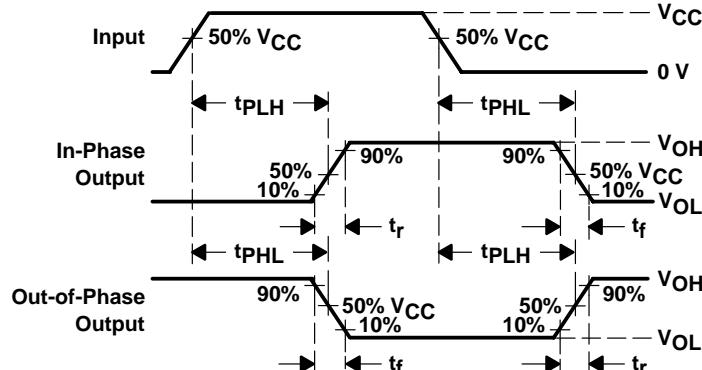


VOLTAGE WAVEFORMS RECOVERY TIME

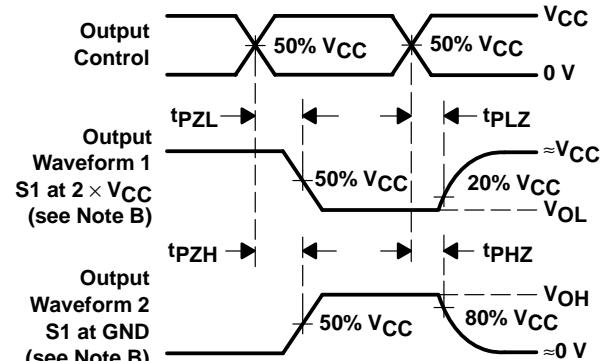


VOLTAGE WAVEFORMS

SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS OUTPUT ENABLE AND DISABLE TIMES

NOTES:

- A. C_L includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns. Phase relationships between waveforms are arbitrary.
- D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. t_{PLH} and t_{PHL} are the same as t_{pd} .
- G. t_{PZL} and t_{PZH} are the same as t_{en} .
- H. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- I. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54AC139F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54AC139F3A	Samples
CD74AC139E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC139E	Samples
CD74AC139EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC139E	Samples
CD74AC139M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC139M	Samples
CD74AC139M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC139M	Samples
CD74AC139MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC139M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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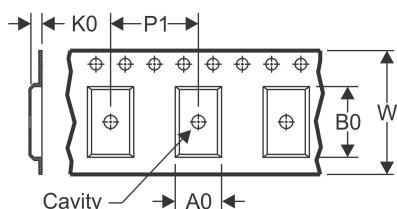
OTHER QUALIFIED VERSIONS OF CD54AC139, CD74AC139 :

- Catalog: [CD74AC139](#)
- Military: [CD54AC139](#)

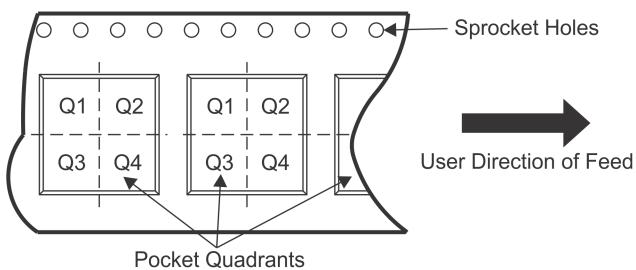
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC139M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

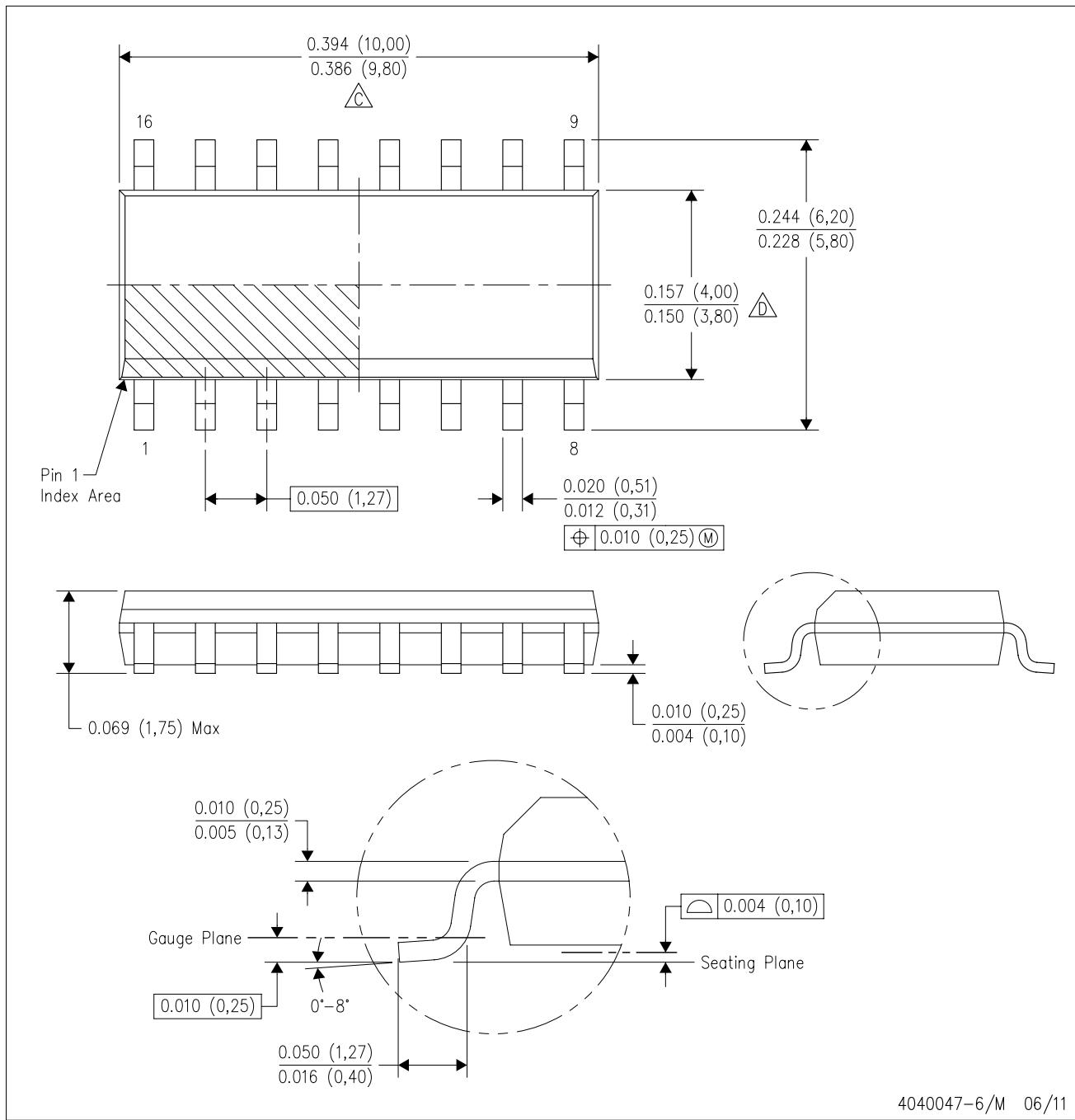
TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC139M96	SOIC	D	16	2500	333.2	345.9	28.6

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

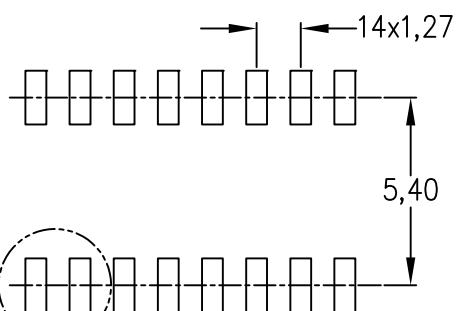
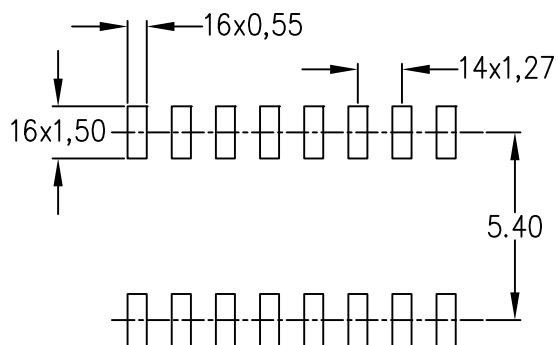
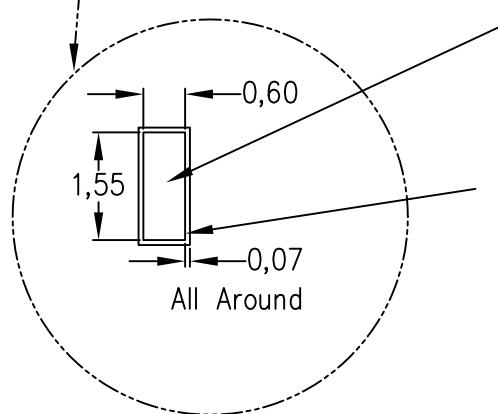
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



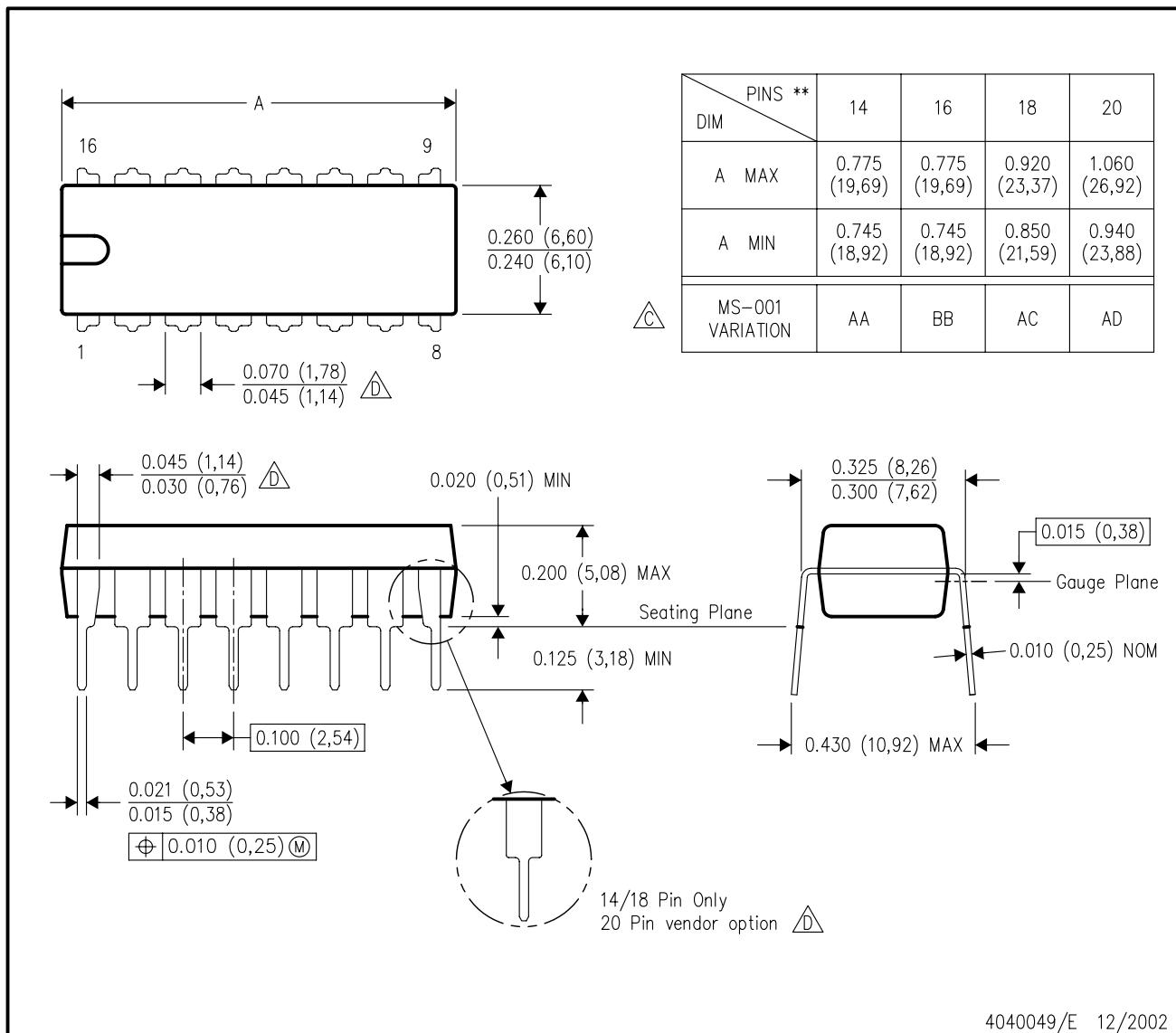
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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