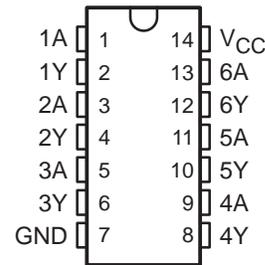# CD74AC14
HEX SCHMITT-TRIGGER INVERTER

SCHS228B – SEPTEMBER 1998 – REVISED MARCH 2004

- **AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage**
- **Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption**
- **Greater Noise Immunity Than Standard Inverters**
- **Operates With Much Slower Than Standard Input Rise and Fall Slew Rates**
- **Balanced Propagation Delays**
- **±24-mA Output Drive Current**
  - **Fanout to 15 F Devices**
- **SCR Latchup-Resistant CMOS Process and Circuit Design**
- **Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015**

E OR M PACKAGE
(TOP VIEW)

1A	1	14	V_{CC}
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
GND	7	8	4Y

description/ordering information

The CD74AC14 contains six independent inverters. This device performs the Boolean function $Y = \overline{A}$.

Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.
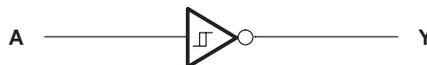
ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	PDIP – E	Tube	CD74AC14E	CD74AC14E
	SOIC – M	Tube	CD74AC14M	AC14M
		Tape and reel	CD74AC14M96	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram, each inverter (positive logic)

A ───▷○─── Y

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TEXAS INSTRUMENTS

CD74AC14
HEX SCHMITT-TRIGGER INVERTER

SCHS228B – SEPTEMBER 1998 – REVISED MARCH 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 6 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 1) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 1) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±100 mA
Package thermal impedance, θ_{JA} (see Note 2): E package .... 80°C/W
                                                       M package .... 86°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
       2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			T_A = 25°C		−55°C to 125°C		−40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		1.5	5.5	1.5	5.5	1.5	5.5	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 4.5 V to 5.5 V		−24		−24		−24	mA
I_{OL}	Low-level output current	V_{CC} = 4.5 V to 5.5 V		24		24		24	mA

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report,
        Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$		$-55°C$ to $125°C$		$-40°C$ to $85°C$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{T+} Positive-going threshold			5 V	2.6	3.4	2.6	3.4	2.6	3.4	V
V_{T-} Negative-going threshold			5 V	1.6	2.4	1.6	2.4	1.6	2.4	V
ΔV_T Hysteresis $(V_{T+} - V_{T-})$			5 V	0.5		0.5		0.5		V
V_{OH}	$V_I = V_{T+}$	$I_{OH} = -50 \mu A$	1.5 V	1.4		1.4		1.4		V
			3 V	2.9		2.9		2.9		
			4.5 V	4.4		4.4		4.4		
		$I_{OH} = -4 mA$	3 V	2.58		2.4		2.48		
		$I_{OH} = -24 mA$	4.5 V	3.94		3.7		3.8		
		$I_{OH} = -50 mA†$	5.5 V			3.85				
		$I_{OH} = -75 mA†$	5.5 V					3.85		
V_{OL}	$V_I = V_{T-}$	$I_{OL} = 50 \mu A$	1.5 V		0.1		0.1		0.1	V
			3 V		0.1		0.1		0.1	
			4.5 V		0.1		0.1		0.1	
		$I_{OL} = 12 mA$	3 V		0.36		0.5		0.44	
		$I_{OL} = 24 mA$	4.5 V		0.36		0.5		0.44	
		$I_{OL} = 50 mA†$	5.5 V				1.65			
		$I_{OL} = 75 mA†$	5.5 V						1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$		5.5 V		4		80		40	μA
C_i					10		10		10	pF

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$-55°C$ TO $125°C$		$-40°C$ TO $85°C$		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2.6	10.5	2.7	9.5	ns
t_{PHL}			2.6	10.5	2.7	9.5	

operating characteristics, $V_{CC} = 5 V$, $T_A = 25°C$

PARAMETER	TYP	UNIT
C_{pd} Power dissipation capacitance	45	pF

PARAMETER MEASUREMENT INFORMATION
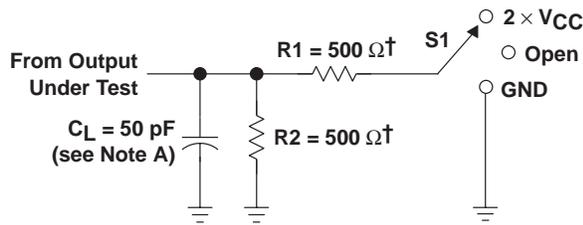
LOAD CIRCUIT

† When V_{CC} = 1.5 V, R1 = R2 = 1 kΩ
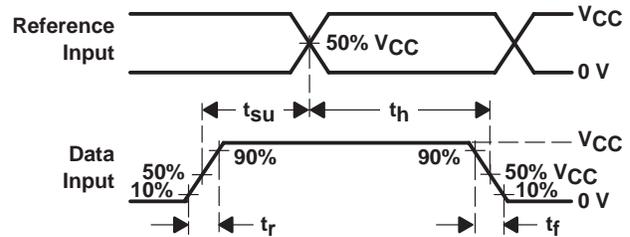
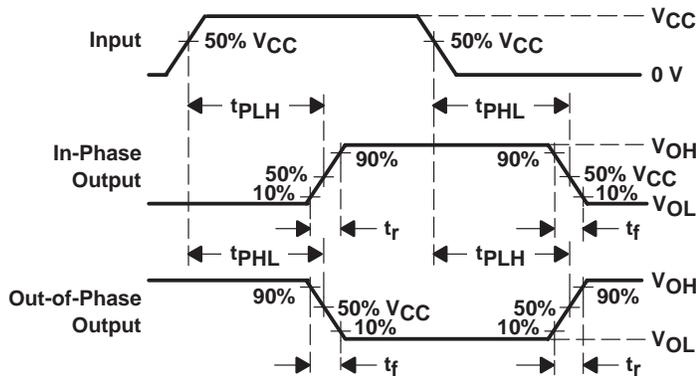| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND
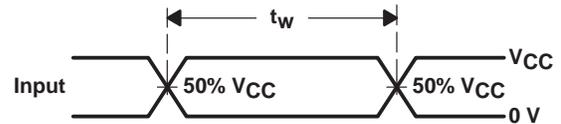
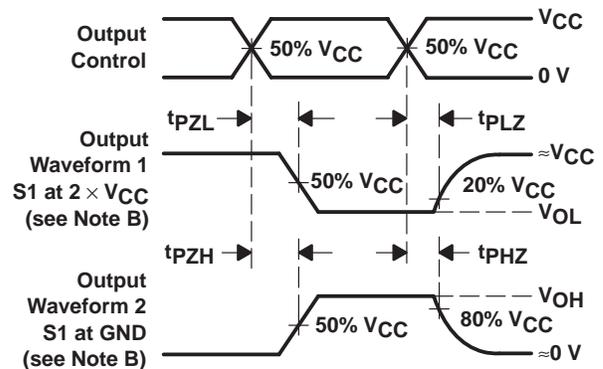**VOLTAGE WAVEFORMS
PULSE DURATION**
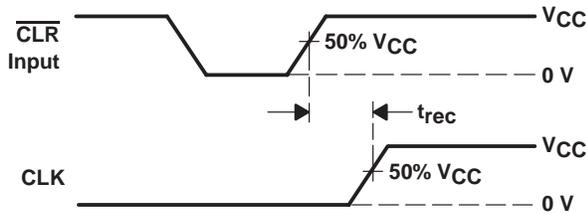
**VOLTAGE WAVEFORMS
RECOVERY TIME**

**VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES**
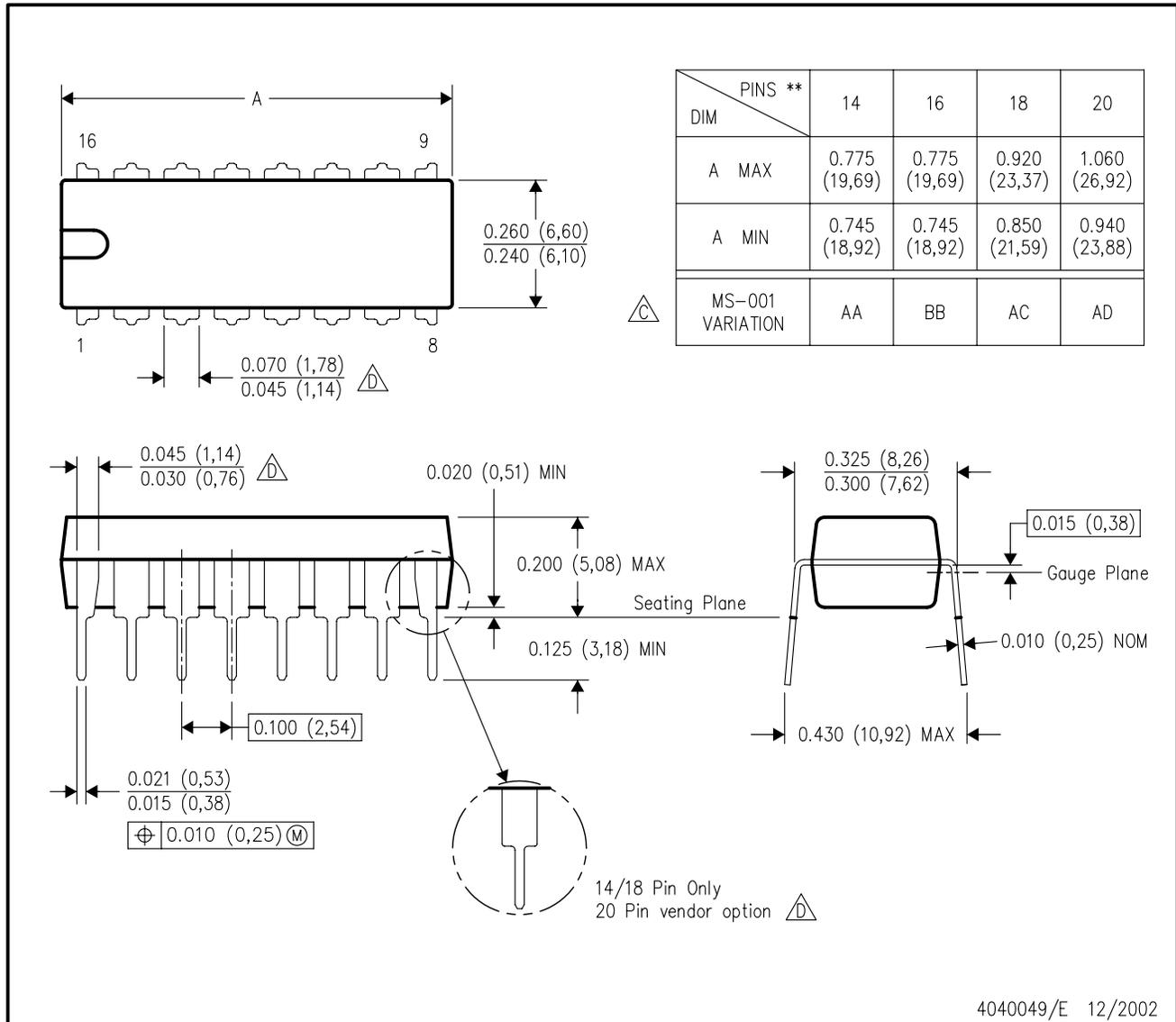

**VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES**

NOTES: A. C_L includes probe and test-fixture capacitance.
     B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
     C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. Phase relationships between waveforms are arbitrary.
     D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
     E. The outputs are measured one at a time, with one input transition per measurement.
     F. t_{PLH} and t_{PHL} are the same as t_{pd}.
     G. t_{PZL} and t_{PZH} are the same as t_{en}.
     H. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

Figure 1. Load Circuit and Voltage Waveforms

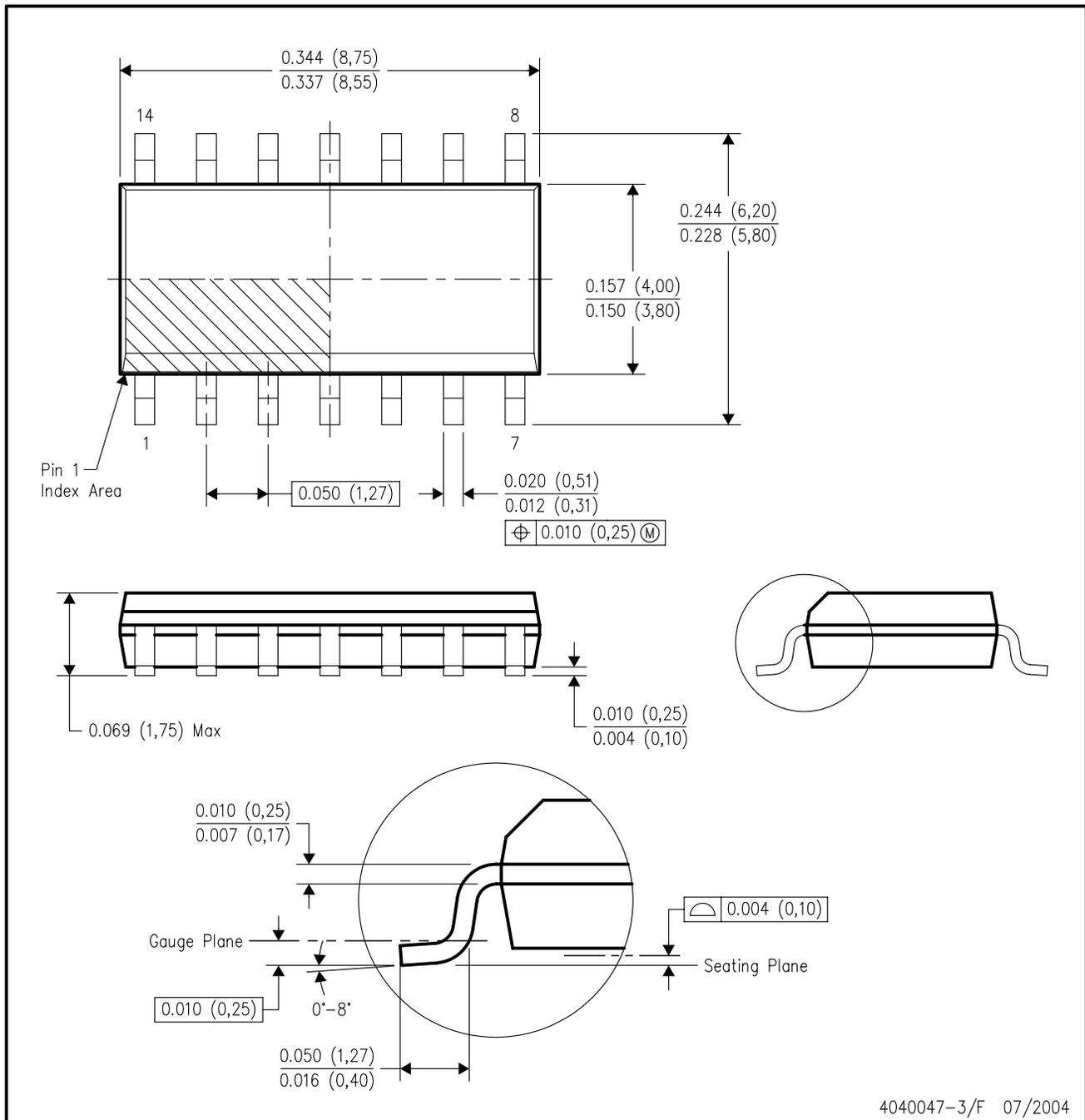## N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE
16 PINS SHOWN

	PINS **	14	16	18	20
DIM					
A MAX		0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN		0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION		AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) △D

0.045 (1,14) / 0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option △D

4040049/E   12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
       △C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
       △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R−PDSO−G14)   PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1   7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)   0°–8°

0.050 (1,27)
0.016 (0,40)

4040047–3/F 07/2004

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−012 variation AB.

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