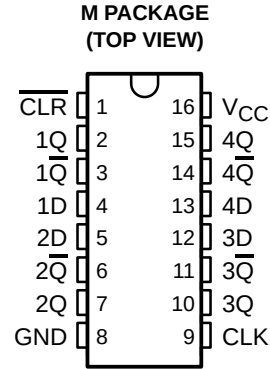


- AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage
- Buffered Inputs
- Contains Four Flip-Flops With Double-Rail Outputs
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ± 24 -mA Output Drive Current
 - Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators



description/ordering information

This positive-edge-triggered D-type flip-flop has a direct clear ($\overline{\text{CLR}}$) input. The CD74AC175 features complementary outputs from each flip-flop.

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – M	Tube	CD74AC175M	AC175M
		Tape and reel	CD74AC175M96	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUTS	
$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q_0}$



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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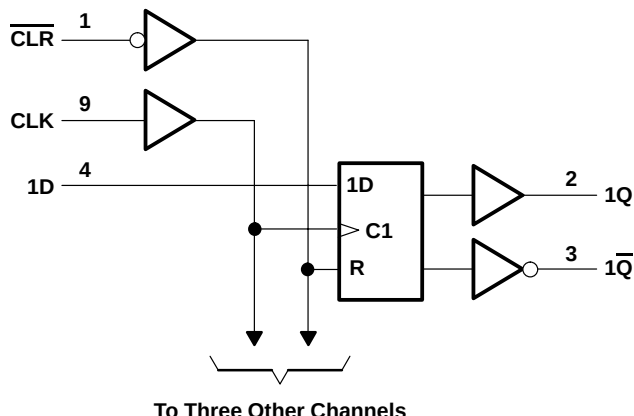
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CD74AC175

QUADRUPLE D-TYPE FLIP-FLOP WITH CLEAR

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0$ V or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ V or $V_O > V_{CC}$) (see Note 1)	±50 mA
Continuous output current, I_O ($V_O > 0$ V or $V_O < V_{CC}$)	±50 mA
Continuous current through V_{CC} or GND	±200 mA
Package thermal impedance, θ_{JA} (see Note 2)	73°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			$T_A = 25^\circ\text{C}$		–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		1.5	5.5	1.5	5.5	1.5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 1.5$ V	1.2		1.2		1.2		V
		$V_{CC} = 3$ V	2.1		2.1		2.1		
		$V_{CC} = 5.5$ V	3.85		3.85		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 1.5$ V		0.3		0.3		0.3	V
		$V_{CC} = 3$ V		0.9		0.9		0.9	
		$V_{CC} = 5.5$ V		1.65		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 4.5$ V to 5.5 V		–24		–24		–24	mA
I_{OL}	Low-level output current	$V_{CC} = 4.5$ V to 5.5 V		24		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.5$ V to 3 V		50		50		50	ns/V
		$V_{CC} = 3.6$ V to 5.5 V		20		20		20	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = –50 µA	1.5 V	1.4		1.4		1.4		V
			3 V	2.9		2.9		2.9		
			4.5 V	4.4		4.4		4.4		
		I _{OH} = –4 mA	3 V	2.58		2.4		2.48		
		I _{OH} = –24 mA	4.5 V	3.94		3.7		3.8		
		I _{OH} = –50 mA [†]	5.5 V			3.85				
		I _{OH} = –75 mA [†]	5.5 V					3.85		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 50 µA	1.5 V	0.1		0.1		0.1		V
			3 V	0.1		0.1		0.1		
			4.5 V	0.1		0.1		0.1		
		I _{OL} = 12 mA	3 V	0.36		0.5		0.44		
		I _{OL} = 24 mA	4.5 V	0.36		0.5		0.44		
		I _{OL} = 50 mA [†]	5.5 V			1.65				
		I _{OL} = 75 mA [†]	5.5 V					1.65		
I _I	V _I = V _{CC} or GND		5.5 V	±0.1		±1		±1		µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0		5.5 V	8		160		80		µA
C _i				10		10		10		pF

[†] Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

timing requirements over recommended operating free-air temperature range, V_{CC} = 1.5 V (unless otherwise noted)

				–55°C to 125°C		–40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency				8		9	MHz
t _w	Pulse duration			CLR low		50	44	ns
				CLK high or low		63	55	
t _{su}	Setup time before CLK↑			Data		2	2	ns
t _h	Hold time, data after CLK↑					2	2	ns
t _{rec}	Recovery time, before CLK↑			CLR↑		1	1	ns

CD74AC175

QUADRUPLE D-TYPE FLIP-FLOP

WITH CLEAR

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

			–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		71		81		MHz
t _w	Pulse duration	CLR low	5.6		4.9		ns
		CLK high or low	7		6.1		
t _{su}	Setup time before CLK↑	Data	2		2		ns
t _h	Hold time, data after CLK↑		2		2		ns
t _{rec}	Recovery time, before CLK↑	CLR↑	1		1		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted)

			–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		100		114		MHz
t _w	Pulse duration	CLR low	4		3.5		ns
		CLK high or low	5		4.4		
t _{su}	Setup time before CLK↑	Data	2		2		ns
t _h	Hold time, data after CLK↑		2		2		ns
t _{rec}	Recovery time, before CLK↑	CLR↑	1		1		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 1.5\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f _{max}			8		9		MHz
t _{PLH}	CLK	Any Q	153		139		ns
t _{PHL}			153		139		
t _{PLH}	$\overline{\text{CLR}}$	Any Q	153		139		ns
t _{PHL}			153		139		

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			71		81		MHz
t_{PLH}	CLK	Any Q	4.3	17.1	4.4	15.5	ns
t_{PHL}			4.3	17.1	4.4	15.5	
t_{PLH}	CLR	Any Q	4.3	17.1	4.4	15.5	ns
t_{PHL}			4.3	17.1	4.4	15.5	



switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{\max}$			100		114		MHz
t_{PLH}	CLK	Any Q	3.1	12.2	3.2	11.1	ns
t_{PHL}			3.1	12.2	3.2	11.1	
t_{PLH}	$\overline{\text{CLR}}$	Any Q	3.1	12.2	3.2	11.1	ns
t_{PHL}			3.1	12.2	3.2	11.1	

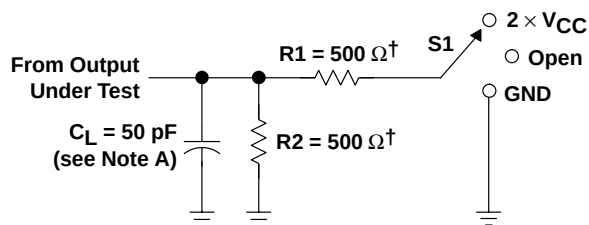
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	55	pF

CD74AC175 QUADRUPLE D-TYPE FLIP-FLOP WITH CLEAR

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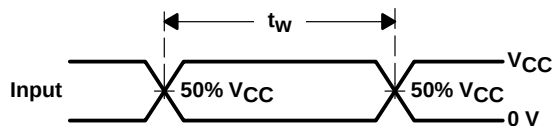
PARAMETER MEASUREMENT INFORMATION



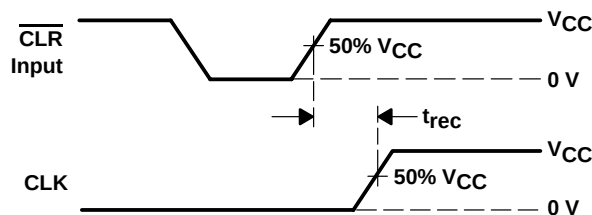
† When $V_{CC} = 1.5 \text{ V}$, $R1 = R2 = 1 \text{ k}\Omega$

LOAD CIRCUIT

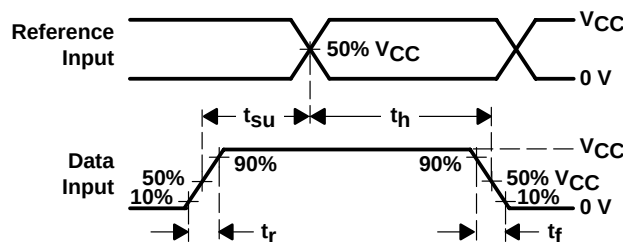
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



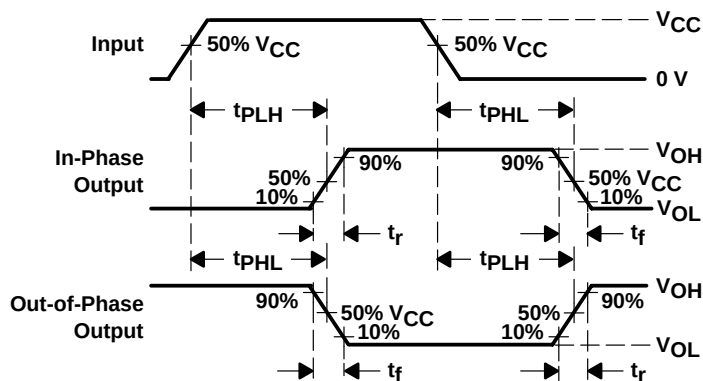
VOLTAGE WAVEFORMS
PULSE DURATION



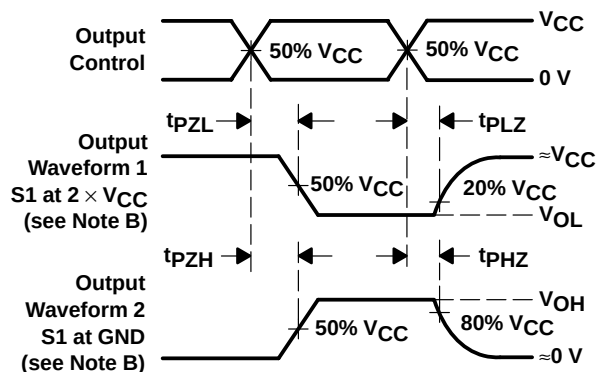
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



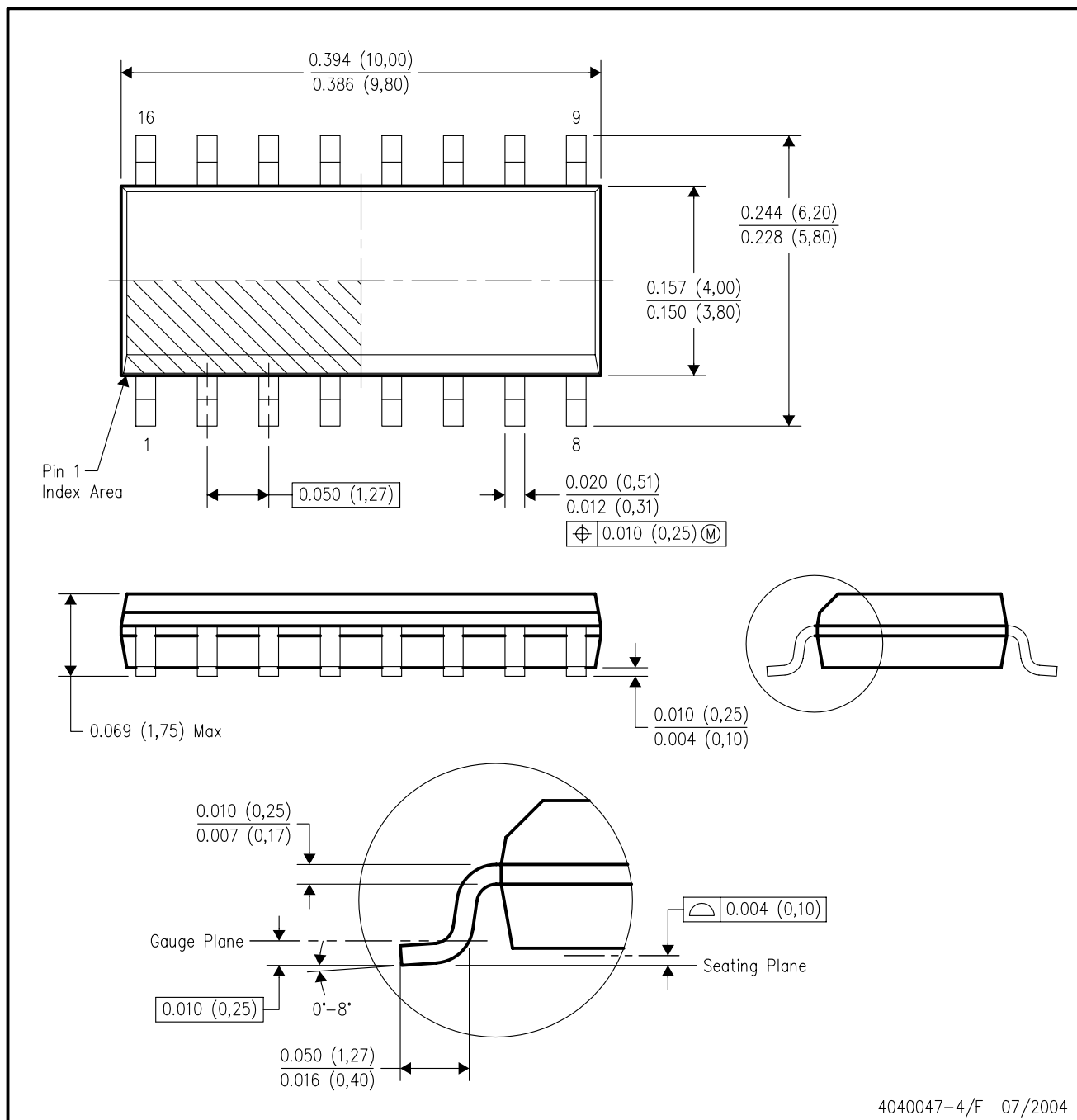
VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$. Phase relationships between waveforms are arbitrary.
 - For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

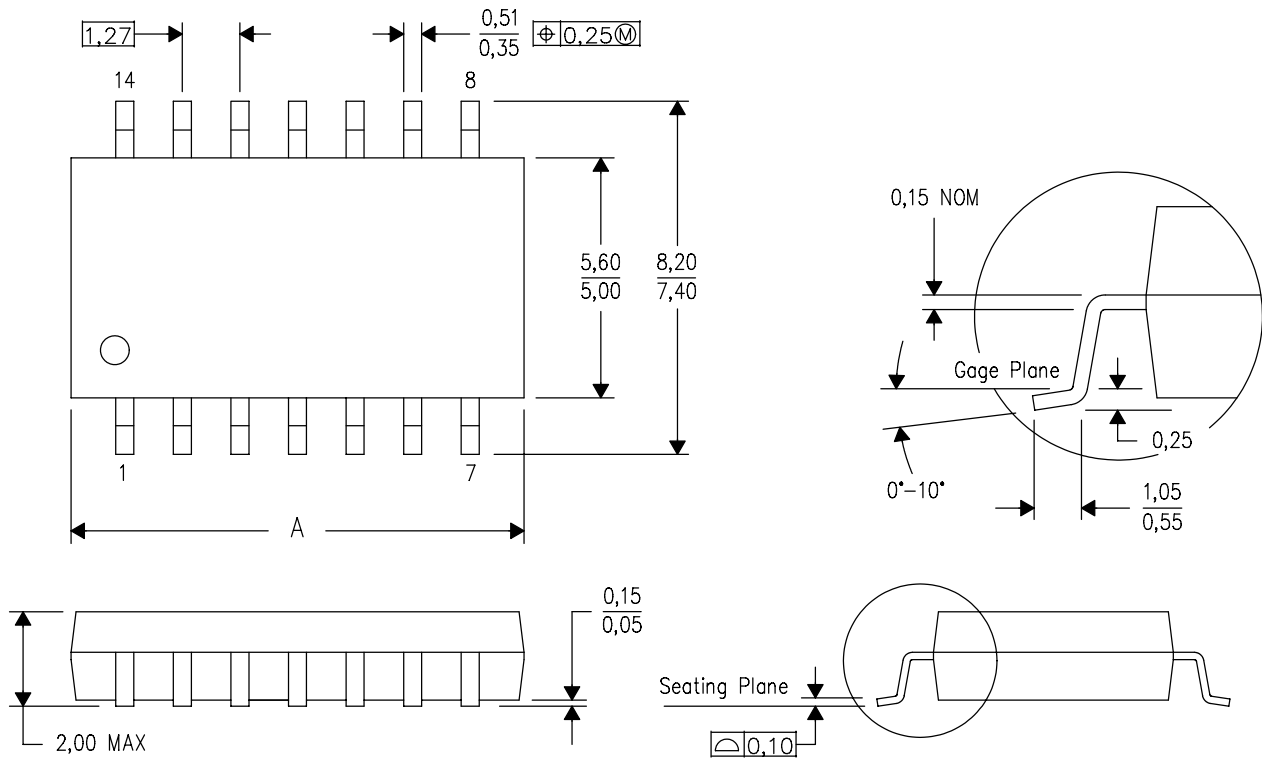
- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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