

- Inputs Are TTL-Voltage Compatible
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable

description/ordering information

The 'ACT163 devices are 4-bit binary counters. These synchronous, presetable counters feature an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change, coincident with each other, when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

The counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. Presetting is synchronous; therefore, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function is synchronous. A low level at the clear (CLR) input sets all four of the flip-flop outputs low after the next low-to-high transition of CLK, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to CLR to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP, ENT, and a ripple-carry output (RCO) are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15, with Q_A high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These devices feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or LOAD) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

ORDERING INFORMATION

| T _A | PACKAGE [†] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------|---------------|-----------------------|------------------|
| -55°C to 125°C | PDIP – E | Tube | CD74ACT163E | CD74ACT163E |
| | SOIC – M | Tube | CD74ACT163M | ACT163M |
| | | Tape and reel | CD74ACT163M96 | |
| | CDIP – F | Tube | CD54ACT163F3A | CD54ACT163F3A |



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 **TEXAS
INSTRUMENTS**

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CD54ACT163, CD74ACT163 4-BIT SYNCHRONOUS BINARY COUNTERS

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FUNCTION TABLE

| INPUTS | | | | | | OUTPUTS | | FUNCTION |
|--------|-----|-----|-----|------|---------|----------------|--------|---------------|
| CLR | CLK | ENP | ENT | LOAD | A,B,C,D | Q _n | RCO | |
| L | ↑ | X | X | X | X | L | L | Reset (clear) |
| h | ↑ | X | X | l | l | L | L | Parallel load |
| h | ↑ | X | X | l | h | H | Note 1 | |
| h | ↑ | h | h | h | X | Count | Note 1 | Count |
| h | X | l | X | h | X | q _n | Note 1 | Inhibit |
| h | X | X | l | h | X | q _n | L | |

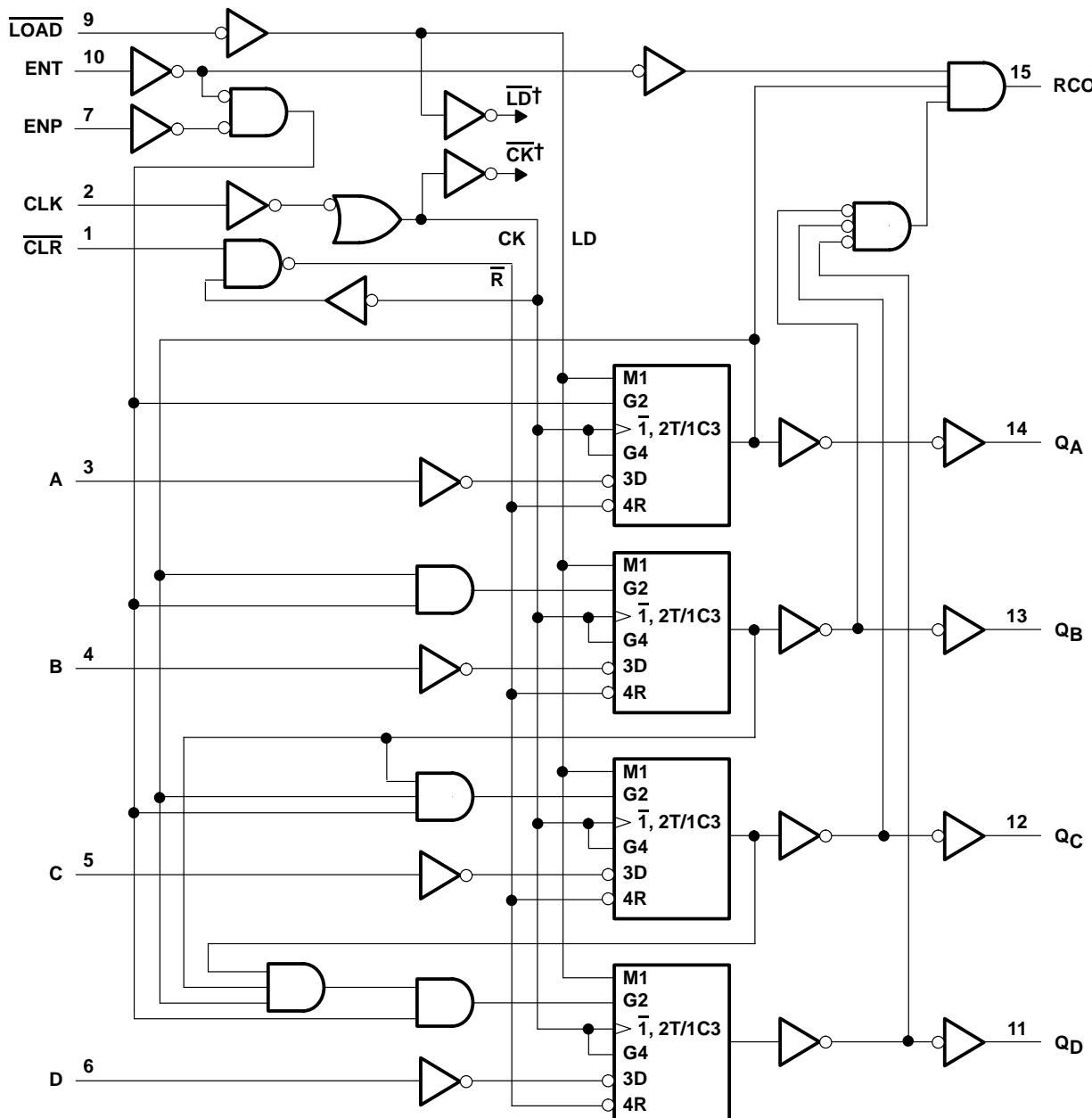
H = high level, L = low level, X = don't care, h = high level one setup time prior to the CLK low-to-high transition, l = low level one setup time prior to the CLK low-to-high transition, q = the state of the referenced output prior to the CLK low-to-high transition, and ↑ = CLK low-to-high transition.

NOTE 1: The RCO output is high when ENT is high and the counter is at terminal count (HHHH).



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logic diagram (positive logic)

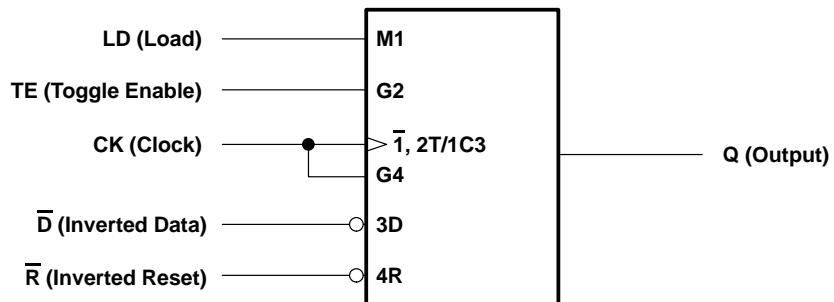


† For simplicity, routing of complementary signals \overline{LD} and \overline{CK} is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

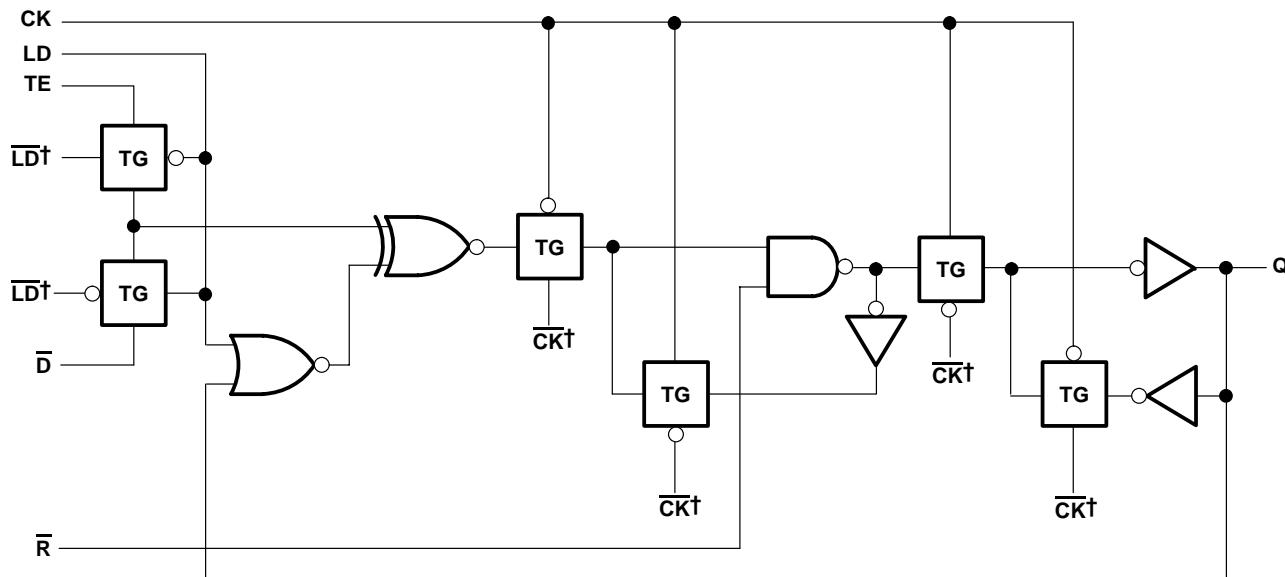
CD54ACT163, CD74ACT163 4-BIT SYNCHRONOUS BINARY COUNTERS

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logic symbol, each D/T flip-flop



logic diagram, each D/T flip-flop (positive logic)

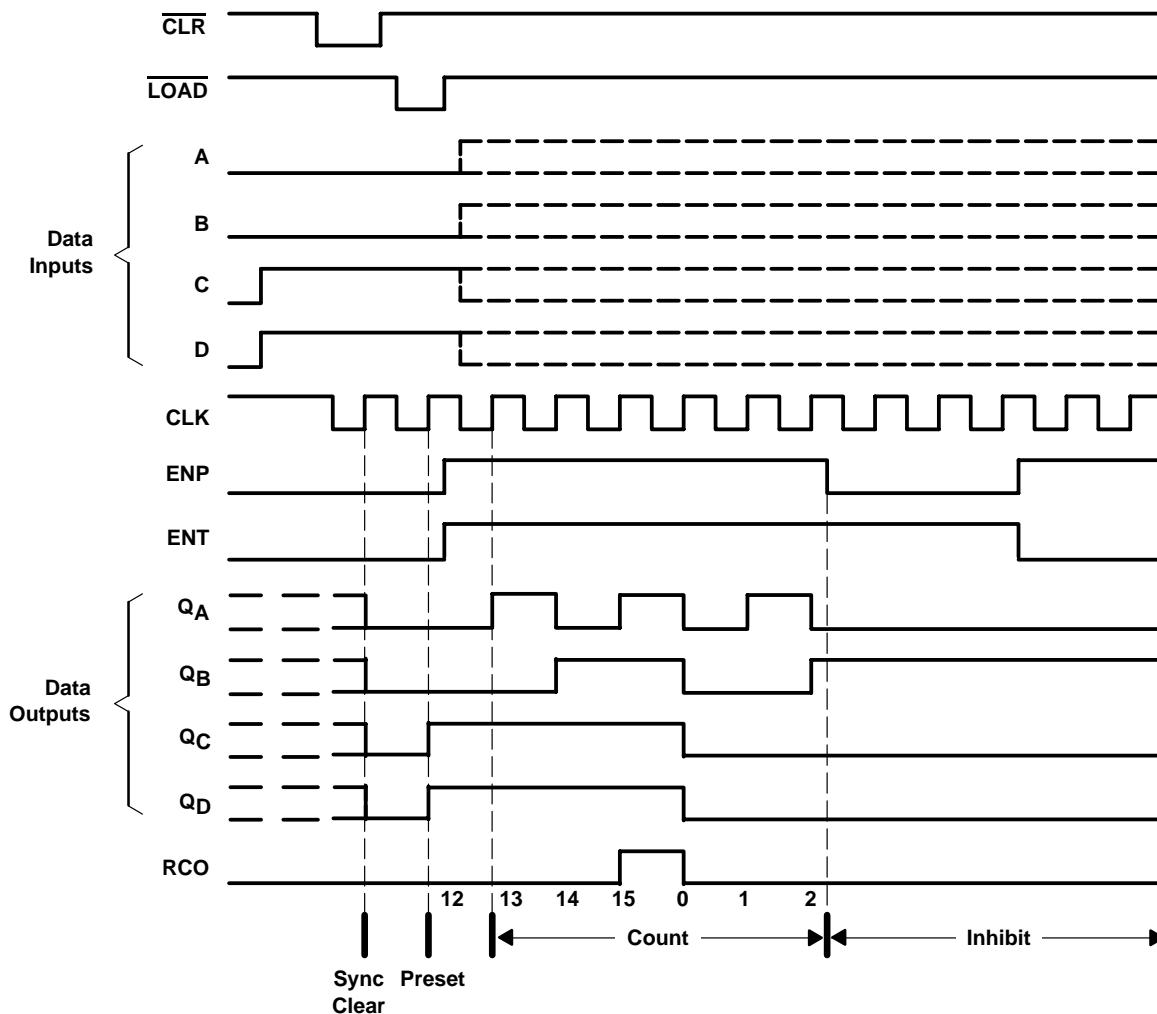


† The origins of \overline{LD} and \overline{CK} are shown in the logic diagram of the overall device.

typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (synchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

| | | TA = 25°C | | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|-----------------|------------------------------------|-----------|-----------------|----------------|-----------------|---------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | 2 | | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | | 0.8 | | 0.8 | V |
| V _I | Input voltage | 0 | V _{CC} | 0 | V _{CC} | 0 | V _{CC} | V |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | | -24 | | -24 | | -24 | mA |
| I _{OL} | Low-level output current | | 24 | | 24 | | 24 | mA |
| Δt/Δv | Input transition rise or fall rate | | 10 | | 10 | | 10 | ns |

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|--------------------|-------------------------------------------------------------|---------------------------|-----------------------|------|----------------|------|---------------|------|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -50 μA | 4.5 V | 4.4 | 4.4 | 4.4 | 4.4 | 4.4 | V |
| | | I _{OH} = -24 mA | 4.5 V | 3.94 | 3.7 | 3.8 | 3.8 | 3.8 | |
| | | I _{OH} = -50 mA† | 5.5 V | – | 3.85 | – | – | 3.85 | |
| | | I _{OH} = -75 mA† | 5.5 V | – | – | – | 3.85 | 3.85 | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 50 μA | 4.5 V | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | V |
| | | I _{OL} = 24 mA | 4.5 V | 0.36 | 0.5 | 0.44 | 0.44 | 0.44 | |
| | | I _{OL} = 50 mA† | 5.5 V | – | 1.65 | – | – | 1.65 | |
| | | I _{OL} = 75 mA† | 5.5 V | – | – | – | 1.65 | 1.65 | |
| I _I | V _I = V _{CC} or GND | | 5.5 V | ±0.1 | ±1 | ±1 | ±1 | ±1 | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | | 5.5 V | 8 | 160 | 80 | 80 | 80 | μA |
| ΔI _{CC} ‡ | V _I = V _{CC} - 2.1 V | | 4.5 V to 5.5 V | 2.4 | 3 | 2.8 | 2.8 | 2.8 | mA |
| C _i | | | | 10 | 10 | 10 | 10 | 10 | pF |

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

‡ Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

ACT INPUT LOAD TABLE

| INPUT | UNIT LOAD |
|---------------|-----------|
| A, B, C, or D | 0.13 |
| CLK | 1 |
| CLR, ENT | 0.83 |
| LOAD | 0.67 |
| ENP | 0.5 |

Unit Load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

timing requirements over recommended operating conditions (unless otherwise noted)

| | | | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|--------------------|-------------------------|-----------------|----------------|-----|---------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | | | 80 | 91 | 91 | MHz |
| t _w | Pulse duration | CLK high or low | 6.2 | 5.4 | 5.4 | 5.4 | ns |
| t _{su} | Setup time, before CLK↑ | A, B, C, or D | 5 | 4.4 | 4.4 | 4.4 | ns |
| | | ENP or ENT | 6 | 5.3 | 5.3 | 5.3 | |
| | | LOAD low | 7.5 | 6.6 | 6.6 | 6.6 | |
| | | CLR inactive | 7.5 | 6.6 | 6.6 | 6.6 | |
| t _h | Hold time, after CLK↑ | A, B, C, or D | 0 | 0 | 0 | 0 | ns |
| | | ENP or ENT | 0 | 0 | 0 | 0 | |
| | | LOAD low | 0 | 0 | 0 | 0 | |
| | | CLR inactive | 0 | 0 | 0 | 0 | |

CD54ACT163, CD74ACT163 4-BIT SYNCHRONOUS BINARY COUNTERS

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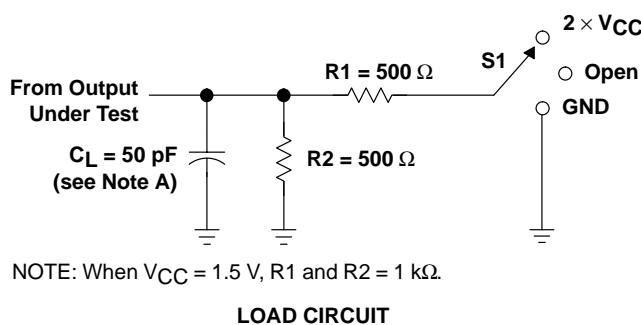
switching characteristics over recommended operating conditions, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|------------|-----------------|----------------|-------------------|------|------------------|------|------|
| | | | MIN | MAX | MIN | MAX | |
| f_{\max} | | | 80 | | 91 | | MHz |
| t_{pd} | CLK | RCO | 4.2 | 16.7 | 4.3 | 15.2 | ns |
| | | Any Q | 4.1 | 16.5 | 4.2 | 15 | |
| | ENT | RCO | 2.7 | 10.8 | 2.8 | 9.8 | |

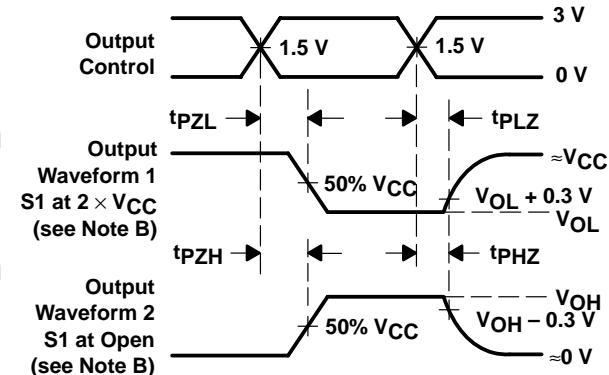
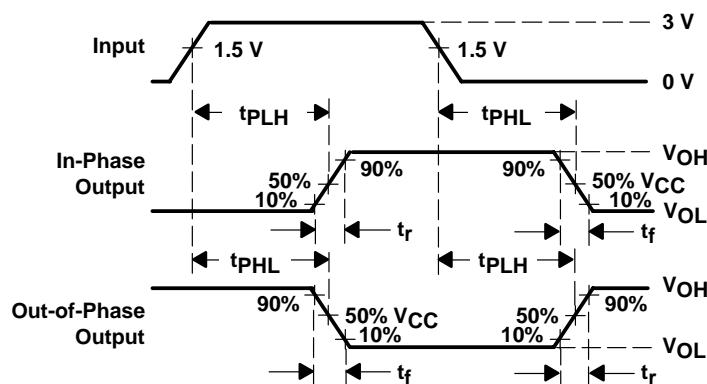
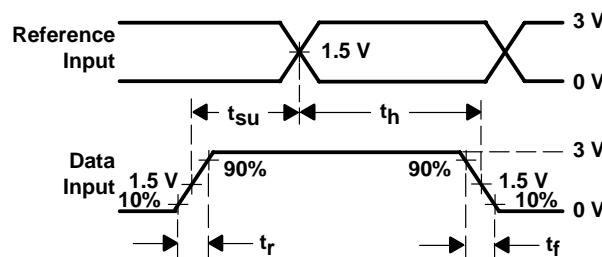
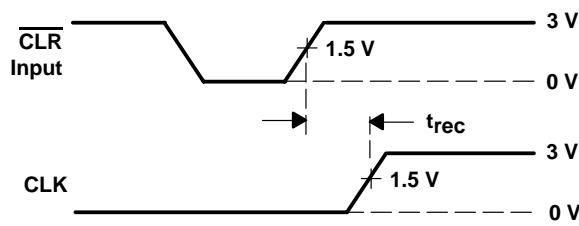
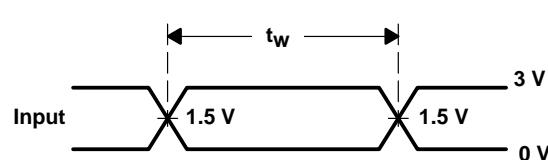
operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|----------------------------------------|-----------------|-----|------|
| C_{pd} Power dissipation capacitance | No load | 66 | pF |

PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PZL}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |



NOTES:

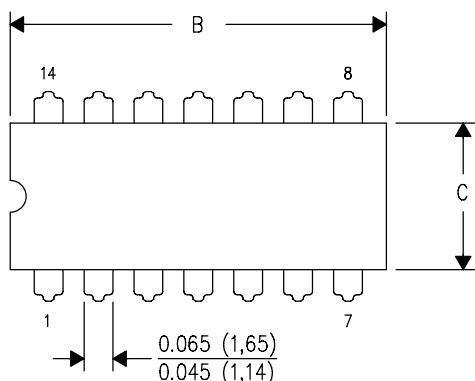
- C_L includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$. Phase relationships between waveforms are arbitrary.
- For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- The outputs are measured one at a time with one input transition per measurement.
- t_{PLH} and t_{PHL} are the same as t_{pd} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

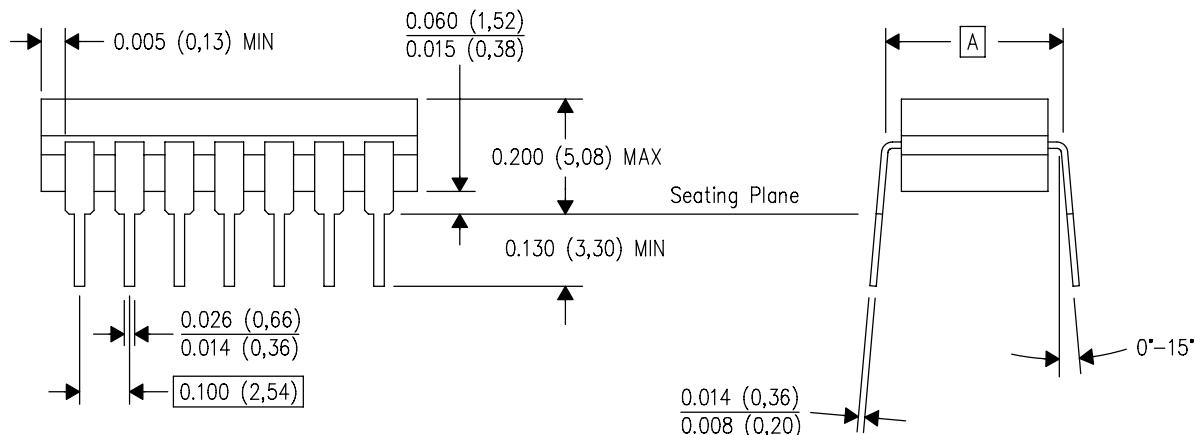
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



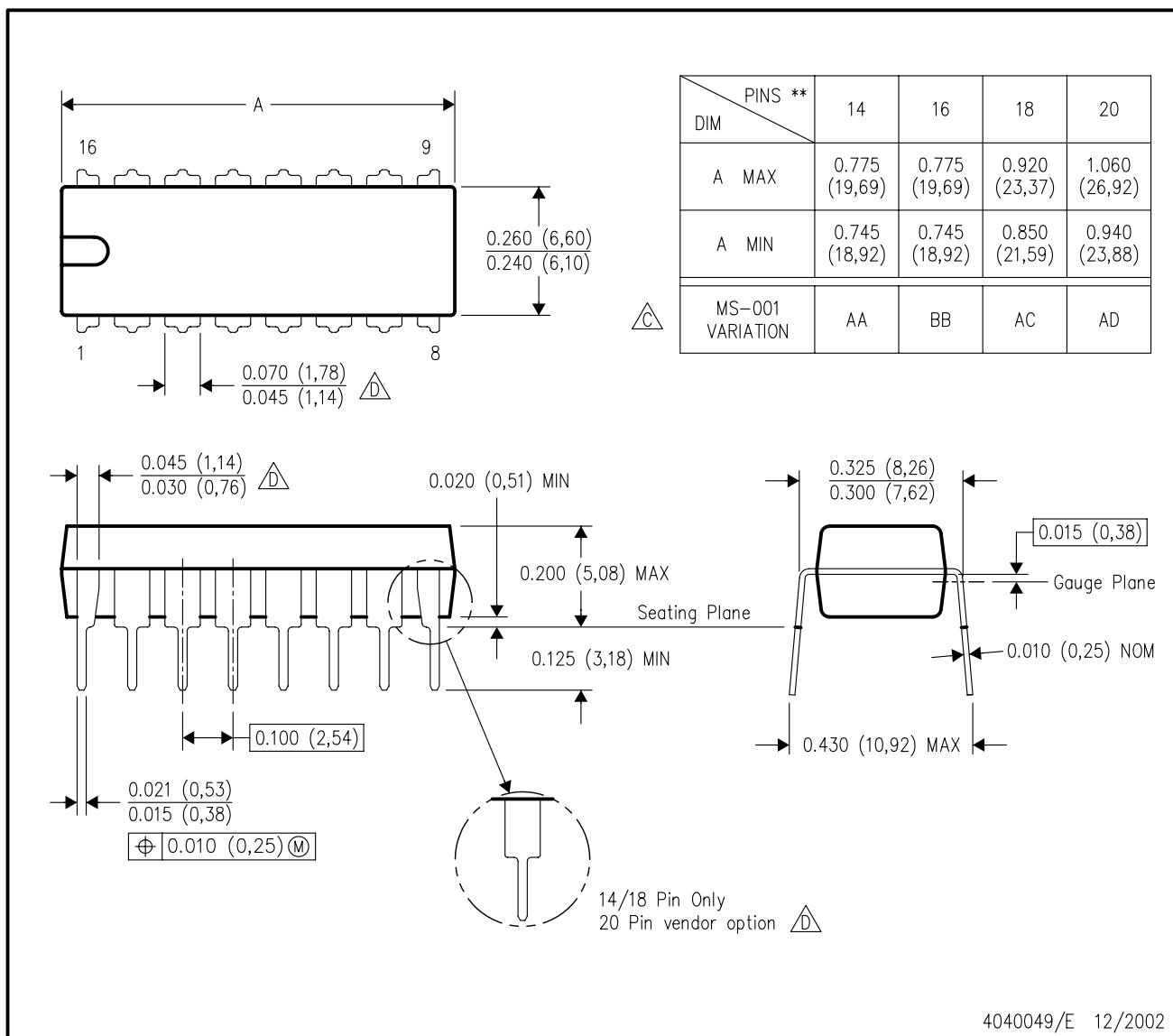
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



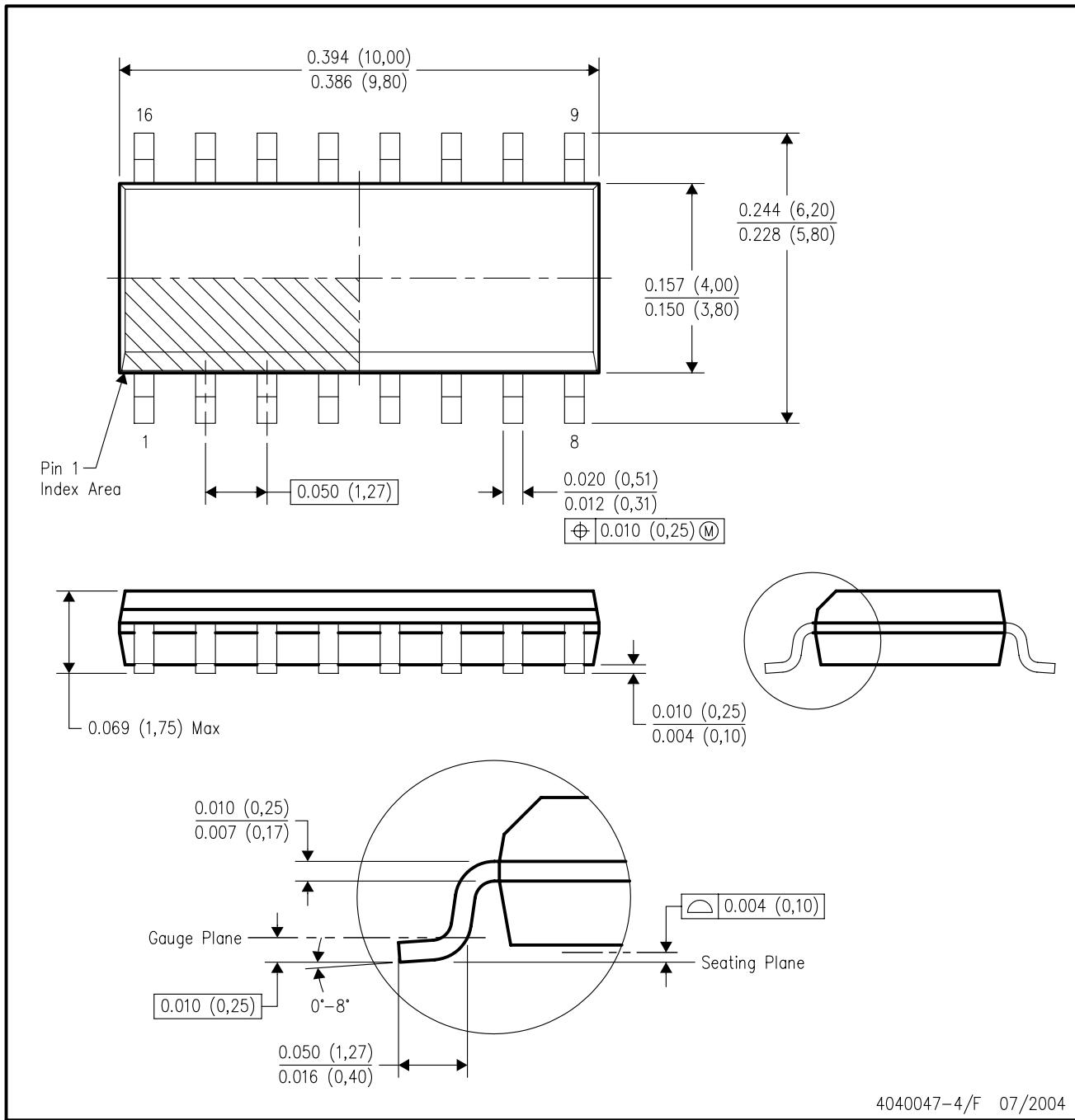
NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/F 07/2004

NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-012 variation AC.

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