

CD54/74HC540, CD74HCT540, CD54/74HC541, CD54/74HCT541

High-Speed CMOS Logic Octal Buffer and Line Drivers, Three-State

Features

- 'HC540, CD74HCT540 Inverting
- 'HC541, 'HCT541 Non-Inverting
- Buffered Inputs
- Three-State Outputs
- Bus Line Driving Capability
- Typical Propagation Delay = 9ns at $V_{CC} = 5V$,
 $C_L = 15pF$, $T_A = 25^{\circ}C$
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range ... $-55^{\circ}C$ to $125^{\circ}C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility,
 $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The 'HC540 and CD74HCT540 are Inverting Octal Buffers and Line Drivers with Three-State Outputs and the capability to drive 15 LSTTL loads. The 'HC541 and 'HCT541 are Non-Inverting Octal Buffers and Line Drivers with Three-State Outputs that can drive 15 LSTTL loads. The Output Enables ($\overline{OE1}$) and ($\overline{OE2}$) control the Three-State Outputs. If either $\overline{OE1}$ or $\overline{OE2}$ is HIGH the outputs will be in the high impedance state. For data output $\overline{OE1}$ and $\overline{OE2}$ both must be LOW.

Ordering Information

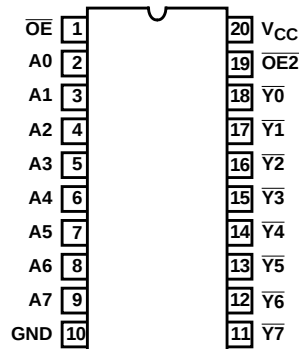
PART NUMBER	TEMP. RANGE ($^{\circ}C$)	PACKAGE
CD54HC540F3A	-55 to 125	20 Ld Cerdip
CD54HC541F3A	-55 to 125	20 Ld Cerdip
CD54HCT541F3A	-55 to 125	20 Ld Cerdip
CD74HC540E	-55 to 125	20 Ld PDIP
CD74HC540M	-55 to 125	20 Ld SOIC
CD74HC540M96	-55 to 125	20 Ld SOIC
CD74HC541E	-55 to 125	20 Ld PDIP
CD74HC541M	-55 to 125	20 Ld SOIC
CD74HC541M96	-55 to 125	20 Ld SOIC
CD74HC541PW	-55 to 125	20 Ld TSSOP
CD74HC541PWR	-55 to 125	20 Ld TSSOP
CD74HCT540E	-55 to 125	20 Ld PDIP
CD74HCT540M	-55 to 125	20 Ld SOIC
CD74HCT540M96	-55 to 125	20 Ld SOIC
CD74HCT541E	-55 to 125	20 Ld PDIP
CD74HCT541M	-55 to 125	20 Ld SOIC
CD74HCT541M96	-55 to 125	20 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

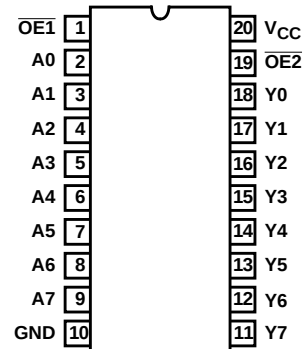
CD54/74HC540, CD74HCT540, CD54/74HC541, CD54/74HCT541

Pinouts

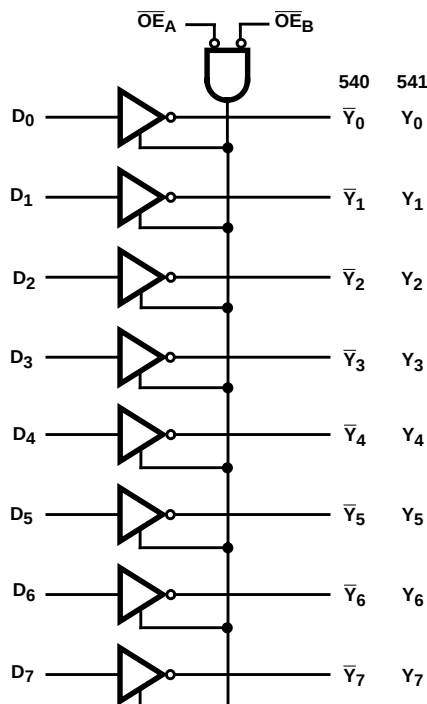
CD54HC540
(CERDIP)
CD74HC540, CD74HCT540
(PDIP, SOIC)
TOP VIEW



CD54HC541, CD54HCT541
(CERDIP)
CD74HC541
(PDIP, SOIC, TSSOP)
CD74HCT541
(PDIP, SOIC)
TOP VIEW



Functional Diagram



CD54/74HC540, CD74HCT540, CD54/74HC541, CD54/74HCT541

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE1}$	$\overline{OE2}$	An	540	541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

X= Don't Care

Z = High Impedance

CD54/74HC540, CD74HCT540, CD54/74HC541, CD54/74HCT541

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Drain Current, per Output, I_O	
For $-0.5V < V_O < V_{CC} + 0.5V$	$\pm 35mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^{\circ}C/W$)
E (PDIP) Package	69
M (SOIC) Package	58
PW (TSSOP) Package	83
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$
(SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range, T_A	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, V_{CC}	
HC Types	.2V to 6V
HCT Types	.4.5V to 5.5V
DC Input or Output Voltage, V_I , V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	V _{OH}	V _{IH} or V _{IL}	-	-	-	-	-	-	-	-	-	V
			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	V _{OL}	V _{IH} or V _{IL}	-	-	-	-	-	-	-	-	-	V
			6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μA

CD54/74HC540, CD74HCT540, CD54/74HC541, CD54/74HCT541

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μA
Three- State Leakage Current	I _{OZ}	V _{IL} or V _{IH}	V _O = V _{CC} or GND	6	-	-	±0.5	-	±5.0	-	±10	μA
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Three- State Leakage Current	I _{OZ}	V _{IL} or V _{IH}	V _O = V _{CC} or GND	5.5	-	-	±0.5	-	±5.0	-	±10	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 2)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

- For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS	
	HCT540	HCT541
A0 - A7	1	0.4
$\overline{OE}2$	0.75	0.75
$\overline{OE}1$	1.15	1.15

NOTE: Unit Load is ΔI_{CC} limit specific in DC Electrical Specifications Table, e.g., 360μA max. at 25°C.

CD54/74HC540, CD74HCT540, CD54/74HC541, CD54/74HCT541

Switching Specifications $C_L = 50\text{pF}$, Input t_r , $t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay Data to Outputs (540)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	110	-	140	-	165	ns
			4.5	-	-	22	-	28	-	33	ns
		C _L = 15pF	5	-	9	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	19	-	24	-	28	ns
Data to Outputs (541)	t _{PLZ} , t _{PHZ}	C _L = 50pF	2	-	-	115	-	145	-	175	ns
			4.5	-	-	23	-	29	-	35	ns
		C _L = 15pF	5	-	9	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	20	-	25	-	30	ns
Output Enable and Disable to Outputs (540)	t _{PLZ} , t _{PHZ}	C _L = 50pF	2	-	-	160	-	200	-	240	ns
			4.5	-	-	32	-	40	-	48	ns
		C _L = 15pF	5	-	13	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	27	-	34	-	41	ns
Output Enable and Disable to Outputs (541)	t _{PLZ} , t _{PHZ}	C _L = 50pF	2	-	-	160	-	200	-	240	ns
			4.5	-	-	32	-	40	-	48	ns
		C _L = 15pF	5	-	14	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	23	-	29	-	35	ns
Output Transition Time	t _{THL} , t _{TLH}	C _L = 50pF	2	-	-	60	-	75	-	90	ns
			4.5	-	-	12	-	15	-	18	ns
			6	-	-	10	-	13	-	15	ns
Input Capacitance	C _I	C _L = 50pF	-	10	-	10	-	10	-	10	pF
Three-State Output Capacitance	C _O	-	-	20	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 3, 4) (540)	C _{PD}	C _L = 15pF	5	-	50	-	-	-	-	-	pF
Power Dissipation Capacitance (Notes 3, 4) (541)	C _{PD}	C _L = 15pF	5	-	48	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay Data to Outputs (540)	t _{PHL} , t _{PLH}	C _L = 50pF	4.5	-	-	24	-	30	-	36	ns
		C _L = 15pF	5	-	9	-	-	-	-	-	ns
Data to Outputs (541)	t _{PHL} , t _{PLH}	C _L = 50pF	4.5	-	-	28	-	35	-	42	ns
		C _L = 15pF	5	-	11	-	-	-	-	-	ns
Output Enable and Disable to Outputs (540, 541)	t _{PLZ} , t _{PHZ}	C _L = 50pF	4.5	-	-	35	-	44	-	53	ns
		C _L = 15pF	5	-	14	-	-	-	-	-	ns
Output Transition Time	t _{TLH} , t _{THL}	C _L = 50pF	4.5	-	-	12	-	15	-	18	ns
Input Capacitance	C _I	C _L = 50pF	-	10	-	10	-	10	-	10	pF

CD54/74HC540, CD74HCT540, CD54/74HC541, CD54/74HCT541

Switching Specifications $C_L = 50\text{pF}$, Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Three-State Output Capacitance	C_O	-	-	20	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 3, 4) (540, 541)	C_{PD}	$C_L = 15\text{pF}$	5	-	55	-	-	-	-	-	pF

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per channel.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

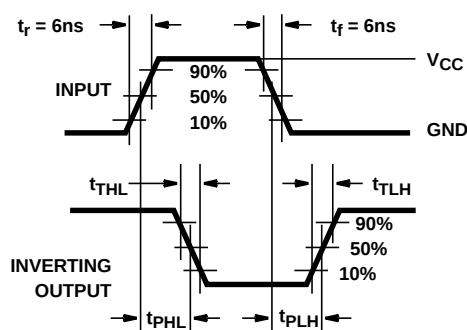


FIGURE 1. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

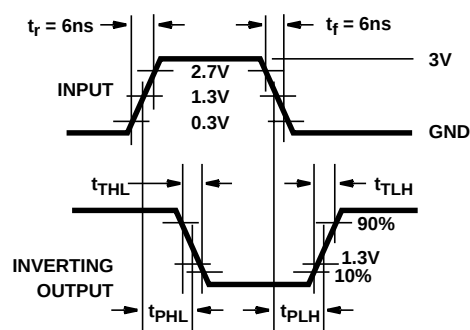


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

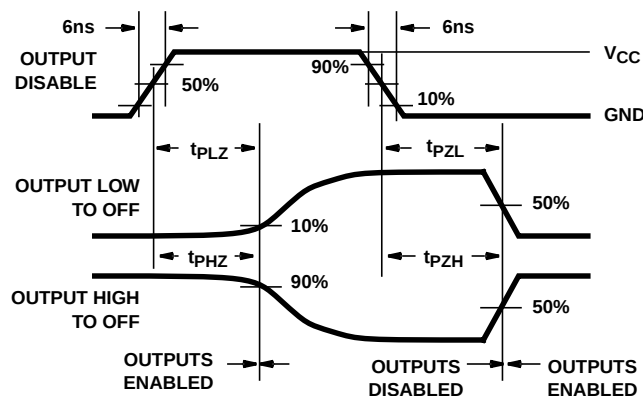


FIGURE 3. HC THREE-STATE PROPAGATION DELAY WAVEFORM

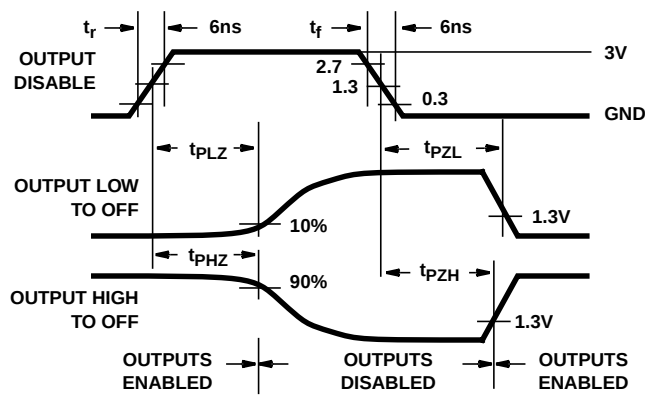
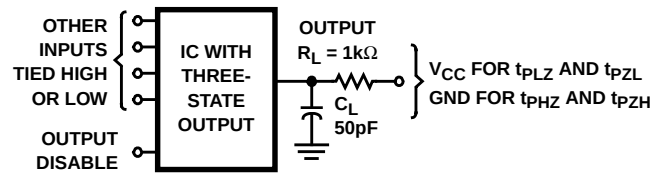


FIGURE 4. HCT THREE-STATE PROPAGATION DELAY WAVEFORM

Test Circuits and Waveforms (Continued)



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC} , $C_L = 50pF$.

FIGURE 5. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



4040000-4/F 06/2004

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AC.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

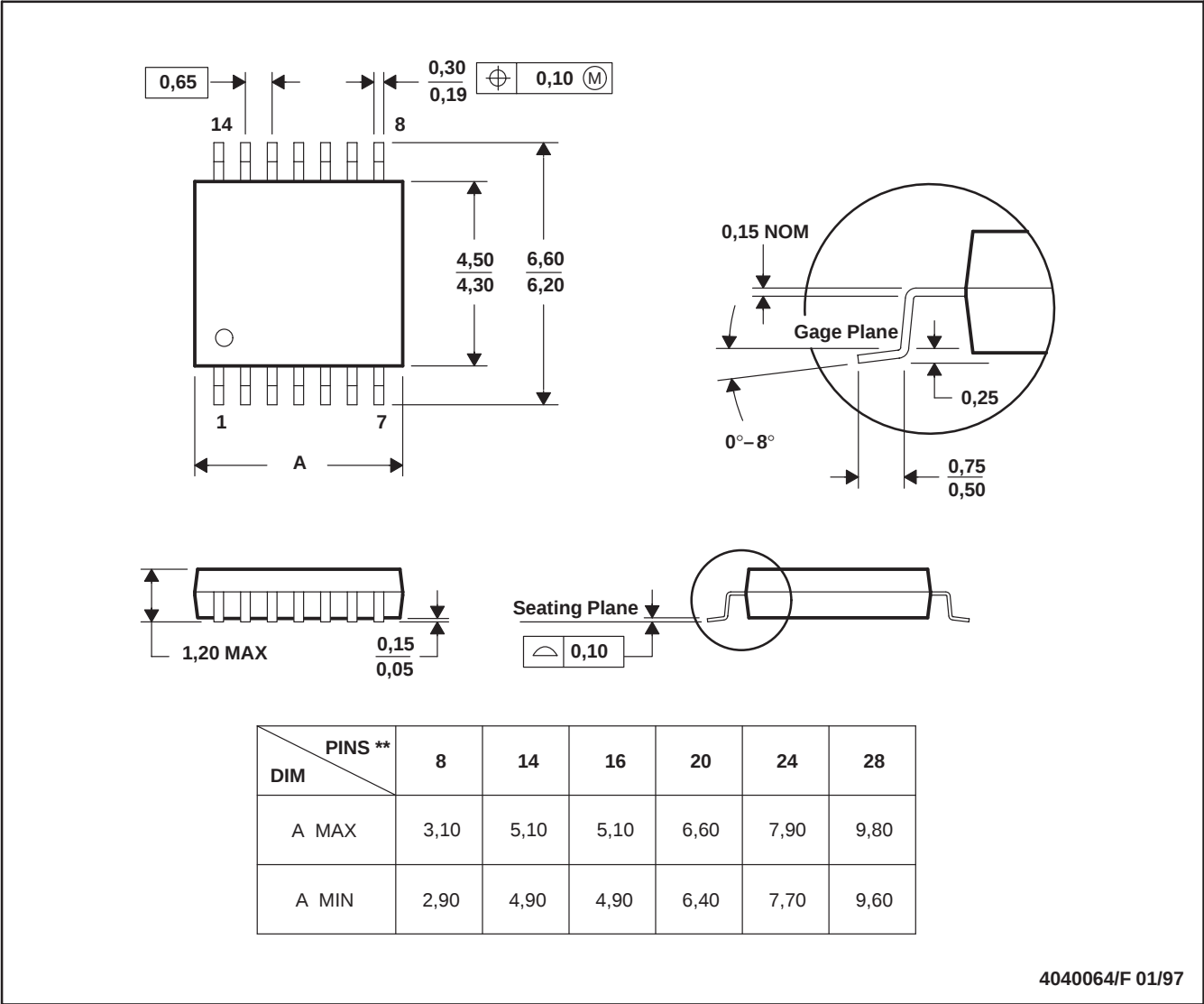
28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)
14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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