CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX7011
Digital Voice Processor

D/7011_FI1.x/5 February 2013

DATASHEET

Advance Information

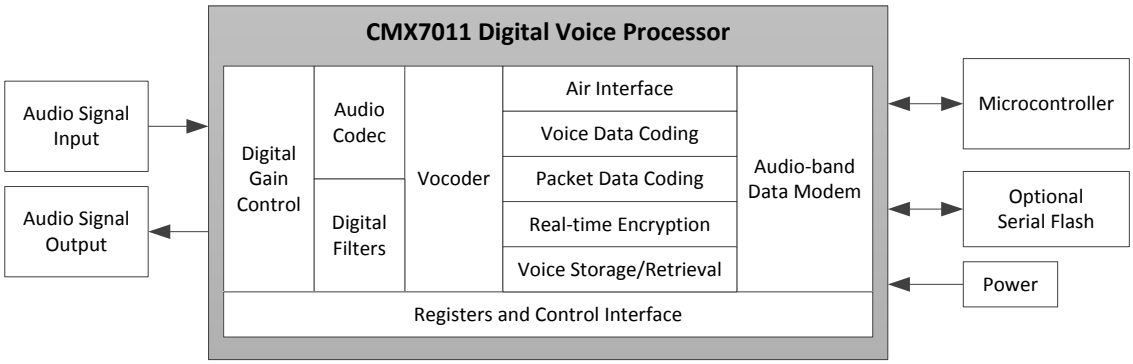
7011FI-1.x: Digital Voice Encryption for Analogue Radio Systems

Features

- Digital voice security on analogue PMR channels (12.5kHz/25kHz)
- Simple interfacing, via audio connections, to existing PMR radio
- Ultimate in high-level analogue radio security
- Embedded RALCWI Vocoder (supplied under licence and royalty free)
- Embedded audio-band modem
- Built in robust over-air data protocol with good tolerance to bit errors
- Ultimate in high-level analogue radio security
- Real-time digital voice encryption with user-programmable 16-bit encryption keys
- External voice data routing option
- Programmable instant voice capture – eliminating 'PTT' clipping
- Voice storage and retrieval with 'step back' feature
- Packet data with user-programmable packet data size
- Flexible 256 address programming
- Late entry/re-entry operation, provides optimum performance in fading conditions
- Small 48-pin LQFP/VQFN package options

Applications

- Real-time voice security
- Voice encryption on analogue PMR radios
- Secure wireless door access and gate entry systems
- Providing the digital advantage on analogue radio systems
- A Plug and Play device (the CMX188) can be made available for high quantity applications



1 Brief Description

The CMX7011 is a flexible, half duplex, digital voice processor specifically designed for digital voice encryption applications that transmits and receives secure voice via an embedded robust data modem for use within an analogue PMR. The device allows simple implementation and configuration within existing designs and is intended to be added to a radio via an accessory module or “feature socket”. The device is simple to control via a small, low-power microcontroller. The CMX7011 offers better quality speech than that of traditional analogue radios at the fringes of reception and, using the internal digital encryption algorithm, significantly higher levels of security are achieved.

Built in to the CMX7011 is CML's proven and reliable RALCWI (Robust Advanced Low Complexity Waveform Interpolation) vocoder providing near toll quality speech at a low bit rate. One of the most significant features in the CMX7011's design is the programmable push-to-talk (PTT) buffer which offers instant voice capture in transmit mode. The PTT buffer temporarily stores the initial part of the speech and can therefore eliminate clipping that can be caused by the time taken to decode sub audio signals like CTCSS and system delays caused by repeaters. Within the CMX7011's header frame is a user-programmable 8-bit address field which allows up to 256 individual user addresses to be defined.

The device includes programmable voice storage and retrieval with step-back feature which permits storage of a minimum of 20 seconds of vocoded speech in receive mode.

Packet data enables secure data transfer with CRC and optional interleaving of data bits with user-programmable packet data size.

Late entry allows a receiving radio to re-join a call after recovering from deep fade conditions

Note that text shown in pale grey indicates features that will be supported in future versions of the device.

This Data Sheet is the first part of a two-part document.

CONTENTS

It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

History

Version	Changes	Date
5	• Voice store and retrieve functionality added • Packet data functionality added	18th Feb 2013
4	• Correction of VDD to DVDD • Correction of streaming C-BUS description and timing constraints • Correction of I/O to GPIO, also references to GPIO1 and GPIO2 • Minor typographical improvements	24th Oct 2012
3	• New system diagram added to front of datasheet • New block diagram added to Section 2 • Information on external data routing added to Section 7.7 • Information on external data routing registers added to Section 9	3rd September 2012
2	• Information on noise gate registers added to Section 9.1 • Modification to IOCTRL register in Section 9.1 • Application note added for basic device operation in Section 10. • Various typographical and editorial changes	28th May 2012
1	• First release, Advance Information	5th Apr 2012

This is Advance Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document. Information in this advance document should not be relied upon for final product design.

2 Block Diagram

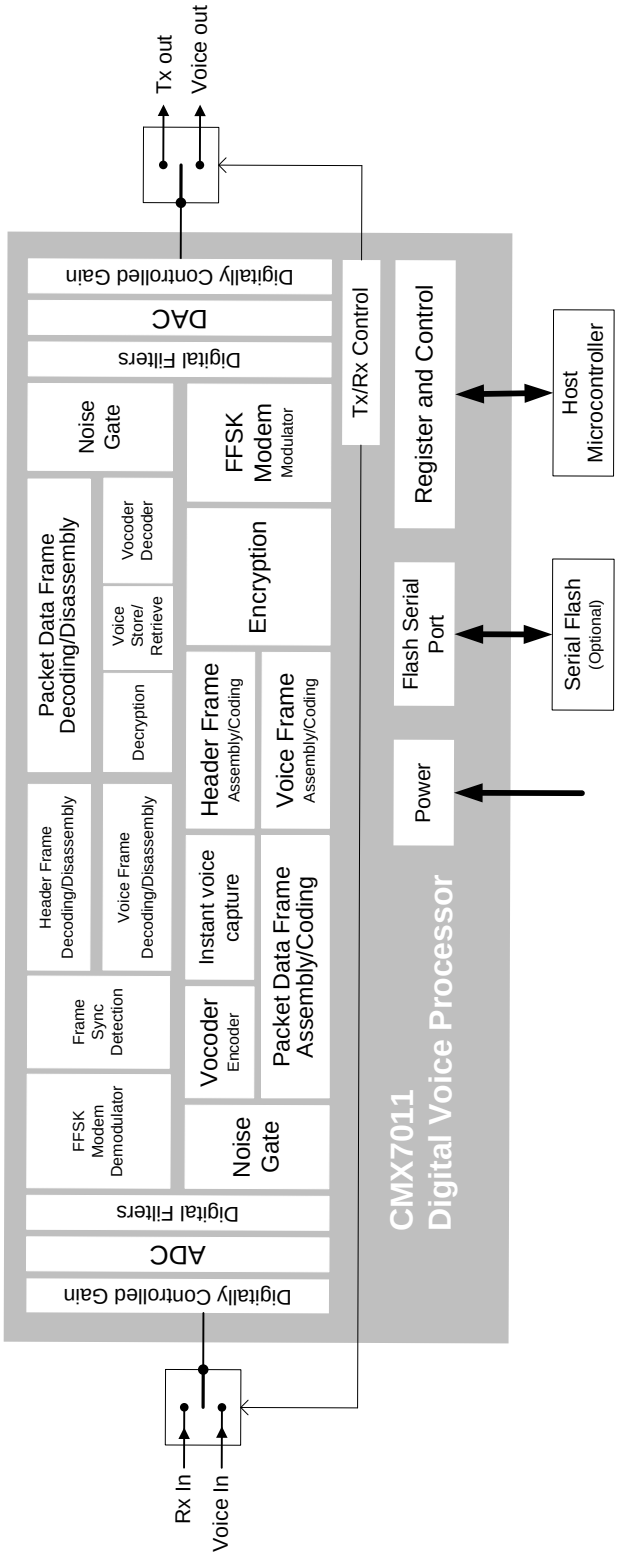


Figure 1 Block Diagram

3 Pin and Signal List

CMX7011 L4/Q3	Pin		Signal Description	
Pin No.	**Name**	**Type**		
1	AVDD	Power	Analogue Positive Power Supply 3.3V	
2	AVSS	Power	Analogue Negative Power Supply 0V	
3	VBIAS	Analogue Output	Analogue Bias (approximately 1.65 Volts)	
4	VSSREF	Power	Analogue Negative Reference	
5	INPUTP	Analogue Input	Audio CODEC Positive Input (self biased)	
6	INPUTN	Analogue Input	Audio CODEC Negative Input (self biased)	
7	AVDD	Power	Analogue Positive Power Supply 3.3V	
8	AVSS	Power	Analogue Negative Power Supply 0V	
9	VSSPA	Power	Output Amplifier Negative Power Supply 0V	
10	OUTP	Analogue Output	Audio CODEC – Amplifier Positive Output	
11	OUTN	Analogue Output	Audio CODEC – Amplifier Negative Output	
12	VDDPA	Power	Output Amplifier Positive Power Supply 3.3V	
13	DVDD	Power	Digital Positive Power Supply 1.8V	
14	~	NC	Reserved for future use. Do not connect to this pin.	
15	SDI	Digital Input	SSP port serial data input	FLASH PORT
16	SDO	Digital Output	SSP port serial data output	
17	SCLK	Digital Input	SSP port serial clock input	
18	~	NC	Reserved for future use. Do not connect to this pin.	
19	GPIO1	Digital Input/Output	General Purpose Input/Output	
20	GPIO2	Digital Input/Output	General Purpose Input/Output	
21	SSOUT	Digital Output	SSP Slave Select	
22	DVSS	Power	Negative Power Supply 0V	
23	~	NC	Reserved for future use. Do not connect to this pin.	
24	IOVDD	Power	Digital I/O Positive Power Supply 3.3V	
25	TEST	TEST	Must be connected to DV_{SS} via external 100kΩ resistor.	

CMX7011 L4/Q3	Pin		Signal Description	
Pin No.	**Name**	**Type**		
26	DVSS	Power	Negative Power Supply 0V	
27	XTAL/CLK	Input	Crystal Input	
28	XTALN	Output	Crystal Output	
29	IOVDD	Power	Digital I/O Positive Power Supply 3.3V	
30	RESETN	Digital Input	General Reset (active low)	
31	XTALSEL1	Digital Input	These bits select the crystal/clock frequency, according to Table 3.	
32	XTALSEL2	Digital Input		
33	XTALSEL3	Digital Input		
34	ENABXTAL	Digital Input	Enable Crystal Oscillator/External Clock Input	
35	IOVDD	Power	Digital I/O Positive Power Supply 3.3V	
36	~	NC	Reserved for future use. Do not connect to this pin.	
37	~	NC	Reserved for future use. Do not connect to this pin.	
38	~	NC	Reserved for future use. Do not connect to this pin.	
39	~	NC	Reserved for future use. Do not connect to this pin.	
40	~	NC	Reserved for future use. Do not connect to this pin.	
41	VSS	Power	Negative Power Supply 0V	
42	CLK	Digital Input	C-BUS Serial Clock	C-BUS
43	CDATA	Digital Input	C-BUS Command Data	
44	RDATA	Tri-state output	C-BUS Reply Data	
45	CSN	Digital Input	C-BUS Chip Select (bar)	
46	IRQN	Open Drain Digital Output	C-BUS Interrupt Request (bar)	
47	IOVDD	Power	Digital I/O Positive Power Supply 3.3V	
48	DVDD	Power	Digital Positive Power Supply 1.8V	
EXPOSED METAL PAD	SUB	NC	On the Q3 package only, the central metal pad may be connected to Analogue Ground (Avss) or left unconnected. **No other electrical connection is permitted.**	

Note: If the GPIO1 and GPIO2 lines on pins 19 and 20 respectively are to be used as inputs, they must be pulled up to VDD or down to VSS, so that they are not left in a floating state.

Table 1 Pin List and Functions

4 External Components

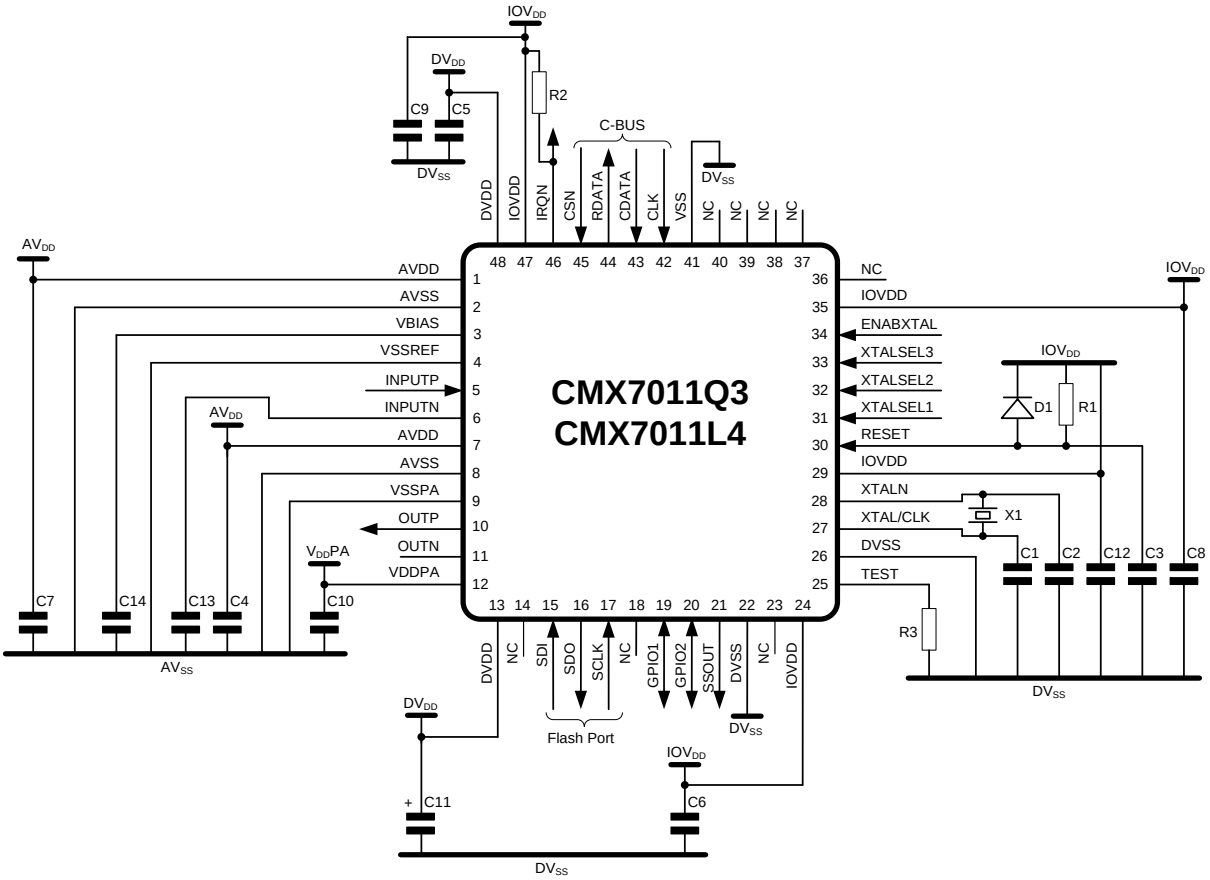


Figure 2 Recommended External Components

C1	22pF	C7	100nF	C13	100nF
C2	22pF	C8	100nF	C14	100nF
C3	1.0µF	C9	100nF	R1	470kΩ
C4	100nF	C10	100nF	R2	100kΩ
C5	1.0µF	C11	1.0µF	R3	100kΩ
C6	100nF	C12	100nF	D1	small signal diode

Table 2 Recommended Component Values

Notes: 1. On the CMX7011, the crystal selection pins (XTALSEL1, XTALSEL2 and XTALSEL3) must be permanently tied to either IOVDD or VSS and not driven from a logic level output of the host microcontroller (see Table 3 for a list of crystal frequencies). For 9.6MHz and 12.0MHz operation, either a crystal or a clock can be used. For all other frequencies, a clock must be injected into the XTALIN pin and the XTALOUT pin must be left unconnected.

2. To use the CMX7011, tie the ENABXTAL pin to IOV_{DD}. If the ENABXTAL pin is connected to VSS it will force the device into a deep powersave mode, where the C-BUS interface and clock input (XTALIN) are disabled and the crystal oscillator is powered down.

3. A single 10µF electrolytic capacitor may be fitted in place of C5 and C11, providing the two V_{DD} pins are connected together on the pcb with an adequate width power supply trace.

4. If the GPIO1 and GPIO2 lines on pins 19 and 20 respectively are to be used as inputs, they must be pulled up to V_{DD} or down to V_{SS}, so that they are not left in a floating state.

Crystal Select Input Pins:			Clock/Crystal Frequency	Clock/Crystal Choice
XTALSEL3	XTALSEL2	XTALSEL1		
0	0	1	9.6MHz	crystal or clock
0	1	0	12.0MHz	crystal or clock
0	1	1	14.4MHz	external clock only
1	0	0	16.8MHz	external clock only
1	0	1	19.2MHz	external clock only
1	1	0	21.6MHz	external clock only
1	1	1	24.0MHz	external clock only

Table 3 Clock/Crystal Selection

5 PCB Layout Guidelines and Power Supply Decoupling

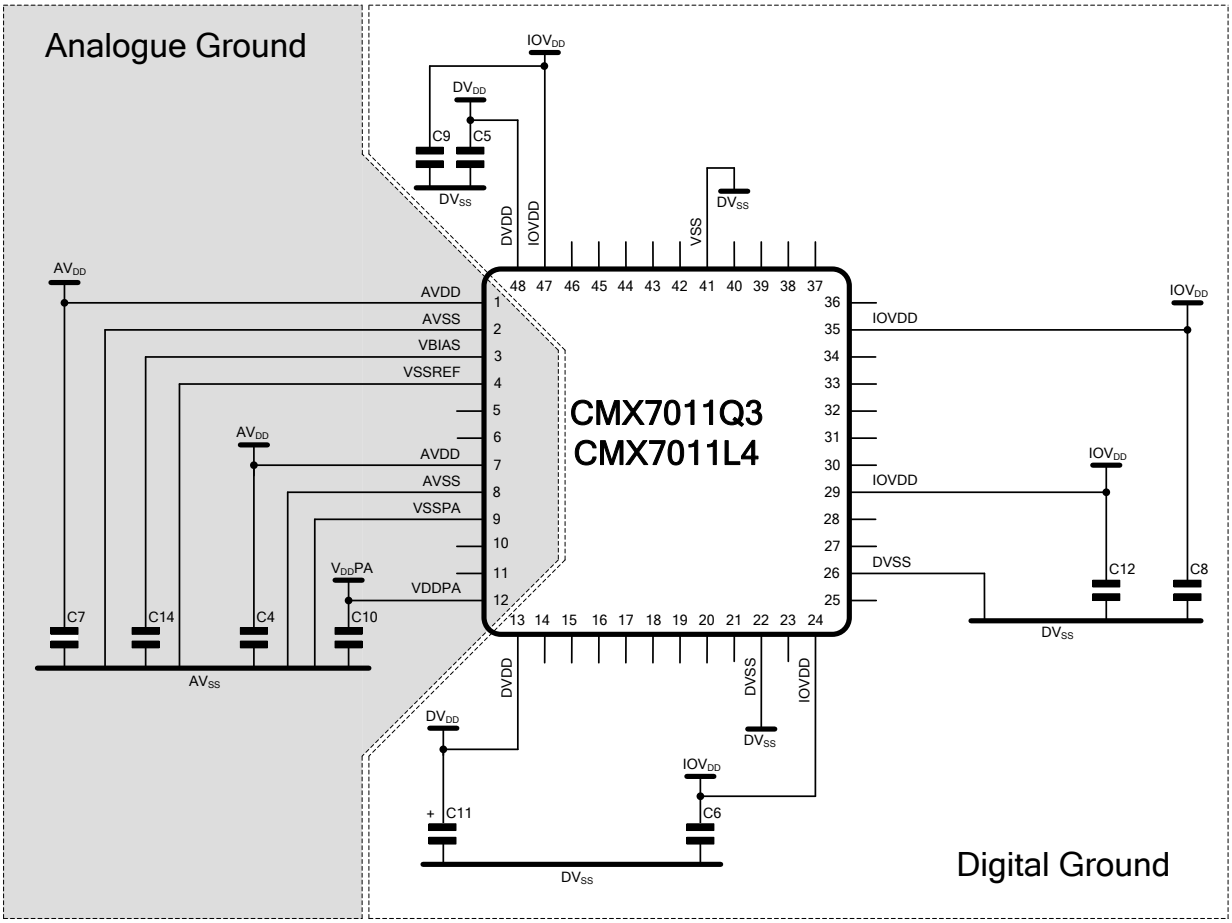


Figure 3 CMX7011 Power Supply and De-coupling

Component values as per Figure 3.

Notes:

It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the CMX7011 and the power supply and bias de-coupling capacitors. The de-coupling capacitors C4, C5, C6, C7, C8, C9, C10, C11, C12 and C14 should be as close as possible to the CMX7011. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS} and (digital) V_{SS} supplies in the area of the CMX7011, with provision to make links between them close to the CMX7011. The use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers, e.g. for use with VQFN packages.

On the CMX7011, V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set an external mid-point reference, it must be buffered with a high input impedance buffer.

6 General Description

The CMX7011, when loaded with Function Image™ 7011FI-1.x, is a half duplex, secure digital voice processor for use in analogue PMR or wireless secure door access and gate entry systems.

The device can be interfaced directly to the radio's audio path. Programmable input and output gain stages assist with signal level setting for optimum performance. The device has one signal input and one signal output and therefore, external switching is required to switch between receive and transmit.

The device uses an embedded RALCWI vocoder and audio-band 2400bps FFSK modem to digitise voice and apply it to an air interface protocol for use in 12.5kHz/25kHz channel analogue PMR radios. The embedded coding scheme provides good tolerance to transmission bit errors and provides real-time voice encryption with programmable 16-bit encryption keys/scramble seeds. An external voice data routing option is also provided to allow voice data to be passed to and from the external host microcontroller.

Instant voice capture is provided to eliminate annoying voice 'clipping' that can occur at the beginning of a voice transmission caused by repeater delays and sub-audio signal decoding in the receiver. Digital voice is buffered in the transmit side and released after a user-programmable period.

Noise gating is included in the Vocoder function, in both transmit and receive operations, to minimise the effects of background noise and improve the overall voice quality.

Voice store and retrieve (VSR) offers storage of a minimum of 20 seconds of vocoded speech in receive mode. The recorded speech can be played back, paused, resumed, or erased so that memory can be reused. VSR also includes a step-back feature which allows the device to step back in discrete steps during playback mode.

Packet data operation allows the device to send packetised data with CRC, FEC and interleaving, as a complete transaction. The only host intervention required is to specify the length of the data packet, transfer it into the device's buffer, and instruct the device to transmit. The CMX7011 performs CRC calculation, FEC coding and interleaving prior to transmission. In receive mode, the device will perform all the de-interleaving, error correction and CRC checking without any host intervention

The device utilises CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™ data file that is uploaded during device initialisation and defines the device's function and feature set. New features and enhancements to existing functions may be provided from time to time, expanding the capabilities of the device.

Please refer to the CMX7011 product page on the CML Website for up-to-date product data and currently available Function Images.

7 Detailed Descriptions

7.1 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7011 and the host microcontroller; this interface is compatible with Microwire/SPI. Interrupt signals notify the host microcontroller when a change in status has occurred and the microcontroller should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set.

To minimise activity on the C-BUS interface, optimise response times and ensure reliable data transfers, it is advised that the IRQ facility be used (using the IRQ enable register, $1F). It is permissible for the host to poll the IRQ pin if the host does not support a fully interrupt-driven architecture. This removes the need to continually poll the C-BUS status register ($40) for status changes.

7.1.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the internal registers of the CMX7011 and the host microcontroller, by using the C-BUS serial bus. Each transaction consists of a single Register Address byte sent from the microcontroller, which may be followed by a data word sent from the microcontroller (written into one of the Write-Only Registers), or a data word sent to the microcontroller (read out from one of the Read-Only Registers). All C-BUS data words are a multiple of 8 bits wide, the width depending on the source or destination register. Note that certain C-BUS transactions require only an address byte to be sent from the microcontroller, no data transfer being required. The operation of the C-BUS is illustrated in Figure 4.

Data sent from the microcontroller on the CDATA (command data) line is clocked into the CMX7011 on the rising edge of the CLK input. Data sent from the CMX7011 to the microcontroller on the RDATA (reply data) line is valid when CLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common microcontroller serial interfaces and may also be easily implemented with general purpose microcontroller I/O pins controlled by a simple software routine. Figure 4 and Figure 5 give detailed C-BUS timing requirements. Note that, due to internal timing constraints, there may be a delay of up to 60µs between the end of a C-BUS write operation and the device reading the data from its internal register.

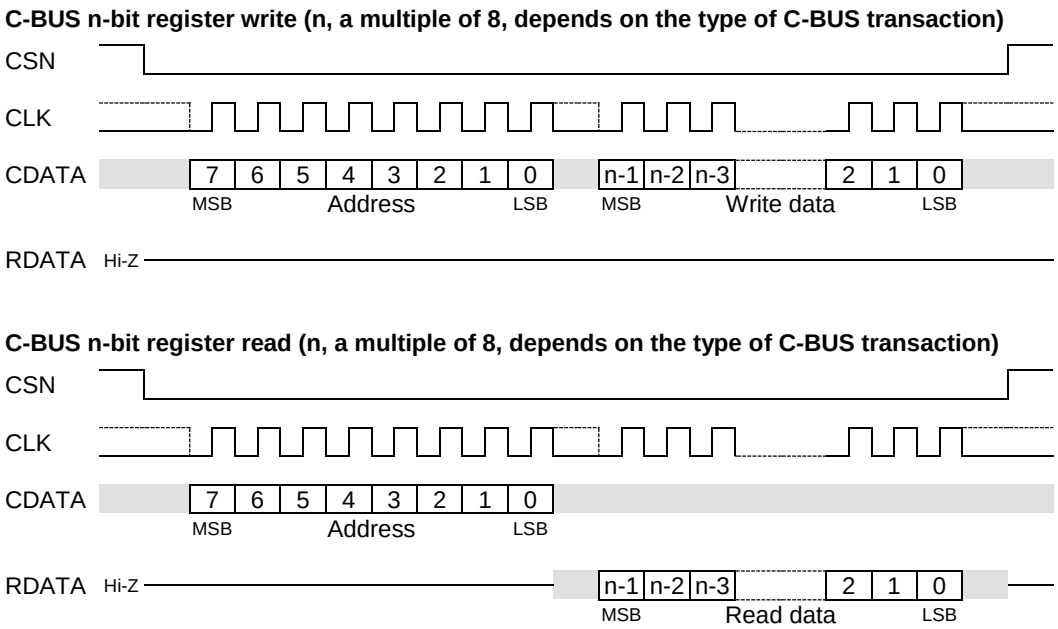


Figure 4 Basic C-BUS Transactions

To increase the data bandwidth between the microcontroller and the CMX7011, certain of the C-BUS read and write registers are capable of data-streaming operation. This allows a single address byte to be followed by the transfer of multiple read or write data words via a FIFO, all within the same C-BUS transaction. This can significantly increase the transfer rate of large data blocks, as shown in Figure 5.

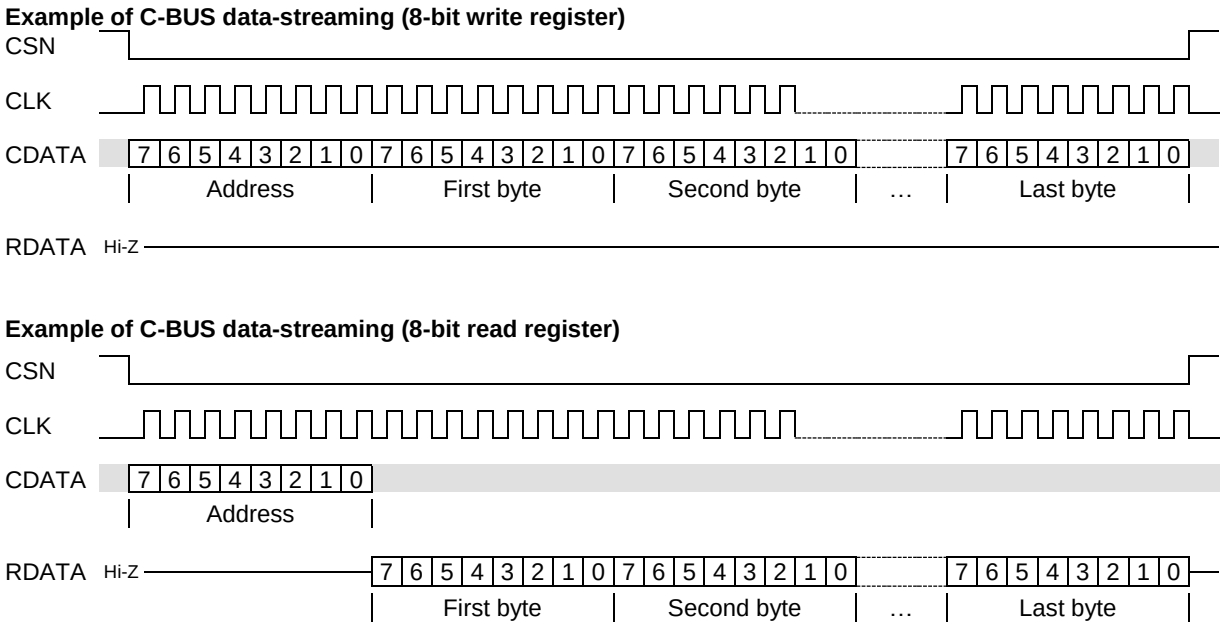


Figure 5 C-BUS Data-Streaming Operation

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset)
2. For single byte data transfers only the first 8 bits of the data are transferred
3. The CDATA and RDATA lines are never active at the same time. The address byte determines the data direction for each C-BUS transfer.
4. The CLK can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

7.2 Input Stage

Voice is fed in to the CMX7011 via the audio inputs at pins 5 and 6 via a variable analogue input gain stage. This input stage includes up to 22.5dB of switchable gain in 1.5dB steps. The input gain blocks are provided to allow for inputs from different audio sources. Depending on the type of audio source used, users may wish to consider an external low-noise preamplifier prior to the input stage. The gain is controlled by the register $05 - AIG (analogue input gain). In addition to the variable gain there is also 20dB of gain available (microphone amplifier gain) in a single step (also controlled by the analogue input gain register). If the user requires an input gain in the order of 20dB or above, the use of this single gain stage is advised to provide the bulk of the gain. Any additional smaller increments can then be added using the variable gain. Using this approach means that the best noise performance will be achieved.

7.3 Peak Level Function

The audio samples may be passed through a peak level measurement function which may be used to determine when the input signal is approaching the threshold at which clipping occurs. The peak level function monitors each 20ms block of speech (160 discrete samples) and will select the sample with the highest value and write the value to the PLEVEL register. This information is useful for setting the value of the input gain stage to obtain the best possible performance of the CMX7011. The function is switched on and off via the PLV register and is controlled by the one of the bits in the CTRL register.

7.4 Noise gate

The programmable noise gate stage that follows peak level detection removes the background noise between speech pauses and can be used to remove noise generated in front-end analogue circuitry or the effects of ambient noise.

Three parameters control the noise gate. An upper threshold level value controls the point at which the gate opens and allows audio to pass. A lower threshold value controls the point at which the gate closes thereby preventing audio to pass. These two parameters together control the hysteresis and prevent 'chattering'. A third parameter controls how many consecutive frames of audio must be below the lower threshold before the gate closes. This 'gate shut delay' prevents the tail end of words (like a trailing 's') from being clipped.

Once the gate shut delay has expired, the gate does not shut abruptly, but closes over a period of 16 frames. Each frame has progressively more attenuation applied, until the frames are silent. This happens in approximately 6dB steps. The diagram below illustrates the difference between a gated and non-gated signal and clearly shows the improvement in background noise level which is a benefit that this stage brings.

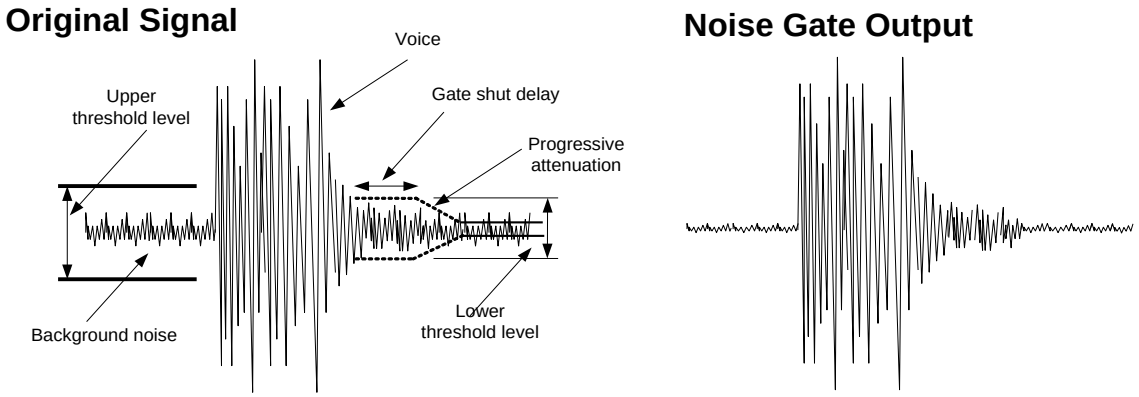


Figure 6 Noise Gate Behaviour

The various parameters of the noise gate such as upper threshold, lower threshold, mute, and gate shut delay are controlled by dedicated C-BUS registers described later.

7.5 Vocoder

The voice encoding/decoding is performed by a low data rate vocoder algorithm which is based on Robust Advanced Low Complexity Waveform Interpolation (RALCWI) technology.

RALCWI technology uses unique proprietary signal decomposition and parameter encoding methods, ensuring high voice quality at high compression ratios. The voice quality of RALCWI-class Vocoders, as estimated by independent listeners, is similar to that provided by standard Vocoders running at bit rates above 4000 bps. The Mean Opinion Score (MOS) of voice quality for this Vocoder is about 3.5-3.6. This value was determined by a paired comparison method, performing listening tests of developed and standard voice Vocoders.

Both input and output stages include a high-order digital channel filter, to constrain the input and output signals to an audio bandwidth of 4kHz. This avoids the necessity of adding external third (or higher) order filters, thus saving external components.

7.6 Voice Store and Retrieve

Following the Vocoder section is the voice store and retrieve sub system, which has the ability to store and play back previously-vocoded speech. Speech is stored, in encoded form, in on-chip RAM. Once stored, it is available for playback until it is either deleted or the device is reset. The maximum amount of memory available will depend on the amount of RAM being used by other operations being carried out by the device. However there will always be a minimum of 20 seconds available specifically for VSR.

Up to eight storage buffers are used to store eight discrete periods of speech and the memory for these buffers is allocated dynamically in 0.8 second (40 frames) blocks as the speech is being stored. The device will indicate when all available memory has been used up by setting a dedicated bit in one of the registers.

All operations within VSR are controlled by one 16-bit write register, one 16-bit read register, the Mode bits of the CTRL register, an interrupt request, and one of the bits in the STATUS register. Commands within the write register are provided for resetting and erasing of the buffers, start, stop and resume for playback mode, start and stop for record mode, and a stepback command which moves the current playback position back, by a specified amount, to a new location. The position of playback at any time is indicated by a playback pointer. This position is saved when playback is stopped so that play can resume from that position. The pointer is moved to a new location when the stepback command is executed. Other commands are provided to interrogate the amount of free memory space available, the amount of speech stored in a specific buffer, and the current status of the VSR, i.e. record, playback or idle. More detailed information covering the operation of the registers is given in the Configuration Guide.

7.7 Real Time Encryption

Note: throughout the following description, and in the register descriptions in the configuration guide (Section 9), the terms ‘scrambling’ and ‘encryption’ are both used and refer to the same functionality. Similarly, ‘scramble seeds’ and ‘encryption keys’ are used in the same manner.

Real time encryption is implemented with a 16-bit pseudo-random sequence which operates on all data bits after the header frame. The encryption uses start codes (‘seeding’) which means that the sequence will be seeded to start from any value other than zero. System security is improved because only receivers with the same seed can decrypt and decode the transmitted data.

There are 16 possible encryption keys (scramble seeds) and these values are held in an internal table - two of the values cannot be modified (scramble “whitening” or scramble disabled). It is also possible to program new scramble seed values into the table. This is covered in more detail in the C-BUS register descriptions.

7.8 External Data Routing

7.8.1 Transmit

If external data routing is used the vocoder output must be redirected to the host microcontroller. One of the bits in the SCRAMBLE register functions as a switch and this must be first set to external data routing (described in detail in the Configuration Guide section of this document). The seed index can be set to any chosen value. When the device is commanded to transmit, and after each 20ms frame of voice has been encoded, it will supply data, a frame at a time, to the host microcontroller via the C-BUS ODATA (out data) register and its associated FIFO. The host is notified when a frame head is available via the VFA (vocoder frame available) bit of the STATUS register. If IRQ (interrupt request) has been enabled in the IRQENAB register, a C-BUS interrupt will be generated and the host will then read the data. The host will subsequently process the data and, when it has completed processing, will return the frame to the device via the IDATA (in data) register, and its associated FIFO, for onward transmission.

7.8.2 Receive

When the device is set to receive, it will receive a valid frame head from the transmitting device and if the transmitter is using external data routing, the receiving device will automatically switch to external data routing mode. The host can establish that the device is in external data routing mode by reading the bit that functions as an external scrambling switch in the DESCRAMBLE register after having received a valid frame head. If this switch is set to external data routing it indicates that the receiver is expecting the host to read, process and return the frames before they are supplied to the device's vocoder for decoding. Processing of the frames is similar to that described for transmit mode. The device will indicate that a frame is ready to be read when the VFA bit in the STATUS register is set.

The host should return as many frames as it is sent – no more, no less. There are registers provided to indicate data flow problems during development and debugging, for example the FSTAT (frame flow status) register can indicate problems such as input or output FIFO full status or the oversupply/underflow of data to the host. These facilities are described in detail in the User Manual section of this document.

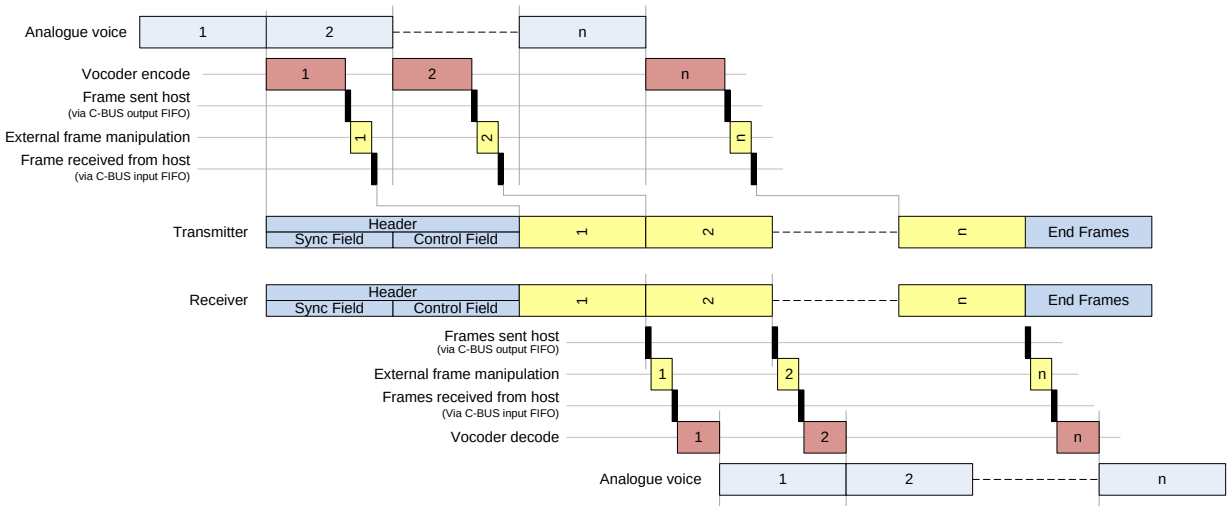


Figure 7 External Data Routing

7.9 Instant Voice Capture

The CMX7011 features instant voice capture which adds a delay between the time when the device starts to encode voice for transmission to the time when it actually transmits the encoded voice. This is useful because in an analogue PMR radio network there are various inherent system delays which can all contribute to an overall time lag before a receiving device starts to respond to a transmission. Examples of such delays are: time taken to decode a CTCSS sub-audio signal, and system delays introduced by

repeaters. The PTT buffer allows a user to programme delay times between 0 and 600ms. The delay times are specified in frames, and the function is controlled by the PTTDELAY register described in the C-BUS register section.

The following diagram illustrates how the PTT delay buffer is implemented.

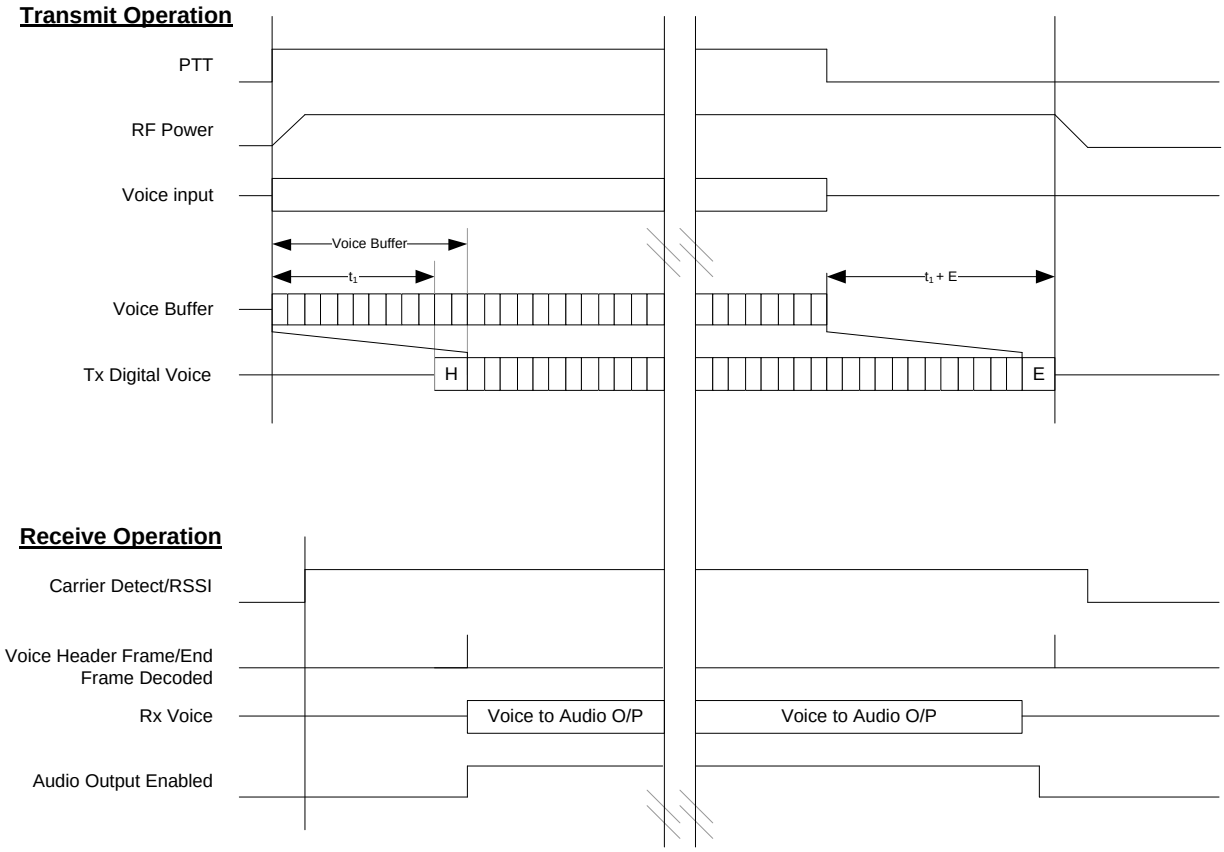


Figure 8 Typical Timing for PTT Delay

In Figure 8 it can be seen that from the time that the PTT button is engaged, there will be a small finite time taken for the RF power to ramp up from zero to full operating power. However, voice input will be captured immediately and vocoded voice data will be buffered in RAM on a frame-by-frame basis. In the example, 12 frames are buffered and this includes the header frame time. Therefore the actual transmission of digital voice is delayed by a period equal to t_1 plus the header frame time. At the end of the transmit operation, following the last frame of buffered voice frames, the actual transmission will continue for a period equal to t_1 plus the end-of-voice (EOV) frames time. The host will then be notified when digital voice transmission has finished.

In receive mode, carrier detect/RSSI may be present, but the audio output will not be enabled until the header frame has been correctly detected. Audio output will continue and will be only be disabled once the final end-of-voice frame has been detected.

7.10 Packet Data Operation

The CMX7011 can send data packets of 0 to a maximum length of 255 bytes, together with a CRC, as one complete transaction. All the host needs to do is to transfer the data into the device, specify its length and then instruct the device to transmit the data. The device will calculate a CRC for the data, split the data up into 4-byte chunks, calculate an FEC for them and interleave the resultant bits for transmission. Each 4 bytes of data is sent as 6 bytes (4 bits of FEC per byte of data).

The receiver will receive a complete packet, de-interleaving the 4-byte chunks, performing any error correction required and then checking the overall CRC without any host intervention. The device will indicate that it has received a complete packet and also report whether or not the CRC is correct. Once the host has been informed, it can read the data from the device, and, optionally, the received CRC.

The device has an internal 260-byte buffer that is used for both transmit and receive. When transmitting, the host must put the required data in the buffer prior to instructing the device to transmit. This is done using the PDATA register ($1D) in conjunction with the streaming input register IDATA ($10). The IDATA register has a 128-byte FIFO behind it, so, up to 128 bytes of message can be sent into the device in one go. Messages of greater than 128 bytes must therefore be written to the device in two parts.

Once the data to be sent has been transferred into the device, the host must indicate how much of it is to be sent by writing the packet length into the TXPL register ($0C) and then command the device to transmit the data by writing the appropriate value to the mode bits of the CTRL register ($11). Before the device transmits the packet, it will calculate a CRC value for the data. If the data length is less that 17 bytes, the CRC will be a 16-bit one otherwise a 32-bit CRC is calculated. The device places the CRC value in the buffer at the end of the data.

The device will indicate that the whole packet has been transmitted by setting the EOT bit in the STATUS register and, if enabled, pull IRQN low.

The receiving device must be placed in the receive mode prior to the data being transmitted. The receiver will first look for the sync word and once found will accept the frame head packet. If this packet is received intact, it will indicate to the receiving device whether the data being transmitted is digital voice data, or packet data. If it is digital voice that is being transmitted, the receiver will start decoding voice. If the transmission is packet data, the receiving device will collect the FEC-protected packets, de-interleave them, apply any error correction required and then place the data in its internal buffer. This will be done until the whole of the data has been received. Once the required amount of data has been collected, the device will calculate the CRC and check it agrees with the CRC that was transmitted. The receiving device will then set the EOT/RSR flag in the status register and set the RSTAT register to indicate that data with a good, or a bad, CRC has been received.

Once the device has indicated that it has received data, the length of the data in bytes may be read from the RXPL register ($2C). The host may then read the data from the buffer using the PDATA register ($1D) in conjunction with the streaming output register ODATA ($30). Like the IDATA register, the ODATA register has a FIFO behind it which allows up to 127 bytes to be read from the buffer in one streaming transaction.

7.11 Initialisation

On first applying power, three actions have to be performed: the crystal oscillator has to start up (if used), the bias chain has to be powered up, so that the decoupling capacitor (C14) has charged to AV_{DD} / 2, and on-chip digital circuits have to be reset into a known state. The crystal oscillator typically takes much less than 20ms to start up, but the actual time will depend on the ESR of the crystal used. With the components shown in Figure 3, the BIAS pin will take 100ms typically to reach its steady-state value of AV_{DD} / 2. There are two sources of reset:

- pulling the RESETN signal (pin 30) to '0' for at least 200ns, then returning it to '1' (the pin does not have an internal pullup resistor). Note that the device does not have an automatic power-up reset.
- writing to the C-BUS RESET register ($01). This is a 1-byte command which has no data.

A hard reset (taking RESETN low) will also force the ENABXTAL signal low, which disables the clock and powersaves the crystal oscillator. On first applying power, the RESETN pin should be held low until all the power supplies have stabilised, to ensure correct operation of the device. When coming out of a hard reset, the device needs the crystal oscillator to be working, then counts 65,536 clock cycles (= 5.4ms delay with a 12.0MHz clock), then automatically performs a soft reset by writing to the C-BUS RESET register.

A soft reset (writing to the RESET register) will clear all registers to '0', unless noted otherwise – in which case the default settings are restored. The device will be ready to accept C-BUS commands approximately 1.5ms after completion of the soft reset action and will indicate that it is ready by setting bit 15 of the STATUS register ($40) to '1' and also by indicating a C-BUS interrupt request by pulling the IRQN pin low. Note that on reset, the IRQENAB register ($1F) bit 15 will automatically be set to '1', thus enabling the RDY interrupt to activate the IRQN pin.

Connecting the ENABXTAL pin to V_{SS} when the device is operational will force the device into a power-save mode where the C-BUS interface and clock input (XTALIN) are disabled and the crystal oscillator is powered down. However, the BIAS pin and C-BUS registers are not disturbed, so normal operation can be resumed by re-connecting the ENABXTAL pin to IOV_{DD} and waiting for the crystal oscillator to re-start.

The device is now ready to accept the loading of the Function Image™. Please refer to the Application Note in Section 10.1.

7.12 C-BUS register Summary

C-BUS Register Name	C-BUS Address	CMX7011 R/W/CMD	CMX7011 Size (bits)
RESET	$01	CMD	-
SCRAMBLE	$04	W	8
AIG	$05	W	8
AOG	$06	W	8
RADDR	$07	W	8
LADDR	$08	W	8
POWERSAVE	$09	W	8
PTTDELAY	$0A	W	8
EOVCOUNT	$0B	W	8
TXPL	$0C	W	8
SVSREQ	$0E	W	8
IOCTRL	$0F	W	8
IDATA	$10	W	8
CTRL	$11	W	16
LSEED	$12	W	16
FSYNC	$13	W	16
ENGUTH	$14	W	16
ENGLTH	$15	W	16
ENGSDY	$16	W	16
DNGTH	$17	W	16
VSRW	$1C	W	16
PDATA	$1D	W	16
IRQENAB	$1F	W	16
FSTAT	$21	R	8
FTYPE	$22	R	8
FHEADV	$23	R	8
DESCRAMBLE	$24	R	8
ADDRESS	$25	R	8
RSTAT	$26	R	8
RXPL	$2C	R	8
SVCACK	$2E	R	8
IORD	$2F	R	8
ODATA	$30	R	8
PLEVEL	$31	R	16
VSRR	$32	R	16
STATUS	$40	R	16

Table 4 C-BUS Registers

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

8 Performance Specification

8.1 Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Power Supplies			
IOV_{DD} - V_{SS}	-0.3	4.0	V
DV_{DD} - DV_{SS}	-0.3	2.16	V
AV_{DD} - AV_{SS}	-0.3	4.0	V
$V_{DD}PA$ - $V_{SS}PA$	-0.3	4.0	V
Voltage on any pin to V_{SS}	-0.3	IOV_{DD} + 0.3	V
Current into or out of any pin, except power supply pins, OUTP and OUTN.	-20	+20	mA
Current into or out of power supply pins, OUTP and OUTN.	-120	+120	mA

L4 Package (48-pin LQFP)	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1600	mW
... Derating	–	16.0	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

8.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min	Typ	Max.	Units
IOV_{DD} - V_{ss}	3.0	3.3	3.6	V
DV_{DD} - DV_{SS}	1.7	1.8	1.9	V
AV_{DD} - AV_{SS}	3.0	3.3	3.6	V
$V_{DD}PA$ - $V_{SS}PA$	3.0	3.3	3.6	V
Operating Temperature	-40	–	+85	°C
Xtal Frequency	9.6	–	12	MHz
External Clock Frequency (injected into XTALin pin)	9.6	–	24	MHz

8.1.3 Operating Characteristics

Using the recommended components in Figure 2 and for the following conditions unless otherwise specified:

Xtal Freq. = 12.0MHz ±100ppm, $V_{DD}PA = AV_{DD} = IOV_{DD}$ = 3.0V to 3.6V; DV_{DD} = 1.7V to 1.9V; T_{AMB} = 25°C;
all gain settings are 0dB. Figures apply to CMX7011, unless otherwise stated.
Note: Parametric measurements in this section are subject to further characterisation.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} Total powersaved (ENABXTAL pin connected to VSS)	1	–	50	–	µA
I_{DD} Digital (after Reset, Xtal enabled)	1, 8, 18	–	14.0	–	mA
I_{DD} IODigital (after Reset, Xtal enabled)	1, 9, 18	–	0.5	–	mA
I_{DD} Digital	1, 8, 19	–	17.5	–	mA
Operational Modes					
I_{DD} IODigital	1, 9, 20	–	0.6	–	mA
I_{DD} Analogue PA	1, 9, 20	–	0.7	–	mA
I_{DD} Analogue Vocoder encoding	1, 9, 20	–	6.5	–	mA
I_{DD} Analogue Vocoder decoding	1, 9, 20	–	2.8	–	mA
I_{DD} Digital Vocoder encoding	1, 8	–	33	–	mA
I_{DD} Digital Vocoder decoding	1, 8	–	20.0	–	mA
I_{DD} Analogue	1, 9, 20	–	10	–	mA
Logic Inputs and Outputs					
Input logic '1' level		80%	–	–	IOV_{DD}
Input logic '0' level		–	–	20%	IOV_{DD}
Input leakage current (Vin = 0 to IOV_{DD})	1	–	–	±5	µA
Input capacitance		–	3	–	pF
Output logic '1' level (I_{OH} = 2mA)		90%	–	–	IOV_{DD}
Output logic '0' level (I_{OL} = -5mA)		–	–	10%	IOV_{DD}
"Off" state leakage current (IRQN or RDATA)	1	–	–	±5	µA
Analogue Inputs					
Minimum input sensitivity	21		1		V
Analogue Outputs					
Differential output dc offset (OUT P – OUT N)	3	–	–	±40	mV
XTALin					
Input logic '1' level		70%	–	–	IOV_{DD}
Input logic '0' level		–	–	30%	IOV_{DD}
Input current (Vin = 0 to IOV_{DD})		–	–	±40	µA
XTALout					
Output logic '1' level (I_{OH} = 0.5mA)		90%	–	–	IOV_{DD}
Output logic '0' level (I_{OL} = -1.2mA)		–	–	10%	IOV_{DD}

	Notes	Min.	Typ.	Max.	Units
AC Parameters					
XTALin					
'High' pulse width	4	15	–	–	ns
'Low' pulse width	4	15	–	–	ns
Input impedance (at 12.0MHz)					
Powered-up Resistance		–	150	–	kΩ
Capacitance		–	20	–	pF
Powered-down Resistance		–	300	–	kΩ
Capacitance		–	20	–	pF
Xtal start up time (from powersave)		–	20	–	ms
BIAS					
Start up time (from powersave)		–	100	–	ms
CODEC					
Input Impedance (INPUT P or INPUT N)		–	10	–	kΩ
Input Voltage Range (INPUT P or INPUT N)	10, 17	–	–	20 to 80	%AV_{DD}
Differential Input Voltage (pk to pk)	11, 12, 17	–	–	100	%AV_{DD}
Output Load Impedance (OUT P or OUT N)	6	32	–	–	Ω
Output Voltage Range (OUT P or OUT N)	3, 13, 17	–	–	10 to 90	% V_{DD}PA
Differential Output Voltage (pk to pk)	3, 11, 17	–	–	160	% V_{DD}PA
Differential Output Power	3	–	120	–	mW
Input Gain Setting Accuracy		–	±0.5	–	dB
Output Gain Setting Accuracy		–	±0.5	–	dB
ADC SINAD	5, 14	–	86	–	dB
DAC SINAD	7, 15	–	80	–	dB
Vocoder Performance					
Sample Rate		–	8	–	ks/s
Data Rate		–	2400	–	bps
Lower Frequency Limit (internally bandlimited)		60	–	–	Hz
Upper Frequency Limit (internally bandlimited)		–	–	3900	Hz
Encoder Algorithmic Delay	16	–	–	20	ms
Decoder Algorithmic Delay	16	–	–	12	ms

		Notes	Min.	Typ.	Max.	Units
C-BUS Timings		2				
t_{CSE}	CSN-Enable to Clock-High time		100	–	–	ns
t_{CSH}	Last Clock-High to CSN-High time		100	–	–	ns
t_{LOZ}	Clock-Low to Reply Output enable time		0.0	–	–	ns
t_{HIZ}	CSN-High to Reply Output 3-state time		–	–	1.0	µs
t_{CSOFF}	CSN-High time between transactions		1.0	–	–	µs
t_{NXT}	Inter-Byte time		200	–	–	ns
t_{CK}	Clock-Cycle time		200	–	–	ns
t_{CH}	Serial Clock-High time		100	–	–	ns
t_{CL}	Serial Clock-Low time		100	–	–	ns
t_{CDS}	Command Data Set-Up time		75	–	–	ns
t_{CDH}	Command Data Hold time		25	–	–	ns
t_{RDS}	Reply Data Set-Up time		50	–	–	ns
t_{RDH}	Reply Data Hold time		0	–	–	ns

Notes:

1. T_{AMB} = 25°C, not including any current drawn from the device pins by external circuitry.
2. Maximum 30pF load on each C-BUS or CODEC (SSP) interface line.
3. Measured whilst driving a 32Ω resistive load between OUTP and OUTN pins.
4. Timing for an external input to the XTALin pin.
5. Differential measurement, 10Hz to 4kHz bandwidth.
6. Care should be taken to avoid shorting the OUTP and OUTN pins together, or to any V_{DD} or V_{SS}.
7. Differential measurement, 300Hz to 4kHz bandwidth, no load.
8. 1.8V nominal supply.
9. 3.3V nominal supply.
10. This is the maximum signal range on each pin of the differential input. The common mode voltage can be any voltage within this range but, for optimum dynamic range, it should be set to about AV_{DD} /2. If the inputs are ac coupled, on-chip resistors will set the dc bias of each input to this voltage automatically.
11. This is the maximum differential peak to peak signal amplitude, which corresponds to a signal on each input of (AV_{DD} /2 ± 25% AV_{DD}). Exceeding this can result in increased distortion products.
12. Because the amplitude of speech fluctuates, it is important to set the average speech level such that the level of distortion that results from the occasional overdriving of the inputs is at an acceptable level.
13. This is the maximum voltage on each pin of the differential output, such that the device does not start to introduce significant harmonic distortion.
14. The internal ADC is a sigma-delta type which samples at 2.4MHz. It is important that there is no significant energy close to this frequency or at any of its harmonics, thus avoiding the need for an external low-pass anti-alias filter.
15. The internal DAC is a sigma-delta type which samples at 2.4MHz. It will output energy at this frequency and its harmonics. Should this present a problem, it is suggested that some external filtering be used at the audio outputs.
16. Excludes the 20/40/60/80 ms sample collection period.
17. Internal gain settings are 0dB on input gain for the optimum vocoded level and +6dB on output gain for the optimum vocoded level, subject to further characterisation.
18. ADC or DAC disabled, Vocoder is disabled.
19. ADC or DAC enabled, Vocoder is disabled.
20. ADC or DAC enabled, Vocoder is enabled.
21. Minimum input sensitivity is quoted as peak-to-peak for an Analogue Input Gain value of 0dB.

8.1.3 Operating Characteristics (continued)

Timing Diagrams

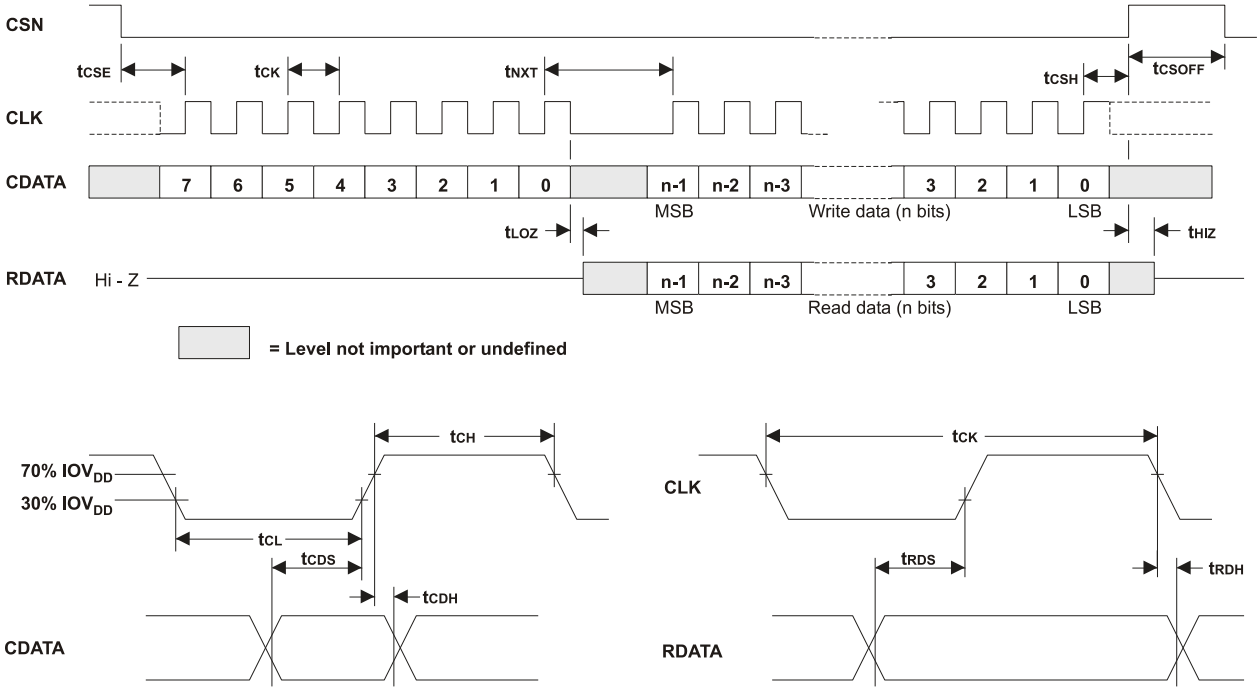
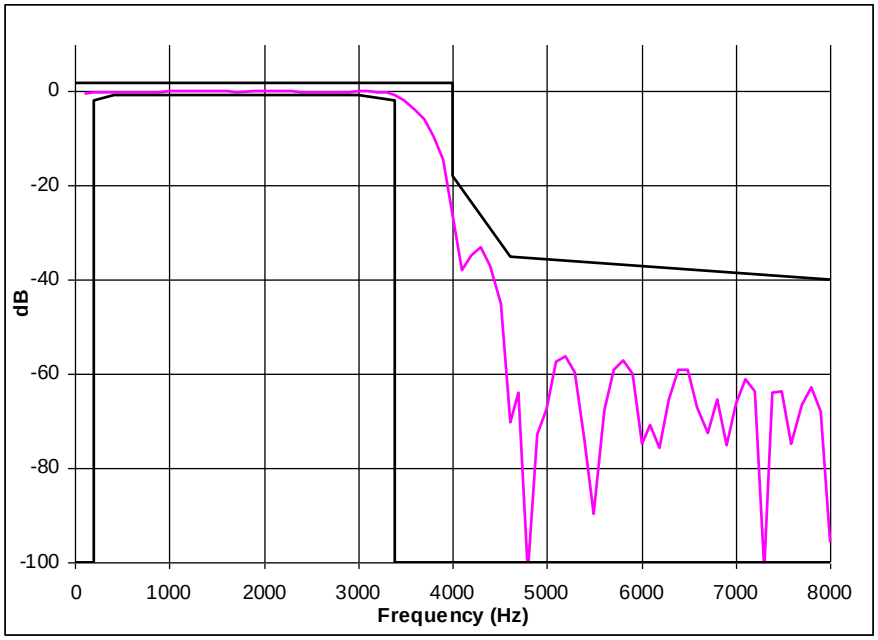


Figure 9 C-BUS Timing



(ADC Input Frequency Vs Fundamental tone power for 750mVrms differential input, normalised to 1kHz)

Figure 10 ADC Input Filter - Typical Response

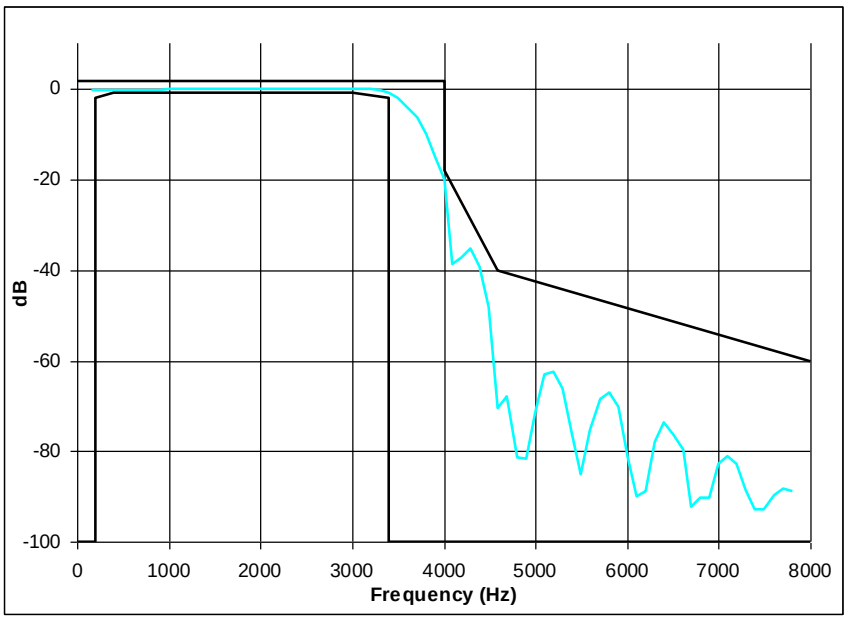
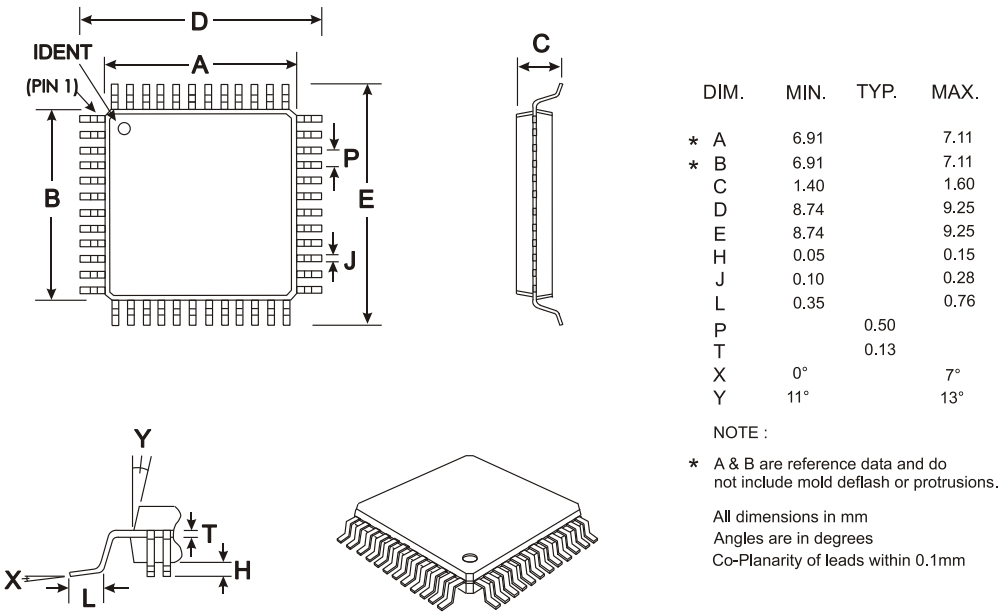


Figure 11 DAC Output Filter - Typical Response

(DAC Output Frequency Vs Measured tone power for 32000 peak sample level differential output, normalised to 1kHz)

8.2 Packaging



DIM.	MIN.	TYP.	MAX.
* A	6.91		7.11
* B	6.91		7.11
C	1.40		1.60
D	8.74		9.25
E	8.74		9.25
H	0.05		0.15
J	0.10		0.28
L	0.35		0.76
P		0.50	
T		0.13	
X	0°		7°
Y	11°		13°

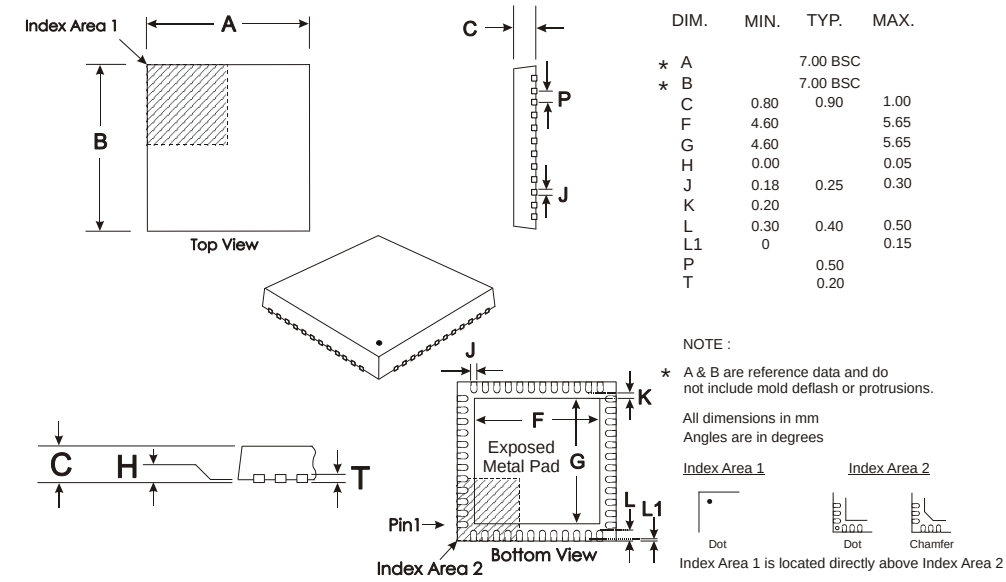
NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 12 48-pin LQFP Mechanical Outline (L4)

Order as part no. CMX7011L4



DIM.	MIN.	TYP.	MAX.
* A		7.00 BSC	
* B		7.00 BSC	
C	0.80	0.90	1.00
F	4.60		5.65
G	4.60		5.65
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 Index Area 2

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 13 48-pin VQFN Mechanical Outline (Q3)

Order as part no. CMX7011Q3

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheets page of the CML website: [http://www.cmlmicro.com/].

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CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX7011
Digital Voice Processor

UM/7011_FI1.x/5 February 2013 **USER MANUAL** Advance Information

7011FI-1.x Digital Voice Encryption for Analogue Radio Systems

Note that text shown in pale grey indicates features that will be supported in future versions of the device.
This User Manual is the second part of a two-part document.

CONTENTS

Section **Page**

It is always recommended that you check for the latest product datasheet version from the CML website: [http://www.cmlmicro.com/].

9 Configuration Guide

9.1 C-BUS Register Details

The detailed descriptions of the C-BUS registers are presented in numerical order and should be read in conjunction with the relevant functional descriptions.

C-BUS Address (hex)	R/W/CMD	REGISTER	Word Size (bits)
$01	CMD	RESET	-
$04	W	SCRAMBLE	8
$05	W	AIG	8
$06	W	AOG	8
$07	W	RADDR	8
$08	W	LADDR	8
$09	W	POWERSAVE	8
$0A	W	PTTDELAY	8
$0B	W	EOVCOUNT	8
$0C	W	TXPL	8
$0E	W	SVSREQ	8
$0F	W	IOCTRL	8
$10	W	IDATA	8
$11	W	CTRL	16
$12	W	LSEED	16
$13	W	FSYNC	16
$14	W	ENGUTH	16
$15	W	ENGLTH	16
$16	W	ENGSDY	16
$17	W	DNGTH	16
$1C	W	VSRW	16
$1D	W	PDATA	16
$1F	W	IRQENAB	16
$21	R	FSTAT	8
$22	R	FTYPE	8
$23	R	FHEADV	8
$24	R	DESCRAMBLE	8
$25	R	ADDRESS	8
$26	R	RSTAT	8
$2C	R	RXPL	8
$2E	R	SVCACK	8
$2F	R	IORD	8
$30	R	ODATA	8
$31	R	PLEVEL	16
$32	R	VSRR	16
$40	R	STATUS	16

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

9.1.1 RESET register - $01

This register has no data associated with it. Writing to it (by the General Reset command) will reset the device and restore all the default settings. **All registers are cleared to '0' on reset, unless marked otherwise**. As a result, the BIAS pin is powered down and the voltage on the external decoupling capacitor (C14) will decay to V_{SS}. The crystal oscillator is unaffected by writing to the RESET register (a "soft" reset). Instead, it is powersaved by connecting the ENABXTAL pin to V_{SS}.

9.1.2 SCRAMBLE - $04, 8-bit write

Mode	7	6	5	4	3	2	1	0
Digital Voice	XSCRAM	PRS	0	0	SINDEX			
Packet Data	0	0	0	0	0	0	SINDEX	

The SCRAMBLE register controls the various scrambler parameters and has two modes of operation: Digital Voice mode and Packet Data mode.

Digital Voice mode

It is possible to select internal or external scrambling, or disable scrambling operation completely. For internal scrambling, the device uses one of two 16-bit pseudo-random sequences: a shorter length and a maximal length with one of the bits in the register acting as a switch to select which is used.

Bits 0 to 3 are the SINDEX (scramble index) bits. The sequence is seeded from one of 16 values held in an internal table shown below. The SINDEX field of the register specifies which entry in the table will be used. Fourteen of the entries in the table are programmable by the host and this is achieved by using the LSEED register in conjunction with this register. If external scrambling is being used the host may use the SINDEX bits freely and the bits will be sent to the receiver unaltered.

3	2	1	0	HEX Value	Default Seed
0	0	0	0	$0	$FFFF cannot be modified
0	0	0	1	$1	$0123
0	0	1	0	$2	$4567
0	0	1	1	$3	$89AB
0	1	0	0	$4	$CDEF
0	1	0	1	$5	$048C
0	1	1	0	$6	$159D
0	1	1	1	$7	$26AE
1	0	0	0	$8	$37BF
1	0	0	1	$9	$369C
1	0	1	0	$A	$05AF
1	0	1	1	$B	$FEDC
1	1	0	0	$C	$BA98
1	1	0	1	$D	$7654
1	1	1	0	$E	$3210
1	1	1	1	$F	$0000 cannot be modified

Note: Two of the values in the above table are fixed and cannot be modified: $0 (seed value $FFFF) is used for “whitening” which is a technique used to decrease the likelihood of long strings of 0s or 1s in the data stream. $F (seed value $0000) is used to disable the scrambling function.

Bits 4 and 5 must be cleared to 0 for correct operation.

Bit 6 is the PRS (pseudo-random sequence) field. If the bit is cleared to zero (the default setting), a relatively short pseudo-random sequence is used for scrambling. If this bit is set to 1, the maximum length pseudo-random sequence is used. If external scrambling is enabled (bit 7 set to 1), this bit must be cleared to zero for correct operation.

Bit 7 is the XSCRAM field and operates as a switch to control whether internal or external scrambling is used. If this bit is cleared to 0 the internal scrambling system is used. If it is set to 1, the digital vocoded voice frames will be sent to the host for external scrambling before being passed back to the CMX7011 prior to transmission. In receive mode, this route to the host will occur prior to decoding. If external scrambling is selected, the value set in the SINDEX field and bit 7 will still be sent in the frame head to the receiving device and the way these bits are used is entirely under the control of the host. Once the receiving device has successfully decoded the frame head, the value of this bit will be held in the DESCRAMBLE register ($24).

When the device is transmitting, the SINDEX value is placed in the frame head at the start of transmission so that the receiving device knows which entry in the table to use for decoding. When the device is receiving the SINDEX, PRS and XSCRAM values may be read from the DESCRAMBLE register after the frame head has been successfully received.

After this register has been written, the host must wait for the RDY bit to be set in the STATUS register before writing to any more registers. If the RDY bit in the IRQENAB register is set, then IRQN will be pulled low.

Packet Data mode

When the device is operating in packet data mode only bits 0 and 1 are used to specify the scramble seed. All other bits should be cleared to zero for correct operation. Only one of the pseudo random sequences is used and this is the same as the shorter length sequence used in digital voice mode.

After this register has been written, the host must wait for the RDY bit (bit 15) to be set in the STATUS register before writing to any more registers. If the RDY bit in the IRQENAB register is set, then IRQN will be pulled low.

Bits 0 and 1 are the SINDEX (scramble index) bits and the seed table below is a sub set of the full table used in digital voice mode.

Bit 1	Bit 0	HEX Value	Default Seed
0	0	$0	$FFFF cannot be modified
0	1	$1	$0123
1	0	$2	$4567
1	1	$3	$0000 cannot be modified

Bits 2 to 7: These bits are reserved and should be cleared to '0' for correct operation.

9.1.3 AIG - $05, 8-bit write

7	6	5	4	3	2	1	0
MAG	0	0	0	INPUT GAIN			

This is the analogue input gain control register. Because the amplitude of speech fluctuates, it is important to set the average speech level such that the level of distortion that results from the occasional overdriving of the inputs is at an acceptable level. The ADC is designed not to saturate, but will clip input signals which are too large. The ADC is a sigma-delta design with a sampling frequency of 2.4MHz and subsequent decimation by a factor of 300.

Bits 0 to 3 INPUT GAIN These bits control the input gain stage according to the following table:

3	2	1	0	Gain (dB)
0	0	0	0	0 (default)
0	0	0	1	1.5
0	0	1	0	3.0
0	0	1	1	4.5
0	1	0	0	6.0
0	1	0	1	7.5
0	1	1	0	9.0
0	1	1	1	10.5
1	0	0	0	12.0
1	0	0	1	13.5
1	0	1	0	15.0
1	0	1	1	16.5
1	1	0	0	18.0
1	1	0	1	19.5
1	1	1	0	21.0
1	1	1	1	22.5

Bits 4 to 6 These bits are reserved and should be cleared to '0' for correct operation.

Bit 7 MICROPHONE AMPLIFIER GAIN In addition to the variable gain there is also an additional 20dB of gain available in a single step. If the user requires an input gain in the order of 20dB, the use of this single gain stage is advised as it will result in better noise performance.
When this bit is set to 1, the additional gain is applied. When the bit is zero no additional gain is applied to the input signal.

9.1.4 AOG register - $06, 8-bit write

7	6	5	4	3	2	1	0
LSG	0	0	0	OUTPUT GAIN			

This is the analogue output gain control register. The output level should be chosen to avoid unnecessary distortion in the output amplifier. This gain block follows the DAC, which is a sigma-delta design with a sampling frequency of 2.4MHz and an on-chip reconstruction filter. An external RC filter should be added across the OUTP and OUTN pins, if clock noise needs further reduction.

Bits 0 to 3 OUTPUT GAIN These bits control the output gain stage according to the following table:

3	2	1	0	Gain (dB)
0	0	0	0	-14 (default)
0	0	0	1	-12
0	0	1	0	-10
0	0	1	1	-8
0	1	0	0	-6
0	1	0	1	-4
0	1	1	0	-2
0	1	1	1	0
1	0	0	0	2
1	0	0	1	4
1	0	1	0	6
1	0	1	1	8
1	1	0	0	10
1	1	0	1	12
1	1	1	0	14
1	1	1	1	16

Bits 4 to 6 These bits are unused and should be cleared to '0'.

Bit 7 LOUD SPEAKER GAIN The loudspeaker gain provides an additional 6dB of gain in a single step. A ‘0’ in this bit sets the gain to 0dB and a ‘1’ in this bit sets the gain to 6dB.

9.1.5 RADDR - $07, 8-bit write

7	6	5	4	3	2	1	0
REMOTE ADDRESS							

This is the remote address register and allows an address from 0 to 255 to be placed in the address field of the header frame at the start of a digital voice transmission. This address should be the same as the local address of the receiving device or devices that the transmission is intended for.

9.1.6 LADDR - $08, 8-bit write

7	6	5	4	3	2	1	0
LOCAL ADDRESS							

This is the local address register and allows the local address of the device to be specified. Unless the PRM bit (promiscuous mode) in the CTRL register is set, the device will only respond to digital voice transmissions from devices that have the matching address in the header frame. If the PRM bit in the CTRL register is set, the device will respond to any address in the header frame.

9.1.7 POWERSAVE - $09, 8-bit write

7	6	5	4	3	2	1	0
0	0	0	THROTTLE			CODEC	BIAS

This write-only register controls the powersaving features of the device. All the bits in this register are cleared to '0' after a power up reset. Before vocoding analogue signals, the BIAS and CODEC functions must be turned on as a minimum.

Bit 0 BIAS Setting this bit to '1' will turn on the analogue bias. The host should wait for approximately 100ms to allow the bias capacitors to charge.
Clearing this bit to '0' will turn off the analogue bias.

Bit 1 CODEC Setting this bit to '1' will turn on the CODEC master clock and set it up for use with the vocoding function.
Clearing this bit to '0' will turn off the master clock of the CODEC.

Bit 4 THROTTLE Setting this bit to '1' will reduce the internal clock rate to a quarter of its normal frequency when the device is not actively encoding or decoding.
Clearing this bit to '0' will leave the internal clock rate at its normal frequency.

When the clock is throttled down, the device will take up to 4 times longer to complete any C-BUS command.

Note: The maximum C-BUS CLK frequency that should be used when this bit is set to '1' is 4MHz.

Bits 5 to 7 These bits are not used and must be cleared to '0' for correct operation.

9.1.8 PTTDELAY - $0A, 8-bit write

7	6	5	4	3	2	1	0
0	0	0	DELAY				

The push to talk (PTT) delay enables a programmable delay to be added between the time that the device starts to encode voice for transmission and when the transmission of encoded voice actually starts. This is to help avoid the effects of PTT clipping at the start of a voice transmission. PTT clipping can be caused by various delays such as the time taken to decode sub audio signals like CTCSS or DCS, and system delays in transmission systems that include repeaters. The programmable delay time can be from 0 to a maximum of 600ms, specified in frames.

Bits 0 to 4 DELAY TIME The delay time in frames. Each frame is the equivalent of 20ms of delay. The delay time can be set according to the following table.

4	3	2	1	0	Delay (frames)	Delay (ms)
0	0	0	0	0	0	0
0	0	0	0	1	1	20
0	0	0	1	0	2	40
0	0	0	1	1	3	60
0	0	1	0	0	4	80
0	0	1	0	1	5	100
0	0	1	1	0	6	120
0	0	1	1	1	7	140
0	1	0	0	0	8	160
0	1	0	0	1	9	180
0	1	0	1	0	10	200
0	1	0	1	1	11	220
0	1	1	0	0	12	240
0	1	1	0	1	13	260
0	1	1	1	0	14	280
0	1	1	1	1	15	300
1	0	0	0	0	16	320
1	0	0	0	1	17	340
1	0	0	1	0	18	360
1	0	0	1	1	19	380
1	0	1	0	0	20	400
1	0	1	0	1	21	420
1	0	1	1	0	22	440
1	0	1	1	1	23	460
1	1	0	0	0	24	480
1	1	0	0	1	25	500
1	1	0	1	0	26	520
1	1	0	1	1	27	540
1	1	1	0	0	28	560
1	1	1	0	1	29	580
1	1	1	1	0	30	600
1	1	1	1	1	30	600

The maximum value that can be specified is 30 frames which gives a delay of 600ms. If Bits 0 to 4 are all set, the value of 30 frames will be used.

Bits 5 to 7 Reserved. Must be cleared to zero for correct operation.

9.1.9 EOVCOUNT - $0B, 8-bit write

7	6	5	4	3	2	1	0
RXCOUNT				TXCOUNT			

This is the End of Voice Count register and specifies how many consecutive end-of-voice (EOV) frames should be sent at the end of a digital voice transmission and how many end-of-voice frames the receiver has to receive before it stops receiving.

Bits 0 to 3 TXCOUNT. This field specifies how many consecutive EOV frames are produced when the device is instructed to stop transmitting and can take values between 1 and 15 as defined in the following table. The default value following reset is 1. The behaviour of the device if this field is cleared to zero is undefined.

3	2	1	0	EOV frames
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Bits 4 to 7 RXCOUNT. This field specifies how many consecutive EOV frames must be received before the receiving device mutes the audio stage and signals to the host microcontroller that it is now idle. This field can take values between 1 and 15 as defined in the following table. The default following reset is 1. The behaviour of the device if this field is cleared to zero is undefined.

Setting this field to a value more than the TXCOUNT of the transmitting device will mean that the device does not recognise the end-of-voice condition. Setting the value equal to TXCOUNT of the transmitting device increases the possibility that the end-of-voice condition may not be detected over a noisy channel with a high bit error rate. Normal practice would be to set the TXCOUNT as slightly greater than the RXCOUNT.

7	6	5	4	EOV frames
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

9.1.10 TXPL - $0C, 8-bit write

7	6	5	4	3	2	1	0
Tx Packet Length							

This is the transmit packet length register. TXPL specifies the number of bytes that should be sent as a packet data message. The packet length should be written to this register before the device is commanded (by writing to the mode bits and the PKT bit of the CTRL register) to send the packet.

Packets can be of any length from 0 to 255 inclusive.

9.1.11 SVCREQ - $0E, 8-bit write

7	6	5	4	3	2	1	0
Service Request Value							

This write only register sends special service requests to the device. Once the request has been processed, bit 14 (SVC) of the STATUS ($40) register will be set to '1' and, if enabled, IRQN will go low. The SVCACK ($2E) register will contain the status value, indicating whether or not the request was successful. No other C-BUS registers should be read or written whilst this command is in progress.

Bits 0 to 7 The 8-bit value written to this register specifies which operation to perform. Currently, only 1 operation is defined. All other values are reserved:

$01 Request to load a Function Image™. Please refer to section 10.1 for further information.

9.1.12 IOCTRL - $0F, 8-bit write

7	6	5	4	3	2	1	0
SEL1	SEL0	n	n	n	n	n	n

This is the input/output control register which controls the direction and level of the 2 x GPIO ports. It also triggers a read of the state of the ports and places the results in the IORD register. The register is split into a number of sub-registers. The sub-register written depends on the value of the SEL1 and SEL0 bits. In all cases, after this register has been written and the action completed, bit 15 of the STATUS register will be set to 1, and if enabled, IRQN will go low. No other C-BUS registers should be read or written to whilst this command is in progress.

SEL1 / SEL0 = 00 - Output control

7	6	5	4	3	2	1	0
0	0	0	0	0	0	IO2	IO1

This sub-register allows direct control of the level of each port that is configured to be an output. After a reset, this register will default to all bits zero. If only the direction of a port is changed to output, it will drive low.

Bit 0 : IO1

If IO1 is configured as an output, setting this bit to 1 causes the GPIO1 port to go high and clearing this bit to 0 causes the port to go low. If the port is configured to be an input, the state of this bit is ignored.

Bit 1 : IO2

If IO2 is configured as an output, setting this bit to 1 causes the GPIO2 port to go high and clearing this bit to 0 causes the port to go low. If the port is configured to be an input, the state of this bit is ignored.

Bits 5 to 2 : Reserved

These bits should be cleared to 0 for correct device operation.

SEL1 / SEL0 = 01 - Direction control

7	6	5	4	3	2	1	0
0	1	0	0	0	0	IO2	IO1

This sub-register controls the direction of each of the GPIO ports. After a device reset, all these ports will be configured to be inputs.

Bit 0 : IO1

Setting this bit to 1 configures the GPIO1 port to be an input. Clearing this bit to 0 configures the GPIO1 port to be an output. When configured to be an output, the level driven will depend on the value written to the Output control or Output command sub registers.

Bit 1 : IO2

Setting this bit to 1 configures the GPIO2 port to be an input. Clearing this bit to 0 configures the GPIO2 port to be an output. When configured to be an output, the level driven will depend on the value written to the Output control or Output command sub registers.

Bits 5 to 2: Reserved

These bits should be cleared to 0 for correct device operation.

SEL1 / SEL0 = 10 - Command

7	6	5	4	3	2	1	0
1	0	0	0	0	PORT	CMD	

This sub-register provides an alternative method of controlling the direction and output state of the GPIO ports. Each write affects one aspect of one port.

Bit 1 and 0 : CMD

This field specifies a direction or output state of a port:

1	0	CMD	Description
0	0	OUTPUT	Set the specified port as an output
0	1	INPUT	Set the specified port as an input
1	0	LOW	When set as an output, the specified port will drive low.
1	1	HIGH	When set as an output, the specified port will drive high

Bit 2: PORT

This field specifies which port is to be controlled.

2	Port
0	GPIO1
1	GPIO2

Bits 5 to 3 : Reserved

These bits should be cleared to 0 for correct device operation.

SEL1 / SEL0 = 11 - Read

7	6	5	4	3	2	1	0
1	1	0	0	0	0	0	0

This sub register triggers a read of the state of both ports without making any changes.

Bits 5 to 0 : Reserved

These bits should be cleared to 0 for correct device operation.

9.1.13 IDATA - $10, 8-bit write

7	6	5	4	3	2	1	0
DATA							

This is the In Data register and is an 8-bit wide C-BUS streaming register used in both packet data and external scrambling modes.

For packet data, this register is used in conjunction with the PDATA register ($1D) to enable the bytes of data to be sent to the device prior to transmission. Refer to the PDATA register for further information on using the packet data mode. For external scrambling, IDATA allows RALCWI-encoded voice frames to be sent back into the device after external data manipulation. Each voice frame is 6 bytes long and is produced every 20ms.

A voice frame should be written, on average, every 20ms. If the manipulation process exhibits algorithmic jitter, then the first frame should be written after enough delay to ensure that subsequent frames will not arrive late. One method is to write in a single voice frame when the device sets the VFA bit in the STATUS register to indicate that an encoded frame is available in the ODATA register. This way, the host puts back the previous frame each time a new frame is available.

It is possible to write back up to 4 previous frames at once. For example, if a manipulation scheme involved reversing the order of every batch of 4 frames, then every 80ms, the host could write the 4 collected frames all at once.

If more frames are written to this register than have been produced by the device, or the FIFO behind this register becomes full due to more than 6 bytes per frame being written, or repeated writing of unnecessary frames, the FOU bit in the STATUS register will be set. The FSTAT register may be interrogated to find the cause.

9.1.14 CTRL - $11, 16-bit write

15	14	13	12	11	10	9	8
PRM	NFHI	PLV	USR4	USR3	USR2	USR1	USR0

7	6	5	4	3	2	1	0
0	0	0	0	0	PKT	MODE	

This is the control register and controls various aspects of the device whilst running. Some settings for this register are set in conjunction with various other registers also described in this section.

Bits 0 and 1: MODE

1	0	Description
0	0	Idle
0	1	Receive
1	0	Transmit
1	1	VSR Playback

Bit 2: PKT Packet

This bit controls the transmission of packet data. If this bit is set to '1' when the device mode is set to transmit, the device will send a data packet instead of digital voice. If this bit is cleared to zero when the mode is set to transmit, digital voice will be sent. This bit has no effect in receive mode (the device recognises the difference between digital voice and packet data via the header frame).

Bits 7 to 3 : Reserved

These bits must be cleared to zero for correct operation.

Bits 10 to 8 : USR2 to USR0: User bits

These bits may be freely used by the host. They are sent as part of the frame head. In receive mode, the value of these bits can be read from the FHEADV register.

Bits 12 to 11: USR4 to USR3: User bits

In digital voice mode, these are two extra user bits that may be freely used by the host. Like the other user bits, the receiver will place these in the FHEADV register unaltered.

When sending packet data, these bits are reserved and should be cleared to zero for correct operation.

Bit 13 : PLV Peak level

This bit controls the peak level facility. If this bit is set to '1', the peak level function will be turned on. If this bit is cleared to zero, no peak level monitoring will take place. Refer to the PLEVEL register for further information.

Bit 14 : NFHI No frame head interleave

This bit controls the interleaving of the frame head. If this bit is clear, the frame head for digital voice and packet data will be interleaved after the FEC has been applied. If this bit is set, no interleaving will be done on the frame head. This non-interleaving option is provided for

backwards compatibility with devices like the CMX882 which do not support frame head interleaving.

Bit 15 : PRM Promiscuous mode

If this bit is set to ‘1’, the device will respond to frame heads for any address, not just the address it is programmed with. If this bit is cleared to zero, then the device will ignore any frame heads that do not contain the device's address that is set up in the LADDR register.

9.1.15 LSEED - $12, 16-bit write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRAMBLE SEED VALUE															

This is the load seed register and enables new scramble seed values to be placed in the scrambler seed table. LSEED should be used in conjunction with the SCRAMBLE register. If the preference is to use seed values other than the defaults, a custom value can be defined in this register. The SINDEX field of the SCRAMBLE register should be set to the index of the seed that is to be written in the table. Note that the SINDEX field should not be set to 0 or 15 as these values are both preset to “whitening” and “disable scrambling” respectively and cannot be modified.

After this register has been written to, the host must wait for the RDY bit to be set in the STATUS register. If the RDY bit in the IRQENAB register is set, then IRQN will be pulled low.

Once the operation is performed, the SVCACK register will contain the status value, indicating whether writing the seed was successful. If the SINDEX field of the SCRAMBLE register is either 0 or 15, then the SVCACK register will be set to 0, indicating an error, otherwise, the SVCACK register will contain 1. Note that the other bits of the SCRAMBLE register are ignored for this function. Following a device reset, the device will be reset to the default seed values as defined in the SCRAMBLE register.

9.1.16 FSYNC - $13, 16-bit write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRAME SYNCHRONISATION WORD															

This is the frame sync register and the value specified defines the bit pattern to be used as the frame synchronisation which marks the start of the frame head. After a device reset, the default value for the frame sync. is $CB23.

9.1.17 ENGUTH - $14, 16-bit write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MUTE	UPPER THRESHOLD LEVEL														

This is one of four registers that are used to control the noise gate functionality. On the transmit side, the encoder noise gate helps to remove noise generated in front-end analogue circuitry or background ambient noise.

The ENGUTH register is the encoder upper threshold level and is used to control the level at which the noise gate will open and allow the audio signal to pass. The upper threshold level is illustrated in Figure 6.

Bits 14 to 0: Upper threshold level

If the value set is zero, the noise gate will be switched off. All other values turn the noise gate on and will set its upper level. No audio will pass through to the vocoder until a sample exceeds this threshold value.

Bit 15: Mute

If this bit is set to 1, the level set in Bits 14 to 0 will be ignored and audio will be prevented from passing to the vocoder section, irrespective of the setting of the upper threshold level. If the bit is cleared to zero, the upper threshold level value controls the noise gate as described above.

After this register has been written to, the host must wait for the RDY bit to be set in the STATUS register. If the RDY bit in the IRQENAB register is set, then IRQN will be pulled low.

9.1.18 ENGLTH - $15, 16-bit write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LOWER THRESHOLD LEVEL														

The ENGLTH is the encoder noise gate lower threshold level. The lower threshold level is illustrated in Figure 6.

Bits 14 to 0: Lower threshold level

This value specifies the level that all samples must be below before the gate will shut after having been opened.

Bit 15: Reserved

This bit should be cleared to zero for correct operation.

After this register has been written to, the host must wait for the RDY bit to be set in the STATUS register. If the RDY bit in the IRQENAB register is set, then IRQN will be pulled low.

9.1.19 ENGSDY - $16, 16-bit write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GATE SHUT DELAY															

The ENGSDY is the encoder noise gate shut delay. This register controls the delay in shutting the noise gate after the value of samples has become lower than that set for the lower threshold level. The gate shut delay is illustrated in Figure 6.

Bits 15 to 0: Gate shut delay

This value specifies the number of consecutive 20ms frames whose samples must all be at a value lower than the lower threshold level before the noise gate begins to close. The noise gate takes a further 16 frames to close, by increasing an attenuator in 6dB steps. If, at any point in this procedure, a sample exceeds the lower threshold level, the sequence will start again.

After this register has been written to, the host must wait for the RDY bit to be set in the STATUS register. If the RDY bit in the IRQENAB register is set, then IRQN will be pulled low.

9.1.20 DNGTH - $17, 16-bit write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MUTE	0	LOWER THRESHOLD LEVEL													

DNGTH is the decoder noise gate threshold level register. On the receive side, the decoder noise gate is used to remove audio artefacts after decoding packets of vocoded silence. The noise gate operation is the same as for the encoder noise gate used on the transmit side. However, only the lower threshold value is programmable. The upper threshold level value is fixed to be twice the lower threshold level, and the gate shut delay is fixed to be 10 frames (200ms).

Bits 13 to 0 : Lower threshold level

If this value is zero, the decoder noise gate is turned off. All other values turn on the noise gate and set its lower level. The upper threshold level is preset to be double this value.

Bit 14: Reserved

This bit should be cleared to zero for correct operation.

Bit 15: Mute

If this bit is set to 1, no audio will pass through from the vocoder irrespective of the lower threshold level value. If this bit is cleared to zero, the lower threshold level value controls the noise gate as described above.

After this register has been written to, the host must wait for the RDY bit to be set in the STATUS register. If the RDY bit in the IRQENAB register is set, then IRQN will be pulled low.

9.1.21 VSRW - $1C, 16-bit write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PARAMETER					BUFFER			0	0	0	COMMAND				

VSRW is the Voice Store and Retrieve Write register and controls all aspects of the VSR feature. Bits 0 to 4 specify a command that the VSR sub-system should perform. Bits 8 to 10 specify the buffer to be used. Bits 11 to 15 are the parameter bits and are used to set the number of 0.8s (40 x 20ms frames) blocks that the playback pointer should move by when executing the STEPBACK command. Bits 5 to 7 are reserved and should be set to 0 for correct operation. After this register has been written bit 15 (RDY) of the STATUS register ($40) will be set and, if enabled, IRQN will go low. The SVCACK register ($2E) will contain a flag in bit 0 indicating whether the write to this register was successful. If this bit is set to 1, the action was successful. If cleared to 0, then the action failed. Commands that return information to the controlling host will place that information in the VSRR register ($32). This register may be read after bit 15 of the STATUS register has been set, and SVCACK register indicates that the action was successful.

The commands that the VSR sub-system can perform are shown in the table below:

Command	Mnemonic	Description
$0	VSR_RESET	Resets the entire VSR subsystem. This command should be the first one issued and restores all internal data structures to a known default state, thereby preparing the feature for use. The buffer field (bits 8 to 10) should be set to $00 for correct operation. This command will fail if the device is currently recording or playing back.
$1	VSR_ERASE_ALL	Erases all buffers, returning any used memory to the main memory pool for re-use. The buffer field (bits 8 to 10) should be set to $00 for correct operation. This command will fail if the device is currently recording or playing back.
$2	VSR_ERASE	Erases a single buffer, returning used memory to the main memory pool for re-use. The buffer field (bits 8 to 10) should specify which buffer is to be erased. This command will fail if the buffer specified is currently being used to record or play back.
$3	VSR_PSTART	Start playing the contents of the buffer specified in the buffer field. Playback will start at the beginning of the buffer. It is necessary for the Mode bits (bits 1 and 0) of the CTRL ($11) register to be set to 1 for this command to be successful otherwise the command will fail and an error will be returned. If, whilst playing, the end of the buffer is reached, then playback will stop and bit 5 (VSR) of the STATUS register ($40) will be set. If enabled, IRQN will go low. This command will fail if the device is already recording or playing back

$4	VSR_PSTOP	Stop playing the currently playing buffer. The current position of the playback pointer is saved so playback may be resumed. This command will fail if the device is not currently playing back.
$5	VSR_PRESUME	Start playing the contents of the buffer specified in the buffer field. Playback will start from where it was last stopped. If, whilst playing, the end of the buffer is reached, then playback will stop and bit 5 (VSR) of the STATUS register ($40) will be set and, If enabled, IRQN will go low. This command will fail if the device is already recording or playing back.
$6	VSR_RSTART	Start saving vocoder packets in the buffer specified in the buffer field. If the buffer was not empty when this command is sent, then the vocoder packets will be appended to the buffer. If, whilst recording, no more memory is available, recording will stop and bit 5 (VSR) of the STATUS register ($40) will be set and, If enabled, IRQN will go low. This command will fail if the device is already recording or playing back.
$7	VSR_RSTOP	Stop the current recording operation. This command will fail if the device is not currently recording.
$8	VSR_FREE	Return the amount of free space available for storage in the VSRR register ($32). The value returned is the number of 20 millisecond frames that remain in the free memory pool. This value should be divided by 50 to obtain the number of seconds available.
$9	VSR_LENGTH	Return the amount of speech stored in the buffer specified in the buffer field. The value returned in the VSRR register ($32) is the number of 20 millisecond frames that have been recorded.
$A	VSR_STATUS	Returns a status value in VSRR register ($32) indicating whether the VSR subsystem is recording, playing back, or idle. The active buffer is also included where the status indicates that it is not idle. There are no error conditions associated with this command.

$B	STEPBACK	Within the buffer specified in the buffer field, step back by the number of blocks specified in bits 15 to 11, to a maximum of 31. After executing this command, the playback pointer will move to the start of the specified block. VSR_PRESUME can then be executed and playback will commence from that point. If zero is specified as the value in bits 15 to 11, the playback pointer will move to the start of the current block. If the command is executed whilst the device is playing back from, or recording to, the buffer specified in the buffer field, an error will be returned. If an attempt is made to step back further than the start of the audio, the playback pointer will only return to the start of the audio. If an attempt is made to step back within an empty buffer the command will be ignored.

9.1.22 PDATA - $1D, 16-bit write

15	14	13	12	11	10	9	8
R/W	RCOUNT						

7	6	5	4	3	2	1	0
OFFSET							

This is the packet data register. PDATA is used to transfer packet data into and out from the device and works in conjunction with TXPL (transmit packet length), RXPL (receive packet length), IDATA (input data), ODATA (output data) and various bits of the CTRL register.

The device has a 260-byte buffer which can store an incoming or outgoing data packet. PDATA, together with IDATA and ODATA, enables data to be written to or read from this buffer.

To write data to the buffer, the controlling host should first write the required data to the IDATA register (no more than 128 bytes) Then the position in the buffer to start writing the data should be written into the OFFSET field of this register with the R/W bit (bit 15) set to '1'. Once the device has transferred the data, it will set the RDY bit of the STATUS register to '1'. The device will also indicate how much of the data was written by writing an appropriate value to the RXPL register.

To read data from the buffer, the controlling host should write the desired amount of data to be read from the buffer in the RCOUNT field and the position in the buffer to start reading in the OFFSET field of this register, with the R/W bit cleared to zero. Once the device has transferred the data from the buffer into the ODATA register, the RDY bit of the STATUS register will be set to '1' and the actual number of bytes read from the buffer will be placed in the RXPL register. The controlling host may now read the data from the ODATA register.

The device does not allow reads or writes that extend beyond the end of the buffer. If this is attempted, the data that exceeds the end of the buffer will be ignored, and the data byte count placed in the RXPL register will reflect the amount of data actually read or written.

Bit 7 to 0 : OFFSET

These bits specify the location in the 260-byte buffer that a read or write operation will start. This value can be any value from 0 to 255.

Bit 14 to 8 : RCOUNT

When reading, these bits specify how many bytes should be read from the buffer. When writing, these bits should all be set to zero for correct operation.

Bit 15: R/W

If this bit is cleared to zero a read operation will be performed. If this bit is set to '1' a write operation will be performed.

Note: If ALL the bits in this register are set to zero (a zero byte read from offset 0) then the device will reset the FIFO that is behind the IDATA register. It is good practice to do this before writing new data for transmission, especially if the device has been sending or receiving digital voice with external scrambling.

9.1.23 IRQENAB - $1F, 16-bit write

15	14	13	12	11	10	9	8
RDY	SVC	0	0	0	0	0	0

7	6	5	4	3	2	1	0
0	PLV	VSR	FOU	VFA	0	FHD	EOT/RSR

This is the interrupt request enable register. IRQENAB specifies which of the bits in the STATUS register ($40) will cause a C-BUS interrupt to be generated (IRQN pin is pulled low).

Setting a bit to '1' will cause the corresponding status bit to generate a C-BUS interrupt when the status bit is set to '1'. Please refer to the STATUS register ($40) for an explanation of the bits.

The default state of this register after a power-up reset is for all bits, except for bit 15 (RDY), to be cleared to '0'. Bit 15 is set to '1', so that when the device is ready to accept commands (signified by bit 15 (RDY) of the STATUS register ($40) being set to '1'), there will also be a C-BUS interrupt.

Bits 2, 5 and 7 to 13 should be cleared to 0 for correct operation.

9.1.24 FSTAT - $21, 8-bit read

7	6	5	4	3	2	1	0
X	X	X	X	UNDF	OVRS	IPFF	OPFF

FSTAT (frame flow status) is an 8-bit read-only register and is used only in external scrambling mode. It indicates the reason why the FOU (frame overflow underflow) bit has been set in the STATUS register. Data flow errors suggest a problem with the host's handling of external scrambling. This value in this register is valid after the FOU bit in the STATUS register has been set.

Bit 0 : OPFF Output FIFO full

The FIFO behind the ODATA register ($30) has been allowed to become full. This will happen if the controlling host does not read the frames.

Bit 1 : IPFF Input FIFO full

The FIFO behind the IDATA register ($10) has been overfilled. This will happen if the controlling host writes too much data to this register.

Bit 2 : OVRS Over supply

The host has sent more frames into the device than the device has produced.

Bit 3 : UNDF Underflow

The host has failed to write enough frames into the device, and the data flow within the device has now been interrupted. If this happens, the device will just re-use the last frame.

BitS 7 to 4 : Reserved

These bits should be ignored. The value of these bits is indeterminate.

9.1.25 FTYPE - $22, 8-bit read

7	6	5	4	3	2	1	0
DATA							

This read-only register is used only when the device is transmitting in external scrambling mode and indicates what type of frame has been produced.

FTYPE is valid after the VFA (vocoder frame available) bit in the STATUS register has been set. The value will remain in the register until updated when the next frame becomes available, and the VFA bit is set once again.

The following frame types are currently defined:

Value	Mnemonic	Description
$01	FTYPE_VOICE	The frame that has just been produced is a voice frame
$02	FTYPE_EOV	The frame that has just been produced is an end of voice frame
$03	FTYPE_EOVL	The frame that has just been produced is an end of voice frame, and is the last frame.

9.1.26 FHEADV - $23, 8-bit read

7	6	5	4	3	2	1	0
VALID	PKT	X	USR4	USR3	USR2	USR1	USR0

The frame head validity register indicates whether or not the received frame head is valid. If the frame is valid, the format field of the frame will indicate the type of data (digital voice or packet data) and the user bits (bits 12 to 8) set in the CTRL register ($11) of the transmitter will be returned. Three user bits will be written if the format is packet data, and two additional bits will be written if the format is digital voice. Please refer to the description for the CTRL register, $11. The value in the register is updated just before the FHD bit is set in the STATUS register.

Bits 2 to 0: USR2 to USR0 user bits
These bits contain the user bits set in the CTRL register of the transmitter.

Bits 4 to 3: USR4 to USR3 user bits
If the frame head is for digital voice, these are the two additional user bits that are set in the CTRL register of the transmitter. If the frame head is for packet data, these bits should be ignored. Their value will be indeterminate.

Bit 5: Reserved
This bit should be ignored as its value is indeterminate.

Bits 6: PKT
If this bit is set to '1', then the data that follows is a packet data message. If this bit is cleared to zero, then, the data that follows is digital voice.

Bit 7 : VALID
If this bit is set to '1', the received frame head is valid and has the correct address. If the PRM (promiscuous mode) bit is set in the CTRL register, then the frame head is valid (this means that the device will respond to frame heads for any address), and the address may be read from the ADDRESS register. If this bit is cleared to zero, then the frame head is either corrupted or does not have the correct address. If the PRM bit is set in the CTRL register, then the frame head is corrupted.

9.1.27 DESCRAMBLE - $24, 8-bit read

Mode	7	6	5	4	3	2	1	0
Digital Voice	XSCRAM	PRS	0	0	SINDEX			
Packet Data	X	X	X	X	X	X	SINDEX	

This is the descramble register. The register will contain the scrambler information extracted from the received header frame. DESCRAMBLE will only be updated after a valid header frame has been received as set in the FHEADV register. For internal scrambling, the receiver will automatically descramble using the scrambler seed value held in the SINDEX field. Please refer to the SCRAMBLE register for further information.

The contents of the register will be different depending on whether the device is operating in digital voice or packet data mode.

Digital Voice Mode

Bits 3 to 0 : SINDEX Seed index
This field reports the seed index that the transmitter has specified.

Bits 5 and 4 : Reserved
These bits should be ignored. The value of these bits is indeterminate.

Bit 6: **PRS**
This is the PRS (pseudo-random sequence) field for internal scrambling and indicates which of the two possible sequences is being used. If the bit is cleared to zero (the default setting), a relatively short pseudo-random sequence is in use. If this bit is set to 1, the maximum length pseudo-random sequence is in use. If bit 7 (XSCRAM) is set to 1 the value of this bit, like bits 5 and 4, will be indeterminate.

Bit 7 : XSCRAM External scrambling
If this bit is cleared to 0, the internal descrambling facility will be used, and requires no intervention from the host. If this bit is set to 1, the internal scrambling algorithm will be ignored and the vocoded data frames will be passed out of the device and to the host microcontroller. The host must therefore perform the de-scrambling itself using the value of SINDEX field using a suitable scrambling method.

Packet Data Mode

Bits 1 to 0: SINDEX Seed index
This field reports the seed index that the transmitter has specified.

Bits 7 to 2 Reserved
These bits should be ignored. The value of these bits is indeterminate.

9.1.28 ADDRESS - $25, 8-bit read

7	6	5	4	3	2	1	0
ADDRESS							

This is the address register and contains the address field extracted from the received header frame. This is only updated if the received frame head is considered valid i.e. the address matches the local address (set by writing to the LADDR register) or the device has been set to the promiscuous mode by setting bit-15 of the CTRL register to 1. Please refer to the description of the CTRL register for further information.

9.1.29 RSTAT - $26, 8-bit read

7	6	5	4	3	2	1	0
STATUS							

This is the receiver status register. RSTAT will contain the status of the receiver after the device has indicated that it has finished receiving. At the end of a transmission, the received data will contain a number of End-of-Voice (EOV) frames. When these EOV frames are received, the EOT (end of transmission) bit in the STATUS register will be set to 1 and will remain valid until the device is instructed to receive again.

The following status values are currently defined.

VALUE	MNEMONIC	DESCRIPTION
$01	RSTAT_EOV	The receiver has detected the correct number of EOV frames
$02	RSTAT_QUIT	The receiver has received too many consecutive frames with errors
$06	RSTAT_GCRC	The device has received a complete data packet with correct CRC
$07	RSTAT_BCRC	The device has received a data packet with an incorrect CRC

9.1.30 RXPL - $2C, 8-bit read

7	6	5	4	3	2	1	0
Rx Packet Length							

The receive packet length (RXPL) register serves a dual purpose:

When the device has received a data packet, the length of the packet that just been received will be placed in this register. The value in this register is valid once the device has indicated that a complete packet has been received by setting the EOT/RSR (bit 0) of the STATUS register.

When transferring data in and out of the device, this register reports how much data was actually read or written. In this case, the value in this register is valid once the RDY bit of the STATUS register has been set to ‘1’. Refer to the PDATA register for further information.

9.1.31 SVCACK - $2E, 8-bit read

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	ACK

This read-only register contains the acknowledgement result from a service request or some other operation, as detailed in the STATUS register ($40). The contents of this register are only valid after status bit 14 or 15 (in certain cases) has been set, and before another C-BUS register is written.

Bit 0
ACK This bit is set to '1' to indicate a success result.
This bit is cleared to '0' to indicate an error or unsuccessful result.

Bits 1 to 7 These bits are undefined.

9.1.32 IORD - $2F, 8-bit read

7	6	5	4	3	2	1	0
X	X	X	X	X	X	IO2	IO1

This register contains the state of the two GPIO ports. The register is updated after every write cycle to the IOCTRL register ($0F).

Bit 0 : IO1

This bit contains the state of the GPIO1 port at the device's pin.

Bit 1 : IO2

This bit contains the state of the GPIO2 port at the device's pin.

Bits 7 to 2 : Reserved

These bits should be ignored. The values of these bits are indeterminate.

9.1.33 ODATA - $30, 8-bit read

7	6	5	4	3	2	1	0
DATA							

This is the Out Data register and is an 8-bit wide C-BUS streaming register used in both packet data and external scrambling modes.

For packet data, this register is used in conjunction with the PDATA register ($1D) to retrieve the bytes of data from the buffer in receive mode. Refer to the PDATA register for further information on using the packet data mode. For external scrambling ODATA allows RALCWI-encoded voice frames to be sent to the host for external data manipulation. Each voice frame is 6 bytes long and is produced every 20ms. Data sent to the host is streamed from a FIFO which can accommodate at least 4 frames. It is possible to allow these frames to accumulate before reading the register. It would thus be possible to swap the order of the frames as part of a scrambling strategy. For each available frame, exactly 6 bytes must be read - no more, no less.

This register should be read whenever the VFA bit in the status register is set. The VFA (vocoder frame available) bit indicates that there is a frame of vocoded data available to be read from the FIFO.

If the device is in transmit mode the FTYPE register will indicate what sort of frame has been produced - voice, end of voice, or last frame.

If the FIFO behind this register is allowed to become full, the FOU bit in the STATUS register will be set.

9.1.34 PLEVEL - $31, 16-bit read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Peak Level															

This read-only register contains the peak sample value of the last 20ms frame of audio collected for encoding. This peak sample value will be available for every 20ms frame. Bit 6 of the STATUS register ($40) will be set to '1' (and a C-BUS interrupt generated, if enabled) when this register is updated. This value is only updated when the facility is turned on in the CTRL register. The audio level should not be allowed to limit: for single-ended operation this can be ensured by keeping the Peak Level below 16384, i.e. bit 14 of the PLEVEL register should not become set to '1'.

9.1.35 VSRR - $32, 16-bit read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRAMES															
R	P	X	X	X	X	X	X	X	X	X	X	X	BUFFER		

This is the Voice Store and Retrieve Read register and contains the results returned by some of the VSR commands. For commands that return a frame count, this can be read as a 16-bit unsigned value. The VSR_STATUS command returns two flags and a buffer number.

Bit 15 : R: This flag is set to 1 if the device is recording. The buffer field indicates which is the active buffer.

Bit 14 : P: This flag is set to 1 if the device is playing. The buffer field indicates which is the active buffer.

When both bits 15 and 14 are clear, the buffer value has no meaning and indicates the VSR sub-system is idle. Bits 13 to 3 should be ignored.

9.1.36 STATUS - $40, 16-bit read

15	14	13	12	11	10	9	8
RDY	SVC	X	X	X	X	X	X

7	6	5	4	3	2	1	0
X	PLV	VSR	FOU	VFA	X	FHD	EOT/RSR

This read-only register indicates that the device has data or needs servicing. The device can be used in an interrupt driven mode or a polled mode.

If being used in an interrupt driven mode, after a C-BUS interrupt, this register should be read to establish the reason for the interrupt. An interrupt will only be generated if the corresponding bit of the IRQENAB register ($1F) is also set to '1'. If the device is being used in a polled mode, then this register should be read at regular intervals. The register is cleared to '0' after it is read. It is possible for more than one bit to be set to '1', so each bit should be dealt with as appropriate.

Bits 2 and 5
Bits 7 to 13 These bits should be ignored. The values of these bits are indeterminate.

Bit Mnemonic	Function	Description
EOT RSR (Bit 0)	End Of Transmission/ Receiver Status Register	If the device is transmitting, this indicates that the FFSK signal has stopped and the analogue output of the device has gone to BIAS. If the device is receiving, this indicates a change in receiver state. The RSTAT register should be read to determine the reason.
FHD (Bit 1)	Frame Head Detected	Indicates that the device has received a frame head. The FHEADV register should be read to determine whether or not the frame head is valid and the type of transmission – digital voice or packet data.
VFA (Bit 3)	Vocoder Frame Available	Indicates that a frame of vocoder data is ready to be read from the ODATA register. The type of frame may be determined by reading the FTYPE register.
FOU (Bit 4)	Frame Overflow Underflow	Indicates that an overflow and/or underflow of vocoder frames has occurred. The reason for this can be determined from the FSTAT register.
VSR (Bit 5)	Voice Store and Retrieve	When the device is in VSR (record) mode, this bit will be set to 1 when all available memory has been used up and recording has stopped. When the device is in VSR (playback) mode this bit will be set to 1 when the end of the buffer has been reached and playback has been stopped. It may take up to 20ms after this bit has been set for audio to stop playing because the output buffer needs time to empty.
PLV (Bit 6)	Peak Level sample available	The peak level sample for the last 20ms is available. This may be read from the PLEVEL register.

SVC (Bit 14)	Service acknowledgement available	A service request has been completed, and its status may be read from the SVCACK register.
RDY (Bit 15)	Ready	Indicates that the device is ready to accept commands after certain time consuming operations. This bit will be set to '1' after the following: 1. Hard or soft reset 2. Writing to the following registers: SCRAMBLE, IOCTRL, CTRL, LSEED, ENGUTH, ENGLTH, ENGSDY, DNGTH, VSRW, PDATA

9.2 Function Image™ Updates

```
;*****************************************************************
;Version 7011FI-1.0.3.*
;*****************************************************************
Voice store and retrieve added.
Packet data functionality added.



;*****************************************************************
;Version 7011FI-1.0.2.0
;*****************************************************************
External data routing capability added.



;*****************************************************************
;Version 7011FI-1.0.1.0
;*****************************************************************
Encoder and decoder noise gate functionality added.
GPIO3 removed, leaving GPIO1 and GPIO2 as general purpose input/outputs



;*****************************************************************
;Version 7011FI-1.0.0.0
;*****************************************************************
First FI release
;*****************************************************************
```

10 Application Notes

10.1 Function Image™ Load and Activation

The initial Function Image™ for the CMX7011 and Function Images™ that will bring future enhancements are downloaded into the device over the C-BUS via the IDATA register ($10). The data is sent in packets of 128 bytes. The Function Image™ will always be a whole multiple of 128 bytes. The following steps should be taken to download a Function Image™. Please check the documentation supplied with any Function Image™ which may detail a deviation from the following instructions.

1. Reset the device. This can be achieved by using either the RESETN pin (30), or by writing to the C-BUS RESET register ($01).

2. Wait until the device indicates that it is ready to accept the Function Image™ download (normally approximately 1.5ms after a reset). This can be done by either polling the STATUS register ($40) and waiting for bit 15 (RDY) to be set to '1', or waiting until IRQN goes low, and then reading the STATUS register to reset it (bit 15 will have been set to '1').

3. If the process is to be interrupt driven (i.e. using IRQN to indicate a change in the STATUS register), then write the value of $C000 to the IRQENAB register ($1F). This will enable interrupts for the SVC bit (bit 14), which is used in the download protocol.

4. Write the value of $01 to the SVCREQ register ($0E). This indicates to the device that a Function Image™ is to be downloaded.

5. Wait for bit 14 to be set to '1' in the STATUS register (either by polling or waiting for IRQN to go low).

6. Read the SVCACK register ($2E) and check that bit 0 is set to '1'. This indicates that the device is able to accept a Function Image™.

7. Write 128 bytes of Function Image™ data to the IDATA register ($10). This may be done as a single 128-byte streaming write, 128 single byte writes or 64 x 2-byte writes.

8. Wait for bit 14 to be set to '1' in the STATUS register (either by polling or waiting for IRQN to go low).

9. Read the SVCACK register ($2E) and check that bit 0 is set to '1'. This indicates that the device has accepted the data packet.

10. If there is more data to send, go back to step 7.

11. Write the value of $01 to the SVCREQ register ($0E). This indicates to the device that all of the Function Image™ has now been sent.

12. Wait for bit 15 to be set to '1' in the STATUS register (either by polling or waiting for IRQN to go low).

13. Read the 16-bit PLEVEL register ($31) and check that the value read is $7011. This indicates that the device has accepted the Function Image™ and is now ready to be used.

The device should be reset if at any time through the above sequence if, when read, the SVCACK does not have bit 0 set to '1'.

IMPORTANT! – Once the Function Image™ has been loaded, it is important that that the general purpose input/outputs GPIO1 and GPIO2 are not left in a 'floating' condition where the state of the lines may be indeterminate. First read the value of the PLEVEL register ($31) and verify that the FI has been successfully loaded as described in step 13. If the lines are to be configured as outputs, they must be programmed as such by writing a value of $40 to the IOCTRL register ($0F). If they are to be configured as inputs they must be pulled up to V_{DD} or down to V_{SS}.

10.2 Basic Device Operation

The instructions given in this section assume that the device has already had the Function Image™ successfully loaded as described in Section 10.1.

The last steps in loading a Function Image™ ask for the host to wait for the RDY bit in the STATUS register ($40) to be set and to read the SVCACK register ($2E) and verify that it holds the value of 1. After this has been done, the following steps may be taken to start the device either transmitting or receiving.

This device may be used in either an interrupt driven system, or a polled system. The device will indicate that it needs attention by setting a particular bit in the STATUS register and, if enabled, generate an interrupt by setting IRQN low.

Assuming that two CMX7011s are available, the following step can be carried out to demonstrate a complete transmit and receive path.

10.2.1 Basic Configuration

Note – this sequence should be performed on the receiver and transmitter.

1. **Enable interrupts**

   Write $8003 into the IRQENAB register ($1F) – This enables the interrupts for RDY (ReaDY), FHD (Frame Head Detected), and EOT (End Of Transmission).

2. **Turn on BIAS, the ADC/DAC, and reduce internal clock speed when idle.**

   Write $13 into the POWERSAVE register ($09).

3. **Set the output gain to 0dB**

   Write $07 into the AOG register ($06) – This is a reasonable output level if feeding the FFSK signal directly into another CMX7011 with its input gain set to 0dB.

4. **Set the local and remote addresses**

   Write $01 into the RADDR register ($07)

   Write $01 into the LADDR register ($08)

   This sets the device to transmit to, and receive from, address number 1

10.2.2 The Receiver

1. **Start Receiving**

   Write $0001 into the CTRL register ($11)

2. **Wait for the command to complete**

   Wait for a CBUS interrupt, or poll the STATUS register ($40) until RDY (bit 15) is set to 1

3. **Start the Transmitter using the sequence described in section 10.2.3 below**.

4. **Wait for the frame head to be detected**.

   Wait for a CBUS interrupt, or poll the STATUS register ($40) until FHD (bit 1) is set to 1

   Read the FHEADV register ($23) and check that the most significant bit (bit 7) is set to 1. This indicates that the frame head has been received without error and that the address (RADDR of the transmitter) matches our local address (LADDR).

5. **Wait for the transmission to end**.

   Wait for a C-BUS interrupt, or poll the status register ($40) until EOT (bit 0) is set to 1.

   Read the RSTAT register ($26) to find out why the transmission ended. This should be either $01 to indicate that the receiver received enough end-of-voice (EOV) frames, or $02 to indicate that the receiver encountered too many errors and gave up.

6. **Go To Idle Mode**

   Write $0000 into the CTRL register ($11).

7. **Wait for the command to complete**.

   Wait for a CBUS interrupt, or poll the STATUS register ($40) until RDY (bit 15) is set to 1.

   The device should now be in an idle state.

10.2.3 The Transmitter

1. **Start transmitting**

   Write $0002 into the CTRL register ($11)

2. **Wait for the command to complete**

   Wait for a CBUS interrupt, or poll the STATUS register ($40) until RDY (bit 15) is set to 1

   The device should now output FFSK at the analogue output pin of the device, the receiver sequence should have progressed to step 5, and the receiver should be reproducing any voice that is present at the transmitter's analogue input pin.

3. **Stop transmitting**

   Write $0000 into the CTRL register ($11)

4. **Wait for the command to complete**

   Wait for a CBUS interrupt, or poll the STATUS register ($40) until RDY (bit 15) is set to 1

5. **Wait for the FFSK to stop**

   Wait for a CBUS interrupt, or poll the STATUS register ($40) until EOT (bit 0) is set to 1
   The transmitter should now be idle. The receiver sequence should have progressed to step 6.

10.3 Example Packet Data Operations

The following sequences of instructions assume that the device has already had the Function Image^{tm} successfully loaded.

The final steps in loading a Function Image^{tm} ask for the host to wait for the RDY bit in the STATUS register ($40) to be set and to read the PLEVEL register ($31) and verify that the value read is $7011. After this has been done, the following steps may be carried out to either transmit or receive.

10.3.1 Transmit 20 bytes to the receiver with address $03

1. **Enable interrupts**

   Write $8001 into the IRQENAB register ($1F)

   This enables the interrupts for RDY (ReaDY), and EOT (End Of Transmission)

2. **Turn on BIAS, the ADC/DAC, and reduce the internal clock speed when idle**

   Write $13 into the POWERSAVE register ($09)

3. **Ensure the IDATA input FIFO is empty**

   Write $0000 into the PDATA register ($1D)

4. **Wait for the command to complete**

   Wait for a CBUS interrupt, or poll the STATUS register ($40) until RDY (bit 15) is set to 1

5. **Send the data into the device**

   Write the 20 bytes of data into the IDATA register ($10). This may be done as a single 20-byte streaming write, or 20 single byte writes (or 10 16-bit word writes, for that matter).

6. **Place the data into the internal buffer**

   Write $8000 into the PDATA register ($1D).

   This causes the device to fetch all the bytes in the input FIFO and place them in the buffer starting at position 0.

7. **Wait for the command to complete**

   Wait for a CBUS interrupt, or poll the STATUS register ($40) until RDY (bit 15) is set to 1

8. **Check the number of bytes written to the buffer**

   Read the RXPL register ($2C) and check that the value read is 20 ($14).

9. Set the byte count for the transmission

Write 20 ($14) into the TXPL register ($0C).

10. Set the destination address

Write $03 into the RADDR register ($07)

11. Command the device to send the data

Write $0006 into the CTRL register ($11).

This will instruct the device to calculate the CRC for the data, and transmit the data complete with preamble, sync word, and frame head.

12. Wait for the command to complete

Wait for a CBUS interrupt, or poll the STATUS register ($40) until RDY (bit 15) is set to 1.

The device should now be outputting FFSK at the analogue output pin.

13. Wait for the transmission to complete

Wait for a CBUS interrupt, or poll the STATUS register ($40) until EOT (bit 0) is set to 1

The device should now have finished outputting FFSK at the analogue output pin.

10.3.2 Receive a number of bytes from the transmitter sending to address $03

1. Enable interrupts

Write $8003 into the IRQENAB register ($1F)

This enables the interrupts for RDY (ReaDY), FHD (Frame Head Detected), and RSR (Receiver Status Register)

2. Turn on BIAS, the ADC/DAC, and reduce the internal clock speed when idle

Write $13 into the POWERSAVE register ($1D)

3. Set our local address

Write $03 into the LADDR register ($08)

This will allow the receiver to accept the data transmission described by the above example.

4. Start receiving

Write $0001 into the CTRL register ($11)

5. Wait for the command to complete

Wait for a CBUS interrupt, or poll the STATUS register ($40) until RDY (bit 15) is set to 1

The device will now be looking for the SYNC word from the transmitter.

6. Wait for the frame head to be detected

Wait for a CBUS interrupt, or poll the STATUS register ($40) until FHD (bit 1) is set to 1

Read the FHEADV register ($23) and check that VALID (bit 7) is set to 1 to indicate that the frame head is valid and for this station. Check that PKT (bit 6) is also set to 1 to indicate that this is a packet data transmission.

7. Wait for the complete data transmission to complete

Wait for a CBUS interrupt, or poll the STATUS register ($40) until RSR (bit 0) is set to 1

8. Check the state of the received data

Read the RSTAT register ($26). If the value of this register is $06, the device received a complete data packet with a correct CRC. If the value of this register is $07, the received data packet failed its CRC.

9. Check the length of the data packet received

Read the RXPL register. The value returned is the length of the data in the received transmission.

10. Retrieve the data

If the length of the data received is less than 128 bytes, it may be read from the device in one hit. If it is greater than 127 bytes, then more than one read transaction must be performed.

Assuming the device has just received 20 bytes of data, such as was transmitted in the previous example;

Write $1400 into the PDATA register ($1D). This instructs the device to transfer 20 bytes ($14) of data from the beginning of the buffer to the output FIFO.

11. Wait for the command to complete

Wait for a CBUS interrupt, or poll the STATUS register ($40) until RDY (bit 15) is set to 1.

12. Check the number of bytes read from the buffer

Read the RXPL register ($2C) and check that the value read is 20 ($14).

13. Read the data

Read 20 bytes of data from the ODATA register ($30). This may be done as a single 20-byte streaming read, or 20 single byte reads (or 10 16-bit word reads, for that matter).

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